PSMN050-80BS

N-channel 80 V 46 mΩ standard level MOSFET in D2PAK

Rev. 1 — 2 March 2012 Product data sheet

1. Product profile

1.1 General description

Standard level N-channel MOSFET in D2PAK package qualified to 175 °C. This product is designed and qualified for use in a wide range of industrial, communications and domestic equipment.

1.2 Features and benefits

- High efficiency due to low switching and conduction losses
- Suitable for standard level gate drive sources

1.3 Applications

- DC-to-DC converters
- Load switching
- Motor control
- Server power supplies

1.4 Quick reference data

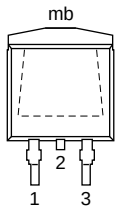
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25$ °C; $T_j \leq 175$ °C	-	-	80	V
I_D	drain current	T_{mb} = 25 °C; V_{GS} = 10 V; see Figure 1	-	-	22	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; see Figure 2	-	-	56	W
T_j	junction temperature		-55	-	175	°C
Static characteristics						
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 10 A; T_j = 25 °C	-	37	46	mΩ
Dynamic characteristics						
Q_{GD}	gate-drain charge	V_{GS} = 10 V; I_D = 25 A; V_{DS} = 40 V; see Figure 14; see Figure 15	-	2.3	-	nC
$Q_{G(tot)}$	total gate charge		-	11	-	nC
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; I_D = 22 A; $V_{sup} \leq 80$ V; R_{GS} = 50 Ω; unclamped	-	-	18	mJ

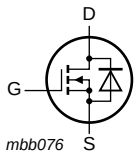
2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate		
2	D	drain[1]		
3	S	source		
mb	D	mounting base; connected to drain		



SOT404 (D2PAK)



[1] It is not possible to make connection to pin 2.

3. Ordering information

Table 3. Ordering information

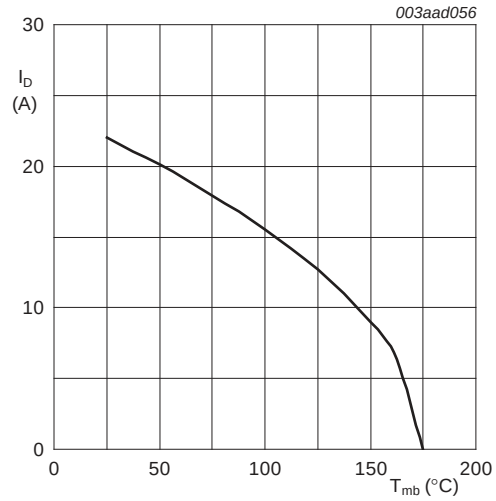
Type number	Package		
	Name	Description	Version
PSMN050-80BS	D2PAK	plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)	SOT404

4. Limiting values

Table 4. Limiting values

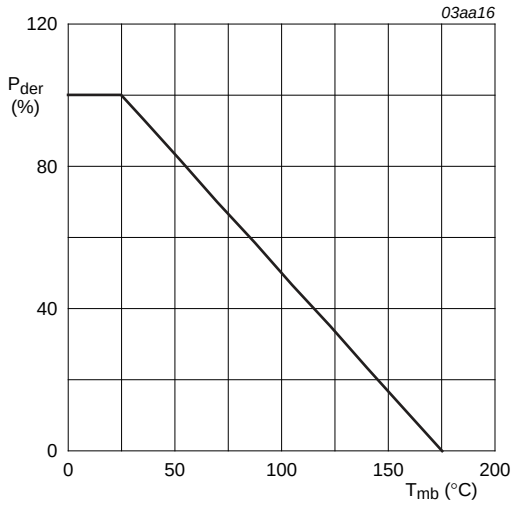
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25$ °C; $T_j \leq 175$ °C	-	80	V
V_{DGR}	drain-gate voltage	$T_j \geq 25$ °C; $T_j \leq 175$ °C; $R_{GS} = 20$ kΩ	-	80	V
V_{GS}	gate-source voltage		-20	20	V
I_D	drain current	$V_{GS} = 10$ V; $T_{mb} = 100$ °C; see Figure 1	-	16	A
		$V_{GS} = 10$ V; $T_{mb} = 25$ °C; see Figure 1	-	22	A
I_{DM}	peak drain current	pulsed; $t_p \leq 10$ µs; $T_{mb} = 25$ °C; see Figure 3	-	88	A
P_{tot}	total power dissipation	$T_{mb} = 25$ °C;see Figure 2	-	56	W
T_{stg}	storage temperature		-55	175	°C
T_j	junction temperature		-55	175	°C
$T_{sld(M)}$	peak soldering temperature		-	260	°C
Source-drain diode					
I_S	source current	$T_{mb} = 25$ °C	-	22	A
I_{SM}	peak source current	pulsed; $t_p \leq 10$ µs; $T_{mb} = 25$ °C	-	88	A
Avalanche ruggedness					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10$ V; $T_{j(init)} = 25$ °C; $I_D = 22$ A; $V_{sup} \leq 80$ V; $R_{GS} = 50$ Ω; unclamped	-	18	mJ



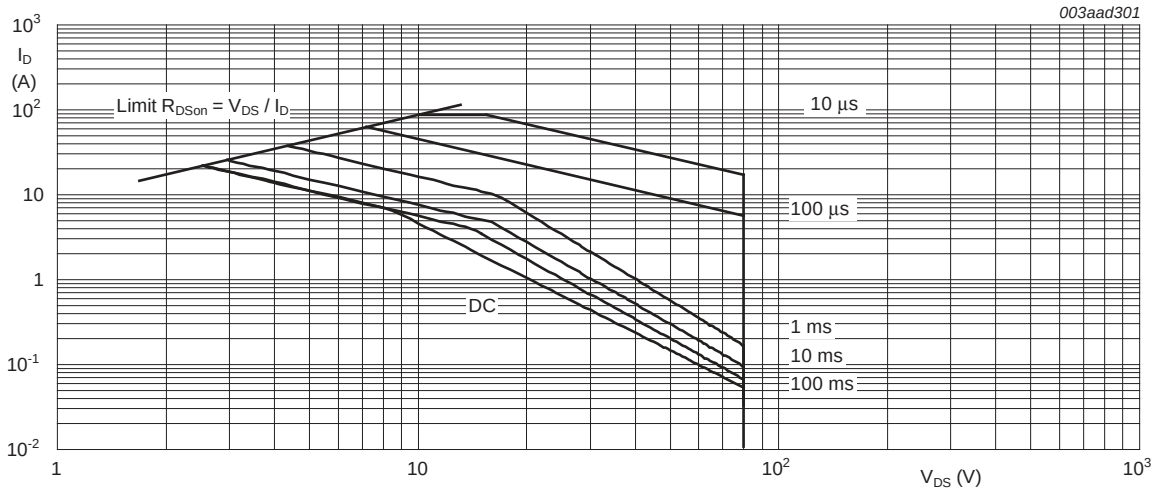
$V_{GS} \geq 10\,V$

Fig 1. Continuous drain current as a function of mounting base temperature



$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\,\%$$

Fig 2. Normalized total power dissipation as a function of mounting base temperature



$T_{mb} = 25°C$; I_{DM} is a single pulse

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j\text{-}mb)}$	thermal resistance from junction to mounting base	see Figure 4	-	2.2	2.7	K/W
$R_{th(j\text{-}a)}$	thermal resistance from junction to ambient	Minimum footprint; mounted on a printed circuit board	-	50	-	K/W

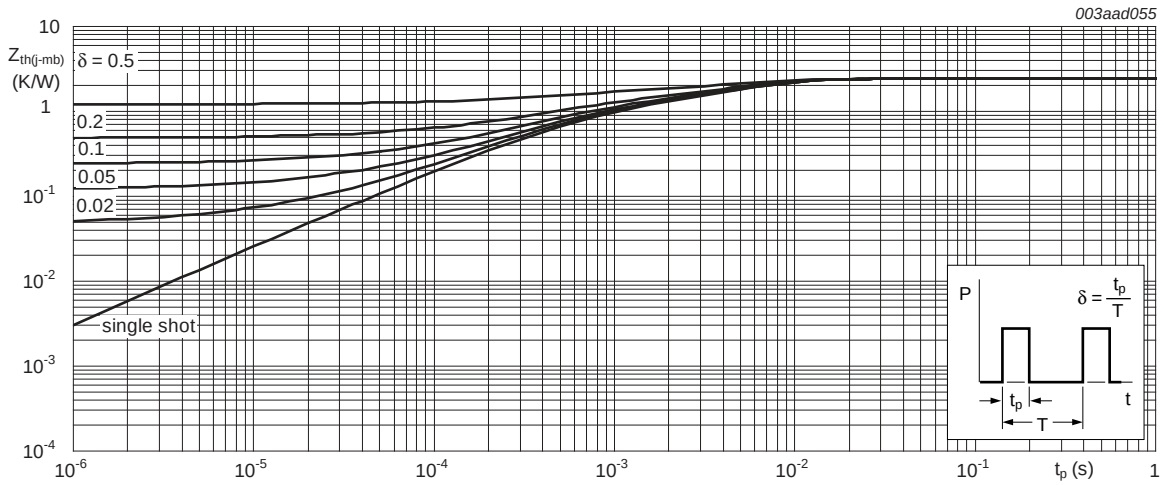


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

6. Characteristics

Table 6. Characteristics

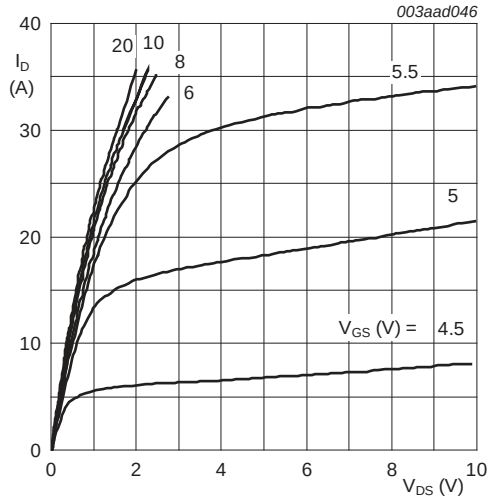
Tested to JEDEC standards where applicable.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 250 µA; V_{GS} = 0 V; T_j = -55 °C	73	-	-	V
		I_D = 250 µA; V_{GS} = 0 V; T_j = 25 °C	80	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}; T_j = 175 °C; see Figure 11; see Figure 12	1	-	-	V
		I_D = 1 mA; V_{DS} = V_{GS}; T_j = -55 °C; see Figure 11; see Figure 12	-	-	4.6	V
		I_D = 1 mA; V_{DS} = V_{GS}; T_j = 25 °C; see Figure 11; see Figure 12	2	3	4	V
I_{DSS}	drain leakage current	V_{DS} = 80 V; V_{GS} = 0 V; T_j = 25 °C	-	-	1	µA
		V_{DS} = 80 V; V_{GS} = 0 V; T_j = 125 °C	-	-	15	µA
I_{GSS}	gate leakage current	V_{GS} = -20 V; V_{DS} = 0 V; T_j = 25 °C	-	-	100	nA
		V_{GS} = 20 V; V_{DS} = 0 V; T_j = 25 °C	-	-	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 10 A; T_j = 100 °C; see Figure 13	-	-	74	mΩ
		V_{GS} = 10 V; I_D = 10 A; T_j = 25 °C	-	37	46	mΩ
R_G	internal gate resistance (AC)	f = 1 MHz	-	2	-	Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	I_D = 0 A; V_{DS} = 0 V; V_{GS} = 10 V	-	9	-	nC
		I_D = 25 A; V_{DS} = 40 V; V_{GS} = 10 V; see Figure 14; see Figure 15	-	11	-	nC
Q_{GS}	gate-source charge		-	3.8	-	nC
$Q_{GS(th)}$	pre-threshold gate-source charge	I_D = 25 A; V_{DS} = 40 V; V_{GS} = 10 V; see Figure 14	-	1.9	-	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge		-	1.9	-	nC
Q_{GD}	gate-drain charge	I_D = 25 A; V_{DS} = 40 V; V_{GS} = 10 V; see Figure 14; see Figure 15	-	2.3	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	V_{DS} = 40 V	-	5.2	-	V
C_{iss}	input capacitance	V_{DS} = 12 V; V_{GS} = 0 V; f = 1 MHz; T_j = 25 °C; see Figure 17	-	633	-	pF
C_{oss}	output capacitance		-	100	-	pF
C_{rss}	reverse transfer capacitance		-	50	-	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 12 V; R_L = 0.5 Ω; V_{GS} = 10 V; $R_{G(ext)}$ = 4.7 Ω	-	9.2	-	ns
t_r	rise time		-	1	-	ns
$t_{d(off)}$	turn-off delay time		-	16	-	ns
t_f	fall time		-	2.4	-	ns

Table 6. Characteristics *...continued*

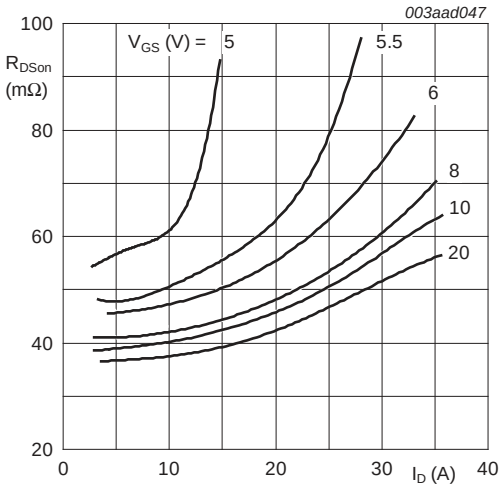
Tested to JEDEC standards where applicable.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Source-drain diode						
V_{SD}	source-drain voltage	I_S = 15 A; V_{GS} = 0 V; T_j = 25 °C; see Figure 16	-	0.86	1.2	V
t_{rr}	reverse recovery time	I_S = 50 A; dI_S/dt = 100 A/µs; V_{GS} = 0 V; V_{DS} = 40 V	-	32	-	ns
Q_r	recovered charge		-	28	-	nC



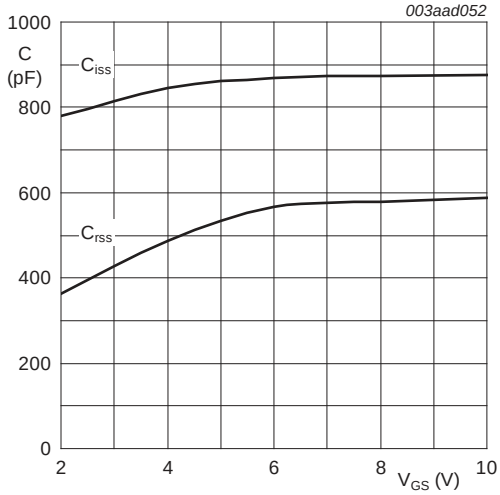
$T_j = 25\,°C;\ t_p = 300\,\mu s$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values



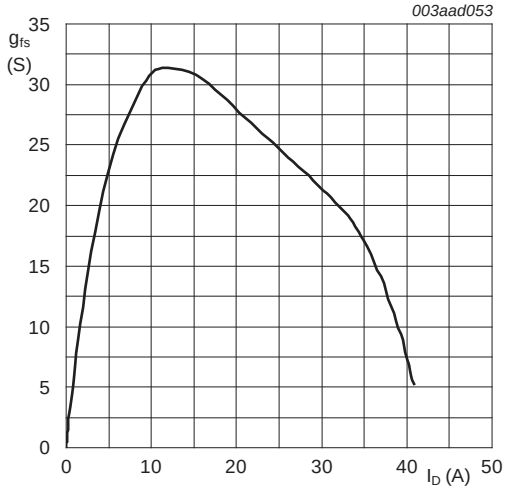
$T_j = 25\,°C;\ t_p = 300\,\mu s$

Fig 6. Drain-source on-state resistance as a function of drain current; typical values



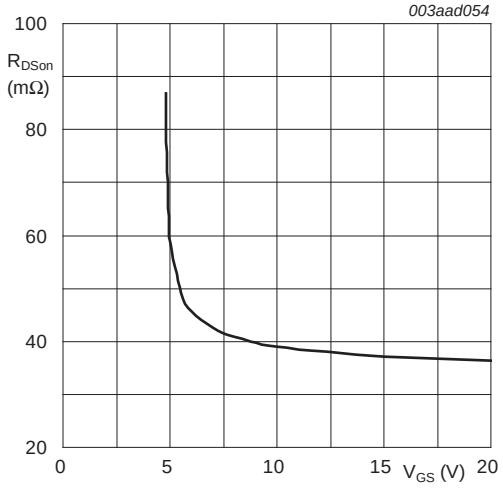
$V_{DS} = 0\,V;\ f = 1\,MHz$

Fig 7. Input and reverse transfer capacitances as a function of gate-source voltage; typical values



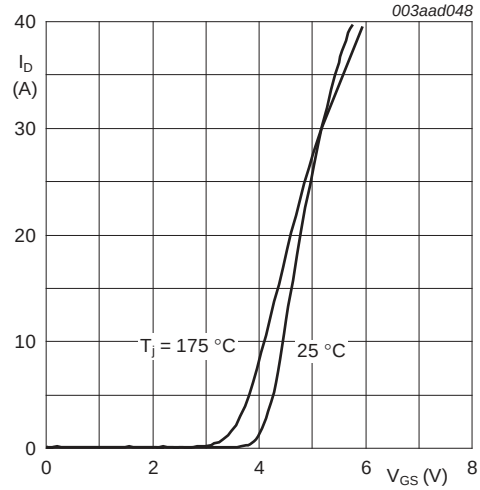
$T_j = 25\,°C;\ V_{DS} = 15\,V$

Fig 8. Forward transconductance as a function of drain current; typical values



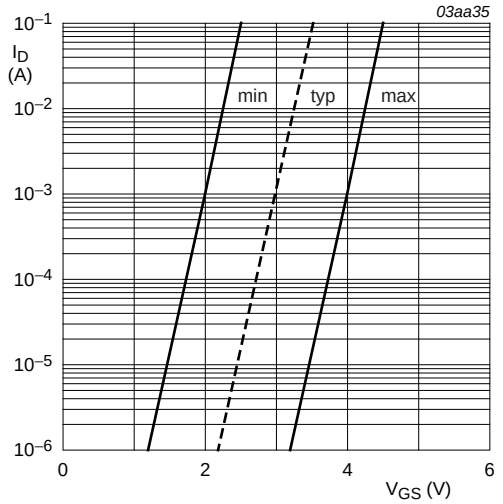
$T_j = 25\,°C; I_D = 10A$

Fig 9. Drain-source on-state resistance as a function of gate-source voltage; typical values



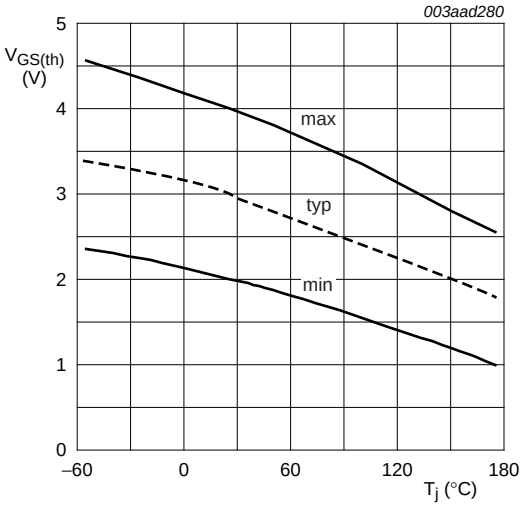
$V_{DS} = 15V$

Fig 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values



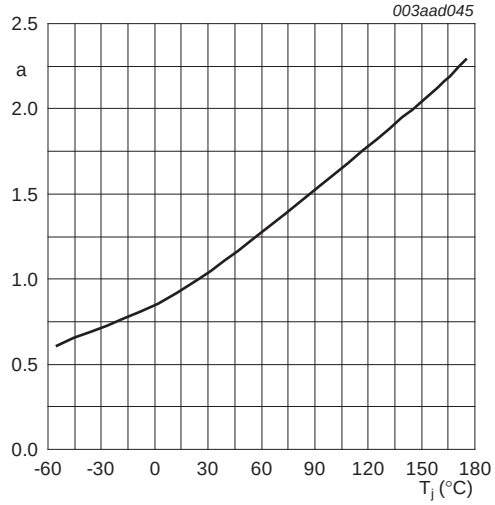
$T_j = 25\,°C; V_{DS} = 5V$

Fig 11. Sub-threshold drain current as a function of gate-source voltage



$I_D = 1\,\text{mA}; V_{DS} = V_{GS}$

Fig 12. Gate-source threshold voltage as a function of junction temperature



$$a = \frac{R_{DSon}}{R_{DSon(25°C)}}$$

Fig 13. Normalized drain-source on-state resistance factor as a function of junction temperature

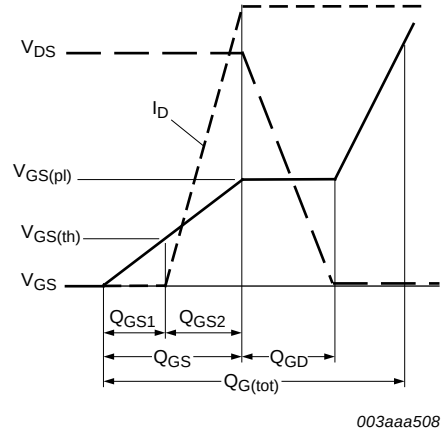
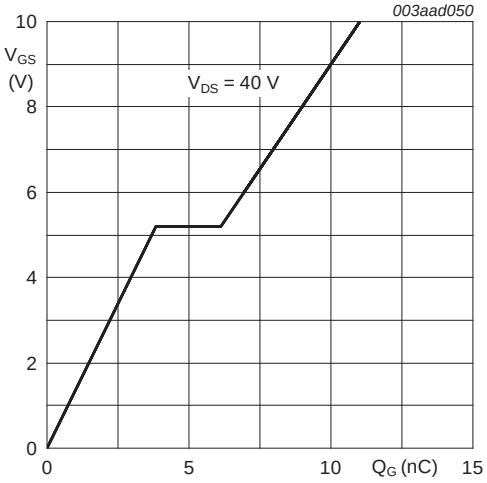
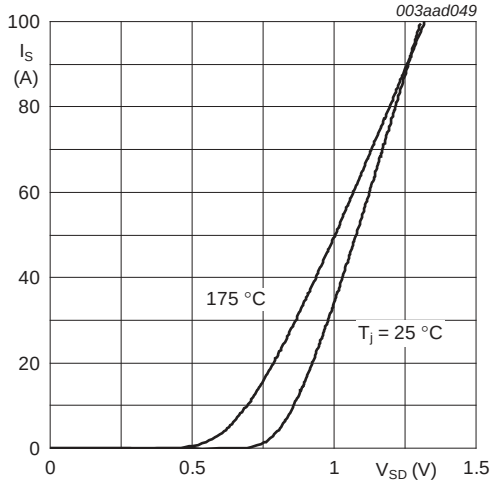


Fig 14. Gate charge waveform definitions



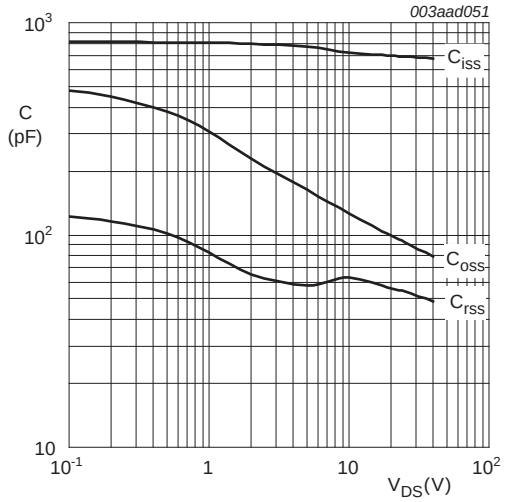
$$T_j = 25\,°C; I_D = 25A$$

Fig 15. Gate-source voltage as a function of gate charge; typical values



$$V_{GS} = 0V$$

Fig 16. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values

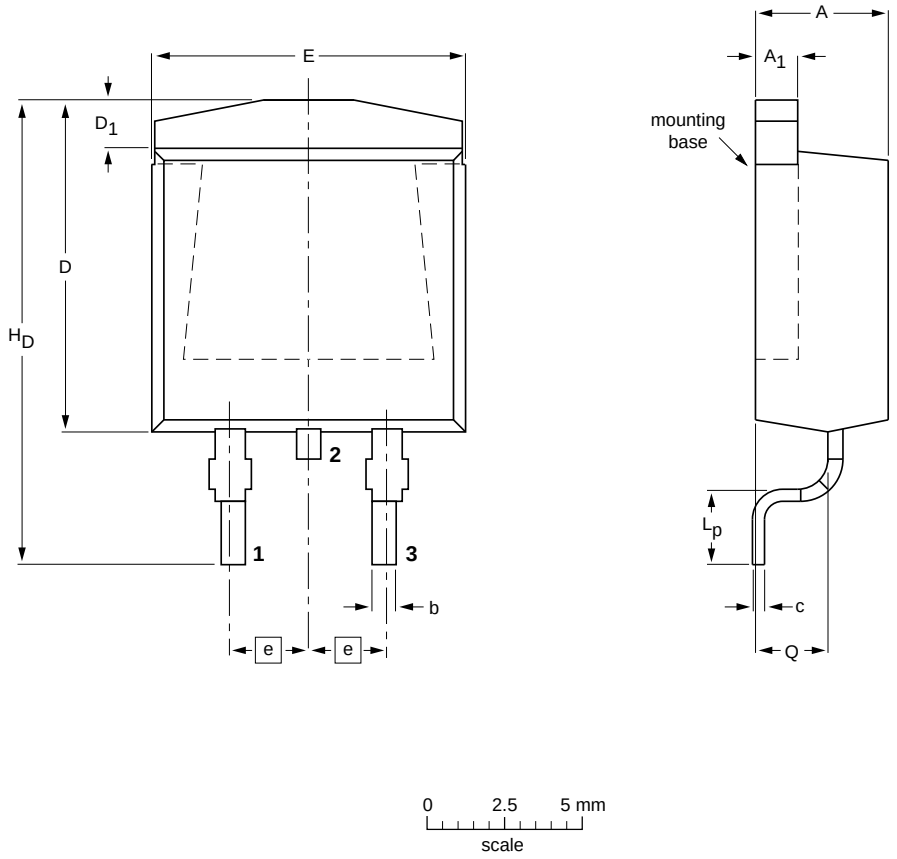


$V_{GS} = 0V; f = 1MHz$

Fig 17. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

7. Package outline

Plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped) **SOT404**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b	c	D max.	D_1	E	e	L_p	H_D	Q
mm	4.50 4.10	1.40 1.27	0.85 0.60	0.64 0.46	11	1.60 1.20	10.30 9.70	2.54	2.90 2.10	15.80 14.80	2.60 2.20

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT404						~~05-02-11~~ 06-03-16

Fig 18. Package outline SOT404 (D2PAK)

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PSMN050-80BS v.1	20120302	Product data sheet	-	-

9. Legal information

9.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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11. Contents

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