# MC14020B

# 14-Bit Binary Counter

The MC14020B 14−stage binary counter is constructed with MOS P−channel and N−channel enhancement mode devices in a single monolithic structure. This part is designed with an input wave shaping circuit and 14 stages of ripple−carry binary counter. The device advances the count on the negative−going edge of the clock pulse. Applications include time delay circuits, counter controls, and frequency−dividing circuits.

- Fully Static Operation
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low−power TTL Loads or One Low−power Schottky TTL Load Over the Rated Temperature Range
- Buffered Outputs Available from stages 1 and 4 thru 14
- Common Reset Line
- Pin−for−Pin Replacement for CD4020B

**MAXIMUM RATINGS** (Voltages Referenced to $V_{SS}$) (Note 2.)

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ | DC Supply Voltage Range | −0.5 to +18.0 | V |
| $V_{in}$, $V_{out}$ | Input or Output Voltage Range (DC or Transient) | −0.5 to $V_{DD}$ + 0.5 | V |
| $I_{in}$, $I_{out}$ | Input or Output Current (DC or Transient) per Pin | ±10 | mA |
| $P_D$ | Power Dissipation, per Package (Note 3.) | 500 | mW |
| $T_A$ | Ambient Temperature Range | −55 to +125 | °C |
| $T_{stg}$ | Storage Temperature Range | −65 to +150 | °C |
| $T_L$ | Lead Temperature (8−Second Soldering) | 260 | °C |

2. Maximum Ratings are those values beyond which damage to the device may occur.
3. Temperature Derating:
   Plastic “P and D/DW” Packages: – 7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, $V_{in}$ and $V_{out}$ should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either $V_{SS}$ or $V_{DD}$). Unused outputs must be left open.

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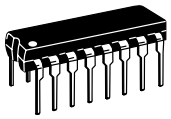
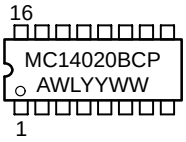
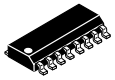
**MARKING DIAGRAMS**

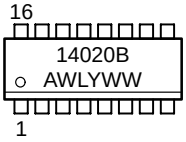


**PDIP−16**
**P SUFFIX**
**CASE 648**

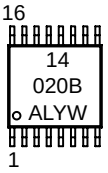


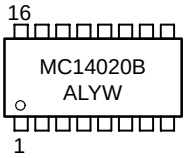
**SOIC−16**
**D SUFFIX**
**CASE 751B**




**TSSOP−16**
**DT SUFFIX**
**CASE 948F**




**SOEIAJ−16**
**F SUFFIX**
**CASE 966**



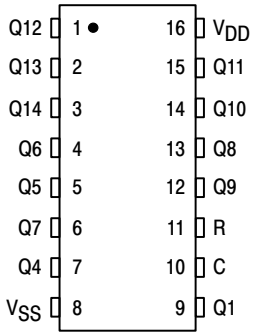

A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MC14020BCP | PDIP−16 | 2000/Box |
| MC14020BD | SOIC−16 | 48/Rail |
| MC14020BDR2 | SOIC−16 | 2500/Tape & Reel |
| MC14020BDT | TSSOP−16 | 96/Rail |
| MC14020BF | SOEIAJ−16 | See Note 1. |
| MC14020BFEL | SOEIAJ−16 | See Note 1. |

1. For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.

## PIN ASSIGNMENT

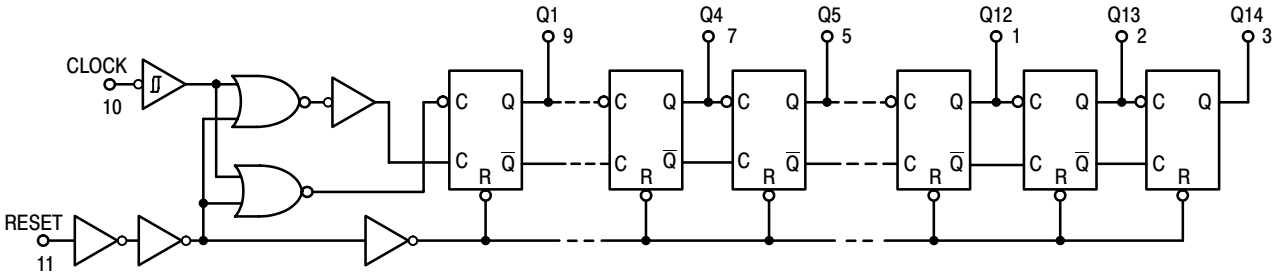



## TRUTH TABLE

| Clock | Reset | Output State |
|---|---|---|
| ↗ | 0 | No Change |
| ↘ | 0 | Advance to Next State |
| X | 1 | All Outputs are Low |

X = Don't Care

## LOGIC DIAGRAM




Q6 = PIN 4
Q7 = PIN 6
Q8 = PIN 13
Q9 = PIN 12
Q10 = PIN 14
Q11 = PIN 15
$V_{DD}$ = PIN 16
$V_{SS}$ = PIN 8

**ELECTRICAL CHARACTERISTICS** (Voltages Referenced to $V_{SS}$)

| Characteristic | Symbol | $V_{DD}$ Vdc | − 55°C Min | − 55°C Max | 25°C Min | 25°C Typ (4.) | 25°C Max | 125°C Min | 125°C Max | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| Output Voltage “0” Level<br>$V_{in}$ = $V_{DD}$ or 0 | $V_{OL}$ | 5.0 | — | 0.05 | — | 0 | 0.05 | — | 0.05 | Vdc |
| | | 10 | — | 0.05 | — | 0 | 0.05 | — | 0.05 | |
| | | 15 | — | 0.05 | — | 0 | 0.05 | — | 0.05 | |
| “1” Level<br>$V_{in}$ = 0 or $V_{DD}$ | $V_{OH}$ | 5.0 | 4.95 | — | 4.95 | 5.0 | — | 4.95 | — | Vdc |
| | | 10 | 9.95 | — | 9.95 | 10 | — | 9.95 | — | |
| | | 15 | 14.95 | — | 14.95 | 15 | — | 14.95 | — | |
| Input Voltage “0” Level | $V_{IL}$ | | | | | | | | | Vdc |
| ($V_O$ = 4.5 or 0.5 Vdc) | | 5.0 | — | 1.5 | — | 2.25 | 1.5 | — | 1.5 | |
| ($V_O$ = 9.0 or 1.0 Vdc) | | 10 | — | 3.0 | — | 4.50 | 3.0 | — | 3.0 | |
| ($V_O$ = 13.5 or 1.5 Vdc) | | 15 | — | 4.0 | — | 6.75 | 4.0 | — | 4.0 | |
| “1” Level | $V_{IH}$ | | | | | | | | | Vdc |
| ($V_O$ = 0.5 or 4.5 Vdc) | | 5.0 | 3.5 | — | 3.5 | 2.75 | — | 3.5 | — | |
| ($V_O$ = 1.0 or 9.0 Vdc) | | 10 | 7.0 | — | 7.0 | 5.50 | — | 7.0 | — | |
| ($V_O$ = 1.5 or 13.5 Vdc) | | 15 | 11 | — | 11 | 8.25 | — | 11 | — | |
| Output Drive Current | $I_{OH}$ | | | | | | | | | mAdc |
| ($V_{OH}$ = 2.5 Vdc) Source | | 5.0 | – 3.0 | — | – 2.4 | – 4.2 | — | – 1.7 | — | |
| ($V_{OH}$ = 4.6 Vdc) | | 5.0 | – 0.64 | — | – 0.51 | – 0.88 | — | – 0.36 | — | |
| ($V_{OH}$ = 9.5 Vdc) | | 10 | – 1.6 | — | – 1.3 | – 2.25 | — | – 0.9 | — | |
| ($V_{OH}$ = 13.5 Vdc) | | 15 | – 4.2 | — | – 3.4 | – 8.8 | — | – 2.4 | — | |
| ($V_{OL}$ = 0.4 Vdc) Sink | $I_{OL}$ | 5.0 | 0.64 | — | 0.51 | 0.88 | — | 0.36 | — | mAdc |
| ($V_{OL}$ = 0.5 Vdc) | | 10 | 1.6 | — | 1.3 | 2.25 | — | 0.9 | — | |
| ($V_{OL}$ = 1.5 Vdc) | | 15 | 4.2 | — | 3.4 | 8.8 | — | 2.4 | — | |
| Input Current | $I_{in}$ | 15 | — | ± 0.1 | — | ±0.00001 | ± 0.1 | — | ± 1.0 | µAdc |
| Input Capacitance ($V_{in}$ = 0) | $C_{in}$ | — | — | — | — | 5.0 | 7.5 | — | — | pF |
| Quiescent Current (Per Package) | $I_{DD}$ | 5.0 | — | 5.0 | — | 0.005 | 5.0 | — | 150 | µAdc |
| | | 10 | — | 10 | — | 0.010 | 10 | — | 300 | |
| | | 15 | — | 20 | — | 0.015 | 20 | — | 600 | |
| Total Supply Current (5.) (6.) (Dynamic plus Quiescent, Per Package) ($C_L$ = 50 pF on all outputs, all buffers switching) | $I_T$ | 5.0 | $I_T$ = (0.42 µA/kHz)f + $I_{DD}$ | | | | | | | µAdc |
| | | 10 | $I_T$ = (0.85 µA/kHz)f + $I_{DD}$ | | | | | | | |
| | | 15 | $I_T$ = (1.43 µA/kHz)f + $I_{DD}$ | | | | | | | |

4. Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.
5. The formulas given are for the typical characteristics only at 25°C.
6. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

where: $I_T$ is in µA (per package), $C_L$ in pF, V = ($V_{DD}$ – $V_{SS}$) in volts, f in kHz is input frequency, and k = 0.001.

**SWITCHING CHARACTERISTICS (7.)** ($C_L$ = 50 pF, $T_A$ = 25°C)

| Characteristic | Symbol | $V_{DD}$ Vdc | Min | Typ (8.) | Max | Unit |
|---|---|---|---|---|---|---|
| Output Rise and Fall Time | $t_{TLH}$, | | | | | ns |
| $t_{TLH}$, $t_{THL}$ = (1.5 ns/pF) $C_L$ + 25 ns | $t_{THL}$ | 5.0 | — | 100 | 200 | |
| $t_{TLH}$, $t_{THL}$ = (0.75 ns/pF) $C_L$ + 12.5 ns | | 10 | — | 50 | 100 | |
| $t_{TLH}$, $t_{THL}$ = (0.55 ns/pF) $C_L$ + 9.5 ns | | 15 | — | 40 | 80 | |
| Propagation Delay Time | $t_{PLH}$, | | | | | ns |
| Clock to Q1 | $t_{PHL}$ | | | | | |
| $t_{PHL}$, $t_{PLH}$ = (1.7 ns/pF) $C_L$ + 175 ns | | 5.0 | — | 260 | 520 | |
| $t_{PHL}$, $t_{PLH}$ = (0.66 ns/pF) $C_L$ + 82 ns | | 10 | — | 115 | 230 | |
| $t_{PHL}$, $t_{PLH}$ = (0.5 ns/pF) $C_L$ + 55 ns | | 15 | — | 80 | 160 | |
| Clock to Q14 | | | | | | ns |
| $t_{PHL}$, $t_{PLH}$ − (1.7 ns/pF) $C_L$ + 1735 ns | | 5.0 | — | 1820 | 3900 | |
| $t_{PHL}$, $t_{PLH}$ = (0.66 ns/pF) $C_L$ + 772 ns | | 10 | — | 805 | 1725 | |
| $t_{PHL}$, $t_{PLH}$ = (0.5 ns/pF) $C_L$ + 535 ns | | 15 | — | 560 | 1200 | |
| Propagation Delay Time | $t_{PHL}$ | | | | | ns |
| Reset to $Q_n$ | | | | | | |
| $t_{PHL}$ = (1.7 ns/pF) $C_L$ + 285 ns | | 5.0 | — | 370 | 740 | |
| $t_{PHL}$ = (0.66 ns/pF) $C_L$ + 122 ns | | 10 | — | 155 | 310 | |
| $t_{PHL}$ = (0.5 ns/pF) $C_L$ + 90 ns | | 15 | — | 115 | 230 | |
| Clock Pulse Width | $t_{WH}$ | 5.0 | 500 | 140 | — | ns |
| | | 10 | 165 | 55 | — | |
| | | 15 | 125 | 38 | — | |
| Clock Pulse Frequency | $f_{cl}$ | 5.0 | — | 2.0 | 1.0 | MHz |
| | | 10 | — | 6.0 | 3.0 | |
| | | 15 | — | 8.0 | 4.0 | |
| Clock Rise and Fall Time | $t_{TLH}$, $t_{THL}$ | 5.0 | No Limit | | | — |
| | | 10 | | | | |
| | | 15 | | | | |
| Reset Pulse Width | $t_{WL}$ | 5.0 | 3000 | 320 | — | ns |
| | | 10 | 550 | 120 | — | |
| | | 15 | 420 | 80 | — | |
| Reset Removal Time | $t_{rem}$ | 5.0 | 130 | 65 | — | ns |
| | | 10 | 50 | 25 | — | |
| | | 15 | 30 | 15 | — | |

7. The formulas given are for the typical characteristics only at 25°C.
8. Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.

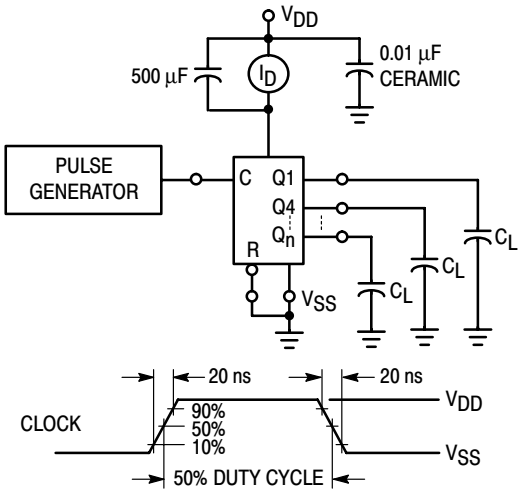



**Figure 1. Power Dissipation Test Circuit and Waveform**

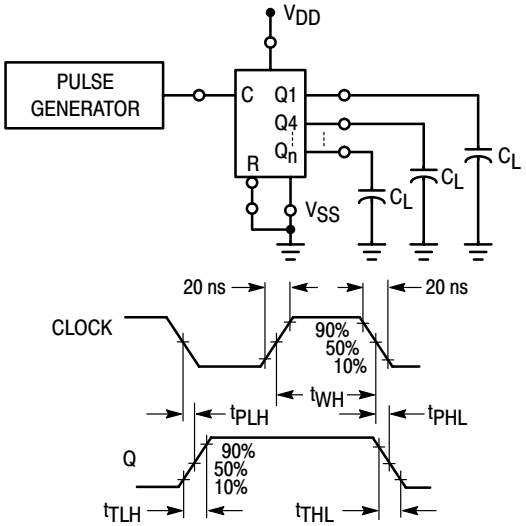



**Figure 2. Switching Time Test Circuit and Waveforms**

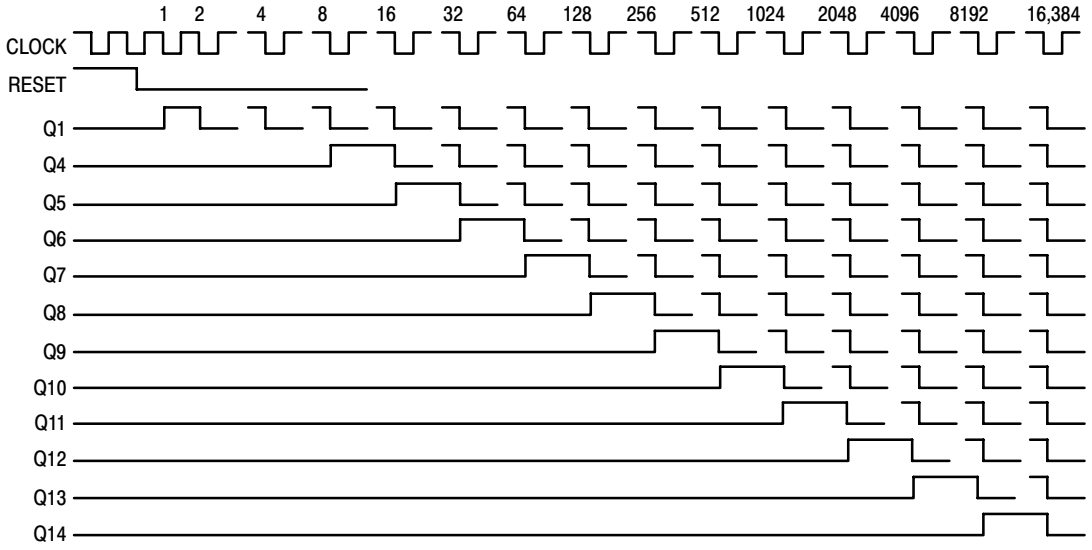



**Figure 3. Timing Diagram**