Advance Information

MCF5485EC/D
Rev. 1.2, 3/2004

MCF548x Integrated Microprocessor Hardware Specifications

The MCF548*x* is a highly-integrated implementation of the ColdFire® family of reduced instruction set computing (RISC) microprocessors. This document describes pertinent electrical and physical characteristics of the MCF548*x* family: the MCF5480, MCF5481, MCF5482, MCF5483, MCF5484, and MCF5485.

This document contains the following topics:

To locate any published errata or updates for this document, refer to the web site at http://motorola.com/semiconductors.

1.1 MCF548*x* Family Overview

The MCF548*x* family is based on the ColdFire V4e core, a complex which comprises the ColdFire V4 central processor unit (CPU), an enhanced multiply-accumulate unit (EMAC), a memory management unit (MMU), a double-precision floating point unit (FPU) conforming to standard IEEE-754, and controllers for caches and local data memories. The MCF548*x* family is capable of performing at an operating frequency of up to 200 MHz or 308 MIPS (Dhrystone 2.1).

To maximize throughput, the MCF548*x* family incorporates three independent external bus interfaces:

1. The general-purpose local bus (FlexBus) is used for system boot memories and simple peripherals and has up to six chip selects.
2. Program code and data can be stored in SDRAM connected to a dedicated 32-bit double data rate (DDR) bus that can run at up to one half of the CPU core frequency. The glueless DDR SDRAM controller handles all address multiplexing, input and output strobe timing, and memory bus clock generation.
3. A 32-bit PCI bus compliant with the version 2.2 specification and running at a typical frequency of 33 MHz or 66 MHz supports peripherals that require high bandwidth, the ability to arbitrate for bus mastership, and access to internal MCF548*x* memory resources.

The MCF548*x* family provides substantial communications functionality by integrating the following connectivity peripherals:

- Up to two 10/100 Mbps fast Ethernet controllers (FECs)
- An optional USB 2.0 device (slave) module with seven endpoints and an integrated transceiver
- Up to four UART/USART/IRDA/modem programmable serial controllers (PSCs)
- A DMA serial peripheral interface (DSPI)
- An inter-integrated circuit ($I^2C^{™}$) bus controller
- Two controller area network 2.0B (FlexCAN) interfaces with 16 message buffers each

Additionally, the MCF548*x* provides hardware support for a range of Internet security standards with an optional bus-mastering cryptography accelerator. This module incorporates units to speed DES/3DES and AES block ciphers, the RC4 stream cipher, bulk data hashing (MD5/SHA-1/SHA-256/HMAC), and random number generation. Hardware acceleration of these functions is critical to avoiding the throughput bottlenecks associated with software-only implementations of SSH, SSL/TLS, IPsec, SRTP, WEP, and other security standards. The incorporation of cryptography acceleration makes the MCF548*x* family a compelling solution for a wide range of office automation, industrial control, and SOHO networking devices that must have the ability to securely transmit critical equipment control information across typically insecure Ethernet data networks.

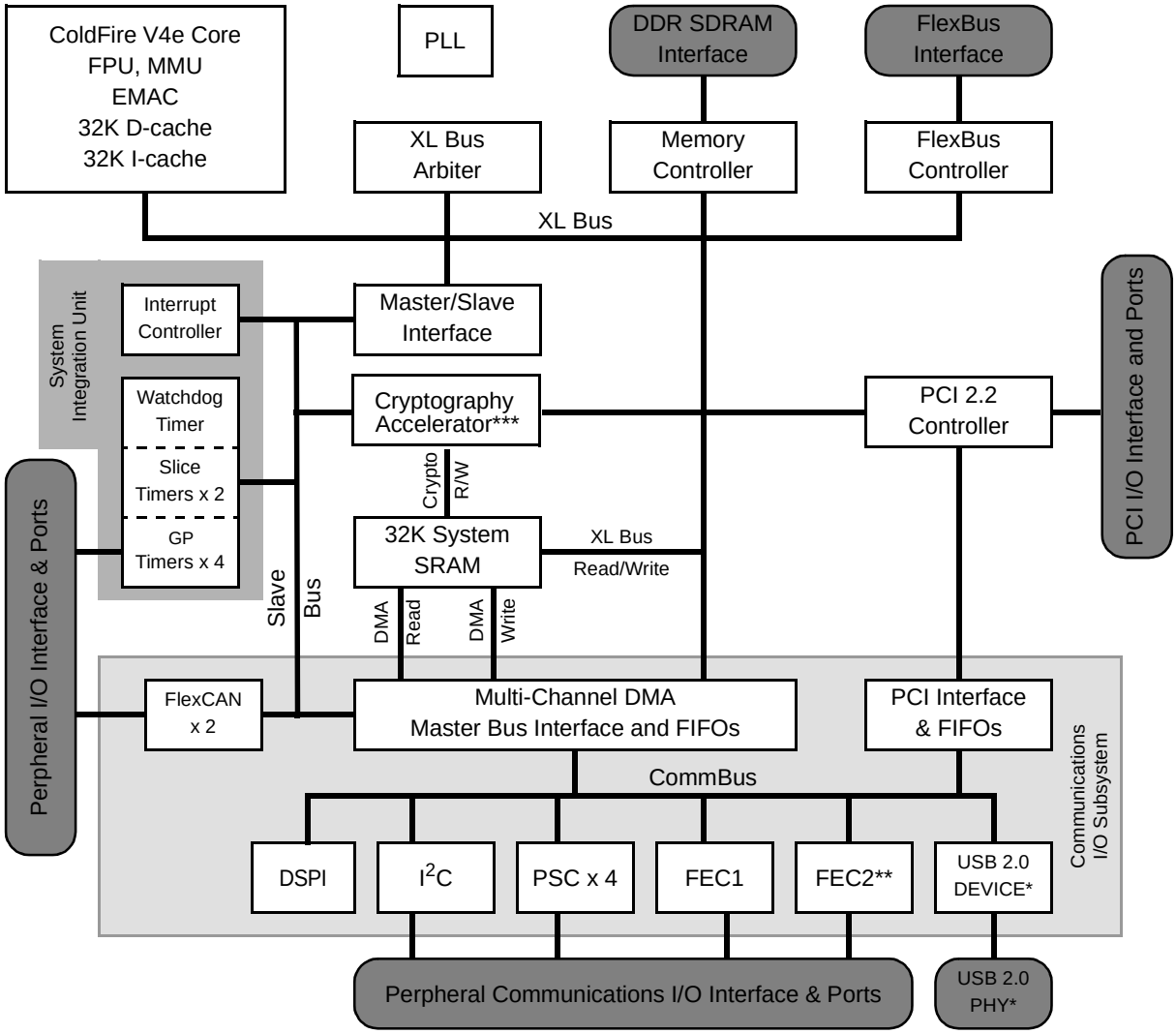
Additional features of MCF548*x* products include a watchdog timer, two 32-bit slice timers for RTOS scheduling and alarm functionality, up to four 32-bit general-purpose timers with capture, compare, and pulse width modulation capability, a multisource vectored interrupt controller, a phase-locked loop (PLL) to generate the system clock, 32 Kbytes of SRAM for high-speed local data storage, and multiple general-purpose I/O ports. To manage current consumption, MCF548*x* products provide chip-wide internal clock gating control on a per module basis under software control.

With on-chip support for multiple common communications interfaces, MCF548*x* products require only the addition of memories and certain physical layer transceivers to be cost-effective system solutions for many applications, such as industrial routers, high-end POS terminals, building automation systems, and process control equipment.

MCF548*x* products require four supply voltages: 1.5V for the high-performance, low power, internal core logic, 2.5V for the DDR SDRAM bus interface, 1.25V for the DDR SDRAM V_{REF}, and 3.3V for all other I/O functionality, including the PCI and FlexBus interfaces.

1.2 MCF548*x* Block Diagram

Figure 1 shows a top-level block diagram of the MCF548*x* products.



*Available in MCF5485, MCF5484, MCF5483, and MCF5482 devices.
**Available in MCF5485, MCF5484, MCF5481, and MCF5480 devices.
***Available in MCF5485, MCF5483, and MCF5481 devices.

Figure 1. MCF548*x* Block Diagram

1.3 MCF548*x* Family Products

Table 1 summarizes the products available within the MCF548*x* product family. All products are available in pin-compatible, 388 pin PBGA packaging allowing for ease of mirgration between products within the family. A printed circuit board designed using the MCF5485/4 footprint is compatible with any of the MCF548*x* family devices.

Table 1. MCF548*x* Family Products

Product	Performance	Features	Temperature Range
MCF5485	308 MIPS 200 MHz	Two 10/100 Ethernet Controllers Two CAN Controllers USB 2.0 Device with Integrated PHY v2.2 PCI Controller DDR Memory Controller Encryption Accelerator	-40 to 85 ° C
MCF5484	308 MIPS 200 MHz	Two 10/100 Ethernet Controllers Two CAN Controllers USB 2.0 Device with Integrated PHY v2.2 PCI Controller DDR Memory Controller	-40 to 85 ° C
MCF5483	255 MIPS 166 MHz	One 10/100 Ethernet Controller Two CAN Controllers USB 2.0 Device with Integrated PHY v2.2 PCI Controller DDR Memory Controller Encryption Accelerator	-40 to 85 ° C
MCF5482	255 MIPS 166 MHz	One 10/100 Ethernet Controller Two CAN Controllers USB 2.0 Device with Integrated PHY v2.2 PCI Controller DDR Memory Controller	-40 to 85 ° C
MCF5481	255 MIPS 166 MHz	Two 10/100 Ethernet Controllers Two CAN Controllers v2.2 PCI Controller DDR Memory Controller Encryption Accelerator	-40 to 85 ° C
MCF5480	255 MIPS 166 MHz	Two 10/100 Ethernet Controllers Two CAN Controllers v2.2 PCI Controller DDR Memory Controller	-40 to 85 ° C

1.4 MCF548*x* Family Features

- ColdFire V4e core
  - — Limited superscalar V4 ColdFire processor core
  - — Up to 200 MHz peak internal core frequency (308 Dhrystone 2.1 MIPS)
  - — Harvard architecture
    - – 32-Kbyte instruction cache
    - – 32-Kbyte data cache
  - — Memory management unit (MMU)
    - – Separate, 32-entry, fully-associative instruction and data translation lookahead buffers
  - — Floating point unit (FPU)
    - – Double-precision support that conforms to IEEE-754 standard
    - – Eight floating point registers
- Internal master bus (XLB) arbiter
  - — High performance split address and data transactions
  - — Support for various parking modes
- 32-bit double data rate (DDR) synchronous DRAM (SDRAM) controller
  - — 66–133 MHz operation
  - — Supports both DDR and SDR DRAM
  - — Built-in initialization and refresh
  - — Up to four chip selects enabling up to 1 GB of external memory
- Version 2.2 peripheral component interconnect (PCI) bus
  - — 32-bit target and initiator operation
  - — Support for up to five external PCI masters
  - — 33–66 MHz operation with PCI bus to XLB divider ratios of 1:1, 1:2, and 1:4
- Flexible multifunction external bus (FlexBus)
  - — Supports operation with the following:
    - – Non-multiplexed 32-bit address and 32-bit data (32-bit address muxed over PCI bus–PCI not usable)
    - – Multiplexed 32-bit address and 32-bit data (PCI usable)
    - – Multiplexed 32-bit address and 16-bit data
    - – Multiplexed 32-bit address and 8-bit data
  - — Provides a glueless interface to boot Flash/ROM, SRAM, and peripheral devices
  - — Up to six chip selects
  - — 33–66 MHz operation
- Communications I/O subsystem
  - — Intelligent 16-channel DMA controller
  - — Dedicated DMA channels for receive and transmit on all subsystem peripheral interfaces

  - — Up to two 10/100 Mbps fast Ethernet controllers (FECs), each with separate 2-Kbyte receive and transmit FIFOs
  - — Universal serial bus (USB) version 2.0 device controller
    - – Support for one control and six programmable endpoints — interrupt, bulk, or isochronous
    - – 4 Kbytes of shared endpoint FIFO RAM and 1 Kbyte of endpoint descriptor RAM
    - – Integrated physical layer interface
  - — Up to four programmable serial controllers (PSCs) each with separate 512-byte receive and transmit FIFOs for UART, USART, modem, codec, and IrDA 1.1 interfaces
  - — I^2C peripheral interface
  - — Two FlexCAN controller area network 2.0B controllers each with 16 message buffers
  - — DMA serial peripheral interface (DSPI)
- Optional security encryption controller (SEC) module
  - — Execution units for the following:
    - – DES/3DES block cipher
    - – AES block cipher
    - – RC4 stream cipher
    - – MD5/SHA-1/SHA-256/HMAC hashing
    - – Random number generator compliant with FIPS 140-1 standards for randomness and non-determinism
  - — Dual-channel architecture permits single-pass encryption and authentication
- 32-Kbyte system SRAM
  - — Arbitration mechanism shares bandwidth between internal bus masters (CPU, cryptography accelerator, PCI, and DMA)
- System integration unit (SIU)
  - — Interrupt controller
  - — Watchdog timer
  - — Two 32-bit slice timers for periodic alarm and interrupt generation
  - — Up to four 32-bit general-purpose timers with capture, compare, and PWM capability
  - — General-purpose I/O ports multiplexed with peripheral pins
- Debug and test features
  - — Core debug support via ColdFire background debug mode (BDM) port
  - — Chip debug support via JTAG/ IEEE 1149.1 test access port
- PLL and clock generator
  - — 30–66.67 MHz input frequency range
- Operating Voltages
  - — 1.5V internal logic
  - — 2.5V DDR SDRAM bus I/O (1.25V V_{REF})
  - — 3.3V PCI, FlexBus, and all other I/O
- Estimated power consumption
  - — <1.5W

1.4.1 ColdFire V4e Core Overview

The ColdFire V4e core is a variable-length RISC, clock-multiplied core that includes a Harvard memory architecture, branch cache acceleration logic, and limited superscalar dual-instruction issue capabilities. The limited superscalar design approaches dual-issue performance with the cost of a scalar execution pipeline.

The ColdFire V4e processor core is comprised of two separate pipelines that are decoupled by an instruction buffer. The four-stage instruction fetch pipeline (IFP) prefetches the instruction stream, examines it to predict changes of flow, partially decodes instructions, and packages fetched data into instructions for the operand execution pipeline (OEP). The IFP can prefetch instructions before the OEP needs them, minimizing the wait for instructions. The instruction buffer is a 10 instruction, first-in-first-out (FIFO) buffer that decouples the IFP and OEP by holding prefetched instructions awaiting execution in the OEP. The OEP includes five pipeline stages: the first stage decodes instructions and selects operands (DS), and the second stage generates operand addresses (OAG). The third and fourth stages fetch operands (OC1 and OC2), and the fifth stage executes instructions (EX).

The ColdFire V4e processor contains a double-precision floating point unit (FPU). The FPU conforms to the American National Standards Institute (ANSI)/Institute of Electrical and Electronics Engineers (IEEE) *Standard for Binary Floating-Point Arithmetic* (ANSI/IEEE Standard 754). The FPU operates on 64-bit, double-precision floating point data and supports single-precision and signed integer input operands. The FPU programming model is like that in the MC68060 microprocessor. The FPU is intended to accelerate the performance of certain classes of embedded applications, especially those requiring high-speed floating point arithmetic computations.

The ColdFire V4e processor also incorporates the ColdFire memory management unit (MMU), which provides virtual-to-physical address translation and memory access control. The MMU consists of memory-mapped control, status, and fault registers that provide access to translation lookaside buffers (TLBs). Software can control address translation and access attributes of a virtual address by configuring MMU control registers and loading TLBs. With software support, the MMU provides demand-paged, virtual addressing.

The ColdFire V4e core implements the ColdFire instruction set architecture revision B with support for floating Point instructions. Additionally, the ColdFire V4e core includes the enhanced multiply-accumulate unit (EMAC) for improved signal processing capabilities. The EMAC implements a 4-stage execution pipeline, optimized for 32 x 32 bit operations, with support for four 48-bit accumulators. Supported operands include 16- and 32-bit signed and unsigned integers as well as signed fractional operands and a complete set of instructions to process these data types. The EMAC provides superb support for execution of DSP operations within the context of a single processor at a minimal hardware cost.

1.4.2 Debug Module (BDM)

The ColdFire processor core debug interface is provided to support system debugging in conjunction with low-cost debug and emulator development tools. Through a standard debug interface, users can access real-time trace and debug information. This allows the processor and system to be debugged at full speed without the need for costly in-circuit emulators.

The MCF548*x* debug module provides support in three different areas:

- Real-time trace support: The ability to determine the dynamic execution path through an application is fundamental for debugging. The ColdFire solution implements an 8-bit parallel output bus that reports processor execution status and data to an external BDM emulator system.

- Background debug mode (BDM): Provides low-level debugging in the ColdFire processor complex. In BDM, the processor complex is halted and a variety of commands can be sent to the processor to access memory and registers. The external BDM emulator uses a three-pin, serial, full-duplex channel.
- Real-time debug support: BDM requires the processor to be halted, which many real-time embedded applications cannot permit. Debug interrupts let real-time systems execute a unique service routine that can quickly save key register and variable contents and return the system to normal operation without halting. External development systems can access saved data because the hardware supports concurrent operation of the processor and BDM-initiated commands. In addition, the option is provided to allow interrupts to occur.

1.4.3 JTAG

The MCF548*x* family supports circuit board test strategies based on the Test Technology Committee of IEEE and the Joint Test Action Group (JTAG). The test logic includes a test access port (TAP) consisting of a 16-state controller, an instruction register, and three test registers (a 1-bit bypass register, a 256-bit boundary-scan register, and a 32-bit ID register). The boundary scan register links the device's pins into one shift register. Test logic, implemented using static logic design, is independent of the device system logic. The MCF548*x* implementation can do the following:

- Perform boundary scan operations to test circuit board electrical continuity
- Sample MCF548*x* system pins during operation and transparently shift out the result in the boundary scan register
- Bypass the MCF548*x* for a given circuit board test by effectively reducing the boundary-scan register to a single bit
- Disable the output drive to pins during circuit-board testing
- Drive output pins to stable levels

1.4.4 On-Chip Memories

1.4.4.1 Caches

There are two independent caches associated with the ColdFire V4e core complex: a 32-Kbyte instruction cache and a 32-Kbyte data cache. Caches improve system performance by providing single-cycle access to the instruction and data pipelines. This decouples processor performance from system memory performance, increasing bus availability for on-chip DMA or external devices.

1.4.4.2 System SRAM

The SRAM module provides a general-purpose 32-Kbyte memory block that the ColdFire core can access in a single cycle. The location of the memory block can be set to any 32-Kbyte address boundary within the 4-Gbyte address space. The memory is ideal for storing critical code or data structures, for use as the system stack, or for storing FEC data buffers. Because the SRAM module is physically connected to the processor's high-speed local bus, it can quickly service core-initiated accesses or memory-referencing commands from the debug module.

The SRAM module is also accessible by multiple non-core bus masters, such as the DMA controller, the encryption accelerator, and the PCI Controller.

1.4.5 PLL and Chip Clocking Options

MCF548*x* products contain an on-chip PLL capable of accepting input frequencies from 30–66.66 MHz. Table 2 contains the frequencies of the system buses for the members of the MCF548*x* family under various core/SDRAM/PCI/Flexbus clocking options.

Table 2. MCF548x Family Clocking Options

Core (MHz)	Internal XLB and SDRAM Bus Frequency (MHz)	CLKIN—PCI and FlexBus Frequency (MHz)	Clock Ratio
120.0–200	60.0–100	30.0–50.0	1:2

1.4.6 Communications I/O Subsystem

1.4.6.1 DMA Controller

The communications subsystem contains an intelligent DMA unit that provides front line interrupt control and data movement interface via a separate peripheral bus to the on-chip peripheral functions, leaving the processor core free to handle higher level activities. This concurrent operation enables a significant boost in overall system performance.

The communications subsystem can support up to 16 simultaneously enabled DMA tasks, with support for up to 2 external DMA requests. It uses internal buffers to prefetch reads and post writes such that bursting is used whenever possible. This optimizes both internal and external bus activity. The following communications and computer control peripheral functions are integrated and controlled by the communications subsystem:

- Up to two 10/100 Mbps fast Ethernet controllers (FECs)
- Optional universal serial bus (USB) version 2.0 device controller
- Up to four programmable serial controllers (PSCs)
- I^2C peripheral interface
- DMA serial peripheral interface (DSPI)
- Two FlexCAN controller area network 2.0B controllers

1.4.6.2 10/100 Fast Ethernet Controller (FEC)

The FEC supports the following standard MAC/PHY interfaces: 10/100 Mbps IEEE 802.3 MII, and 10Mbps 7-wire interface. The controller is full duplex, supports a programmable maximum frame length and retransmission from the transmit FIFO following a collision.

Support for different Ethernet physical interfaces:

  - 100 Mbps IEEE 802.3 MII
  - 10 Mbps IEEE 802.3 MII
  - 10 Mbps 7-wire interface
- IEEE 802.3 full-duplex flow control.
- Support for full-duplex operation (200 Mbps throughput) with a minimum system clock frequency of 50 MHz.

- Support for half duplex operation (100 Mbps throughput) with a minimum system clock frequency of 25 MHz.
- Retransmit from transmit FIFO following collision.
- Internal loopback for diagnostic purposes.

1.4.6.3 USB 2.0 Device (Universal Serial Bus)

The USB module implementation on the MCF548*x* product family provides all the logic necessary to process the USB protocol as defined by version 2.0 specification for peripheral devices.

- High-speed operation up to 480 Mbps, full-speed operation at 12 Mbps, and low-speed operation at 1.5 Mbps
- Physical interface on chip
- Bulk, interrupt, and isochronous transport modes.
- Six programmable in/out endpoints and one control endpoint
- 4 Kbytes of shared endpoint FIFO RAM and 1 Kbyte of endpoint descriptor RAM

1.4.6.4 Programmable Serial Controllers (PSCs)

The MCF548*x* product family supports four PSCs that can be independently configured to operate in the following modes:

- Universal asynchronous receiver transmitter (UART) mode
  - 5,6,7,8 bits of data plus parity
  - Odd, even, none, or force parity
  - Stop bit width programmable in 1/16 bit increments
  - Parity, framing, and overrun error detection
  - Automatic $\overline{\text{PSCCTS}}$ and $\overline{\text{PSCRTS}}$ modem control signals
- IrDA 1.0 SIR mode (SIR)
  - Baud rate range of 2400–115200 bps
  - Selectable pulse width: either 3/16 of the bit duration or 1.6 µs
- IrDA 1.1 MIR mode (MIR)
  - Baud rate of 0.576 or 1.152 Mbps
- IrDA 1.1 FIR mode (FIR)
  - Baud rate of 4.0 Mbps
- 8-bit soft modem mode (modem8)
- 16-bit soft modem mode (modem16)
- AC97 soft modem mode (AC97)

Each PSC supports synchronous (USART) and asynchronous (UART) protocols. The PSCs can be used to interface to external full-function modems or external codecs for soft modem support, as well as IrDA 1.1 or 1.0 interfaces. Both 8- and 16-bit data widths are supported. PSCs can be configured to support 1200 baud plain old telephone system (POTS) modem, V.34 or V.90 protocols. The standard UART interface supports connection to an external terminal/computer for debug support.

1.4.6.5 I^2C (Inter-Integrated Circuit)

The MCF548*x* product family provides an I^2C two-wire, bidirectional serial bus for on-board communication.

- Multimaster operation with arbitration and collision detection
- Calling address recognition and interrupt generation
- Automatic switching from master to slave on arbitration loss
- Software-selectable acknowledge bit
- Start and stop signal generation and detection
- Bus busy status detection

1.4.6.6 DMA Serial Peripheral Interface (DSPI)

The DSPI block operates as a basic SPI block with FIFOs providing support for external queue operation. Data to be transmitted and data received reside in separate FIFOs. The FIFOs can be popped and pushed by host software or by the system DMA controller. The DSPI supports these SPI features:

- Full-duplex, three-wire synchronous transfers
- Master and slave mode—two peripheral chip selects in master mode
- DMA support

1.4.6.7 Controller Area Network (CAN)

The FlexCAN modules are communication controllers implementing the CAN protocol. The CAN protocol can be used as an industrial control serial data bus, meeting the specific requirements of real-time processing and reliable operation in a harsh EMI environment, while maintaining cost-effectiveness. Each of the two CAN controllers on the MCF548*x* family products contains sixteen message buffers. The CAN controllers can be configured to either function as an interface with two separate CAN networks, or as a single 32 message buffer CAN network.

1.4.7 DDR SDRAM Memory Controller

The DDR SDRAM memory controller is a glueless interface to DDR memories. The module uses a 32 bit memory port and can address a maximum of 1 Gbyte of data with sixteen 64M x 8 (512-Mbit) devices, 4 per chip select. The controller supplies two clock lines and respective inverted clock lines to help minimize system complexity when using DDR. The module supports either DDR or SDR but not both. This is due to voltage differences between the memory technologies. The supported memory clock rate is up to 133 MHz. At this memory clock rate, DDR memory can receive data at an effective rate of up to 266 MHz.

- Support for up to 13 lines of row address, 11 lines of column address, 2 lines of bank address, and up to 4 chip selects
- Memory bus width fixed at 32 bits
- Four chip selects support up to 1 GByte of SDRAM memory
- Support for page mode to maximize the data rate. Page mode remembers active pages for all four chip selects
- Support for sleep mode and self refresh

- Cache line reads that can use critical word first. These reads can start in the center of a burst and will wrap to the beginning. This allows the processor quicker access to a needed instruction.

All on-chip bus masters have access to DRAM. This includes PCI, the ColdFire V4e core, the cryptography accelerator, and the DMA controller.

1.4.8 Peripheral Component Interconnect (PCI)

The PCI controller is a PCI V2.2-compliant bus controller and arbiter. The PCI bus is capable of 66-MHz operation with a 32-bit address/data bus and support for five external masters.

The PCI module includes an inbound FIFO to increase performance when using an external bus master. The bus can address all 4 Gbytes of PCI-addressable space.

The PCI bus is also multiplexed with the flexible local bus (FlexBus) address lines. If 32-bit non-muxed local address and data is required it can be obtained at the expense of utilizing the PCI bus.

When implemented, the PCI controller acts as the central resource, bus arbiter, and configuring master on the PCI bus.

1.4.9 Flexible Local Bus (FlexBus)

The FlexBus module is intended to provide the user with basic functionality required to interface to peripheral devices. The FlexBus interface is a multiplexed or non-multiplexed bus, with an operating frequency from 33–66 MHz. The Flexbus is targeted to support external Flash memories, boot ROMs, gate-array logic, or other simple target interfaces. Up to six chip selects are supported by the FlexBus.

Possible combinations of address and data bits are:

- Non-multiplexed 32-bit address and 32-bit data (32-bit address muxed over PCI bus–PCI not usable)
- Multiplexed 32-bit address and 32-bit data (PCI usable)
- Multiplexed 32-bit address and 16-bit data
- Multiplexed 32-bit address and 8-bit data

The non-multiplexed 32-bit address and 32-bit data mode is determined at chip reset. For all other modes, the full 32-bit address is driven during the address phase. The number of bytes used for data are determined on a chip select by chip select basis.

1.4.10 Security Encryption Controller (SEC)

As consumers and businesses continue to embrace the Internet, the need for secure point-to-point communications across what is an entirely insecure network has been met by the development of a range of standard protocols. Computer cryptography fundamentally involves calculations with very large numbers. Personal computers have sufficient processing power to implement these algorithms entirely in software. When placed upon the embedded devices typically used for routing and remote access functions, this same computational burden can potentially decrease the throughput of a 100 Mbps Ethernet interface down to 10 Mbps.

Hardware acceleration of common cryptography algorithms is the solution to the computational bandwidth requirements of Internet security standards. Discrete solutions currently address this problem, but the next

logical step is to integrate a cryptography accelerator on an embedded processor, such as the MCF548*x* family.

Motorola has developed the SEC on the MCF548*x* family for this purpose. This block accelerates the core cryptography algorithms that underlie standard Internet security protocols like SSL/TLS, IPSec, IKE, and WTLS/WAP.

- The SEC includes execution units for the following:
  - — DES/3DES block cipher
  - — AES block cipher
  - — RC4 stream cipher
  - — MD5/SHA-1/SHA-256/HMAC hashing
  - — Random number generator compliant with FIPS 140-1 standards for randomness and non-determinism
- Dual-channel architecture permits single-pass encryption and authentication

1.4.11 System Integration Unit (SIU)

1.4.11.1 Timers

The MCF548*x* family integrates several timer functions required by most embedded systems. Two internal 32-bit slice timers are provided to create short cycle periodic interrupts, typically utilized for RTOS scheduling and alarm functionality. A watchdog timer is included which will reset the processor if not regularly serviced, catching software hang-ups. Four 32-bit general purpose timers are included, which are capable of input capture, output compare, and PWM functionality.

1.4.11.2 Interrupt Controller

The interrupt controller on the MCF548*x* family can support up to 63 interrupt sources. The interrupt controller is organized as seven levels with nine interrupt sources per level. Each interrupt source has a unique interrupt vector, and 56 of the 63 sources of a given controller provide a programmable level [1-7] and priority within the level.

- Support for up to 63 interrupt sources organized as follows:
  - — 56 fully-programmable interrupt sources
  - — 7 fixed-level interrupt sources
- Seven external interrupt signals
- Unique vector number for each interrupt source
- Ability to mask any individual interrupt source or all interrupt sources (global mask-all)
- Support for hardware and software interrupt acknowledge (IACK) cycles
- Combinatorial path to provide wake-up from low power modes

1.4.11.3 General Purpose I/O

All peripheral I/O pins on the MCF548*x* family are muxed with GPIO, adding flexibility and usability to all signals on the chip.

1.5 Signal Description

Table 3 lists the signals for the MCF548*x* in functional group order.

NOTE

In this table and throughout this document, a single signal within a group is designated without square brackets (for example, AD24), while designations for multiple signals within a group use bracketed numbers separated by a colon (for example, AD[31:0]).

Table 3. MCF548*x* Signal Description

PBGA Pin	Pin Functions				Description	I/O	Drive	Reset State
	Primary	GPIO	Secondary	Tertiary				
FlexBus								
AE2, AF3, AF1, AE3, AE4, AD5, AF2, AD4	AD[31:24]	—	—	—	Multiplexed address/data bus	I/O	16	Hi-Z
AD3, AC3, AD2, AC2, AA4, AE1, AC1, AD1	AD[23:16]	—	—	—	Multiplexed address/data bus	I/O	16	Hi-Z
AB2, AA3, W4, AB1, AA2, AA1, Y1, Y2	AD[15:8]	—	—	—	Multiplexed address/data bus	I/O	16	Hi-Z
W3, W1, W2, V3, V1, V2, T4, U3	AD[7:0]	—	—	—	Multiplexed address/data bus	I/O	16	Hi-Z
R1, T2, T3, T1, U2	$\overline{\text{FBCS}}$[5:1]	PFBCS[5:1]	—	—	Chip selects 5–1	O:I/O	24	High
U1	$\overline{\text{FBCS0}}$	—	—	—	Chip select 0	O	24	High
AD6	$\overline{\text{TS}}$	PFBCTL0	$\overline{\text{TBST}}$	—	Transfer start	O:I/O	16	High
AE5	R/$\overline{\text{W}}$	PFBCTL2	$\overline{\text{TBST}}$	—	Read/write	O	16	Hi-Z
AF4,	$\overline{\text{BE}}$/$\overline{\text{BWE3}}$	PFBCTL7	TSIZ1	—	Byte enables	O:I/O	16	High
AF5	$\overline{\text{BE}}$/$\overline{\text{BWE2}}$	PFBCTL6	TSIZ0	—	Byte enables	O:I/O	16	High
AC4	$\overline{\text{BE}}$/$\overline{\text{BWE1}}$	PFBCTL5	FBADDR1	—	Byte enables	O:I/O	16	High
AE7	$\overline{\text{BE}}$/$\overline{\text{BWE0}}$	PFBCTL4	FBADDR0	—	Byte enables	O:I/O	16	High
AE6	$\overline{\text{OE}}$	PFBCTL3	—	—	Output enable	I/O	16	High
AF6	$\overline{\text{TA}}$	PFBCTL1	—	—	Transfer acknowledge	I:I/O	16	—
SDRAM Controller								
C10, B9, A8, D5, A6, C8, B7, A5	SDDATA[31:24]	—	—	—	SDRAM data bus	I/O	24	Hi-Z

[1]This pin is a “no connect” on the MCF5483 and MCF5482 devices.
[2]This pin is a “no connect” on the MCF5481 and MCF5480 devices.
[3]TBD if the USB power pins are connected when the USB is disabled or not used.

Table 3. MCF548*x* Signal Description (continued)

PBGA Pin	Pin Functions				Description	I/O	Drive	Reset State
	Primary	GPIO	Secondary	Tertiary				
A4, C7, B6, B4, C5, B3, C4, D4	SDDATA[23:16]	—	—	—	SDRAM data bus	I/O	24	Hi-Z
E2, D1, G4, E1, K4, F1, G2, H3	SDDATA[15:8]	—	—	—	SDRAM data bus	I/O	24	Hi-Z
N4, G1, H2, J3, J1, M4, K3, K2	SDDATA[7:0]	—	—	—	SDRAM data bus	I/O	24	Hi-Z
A13, A12, D10, B12, C12, A11, D8, B11, C11, A10, D7, B10, A9	SDADDR[12:0]	—	—	—	SDRAM address bus	O	24	Low
M2, M3	SDBA[1:0]	—	—	—	SDRAM bank addresses	O	24	Low
E3	$\overline{\text{RAS}}$	—	—	—	SDRAM row address strobe	O	24	High
C2	$\overline{\text{CAS}}$	—	—	—	SDRAM column address strobe	O	24	High
R2, P2, P1, N3	$\overline{\text{SDCS}}$[3:0]	—	—	—	SDRAM chip selects	O	24	High
B8, A3, G3, J2	SDDM[3:0]	—	—	—	SDRAM write data byte mask	O	24	High
A7, B5, F2, H1	SDDQS[3:0]	—	—	—	SDRAM data strobe	I/O	24	High
L1, N1	SDCLK[1:0]	—	—	—	SDRAM clock	O	24	Low
M1, N2	$\overline{\text{SDCLK}}$[1:0]	—	—	—	Inverted SDRAM clock	O	24	Low
K1	$\overline{\text{SDWE}}$	—	—	—	SDRAM write enable	O	24	Low
E4	SDCKE	—	—	—	SDRAM clock enable	O	24	Low
L2	SDRDQS	—	—	—	SDR SDRAM data strobe	O	24	Low
D2	VREF	—	—	—	SDRAM reference voltage	I	—	—
PCI Controller								
V25, V26, U25, U26, T24, T25, T26, R24	PCIAD[31:24]	—	FBADDR[31:24]	—	PCI address/data bus	I/O	16	Hi-Z

[1]This pin is a “no connect” on the MCF5483 and MCF5482 devices.
[2]This pin is a “no connect” on the MCF5481 and MCF5480 devices.
[3]TBD if the USB power pins are connected when the USB is disabled or not used.

Table 3. MCF548*x* Signal Description (continued)

PBGA Pin	Pin Functions				Description	I/O	Drive	Reset State
	Primary	GPIO	Secondary	Tertiary				
R25, R26, P26, P24, P23, P25, N25, N23	PCIAD[23:16]	—	FBADDR[23:16]	—	PCI address/data bus	I/O	16	Hi-Z
N26, N24, M26, M25, L26, L25, K26, K25	PCIAD[15:8]	—	FBADDR[15:8]	—	PCI address/data bus	I/O	16	Hi-Z
J26, K24, J25, H26, J24, G26, H25, K23	PCIAD[7:0]	—	FBADDR[7:0]	—	PCI address/data bus	I/O	16	Hi-Z
F26, G25, E26, G24	$\overline{\text{PCICXBE}}$[3:0]	—	—	—	PCI command/byte enables	I/O	16	Hi-Z
J23	$\overline{\text{PCIDEVSEL}}$	—	—	—	PCI device select	I/O	16	Hi-Z
F25	$\overline{\text{PCIFRM}}$	—	—	—	PCI frame	I/O	16	Hi-Z
C23	PCIIDSEL	—	—	—	PCI initialization device select	I	—	—
D24	$\overline{\text{PCIIRDY}}$	—	—	—	PCI initiator ready	I/O	16	Hi-Z
F23	PCIPAR	—	—	—	PCI parity	I/O	16	Hi-Z
D26	$\overline{\text{PCIPERR}}$	—	—	—	PCI parity error	I/O	16	Hi-Z
G23	$\overline{\text{PCIRESET}}$	—	—	—	PCI reset	O	16	Low
F24	$\overline{\text{PCISERR}}$	—	—	—	PCI system error	I/O	16	Hi-Z
E25	$\overline{\text{PCISTOP}}$	—	—	—	PCI stop	I/O	16	Hi-Z
C26	PCITRDY	—	—	—	PCI target ready	I/O	16	Hi-Z
W24	$\overline{\text{PCIBG4}}$	PPCIBG4	$\overline{\text{TBST}}$	—	PCI external grant 4	O	16	GPI
Y26, W25, V24, W26	$\overline{\text{PCIBG}}$[3:0]	PPCIBG[3:0]	TOUT[3:0]	—	PCI external grant 3–0	I/O	16	GPI
D21	$\overline{\text{PCIBR4}}$	PPCIBR4	$\overline{\text{IRQ4}}$	—	PCI external request 4	I:I/O	8	GPI
B24, A25, B23, A24	$\overline{\text{PCIBR}}$[3:0]	PPCIBR[3:0]	TIN[3:0]	—	PCI external request 3	I:I/O	8	GPI
External Interrupts Port								
D14	$\overline{\text{IRQ7}}$	PIRQ7	—	—	External interrupt request 7	I	—	—
B14, A14	$\overline{\text{IRQ}}$[6:5]	PIRQ[6:5]	CANRX1	—	External interrupt request 6—5	I	—	—
Ethernet MAC 0								

[1]This pin is a “no connect” on the MCF5483 and MCF5482 devices.
[2]This pin is a “no connect” on the MCF5481 and MCF5480 devices.
[3]TBD if the USB power pins are connected when the USB is disabled or not used.

Table 3. MCF548*x* Signal Description (continued)

PBGA Pin	Pin Functions				Description	I/O	Drive	Reset State
	Primary	GPIO	Secondary	Tertiary				
AF10	E0MDIO	PFECI2C3	—	—	Management channel serial data	I/O	8	GPI
AD11	E0MDC	PFECI2C2	—	—	Management channel clock	O:I/O	8	GPI
AF9	E0TXCLK	PFEC0H7	—	—	MAC transmit clock	I:I/O	8	GPI
AE10	E0TXEN	PFEC0H6	—	—	MAC transmit enable	O:I/O	8	GPI
AD9	E0TXD0	PFEC0H5	—	—	MAC transmit data	O:I/O	8	GPI
AC9	E0COL	PFEC0H4	—	—	MAC collision	I:I/O	8	GPI
AD14	E0RXCLK	PFEC0H3	—	—	MAC receive clock	I:I/O	8	GPI
AE14	E0RXDV	PFEC0H2	—	—	MAC receive enable	I:I/O	8	GPI
AD13	E0RXD0	PFEC0H1	—	—	MAC receive data	I:I/O	8	GPI
AE19	E0CRS	PFEC0H0	—	—	MAC carrier sense	I:I/O	8	GPI
AD8, AC6, AF7	E0TXD[3:1]	PFEC0L[7:5]	—	—	MAC transmit data	O:I/O	8	GPI
AE9	E0TXER	PFEC0L4	—	—	MAC transmit error	O:I/O	8	GPI
AF11, AF12, AF13	E0RXD[3:1]	PFEC0L[3:1]	—	—	MAC receive data	I:I/O	8	GPI
AC14	E0RXER	PFEC0L0	—	—	MAC receive error	I:I/O	8	GPI
Ethernet MAC 1								
AD25[1]	E1MDIO	—	SDA	CANRX0	Management channel serial data	I/O	8	—
AD24[1]	E1MDC	—	SCL	CANTX0	Management channel clock	O:I/O	8	—
AE13[1]	E1TXCLK	PFEC1H7	—	—	MAC Transmit clock	I:I/O	8	GPI
AD25[1]	E1TXEN	PFEC1H6	—	—	MAC Transmit enable	O:I/O	8	GPI
AE12[1]	E1TXD0	PFEC1H5	—	—	MAC Transmit data	O:I/O	8	GPI
AF8[1]	E1COL	PFEC1H4	—	—	MAC Collision	I:I/O	8	GPI
B22[1]	E1RXCLK	PFEC1H3	—	—	MAC Receive clock	I:I/O	8	GPI
B25[1]	E1RXDV	PFEC1H2	—	—	MAC Receive enable	I:I/O	8	GPI
AF24[1]	E1RXD0	PFEC1H1	—	—	MAC Receive data	I:I/O	8	GPI
AC5[1]	E1CRS	PFEC1H0	—	—	MAC Carrier sense	I:I/O	8	GPI

[1]This pin is a “no connect” on the MCF5483 and MCF5482 devices.
[2]This pin is a “no connect” on the MCF5481 and MCF5480 devices.
[3]TBD if the USB power pins are connected when the USB is disabled or not used.

Table 3. MCF548*x* Signal Description (continued)

PBGA Pin	Pin Functions				Description	I/O	Drive	Reset State
	Primary	GPIO	Secondary	Tertiary				
AC8[1], AC11[1], AE11[1]	E1TXD[3:1]	PFEC1L[7:5]	—	—	MAC Transmit data	O:I/O	8	GPI
AE24[1]	E1TXER	PFEC1L4	—	—	MAC Transmit error	O:I/O	8	GPI
D25[1], B26[1], A26[1]	E1RXD[3:1]	PFEC1L[3:1]	—	—	MAC Receive data	I:I/O	8	GPI
AE8[1]	E1RXER	PFEC1L0	—	—	MAC Receive error	I:I/O	8	GPI
USB								
AF16[2]	USBD+	—	—	—	USB differential data	I/O	24	—
AF17[2]	USBD-	—	—	—	USB differential data	I/O	24	—
AC17[2]	USBVBUS	—	—	—	USB Vbus monitor input	I	—	—
AC15[2]	NC	—	—	—	No Connect	I	—	—
AF18[2]	USBRBIAS	—	—	—	USB bias resistor	I	—	—
AF15[2]	USBCLKIN	—	—	—	USB crystal input	I	—	—
AF14[2]	USBCLKOUT	—	—	—	USB crystal output	O	24	—
DSPI								
Y24	DSPISOUT	PDSPI0	PSC3TXD	—	QSPI data out	O:I/O	24	GPI
AC24	DSPISIN	PDSPI1	PSC3RXD	—	QSPI data in	I:I/O	24	GPI
AD22	DSPISCK	PDSPI2	$\overline{\text{PSC3CTS}}$	PSC3BCLK	QSPI clock	I/O	24	GPI
W23	DSPICS5/$\overline{\text{PCS}}$	PDSPI6	—	—	QSPI chip select	O:I/O	24	GPI
V23	DSPICS3	PDSPI5	TOUT3	CANTX1	QSPI chip select	O:I/O	24	GPI
AA26	DSPICS2	PDSPI4	TOUT2	CANTX1	QSPI chip select	O:I/O	24	GPI
Y25	DSPICS0/$\overline{\text{SS}}$	PDSPI3	$\overline{\text{PSC3RTS}}$	PSC3FSYNC	QSPI chip select	O:I/O	24	GPI
I^{2}C								
C24	SDA	PFECI2C1	—	—	I^{2}C Serial data	I/O	8	GPI
C25	SCL	PFECI2C0	—	—	I^{2}C Serial clock	I/O	8	GPI
PSCs								
AA25	PSC0TXD	PPSCL0	—	—	PSC0 transmit data	O:I/O	8	GPI
AC21	PSC0RXD	PPSCL1	—	—	PSC0 receive data	I:I/O	8	GPI

[1]This pin is a “no connect” on the MCF5483 and MCF5482 devices.
[2]This pin is a “no connect” on the MCF5481 and MCF5480 devices.
[3]TBD if the USB power pins are connected when the USB is disabled or not used.

Table 3. MCF548*x* Signal Description (continued)

PBGA Pin	Pin Functions				Description	I/O	Drive	Reset State
	Primary	GPIO	Secondary	Tertiary				
AE23	$\overline{\text{PSC0CTS}}$	PPSCL2	PSC0BCLK	—	PSC0 clear to send	I:I/O	8	GPI
AB26	$\overline{\text{PSC0RTS}}$	PPSCL3	PSC0FSYNC	—	PSC0 request to send	I/O	8	GPI
AB25	PSC1TXD	PPSCL4	—	—	PSC1 transmit data	O:I/O	8	GPI
AE22	PSC1RXD	PPSCL5	—	—	PSC1 receive data	I:I/O	8	GPI
AF25	$\overline{\text{PSC1CTS}}$	PPSCL6	PSC1BCLK	—	PSC1 clear to send	I:I/O	8	GPI
Y23	$\overline{\text{PSC1RTS}}$	PPSCL7	PSC1FSYNC	—	PSC1 request to send	I/O	8	GPI
AC26	PSC2TXD	PPSCH0	—	—	PSC2 transmit data	O:I/O	8	GPI
AD21	PSC2RXD	PPSCH1	—	—	PSC2 receive data	I:I/O	8	GPI
AC19	$\overline{\text{PSC2CTS}}$	PPSCH2	PSC2BCLK	CANRX0	PSC2 clear to send	I:I/O	8	GPI
AD26	$\overline{\text{PSC2RTS}}$	PPSCH3	PSC2FSYNC	CANTX0	PSC2 request to send	I/O	8	GPI
AE26	PSC3TXD	PPSCH4	—	—	PSC3 transmit data	O:I/O	8	GPI
AE21	PSC3RXD	PPSCH5	—	—	PSC3 receive data	I:I/O	8	GPI
AF23	$\overline{\text{PSC3CTS}}$	PPSCH6	PSC3BCLK	—	PSC3 clear to send	I:I/O	8	GPI
AB23	$\overline{\text{PSC3RTS}}$	PPSCH7	PSC3FSYNC	—	PSC3 request to send	I/O	8	GPI
DMA Controller								
AF19	$\overline{\text{DREQ1}}$	PDMA1	TIN1	$\overline{\text{IRQ1}}$	DMA request	I:I/O	8	GPI
AF20	$\overline{\text{DREQ0}}$	PDMA0	TIN0	—	DMA request	I:I/O	8	GPI
AC25, AB24	$\overline{\text{DACK}}$[1:0]	PDMA[3:2]	TOUT[1:0]	—	DMA acknowledge	O:I/O	8	GPI
Timer Module								
AD19	TIN3	PTIM7	$\overline{\text{IRQ3}}$	CANRX1	Timer input	I:I/O	8	GPI
AD23	TOUT3	PTIM6	CANTX1	—	Timer output	O:I/O	8	GPI
AF21	TIN2	PTIM5	$\overline{\text{IRQ2}}$	CANRX1	Timer input	I:I/O	8	GPI
AC22	TOUT2	PTIM4	CANTX1	—	Timer output	O:I/O	8	GPI
AE20	TIN1	—	—	—	Timer input	I:I/O	8	GPI
AC23	TOUT1	—	—	—	Timer output	O:I/O	8	GPI
AF22	TIN0	—	—	—	Timer input	I:I/O	8	GPI
AF26	TOUT0	—	—	—	Timer output	O:I/O	8	GPI

[1]This pin is a “no connect” on the MCF5483 and MCF5482 devices.
[2]This pin is a “no connect” on the MCF5481 and MCF5480 devices.
[3]TBD if the USB power pins are connected when the USB is disabled or not used.

Table 3. MCF548*x* Signal Description (continued)

PBGA Pin	Pin Functions				Description	I/O	Drive	Reset State
	Primary	GPIO	Secondary	Tertiary				
Debug and JTAG Test Port Control								
D20	PSTCLK	—	—	—	Processor clock output	O	8	High
A23, B21, D18, C20, A22, B20, A21, B19	PSTDDATA[7:0]	—	—	—	Processor status debug data	O	8	High
C15	DSCLK	—	$\overline{\text{TRST}}$	—	Debug clock / TAP reset	I	—	—
B15	$\overline{\text{BKPT}}$	—	TMS	—	Breakpoint/TAP test mode select	I	—	—
A15	DSI	—	TDI	—	Debug data in / TAP data in	I	—	—
D17	DSO	—	TDO	—	Debug data out / TAP data out	O	8	High
A16	TCK	—	—	—	TAP clock	I	—	—
Test, Reset, and Clock								
B17, C14, A18, B16	MTMOD[3:0]	—	—	—	Test mode pins	I	—	—
B13	$\overline{\text{RSTI}}$	—	—	—	Reset input	I	—	—
A20	$\overline{\text{RSTO}}$	—	—	—	Reset output	I/O	8	Low
A17	CLKIN	—	—	—	Clock input	I	—	—
D15	NC	—	—	—	No Connect	I	—	—
Power Supplies								
C16, C22, E24, H24K M24, R3, U24, Y3, AA24, AB3, AC13, AC16, AD7, AD10, AD16, AD18, AD15, AE18	EVDD	—	—	—	Positive I/O supply	I	—	—
C18, D11, D12, D19, D22, H4, H23, L23, P4, R23, V4, AA23, AC12, AC20	IVDD	—	—	—	Positive core supply	I	—	—

[1]This pin is a “no connect” on the MCF5483 and MCF5482 devices.
[2]This pin is a “no connect” on the MCF5481 and MCF5480 devices.
[3]TBD if the USB power pins are connected when the USB is disabled or not used.

Table 3. MCF548*x* Signal Description (continued)

PBGA Pin	Pin Functions				Description	I/O	Drive	Reset State
	Primary	GPIO	Secondary	Tertiary				
A2, B2, C3, C17, C19, C21, D6, D9, D13, D23, E23, F4, J4, L4, L11, L12, L13, L14, L15, L16, L24, M11, M12, M13, M14, M15, M16, M23, N11, N12, N13, N14, N15, N16, P11, P12, P13, P14, P15, P16, R4, R11, R12, R13, R14, R15, R16, T11, T12, T13, T14, T15, T16, T23, U4, U23, Y4, AB4, AC7, AC10, AC18, AD12, AE15, AD17, AD20, AE16, AE17	VSS	—	—		Ground			
A1, B1, C1, C6, C9, C13, D3, F3, L3, P3	SDVDD	—	—	—	Positive SDRAM supply			
A19	PLLVDD	—	—	—	Positive PLL analog supply			
B18	PLLVSS	—	—	—	PLL ground			
AC13[3]	USB_OSCVDD	—	—	—	USB oscillator supply			
AC16[3]	USB_PHYVDD	—	—	—	USB PHY supply			
AD14[3]	USB_OSCAVDD	—	—	—	USB oscillator analog supply			
AD15[3]	USB_PLLVDD	—	—	—	USB PLL supply			
AE17[3]	USBVDD	—	—	—	USB supply			

[1]This pin is a “no connect” on the MCF5483 and MCF5482 devices.
[2]This pin is a “no connect” on the MCF5481 and MCF5480 devices.
[3]TBD if the USB power pins are connected when the USB is disabled or not used.

Table 4 lists the MCF548*x* signals in pin number order for the 388 PBGA package.

Table 4. MCF5485/MCF5484 Signal Description by Pin Number

PBGA Pin	Pin Functions				PBGA Pin	Pin Functions			
	Primary	GPIO	Secondary	Tertiary		Primary	GPIO	Secondary	Tertiary
A1	SDVDD	—	—	—	P1	$\overline{\text{SDCS1}}$	—	—	—
A2	VSS	—	—	—	P2	$\overline{\text{SDCS2}}$	—	—	—
A3	SDDM2	—	—	—	P3	EVDD	—	—	—
A4	SDDATA23	—	—	—	P4	IVDD	—	—	—
A5	SDDATA24	—	—	—	P11	VSS	—	—	—
A6	SDDATA27	—	—	—	P12	VSS	—	—	—
A7	SDDQS3	—	—	—	P13	VSS	—	—	—
A8	SDDATA29	—	—	—	P14	VSS	—	—	—
A9	SDADDR0	—	—	—	P15	VSS	—	—	—
A10	SDADDR3	—	—	—	P16	VSS	—	—	—
A11	SDADDR7	—	—	—	P23	PCIAD19	—	FBADDR19	—
A12	SDADDR11	—	—	—	P24	PCIAD20	—	FBADDR20	—
A13	SDADDR12	—	—	—	P25	PCIAD18	—	FBADDR18	—
A14	$\overline{\text{IRQ5}}$	PIRQ5	CANRX1	—	P26	PCIAD21	—	FBADDR21	—
A15	DSI	—	TDI	—	R1	$\overline{\text{FBCS5}}$	PFBCS5	—	—
A16	TCK	—	—	—	R2	$\overline{\text{SDCS3}}$	—	—	—
A17	CLKIN	—	—	—	R3	EVDD	—	—	—
A18	MTMOD1	—	—	—	R4	VSS	—	—	—
A19	PLLVDD	—	—	—	R11	VSS	—	—	—
A20	$\overline{\text{RSTO}}$	—	—	—	R12	VSS	—	—	—
A21	PSTDDATA1	—	—	—	R13	VSS	—	—	—
A22	PSTDDATA3	—	—	—	R14	VSS	—	—	—
A23	PSTDDATA7	—	—	—	R15	VSS	—	—	—
A24	PCIBR0	PPCIBR0	TIN0	—	R16	VSS	—	—	—
A25	PCIBR2	PPCIBR2	TIN2	—	R23	IVDD	—	—	—
A26[1]	E1RXD1	PFEC1L5	—	—	R24	PCIAD24	—	FBADDR24	—
B1	SDVDD	—	—	—	R25	PCIAD23	—	FBADDR23	—
B2	VSS	—	—	—	R26	PCIAD22	—	FBADDR22	—
B3	SDDATA18	—	—	—	T1	$\overline{\text{FBCS2}}$	PFBCS2	—	—

[1]This pin is a “no connect” on the MCF5483 and MCF5482 devices.
[2]This pin is a “no connect” on the MCF5481 and MCF5480 devices.
[3]TBD if the USB power pins are connected when the USB is disabled or not used.

Table 4. MCF5485/MCF5484 Signal Description by Pin Number (continued)

PBGA Pin	Pin Functions				PBGA Pin	Pin Functions			
	Primary	GPIO	Secondary	Tertiary		Primary	GPIO	Secondary	Tertiary
B4	SDDATA20	—	—	—	T2	$\overline{\text{FBCS4}}$	PFBCS4	—	—
B5	SDDQS2	—	—	—	T3	$\overline{\text{FBCS3}}$	PFBCS3	—	—
B6	SDDATA21	—	—	—	T4	AD1	—	—	—
B7	SDDATA25	—	—	—	T11	VSS	—	—	—
B8	SDDM3	—	—	—	T12	VSS	—	—	—
B9	SDDATA30	—	—	—	T13	VSS	—	—	—
B10	SDADDR1	—	—	—	T14	VSS	—	—	—
B11	SDADDR5	—	—	—	T15	VSS	—	—	—
B12	SDADDR9	—	—	—	T16	VSS	—	—	—
B13	RSTI	—	—	—	T23	VSS	—	—	—
B14	$\overline{\text{IRQ6}}$	PIRQ6	CANRX1	—	T24	PCIAD27	—	FBADDR27	—
B15	$\overline{\text{BKPT}}$	—	TMS	—	T25	PCIAD26	—	FBADDR26	—
B16	MTMOD0	—	—	—	T26	PCIAD25	—	FBADDR25	—
B17	MTMOD3	—	—	—	U1	$\overline{\text{FBCS0}}$	—	—	—
B18	PLLVSS	—	—	—	U2	$\overline{\text{FBCS1}}$	PFBCS1	—	—
B19	PSTDDATA0	—	—	—	U3	AD0	—	—	—
B20	PSTDDATA2	—	—	—	U4	VSS	—	—	—
B21	PSTDDATA6	—	—	—	U23	VSS	—	—	—
B22[1]	E1RXCLK	PFEC1H3	—	—	U24	EVDD	—	—	—
B23	PCIBR1	PPCIBR1	TIN1	—	U25	PCIAD29	—	FBADDR29	—
B24	PCIBR3	PPCIBR3	TIN3	—	U26	PCIAD28	—	FBADDR28	—
B25[1]	E1RXDV	PFEC1H2	—	—	V1	AD3	—	—	—
B26[1]	E1RXD2	PFEC1L2	—	—	V2	AD2	—	—	—
C1	SDVDD	—	—	—	V3	AD4	—	—	—
C2	$\overline{\text{CAS}}$	—	—	—	V4	EVDD	—	—	—
C3	VSS	—	—	—	V23	DSPICS3	PDSPI5	TOUT3	CANTX1
C4	SDDATA17	—	—	—	V24	$\overline{\text{PCIBG1}}$	PPCIBG1	TOUT1	—
C5	SDDATA19	—	—	—	V25	PCIAD31	—	FBADDR31	—
C6	SDVDD	—	—	—	V26	PCIAD30	—	FBADDR30	—
C7	SDDATA22	—	—	—	W1	AD6	—	—	—

[1]This pin is a “no connect” on the MCF5483 and MCF5482 devices.
[2]This pin is a “no connect” on the MCF5481 and MCF5480 devices.
[3]TBD if the USB power pins are connected when the USB is disabled or not used.

Table 4. MCF5485/MCF5484 Signal Description by Pin Number (continued)

PBGA Pin	Pin Functions				PBGA Pin	Pin Functions			
	Primary	GPIO	Secondary	Tertiary		Primary	GPIO	Secondary	Tertiary
C8	SDDATA26	—	—	—	W2	AD5	—	—	—
C9	SDVDD	—	—	—	W3	AD7	—	—	—
C10	SDDATA31	—	—	—	W4	AD13	—	—	—
C11	SDADDR4	—	—	—	W23	DSPICS5/$\overline{\text{PCS}}$S	PDSPI6	—	—
C12	SDADDR8	—	—	—	W24	$\overline{\text{PCIBG4}}$	PPCIBG4	$\overline{\text{TBST}}$	—
C13	SDVDD	—	—	—	W25	$\overline{\text{PCIBG2}}$	PPCIBG2	TOUT2	—
C14	MTMOD2	—	—	—	W26	$\overline{\text{PCIBG0}}$	PPCIBG0	TOUT0	—
C15	DSCLK	—	$\overline{\text{TRST}}$	—	Y1	AD9	—	—	—
C16	EVDD	—	—	—	Y2	AD8	—	—	—
C17	VSS	—	—	—	Y3	EVDD	—	—	—
C18	IVDD	—	—	—	Y4	VSS	—	—	—
C19	VSS	—	—	—	Y23	$\overline{\text{PSC1RTS}}$	PPSCL7	PSC1FSYNC	—
C20	PSTDDATA4	—	—	—	Y24	DSPISOUT	PDSPI0	PSC3TXD	—
C21	VSS	—	—	—	Y25	DSPICS0/$\overline{\text{SS}}$	PDSPI3	—	—
C22	EVDD	—	—	—	Y26	$\overline{\text{PCIBG3}}$	PPCIBG3	TOUT3	—
C23	PCIIDSEL	—	—	—	AA1	AD10	—	—	—
C24	SDA	PFECI2C1	—	—	AA2	AD11	—	—	—
C25	SCL	PFECI2C0	—	—	AA3	AD14	—	—	—
C26	PCITRDY	—	—	—	AA4	AD19	—	—	—
D1	SDDATA14	—	—	—	AA23	IVDD	—	—	—
D2	VREF	—	—	—	AA24	EVDD	—	—	—
D3	SDVDD	—	—	—	AA25	PCS0TXD	PPSCL0	—	—
D4	SDDATA16	—	—	—	AA26	DSPICS2	PDSPI4	TOUT2	CANTX1
D5	SDDATA28	—	—	—	AB1	AD12	—	—	—
D6	VSS	—	—	—	AB2	AD15	—	—	—
D7	SDADDR2	—	—	—	AB3	EVDD	—	—	—
D8	SDADDR6	—	—	—	AB4	VSS	—	—	—
D9	VSS	—	—	—	AB23	$\overline{\text{PSC3RTS}}$	PPSCH7	PSC3FSYNC	—
D10	SDADDR10	—	—	—	AB24	$\overline{\text{DACK0}}$	PDMA2	TOUT0	—

[1]This pin is a “no connect” on the MCF5483 and MCF5482 devices.
[2]This pin is a “no connect” on the MCF5481 and MCF5480 devices.
[3]TBD if the USB power pins are connected when the USB is disabled or not used.

Table 4. MCF5485/MCF5484 Signal Description by Pin Number (continued)

PBGA Pin	Pin Functions				PBGA Pin	Pin Functions			
	Primary	GPIO	Secondary	Tertiary		Primary	GPIO	Secondary	Tertiary
D11	IVDD	—	—	—	AB25	PSC1TXD	PPSCL4	—	—
D12	IVDD	—	—	—	AB26	$\overline{\text{PSC0RTS}}$	PPSCL3	PSC0FSYNC	—
D13	VSS	—	—	—	AC1	AD17	—	—	—
D14	$\overline{\text{IRQ7}}$	PIRQ7	—	—	AC2	AD20	—	—	—
D15	NC	—	—	—	AC3	AD22	—	—	—
D16	VSS	—	—	—	AC4	$\overline{\text{BE}}$/$\overline{\text{BWE1}}$	PFBCTL5	FBADDR1	—
D17	DSO	—	TDO	—	AC5[1]	E1CRS	PFEC1H0	—	—
D18	PSTDDATA5	—	—	—	AC6	E0TXD2	PFEC0L6	—	—
D19	IVDD	—	—	—	AC7	VSS	—	—	—
D20	PSTCLK	—	—	—	AC8[1]	E1TXD3	PFEC1L7	—	—
D21	$\overline{\text{PCIBR4}}$	PPCIBR4	$\overline{\text{IRQ4}}$	—	AC9	E0COL	PFEC0H4	—	—
D22	IVDD	—	—	—	AC10	VSS	—	—	—
D23	VSS	—	—	—	AC11[1]	E1TXD2	PFEC1L6	—	—
D24	$\overline{\text{PCIIRDY}}$	—	—	—	AC12	IVDD	—	—	—
D25[1]	E1RXD3[1]	PFEC1L3	—	—	AC13[3]	USB_OSCVDD	—	—	—
D26	$\overline{\text{PCIPERR}}$	—	—	—	AC14	E0RXER	PFEC0L0	—	—
E1	SDDATA12	—	—	—	AC15	NC	—	—	—
E2	SDDATA15	—	—	—	AC16[3]	USB_PHYVDD	—	—	—
E3	$\overline{\text{RAS}}$	—	—	—	AC17[2]	USBVBUS	—	—	—
E4	SDCKE	—	—	—	AC18	VSS	—	—	—
E23	VSS	—	—	—	AC19	$\overline{\text{PSC2CTS}}$	PPSCH2	PSC2BCLK	CANRX0
E24	EVDD	—	—	—	AC20	IVDD	—	—	—
E25	$\overline{\text{PCISTOP}}$	—	—	—	AC21	PSC0RXD	PPSCL1	—	—
E26	$\overline{\text{PCICXBE3}}$	—	—	—	AC22	TOUT2	PTIM4	CANTX1	—
F1	SDDATA10	—	—	—	AC23	TOUT1	—	—	—
F2	SDDQS1	—	—	—	AC24	DSPISIN	PDSPI1	PSC3RXD	—
F3	SDVDD	—	—	—	AC25	$\overline{\text{DACK1}}$	PDMA3	TOUT1	—
F4	VSS	—	—	—	AC26	PSC2TXD	PPSCH0	—	—
F23	PCIPAR	—	—	—	AD1	AD16	—	—	—

[1]This pin is a “no connect” on the MCF5483 and MCF5482 devices.
[2]This pin is a “no connect” on the MCF5481 and MCF5480 devices.
[3]TBD if the USB power pins are connected when the USB is disabled or not used.

Table 4. MCF5485/MCF5484 Signal Description by Pin Number (continued)

PBGA Pin	Pin Functions				PBGA Pin	Pin Functions			
	Primary	GPIO	Secondary	Tertiary		Primary	GPIO	Secondary	Tertiary
F24	$\overline{\text{PCISERR}}$	—	—	—	AD2	AD21	—	—	—
F25	$\overline{\text{PCIFRM}}$	—	—	—	AD3	AD23	—	—	—
F26	$\overline{\text{PCICXBE3}}$	—	—	—	AD4	AD24	—	—	—
G1	SDDATA6	—	—	—	AD5	AD26	—	—	—
G2	SDDATA9	—	—	—	AD6	$\overline{\text{TS}}$	PFBCTL0	$\overline{\text{TBST}}$	—
G3	SDDM1	—	—	—	AD7	EVDD	—	—	—
G4	SDDATA13	—	—	—	AD8	E0TXD3	PFEC0L7	—	—
G23	$\overline{\text{PCIRESET}}$	—	—	—	AD9	E0TXD0	PFEC0H5	—	—
G24	$\overline{\text{PCICXBE0}}$	—	—	—	AD10	EVDD	—	—	—
G25	$\overline{\text{PCICXBE2}}$	—	—	—	AD11	E0MDC	PFECI2C2	—	—
G26	PCIAD2	—	FBADDR2	—	AD12	VSS	—	—	—
H1	SDDQS0	—	—	—	AD13	E0RXD0	PFEC0H1	—	—
H2	SDDATA5	—	—	—	AD14	E0RXLK	PFEC0H3	—	—
H3	SDDATA8	—	—	—	AD15[3]	USB_OSCAVDD	—	—	—
H4	IVDD	—	—	—	AD16[3]	USB_PLLVDD	—	—	—
H23	IVDD	—	—	—	AD17	VSS	—	—	—
H24	EVDD	—	—	—	AD18	EVDD	—	—	—
H25	PCIAD1	—	FBADDR1	—	AD19	E0CRS	PFEC0H0	—	—
H26	PCIAD4	—	FBADDR4	—	AD20	VSS	—	—	—
J1	SDDATA3	—	—	—	AD21	PSC2RXD	PPSCH1	—	—
J2	SDDM0	—	—	—	AD22	DSPISCK	PDSPI2	$\overline{\text{PSC3CTS}}$	PSC3BCLK
J3	SDDATA4	—	—	—	AD23	TOUT3	PTIM6	CANTX1	—
J4	VSS	—	—	—	AD24[1]	E1MDC	—	SCL	CANTX0
J23	$\overline{\text{PCIDEVSEL}}$	—	—	—	AD25[1]	E1TXEN	PFEC1H6	—	—
J24	PCIAD3	—	FBADDR3	—	AD26	$\overline{\text{PSC2RTS}}$	PPSCH3	PSC2FSYNC	CANTX0
J25	PCIAD5	—	FBADDR5	—	AE1	AD18	—	—	—
J26	PCIAD7	—	FBADDR7	—	AE2	AD31	—	—	—
K1	$\overline{\text{SDWE}}$	—	—	—	AE3	AD28	—	—	—
K2	SDDATA0	—	—	—	AE4	AD27	—	—	—

[1]This pin is a “no connect” on the MCF5483 and MCF5482 devices.
[2]This pin is a “no connect” on the MCF5481 and MCF5480 devices.
[3]TBD if the USB power pins are connected when the USB is disabled or not used.

Table 4. MCF5485/MCF5484 Signal Description by Pin Number (continued)

PBGA Pin	Pin Functions				PBGA Pin	Pin Functions			
	Primary	GPIO	Secondary	Tertiary		Primary	GPIO	Secondary	Tertiary
K3	SDDATA1	—	—	—	AE5	R/$\overline{W}$	PFBCTL2	$\overline{TBST}$	—
K4	SDDATA11	—	—	—	AE6	$\overline{OE}$	PFBCTL3	—	—
K23	PCIAD0	—	FBADDR0	—	AE7	$\overline{BE}$/$\overline{BWE0}$	PFBCTL4	FBADDR0	—
K24	PCIAD6	—	FBADDR6	—	AE8[1]	E1RXER	PFEC1L0	—	—
K25	PCIAD8	—	FBADDR8	—	AE9	E0TXER	PFEC0L4	—	—
K26	PCIAD9	—	FBADDR9	—	AE10	E0TXEN	PFEC0H6	—	—
L1	SDCLK1	—	—	—	AE11[1]	E1TXD1	PFEC1L5	—	—
L2	SDRDQS	—	—	—	AE12[1]	E1TXD0	PFEC1h5	—	—
L3	SDVDD	—	—	—	AE13[1]	E1TXCLK	PFEC1H7	—	—
L4	VSS	—	—	—	AE14	E0RXDV	PFEC1H2	—	—
L11	VSS	—	—	—	AE15	EVDD	—	—	—
L12	VSS	—	—	—	AE16	VSS	—	—	—
L13	VSS	—	—	—	AE17	VSS	—	—	—
L14	VSS	—	—	—	AE18[3]	USBVDD	—	—	—
L15	VSS	—	—	—	AE19	E0CRS	PFEC0H0	—	—
L16	VSS	—	—	—	AE20	TIN1	—	—	—
L23	IVDD	—	—	—	AE21	PSC3RXD	PPSCH5	—	—
L24	VSS	—	—	—	AE22	PSC1RXD	PPSCL5	—	—
L25	PCIAD10	—	FBADDR10	—	AE23	$\overline{PSC0CTS}$	PPSCL2	PSC0BCLK	—
L26	PCIAD11	—	FBADDR11	—	AE24[1]	E1TXER	PFEC1L4	—	—
M1	$\overline{SDCLK1}$	—	—	—	AE25[1]	E1MDIO	—	SCL	CANTX0
M2	SDBA1	—	—	—	AE26	PSC3TXD	PPSCH4	—	—
M3	SDBA0	—	—	—	AF1	AD29	—	—	—
M4	SDDATA2	—	—	—	AF2	AD25	—	—	—
M11	VSS	—	—	—	AF3	AD30	—	—	—
M12	VSS	—	—	—	AF4	$\overline{BE}$/$\overline{BWE3}$	PFBCTL7	TSIZ1	—
M13	VSS	—	—	—	AF5	$\overline{BE}$/$\overline{BWE2}$	PFBCTL6	TSIZ0	—
M14	VSS	—	—	—	AF6	$\overline{TA}$	PFBCTL1	—	—
M15	VSS	—	—	—	AF7	E0TXD1	PFEC0L5	—	—
M16	VSS	—	—	—	AF8[1]	E1COL	PFEC1H4	—	—

[1]This pin is a “no connect” on the MCF5483 and MCF5482 devices.
[2]This pin is a “no connect” on the MCF5481 and MCF5480 devices.
[3]TBD if the USB power pins are connected when the USB is disabled or not used.

Table 4. MCF5485/MCF5484 Signal Description by Pin Number (continued)

PBGA Pin	Pin Functions				PBGA Pin	Pin Functions			
	Primary	GPIO	Secondary	Tertiary		Primary	GPIO	Secondary	Tertiary
M23	VSS	—	—	—	AF9	E0TXCLK	PFEC0H7	—	—
M24	EVDD	—	—	—	AF10	E0MDIO	PFECI2C3	—	—
M25	PCIAD12	—	FBADDR12	—	AF11	E0RXD3	PFEC0L3	—	—
M26	PCIAD13	—	FBADDR13	—	AF12	E0RXD2	PFEC0L2	—	—
N1	SDCLK0	—	—	—	AF13	E0RXD1	PFEC0L1	—	—
N2	$\overline{\text{SDCLK0}}$	—	—	—	AF14[2]	USBCLKOUT	—	—	—
N3	$\overline{\text{SDCS0}}$	—	—	—	AF15[2]	USBCLKIN	—	—	—
N4	SDDATA7	—	—	—	AF16[2]	USBD+	—	—	—
N11	VSS	—	—	—	AF17[2]	USBD-	—	—	—
N12	VSS	—	—	—	AF18[2]	USBRBIAS	—	—	—
N13	VSS	—	—	—	AF19	$\overline{\text{DREQ1}}$	PDMA1	TIN1	$\overline{\text{IRQ1}}$
N14	VSS	—	—	—	AF20	$\overline{\text{DREQ0}}$	PDMA0	TIN0	—
N15	VSS	—	—	—	AF21	TIN2	PTIM5	IRQ2	CANRX1
N16	VSS	—	—	—	AF22	TIN0	—	—	—
N23	PCIAD16	—	FBADDR16	—	AF23	$\overline{\text{PSC3CTS}}$	PPSCH6	PSC3BCLK	—
N24	PCIAD14	—	FBADDR14	—	AF24[1]	E1RXD0	PFEC1H1	—	—
N25	PCIAD17	—	FBADDR17	—	AF25	$\overline{\text{PSC1CTS}}$	PPSCL6	PSC1BCLK	—
N26	PCIAD15	—	FBADDR15	—	AF26	TOUT0	—	—	—

[1]This pin is a “no connect” on the MCF5483 and MCF5482 devices.
[2]This pin is a “no connect” on the MCF5481 and MCF5480 devices.
[3]TBD if the USB power pins are connected when the USB is disabled or not used.

1.5.1 Signal Summary

1.5.1.1 FlexBus Signals

1.5.1.1.1 Address / Data Bus (AD[31:0])

The AD[31:0] bus carries address and data. The full 32-bit address is always driven on the first clock of a bus cycle (address phase). The number of bytes used for data during the data phase is determined by the port size associated with the matching chip select.

1.5.1.1.2 Chip Select ($\overline{\text{FBCS}}$[5:0])

$\overline{\text{FBCS}}$[5:0] are asserted to indicate which device is being selected. A particular chip select asserts when the transfer address is within the device’s address space as defined in the base and mask address registers. Each

chip select can be programmed for a base address location, masking addresses, port size, burst-capability indication, wait-state generation, and internal/external termination.

Reset clears all chip select programming; $\overline{\text{FBCS0}}$ is the only chip select initialized out of reset. $\overline{\text{FBCS0}}$ is also unique because it can function at reset as a global chip select that allows boot ROM to be selected at any defined address space. Port size and termination (internal vs. external) for boot $\overline{\text{FBCS0}}$ are configured by the levels on AD[2:0] on the rising edge of $\overline{\text{RSTI}}$, as described in Section 1.5.1.6, “Reset Configuration Pins.”

1.5.1.1.3 Transfer Start ($\overline{\text{TS}}$)

The assertion of $\overline{\text{TS}}$ indicates that the MCF548*x* has begun a bus transaction and that the address and attributes are valid. $\overline{\text{TS}}$ is asserted for one bus clock cycle. $\overline{\text{TS}}$ can be used externally as address latch enable to capture the address phase of the bus transfer.

1.5.1.1.4 Read/Write (R/$\overline{\text{W}}$)

The MCF548*x* drives the R/$\overline{\text{W}}$ signal to indicate the direction of the current bus operation. It is driven high during read bus cycles and driven low during write bus cycles.

1.5.1.1.5 Transfer Burst ($\overline{\text{TBST}}$)

Transfer burst indicates that a burst transfer is in progress. A burst transfer can be 2 to 16 beats depending on the size of the transfer and the port size.

1.5.1.1.6 Transfer Size (TSIZ[1:0])

For memory accesses, these signals along with $\overline{\text{TBST}}$, indicate the data transfer size of the current bus operation. The FlexBus interface supports byte, word, and longword operand transfers and allows accesses to 8-, 16-, and 32-bit data ports.

For misaligned transfers, TSIZ[1:0] indicate the size of each transfer. For example, if a longword access through a 32-bit port device occurs at a misaligned offset of 0x1, a byte is transferred first (TSIZ[1:0] = 01), a word is next transferred at offset 0x2 (TSIZ[1:0] = 10), then the final byte is transferred at offset 0x4 (TSIZ[1:0] = 01).

For aligned transfers larger than the port size, TSIZ[1:0] behaves as follows:

- If bursting is used, TSIZ[1:0] is driven to the size of transfer.
- If bursting is inhibited, TSIZ[1:0] first shows the size of the entire transfer and then shows the port size.

Table 5. Data Transfer Size

TSIZ[1:0]	Transfer Size
00	4 bytes (longword)
01	1 byte
10	2 bytes (word)
11	16 bytes (line)

For burst-inhibited transfers, TSIZ[1:0] changes with each $\overline{TS}$ assertion to reflect the next transfer size. For transfers to port sizes smaller than the transfer size, TSIZ[1:0] indicates the size of the entire transfer on the first access and the size of the current port transfer on subsequent transfers. For example, for a longword write to an 8-bit port, TSIZ[1:0] = 2'b00 for the first transaction and 2'b01 for the next three transactions. If bursting is used and in the case of longword write to an 8-bit port, TSIZ[1:0] is driven to 2'b00 for the entire transfer.

1.5.1.1.7 Byte Selects ($\overline{BE}$/$\overline{BWE}$[3:0])

The four byte enables are multiplexed with the byte-write-enable signals. Each pin can be individually programmed through the chip select control registers (CSCRs). For each chip select, assertion of byte enables for reads and byte-write enables for write cycles can be programmed. Alternatively, users can program byte-write enables to assert on writes and no byte enable assertion for read transfers.

The byte strobe ($\overline{BE}$/$\overline{BWE}$[3:0]) outputs indicate that data is to be latched or driven onto a byte of the data. $\overline{BE}$/$\overline{BWE}$[3:0] signals are asserted only to the memory bytes used during a read or write access.

1.5.1.1.8 Output Enable ($\overline{OE}$)

The output enable signal is sent to the interfacing memory and/or peripheral to enable a read transfer. $\overline{OE}$ is asserted only when a chip select matches the current address decode.

1.5.1.1.9 Transfer Acknowledge ($\overline{TA}$)

The external system drives this input to terminate the bus transfer. For write cycles, the processor continues to drive data at least one clock after $\overline{FBCS}$*x* is negated. During read cycles, the peripheral must continue to drive data until $\overline{TA}$ is recognized. The number of wait states is determined either by an internally programmed auto acknowledgement or the external $\overline{TA}$ input. If the external $\overline{TA}$ is used, the peripheral has total control over the number of wait states.

1.5.1.2 SDRAM Controller Signals

These signals are used for SDRAM accesses.

1.5.1.2.1 SDRAM Data Bus (SDDATA[31:0])

SDDATA[31:0] is the bidirectional, non-multiplexed data bus used for SDRAM accesses. Data is sampled by the MCF548*x* on the rising edge of SDCLK when in SDR mode, and on both the rising and falling edge of SDCLK when in DDR mode.

1.5.1.2.2 SDRAM Address Bus (SDADDR[12:0])

The SDADDR[12:0] signals are the 13-bit address bus used for multiplexed row and column addresses during SDRAM bus cycles. The address multiplexing supports up to 256 Mbits of SDRAM per chip select.

1.5.1.2.3 SDRAM Bank Addresses (SDBA[1:0])

Each SDRAM module has four internal row banks. The SDBA[1:0] signals are used to select the row bank. It is also used to select the SDRAM internal mode register during power-up initialization.

1.5.1.2.4 SDRAM Row Address Strobe ($\overline{\text{RAS}}$)

This output is the SDRAM synchronous row address strobe.

1.5.1.2.5 SDRAM Column Address Strobe ($\overline{\text{CAS}}$)

This output is the SDRAM synchronous column address strobe.

1.5.1.2.6 SDRAM Chip Selects ($\overline{\text{SDCS}}$[3:0])

These signals interface to the chip select lines of the SDRAMs within a memory block. Thus, there is one $\overline{\text{SDCS}}$ line for each memory block (the MCF548*x* supports up to four SDRAM memory blocks).

1.5.1.2.7 SDRAM Write Data Byte Mask (SDDM[3:0])

These output signals are sampled by the SDRAM on both edges of SDDQS to determine which byte lanes of the SDRAM data bus should be latched during a write cycle. In DDR mode, these bits are ignored during read operations.

1.5.1.2.8 SDRAM Data Strobe (SDDQS[3:0])

These bidirectional signals indicate when valid data is on the SDRAM data bus when in DDR mode.

1.5.1.2.9 SDRAM Clock (SDCLK[1:0])

These signals are the output clock for SDRAM cycles.

1.5.1.2.10 Inverted SDRAM Clock ($\overline{\text{SDCLK}}$[1:0])

These signals are the inverted version of the SDRAM clock. They are used with SDCLK to provide the differential clocks for DDR SDRAM.

1.5.1.2.11 SDRAM Write Enable ($\overline{\text{SDWE}}$)

The SDRAM write enable ($\overline{\text{SDWE}}$) is asserted to signify that an SDRAM write cycle is underway. A read cycle is indicated by the negation of $\overline{\text{SDWE}}$.

1.5.1.2.12 SDRAM Clock Enable (SDCKE)

This output is the SDRAM clock enable. SDCKE is negated to put the SDRAM into low-power, self-refresh mode.

1.5.1.2.13 SDR SDRAM Data Strobe (SDRDQS)

This signal is connected to SDDQS inputs. Used in SDR mode only.

1.5.1.2.14 SDRAM Reference Voltage (VREF)

Output reference voltage for differential SSTL_2 inputs. Used in both DDR and SDR modes.

1.5.1.3 PCI Controller Signals

1.5.1.3.1 PCI Address/Data Bus (PCIAD[31:0])

The PCIAD[31:0] lines are a time-multiplexed address data bus. The address is presented on the bus during the address phase while the data is presented on the bus during one or more data phases.

If the FlexBus is used in 32-bit address/32-bit data non-multiplexed mode, PCIAD[31:0] are used as a 32-bit address for FlexBus transfers.

1.5.1.3.2 Command/Byte Enables ($\overline{\text{PCICXBE}}$[3:0])

The $\overline{\text{PCICXBE}}$[3:0] lines are time multiplexed. The PCI command is presented during the address phase and the byte enables are presented during the data phase.

1.5.1.3.3 Device Select ($\overline{\text{PCIDEVSEL}}$)

The $\overline{\text{PCIDEVSEL}}$ signal is asserted active low when the MCF548*x* decodes that it is the target of a PCI transaction from the address presented on the PCI bus during the address phase.

1.5.1.3.4 Frame ($\overline{\text{PCIFRM}}$)

The $\overline{\text{PCIFRM}}$ signal is asserted by a PCI initiator to indicate the beginning of a transaction. It is negated when the initiator is ready to complete the final data phase.

1.5.1.3.5 Initialization Device Select (PCIIDSEL)

The PCIIDSEL signal is asserted during a PCI type-0 configuration cycle to address the PCI configuration header.

1.5.1.3.6 Initiator Ready ($\overline{\text{PCIIRDY}}$)

The $\overline{\text{PCIIRDY}}$ signal is asserted to indicate that the PCI initiator is ready to transfer data. During a write operation, assertion indicates that the master is driving valid data on the bus. During a read operation, assertion indicates that the master is ready to accept data.

1.5.1.3.7 Parity (PCIPAR)

The PCIPAR signal indicates the parity of data on the PCIAD[31:0] and $\overline{\text{PCICXBE}}$[3:0] lines.

1.5.1.3.8 Parity Error ($\overline{\text{PCIPERR}}$)

The $\overline{\text{PCIPERR}}$ signal is asserted when a data phase parity error is detected if enabled.

1.5.1.3.9 Reset ($\overline{\text{PCIRESET}}$)

The $\overline{\text{PCIRESET}}$ signal is asserted active low by MCF548*x* to reset the PCI bus. This signal is asserted after the MCF548*x* is reset and must be negated to enable usage of the PCI bus.

1.5.1.3.10 System Error ($\overline{\text{PCISERR}}$)

The $\overline{\text{PCISERR}}$ signal, if enabled, is asserted when an address phase parity error is detected.

1.5.1.3.11 Stop ($\overline{\text{PCISTOP}}$)

The $\overline{\text{PCISTOP}}$ signal is asserted by the currently addressed target to indicate that it wishes to stop the current transaction.

1.5.1.3.12 Target Ready ($\overline{\text{PCITRDY}}$)

The $\overline{\text{PCITRDY}}$ signal is asserted by the currently addressed target to indicate that it is ready to complete the current data phase.

1.5.1.3.13 External Bus Grant ($\overline{\text{PCIBG}}$[4:1])

The $\overline{\text{PCIBG}}$ signal is asserted to an external master to give it control of the PCI bus. If the internal PCI arbiter is enabled, it asserts one of the PCIBG[4:1] lines to grant ownership of the PCI bus to an external master. When the PCI arbiter module is disabled, PCIBG[4:1] are driven high and should be ignored.

1.5.1.3.14 External Bus Grant/Request Output ($\overline{\text{PCIBG0}}$/$\overline{\text{PCIREQOUT}}$)

The $\overline{\text{PCIBG0}}$ signal is asserted to external master device 0 to give it control of the PCI bus. When the PCI arbiter module is disabled, the signal operates as the $\overline{\text{PCIREQOUT}}$ output. It is asserted when the MCF548*x* needs to initiate a PCI transaction.

1.5.1.3.15 External Bus Request ($\overline{\text{PCIBR}}$[4:0])

The $\overline{\text{PCIBR}}$ signal is asserted by an external PCI master when it requires access to the PCI bus.

1.5.1.3.16 External Request/Grant Input ($\overline{\text{PCIBR0}}$/$\overline{\text{PCIGNTIN}}$)

The $\overline{\text{PCIBR0}}$ signal is asserted by external PCI master device 0 when it requires access to the PCI bus. When the internal PCI arbiter module is disabled, this signal is used as a grant input for the PCI bus, $\overline{\text{PCIGNTIN}}$. It is driven by an external PCI arbiter.

1.5.1.4 Interrupt Control Signals

The interrupt control signals supply the external interrupt level to the MCF548*x* device.

1.5.1.4.1 Interrupt Request ($\overline{\text{IRQ}}$[7:1])

The $\overline{\text{IRQ}}$[7:1] signals are the external interrupt inputs.

1.5.1.5 Clock and Reset Signals

The clock and reset signals configure the MCF548*x* and provide interface signals to the external system.

1.5.1.5.1 Reset In ($\overline{\text{RSTI}}$)

Asserting $\overline{\text{RSTI}}$ causes the MCF548*x* to enter reset exception processing. $\overline{\text{RSTO}}$ is asserted automatically when $\overline{\text{RSTI}}$ is asserted.

1.5.1.5.2 Reset Out ($\overline{\text{RSTO}}$)

After $\overline{\text{RSTI}}$ is asserted, the PLL temporarily loses its lock, during which time $\overline{\text{RSTO}}$ is asserted. When the PLL regains its lock, $\overline{\text{RSTO}}$ negates again. This signal can be used to reset external devices.

1.5.1.5.3 Clock In (CLKIN)

CLKIN is the MCF548*x* input clock frequency to the on-board phase-locked loop (PLL) clock generator. CLKIN is used to internally clock or sequence the MCF548*x* internal bus interface at a selected multiple of the input frequency used for internal module logic. CLKIN is used as the clock reference for PCI and FlexBus transfers.

1.5.1.6 Reset Configuration Pins

This section describes address/data pins, AD[12:0], that are read at reset to configure the MCF548*x*.

1.5.1.6.1 AD[12:8] / CLKIN to SDCLK Ratio (CLKCONFIG[4:0])

The clock configuration inputs, CLKCONFIG[4:0], indicate the CLKIN to SDCLK ratio. CLKIN is used as the external reference for both PCI and FlexBus cycles. The CLKIN to SDCLK ratio is selectable, where SDCLK is the clock frequency used for SDRAM accesses and the internal XLB bus. The core is always clocked at twice the SDCLK frequency.

These signals are sampled on the rising edge of $\overline{\text{RSTI}}$. Table 6 shows how the logic levels of AD[12:8] correspond to the selected clock ratio.

Table 6. MCF548X Divide Ratio Encodings

FB_AD[12:8][1]	Clock Ratio	CLKIN—PCI and FlexBus Frequency Range (MHz)	Internal XLB and SDRAM Bus Frequency Range (MHz)	Core Frequency Range (MHz)
00011	1:2	41.6–50.0	83.33–100	166.66–200
00101	1:2	30.0–44.4	60.0–88.8	120.0–177.66

1 All other values of FB_AD[12:8] are reserved.

1.5.1.6.2 AD5—FlexBus Size Configuration (FBSIZE)

At reset, the enabling and disabling of $\overline{\text{BE}}/\overline{\text{BWE}}$[3:0] versus TSIZ[1:0] and ADDR[1:0] is determined by the logic level driven on AD5 at the rising edge of $\overline{\text{RSTI}}$. FBSIZE is multiplexed with AD5 and sampled only at reset. Table 7 shows how the AD5 logic level corresponds to the $\overline{\text{BE}}/\overline{\text{BWE}}$[3:0] function.

Table 7. AD5/FBSIZE Selection of $\overline{BE}/\overline{BWE}$[3:0] Signals

AD5	FlexBus Byte Enable Mode
0	$\overline{BE}/\overline{BWE}$[3:0] used as byte/byte write enables.
1	$\overline{BE}/\overline{BWE}$[3:2] configured as TSIZ[1:0]. $\overline{BE}/\overline{BWE}$[1:0] configured as FBADDR[1:0].

1.5.1.6.3 AD4—32-bit FlexBus Configuration (FBMODE)

During reset, the FlexBus can be configured to operate in a non-multiplexed 32-bit address with 32-bit data mode. In this mode, the 32-bit FlexBus AD[31:0] is used for the data bus, and the PCI bus PCIAD[31:0] is used as the address bus. The FlexBus operating mode is determined by the logic level driven on AD4 at the rising edge of $\overline{RSTI}$. Table 8 shows how the logic level of AD4 corresponds to the FlexBus mode.

Table 8. AD4/FBMODE Selection of Non-Multiplexed 32-bit Address/32-bit Data Mode

AD4	FlexBus Operating Mode
0	PCIAD[31:0] used for PCI bus. AD[31:0] used for both address and data.
1	AD[31:0] used for data. PCIAD[31:0] used for address [1]

[1] If the non-multiplexed 32-bit address/32-bit data mode is selected the PCI bus cannot be used.

1.5.1.6.4 AD3—Byte Enable Configuration (BECONFIG)

The default byte enable mode of the boot $\overline{FBCS0}$ is determined by the logic level driven on AD3 at the rising edge of $\overline{RSTI}$. This logic level is reflected as the reset value of CSCR0[BEM]. Table 9 shows how the logic level of AD3 corresponds to the byte enable mode for $\overline{FBCS0}$ at reset.

Table 9. AD3/BECONFIG, $\overline{BE}/\overline{BWE}$[3:0] Boot Configuration

AD3	Boot $\overline{FBCS0}$ Byte Strobe Configuration
0	$\overline{BE}$[3:0] can assert for both read and write cycles.
1	$\overline{BWE}$[3:0] are not asserted for reads; $\overline{BWE}$[3:0] only assert for write cycles

1.5.1.6.5 AD2—Auto Acknowledge Configuration (AACONFIG)

At reset, the enabling and disabling of auto acknowledge for boot $\overline{FBCS0}$ is determined by the logic level driven on AD2 at the rising edge of $\overline{RSTI}$. AACONFIG is multiplexed with AD2 and sampled only at reset. The AD2 logic level is reflected as the reset value of CSCR0[AA]. Table 10 shows how the AD2 logic level corresponds to the auto acknowledge timing for $\overline{FBCS0}$ at reset. Note that auto acknowledge can be disabled by driving a logic 0 on AD2 at reset.

Table 10. AD2/AA_CONFIG Selection of $\overline{\text{FBCS0}}$ Automatic Acknowledge

AD2	Boot $\overline{\text{FBCS0}}$ AA Configuration at Reset
0	Disabled
1	Enabled with 63 wait states

1.5.1.6.6 AD[1:0]—Port Size Configuration (PSCONFIG)

The default port size value of the boot $\overline{\text{FBCS0}}$ is determined by the logic levels driven on AD[1:0] at the rising edge of $\overline{\text{RSTI}}$, which are reflected as the reset value of CSCR0[PS]. Table 11 shows how the logic levels of AD[1:0] correspond to the $\overline{\text{FBCS0}}$ port size at reset.

Table 11. AD[1:0]/PSCONFIG[1:0] Selection of $\overline{\text{FBCS0}}$ Port Size

AD[1:0]	Boot $\overline{\text{FBCS0}}$ Port Size
00	32-bit port
01	8-bit port
1X	16-bit port

1.5.1.7 Ethernet Module Signals

The following signals are used by the Ethernet module for data and clock signals.

1.5.1.7.1 Management Data (E0MDIO, E1MDIO)

The bidirectional EMDIO signals transfer control information between the external PHY and the media-access controller. Data is synchronous to EMDC and applies to MII mode operation. This signal is an input after reset. When the FEC operates in 10 Mbps 7-wire interface mode, this signal should be connected to VSS.

1.5.1.7.2 Management Data Clock (E0MDC, E1MDC)

EMDC is an output clock which provides a timing reference to the PHY for data transfers on the EMDIO signal and applies to MII mode operation.

1.5.1.7.3 Transmit Clock (E0TXCLK, E1TXCLK)

This is an input clock which provides a timing reference for ETXEN, ETXD[3:0] and ETXER.

1.5.1.7.4 Transmit Enable (E0TXEN, E1TXEN)

The transmit enable (ETXEN) output indicates when valid nibbles are present on the MII. This signal is asserted with the first nibble of a preamble and is negated before the first ETXCLK following the final nibble of the frame.

1.5.1.7.5 Transmit Data 0 (E0TXD0, E1TXD0)

ETXD0 is the serial output Ethernet data and is only valid during the assertion of ETXEN. This signal is used for 10 Mbps Ethernet data. This signal is also used for MII mode data in conjunction with ETXD[3:1].

1.5.1.7.6 Collision (E0COL, E1COL)

The ECOL input is asserted upon detection of a collision and remains asserted while the collision persists. This signal is not defined for full-duplex mode.

1.5.1.7.7 Receive Clock (E0RXCLK, E1RXCLK)

The receive clock (ERXCLK) input provides a timing reference for ERXDV, ERXD[3:0], and ERXER.

1.5.1.7.8 Receive Data Valid (E0RXDV, E1RXDV)

Asserting the receive data valid (ERXDV) input indicates that the PHY has valid nibbles present on the MII. ERXDV should remain asserted from the first recovered nibble of the frame through to the last nibble. Assertion of ERXDV must start no later than the SFD and exclude any EOF.

1.5.1.7.9 Receive Data 0 (E0RXD0, E1RXD0)

ERXD0 is the Ethernet input data transferred from the PHY to the media-access controller when ERXDV is asserted. This signal is used for 10 Mbps Ethernet data. This signal is also used for MII mode Ethernet data in conjunction with ERXD[3:1].

1.5.1.7.10 Carrier Receive Sense (E0CRS, E1CRS)

ECRS is an input signal which when asserted signals that transmit or receive medium is not idle, and applies to MII mode operation.

1.5.1.7.11 Transmit Data 1–3 (E0TXD[3:1], E1TXD[3:1])

These pins contain the serial output Ethernet data and are valid only during assertion of ETXEN in MII mode.

1.5.1.7.12 Transmit Error (E0TXER, E1TXER)

When the ETXER output is asserted for one or more clock cycles while ETXEN is also asserted, the PHY sends one or more illegal symbols. ETXER has no effect at 10 Mbps or when ETXEN is negated, and applies to MII mode operation.

1.5.1.7.13 Receive Data 1–3 (E0RXD[3:1], E1RXD[3:1])

These pins contain the Ethernet input data transferred from the PHY to the media-access controller when ERXDV is asserted in MII mode operation.

1.5.1.7.14 Receive Error (E0RXER, E1RXER)

ERXER is an input signal which when asserted along with ERXDV signals that the PHY has detected an error in the current frame. When ERXDV is not asserted ERXER has no effect, and applies to MII mode operation.

1.5.1.8 Universal Serial Bus (USB)

1.5.1.8.1 USB Differential Data (USBD+, USBD–)

USBD+ and USBD– are the outputs of the on-chip USB 2.0 transceiver. They provide differential data for the USB 2.0 bus.

1.5.1.8.2 USBVBUS

USB cable Vbus monitor input.

1.5.1.8.3 USBRBIAS

Connection for external current setting resistor. Should be connected to a 1.9kΩ +/– 1% pull down resistor.

1.5.1.8.4 USBCLKIN

Input pin for 12 MHz USB crystal circuit.

1.5.1.8.5 USBCLKOUT

Output pin for 12 MHz USB crystal circuit.

1.5.1.9 DMA Serial Peripheral Interface (DSPI) Signals

1.5.1.9.1 DSPI Synchronous Serial Output (DSPISOUT)

The DSPISOUT output provides the serial data from the DSPI and can be programmed to be driven on the rising or falling edge of DSPISCK.

1.5.1.9.2 DSPI Synchronous Serial Data Input (DSPISIN)

The DSPISIN input provides the serial data to the DSPI and can be programmed to be sampled on the rising or falling edge of DSPISCK.

1.5.1.9.3 DSPI Serial Clock (DSPISCK)

DSPISCK is a serial communication clock signal. In master mode, the DSPI generates the DSPISCK. In slave mode, DSPISCK is an input from an external bus master.

1.5.1.9.4 DSPI Peripheral Chip Select/Slave Select (DSPICS0/$\overline{\text{SS}}$)

In master mode, the DSPICS0 signal is a peripheral chip select output that selects which slave device the current transmission is intended for.

In slave mode, the $\overline{SS}$ signal is a slave select input signal that allows an SPI master to select the DSPI as the target for transmission.

1.5.1.9.5 DSPI Chip Selects (DSPICS[2:3])

The synchronous peripheral chip selects (DSPICS[2:3]) outputs provide DSPI peripheral chip selects that can be programmed to be active high or low.

1.5.1.9.6 DSPI Peripheral Chip Select 5/Peripheral Chip Select Strobe (DSPICS5/PCSS)

DSPICS5 is a peripheral chip select output signal. When the DSPI is in master mode and the DMCR[PCSSE] bit is cleared, this signal is used to select which slave device the current transfer is intended for.

$\overline{PCSS}$ provides a strobe signal that can be used with an external demultiplexer for deglitching of the DSPICS*n* signals. When the DSPI is in master mode and DMCR[PCSSE] is set, the $\overline{PCSS}$ provides the appropriate timing for the decoding of the DSPICS[0,2,3] signals which prevents glitches from occurring.

This signal is not used in slave mode.

1.5.1.10 FlexCAN Signals

1.5.1.10.1 FlexCAN Transmit (CANTX0, CANTX1)

Controller area network transmit data output.

1.5.1.10.2 FlexCAN Receive (CANRX0, CANRX1)

Controller area network receive data input.

1.5.1.11 I^2C I/O SIGNALS

The I^2C serial interface module uses the signals in this section.

1.5.1.11.1 Serial Clock (SCL)

This bidirectional open-drain signal is the clock signal for the I^2C interface. It is either driven by the I^2C module when the bus is in master mode or it becomes the clock input when the I^2C is in slave mode.

1.5.1.11.2 Serial Data (SDA)

This bidirectional open-drain signal is the data input/output for the I^2C interface.

1.5.1.12 PSC Module Signals

The PSC modules use the signals in this section. The baud rate clock inputs are not supported.

1.5.1.12.1 Transmit Serial Data Output (PSC0TXD, PSC1TXD, PSC2TXD, PSC3TXD)

PSC*n*TXD are the transmitter serial data outputs for the PSC modules. The output is held high (mark condition) when the transmitter is disabled, idle, or in the local loopback mode. The PSC*x*TXD pins can be programmed to be driven low (break status) by a command.

1.5.1.12.2 Receive Serial Data Input (PSC0RXD, PSC1RXD, PSC2RXD, PSC3RXD)

PSC*n*RXD are the receiver serial data inputs for the PSC modules. When the PSC clock is stopped for power-down mode, any transition on the pins restarts them.

1.5.1.12.3 Clear-to-Send ($\overline{\text{PSC}n\text{CTS}}$/PSCBCLK)

These signals either operate as the clear to send input signals in UART mode or the bit clock input signals in modem modes and IrDA modes. In MIR and FIR mode, the frequency is a multiple of the input bit clock frequency, and the bit clock frequency should be within +/-0.1% and +/-0.01% of the ideal one, respectively.

1.5.1.12.4 Request to Send ($\overline{\text{PSC}n\text{RTS}}$/PSCFSYNC)

The $\overline{\text{PSC}n\text{RTS}}$ signals act as transmitter request to send ($\overline{\text{RTS}}$) outputs in UART mode, the frame sync input in modem8 and modem16 modes or the RTS output (which acts as frame sync) in AC97 modem mode.

1.5.1.13 DMA Controller Module Signals

The DMA controller module uses the signals in the following subsections to provide external requests for either a source or destination.

1.5.1.13.1 DMA Request ($\overline{\text{DREQ}}$[1:0])

These inputs are asserted by a peripheral device to request an operand transfer between that peripheral and memory by either channel 0 or 1 of the on-chip DMA module.

1.5.1.13.2 DMA Acknowledge ($\overline{\text{DACK}}$[1:0])

These outputs are asserted to acknowledge that a DMA request has been recognized.

1.5.1.14 Timer Module Signals

The signals in the following sections are external interfaces to the four general-purpose MCF548*x* timers. These 32-bit timers can capture timer values, trigger external events or internal interrupts, or count external events.

1.5.1.14.1 Timer Inputs (TIN[3:0])

TIN*n* can be programmed as clocks that cause events in the counter and prescalers. They can also cause captures on the rising edge, falling edge, or both edges.

1.5.1.14.2 Timer Outputs (TOUT[3:0])

The programmable timer outputs, TOUT*n*, pulse or toggle on various timer events.

1.5.1.15 Debug Support Signals

The MCF548*x* complies with the IEEE 1149.1a JTAG testing standard. JTAG test pins are multiplexed with background debug pins. Except for TCK, these signals are selected by the value of MTMOD0. If MTMOD0 is high, JTAG signals are chosen; if it is low, debug module signals are chosen. MTMOD0 should be changed only while $\overline{\text{RSTI}}$ is asserted.

1.5.1.15.1 Processor Clock Output (PSTCLK)

The internal PLL generates this output signal, and is the processor clock output that is used as the timing reference for the debug bus timing (PSTDDATA[7:0]). PSTCLK is at the same frequency as the core processor and cache memory. The frequency is 2x the internal system clock.

1.5.1.15.2 Processor Status Debug Data (PSTDDATA[7:0])

Processor status data outputs indicate both processor status and captured address and data values. They operate at half the processor's frequency, using PSTCLK. Given that real-time trace information appears as a sequence of 4-bit data values, there are no alignment restrictions; that is, PST values and operands may appear on either PSTDDATA[7:0] nibble. The upper nibble, PSTDDATA[7:4], is most significant.

1.5.1.15.3 Development Serial Clock/Test Reset (DSCLK/$\overline{\text{TRST}}$)

If MTMOD0 is low, DSCLK is selected. DSCLK is the development serial clock for the serial interface to the debug module. The maximum DSCLK frequency is 1/5 CLKIN.

If MTMOD0 is high, $\overline{\text{TRST}}$ is selected. $\overline{\text{TRST}}$ asynchronously resets the internal JTAG controller to the test logic reset state, causing the JTAG instruction register to choose the bypass instruction. When this occurs, JTAG logic is benign and does not interfere with normal MCF548*x* functionality.

Although $\overline{\text{TRST}}$ is asynchronous, Motorola recommends that it makes an asserted-to-negated transition only while TMS is held high. $\overline{\text{TRST}}$ has an internal pull-up resistor so if it is not driven low, it defaults to a logic level of 1. If $\overline{\text{TRST}}$ is not used, it can be tied to ground or, if TCK is clocked, to EV_{DD}. Tying $\overline{\text{TRST}}$ to ground places the JTAG controller in test logic reset state immediately. Tying it to EV_{DD} causes the JTAG controller (if TMS is a logic level of 1) to eventually enter test logic reset state after 5 TCK clocks.

1.5.1.15.4 Breakpoint/Test Mode Select ($\overline{\text{BKPT}}$/TMS)

If MTMOD0 is low, $\overline{\text{BKPT}}$ is selected. $\overline{\text{BKPT}}$ signals a hardware breakpoint to the processor in debug mode.

If MTMOD0 is high, TMS is selected. The TMS input provides information to determine the JTAG test operation mode. The state of TMS and the internal 16-state JTAG controller state machine at the rising edge of TCK determine whether the JTAG controller holds its current state or advances to the next state. This directly controls whether JTAG data or instruction operations occur. TMS has an internal pull-up resistor so that if it is not driven low, it defaults to a logic level of 1. But if TMS is not used, it should be tied to V_{DD}.

1.5.1.15.5 Development Serial Input/Test Data Input (DSI/TDI)

If MTMOD0 is low, DSI is selected. DSI provides the single-bit communication for debug module commands.

If MTMOD0 is high, TDI is selected. TDI provides the serial data port for loading the various JTAG boundary scan, bypass, and instruction registers. Shifting in data depends on the state of the JTAG controller state machine and the instruction in the instruction register. Shifts occur on the TCK rising edge. TDI has an internal pull-up resistor, so when not driven low it defaults to high. But if TDI is not used, it should be tied to EVDD.

1.5.1.15.6 Development Serial Output/Test Data Output (DSO/TDO)

If MTMOD0 is low, DSO is selected. DSO provides single-bit communication for debug module responses.

If MTMOD0 is high, TDO is selected. The TDO output provides the serial data port for outputting data from JTAG logic. Shifting out data depends on the JTAG controller state machine and the instruction in the instruction register. Data shifting occurs on the falling edge of TCK. When TDO is not outputting test data, it is three-stated. TDO can be three-stated to allow bused or parallel connections to other devices having a JTAG port.

1.5.1.15.7 Test Clock (TCK)

TCK is the dedicated JTAG test logic clock independent of the MCF548*x* processor clock. Various JTAG operations occur on the rising or falling edge of TCK. Holding TCK high or low for an indefinite period does not cause JTAG test logic to lose state information. If TCK is not used, it must be tied to ground.

1.5.1.16 Test Signals

1.5.1.16.1 Test Mode (MTMOD[3:0])

The test mode signals choose between multiplexed debug module and JTAG signals. If MTMOD0 is low, the part is in normal and background debug mode (BDM); if it is high, it is in normal and JTAG mode. All other MTMOD values are reserved; MTMOD[3:1] should be tied to ground and MTMOD[3:0] should not be changed while $\overline{\text{RSTI}}$ is negated

1.5.1.17 Power and Reference Pins

These pins provide system power, ground, and references to the device. Multiple pins are provided for adequate current capability. All power supply pins must have adequate bypass capacitance for high-frequency noise suppression.

1.5.1.17.1 Positive Pad Supply (EVDD)

This pin supplies positive power to the I/O pads.

1.5.1.17.2 Positive Core Supply (IVDD)

This pin supplies positive power to the core logic.

1.5.1.17.3 Ground (VSS)

This pin is the negative supply (ground) to the chip.

1.5.1.17.4 USB Power (USBVDD)

This pin supplies positive power to the USB module's digital logic.

1.5.1.17.5 USB Oscillator Power (USB_OSCVDD)

This pin supplies positive power to the USB oscillator's digital logic.

1.5.1.17.6 USB PHY Power (USB_PHYVDD)

This pin supplies positive power to the USB PHY's digital logic.

1.5.1.17.7 USB Oscillator Analog Power (USB_OSCAVDD)

This pin supplies positive power to the USB oscillator's analog circuits.

1.5.1.17.8 USB PLL Analog Power (USB_PLLVDD)

This pin supplies positive power to the USB PLL's circuits.

1.5.1.17.9 SDRAM Memory Supply (SDVDD)

This pin supplies positive power to the SDRAM module.

1.5.1.17.10 PLL Analog Power (PLLVDD)

This pin supplies the positive power for the PLL.

1.5.1.17.11 PLL Analog Ground (PLLVSS)

This pin is the negative supply (ground) to the PLL.

1.6 Chip Configuration

1.6.1 Device Operating Options

- $\overline{\text{FBCS0}}$ boot chip select port size:
  - 32-bit
  - 16-bit
  - 8-bit
- $\overline{\text{FBCS0}}$ boot chip select termination:
  - External termination
  - Internal termination
- FlexBus operating mode

  - FlexBus uses AD[31:0] as multiplexed address and data bus
  - FlexBus uses AD[31:0] as non-multiplexed data bus and PCIAD[31:0] as non-multiplexed address bus
- Byte enable mode
  - $\overline{BE}$[3:0] can assert during reads and writes
  - $\overline{BWE}$[3:0] can only assert during writes
- Clock mode:
  - 1:1 SDCLK to CLKIN ratio
  - 2:1 SDCLK to CLKIN ratio

1.6.2 Chip Configuration Pins

Table 12 shows the pins that are sampled at reset time to configure the MCF548*x*.

Table 12. Configuration Pin Descriptions

Pin	Chip Configuration Function	Pin State/Meaning
AD[12:8]	PLL Clock Configuration	See Table 6
AD5	Byte Strobe/Size Configuration	0 Byte Strobe outputs driven 1 Size and Address outputs driven
AD4	FlexBus Operating Mode	0 AD[31:0] used for multiplexed address and data 1 AD[31:0] used for data, PCIAD[31:0] used for address
AD3	Byte Enable Configuration	0 $\overline{BE}$[3:0] can assert on both read and write cycles 1 $\overline{BWE}$[3:0] can only assert on write cycles
AD2	$\overline{FBCS0}$ Boot Chip Select Auto Acknowledge Configuration	0 Auto acknowledge disabled 1 Auto acknowledge enabled with 63 wait states
AD[1:0]	$\overline{FBCS0}$ Boot Chip Select Port Size Configuration	00 32-bit port 01 8-bit port 1X 16-bit port
MTMOD0 [1]	BDM/JTAG Select	0 BDM mode 1 JTAG mode

[1] The MTMOD0 pin should not be changed during normal operation.

1.6.3 Chip Configuration Circuit

Figure 2 shows a block diagram of the recommended circuit used to drive the reset configuration values for the MCF548*x*.The signals are sampled at the rising clock edge immediately before $\overline{RSTI}$ negates, so the signals must be stable and valid at this time.

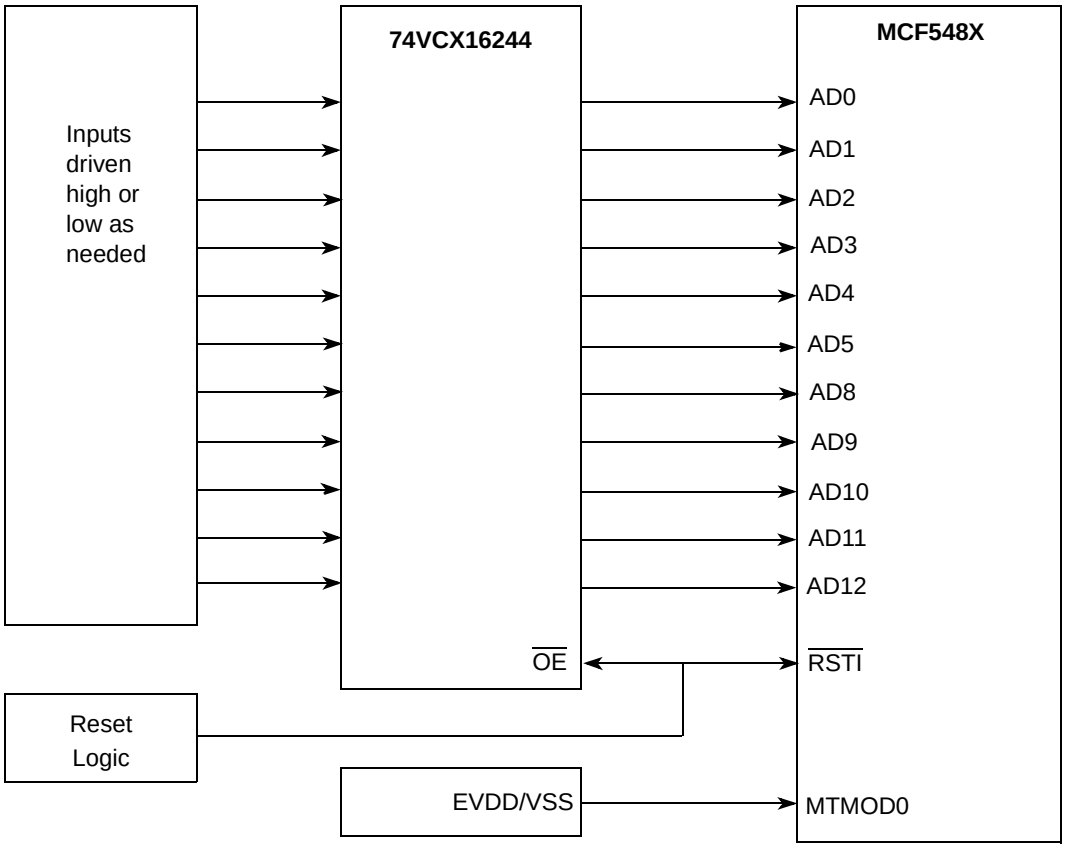


Figure 2. MCF548*x* Recommended Reset Configuration Circuit

1.7 Design Recommendations

1.7.1 Layout

- Use a 6-layer printed circuit board with the EVDD, IVDD, and VSS pins connected directly to the power and ground planes for the MCF548*x*.
- See application note AN1259 System Design and Layout Techniques for Noise Reduction in MCU-Based Systems.
- Match the PC layout trace width and routing to match trace length to operating frequency and board impedance. Add termination (series or therein) to the critical clock traces to dampen reflections. Increase the PCB impedance (if possible) keeping the trace lengths balanced and short. Then do cross-talk analysis to separate traces with significant parallelism or are otherwise ‘noisy.’ Use 6 mils trace and separation. Clocks get extra separation and more precise balancing, plus termination.

1.7.2 Power Supply/Analog Filtering

Figure 3 shows the recommended filter circuit for the MCF548*x* PLL power supply.

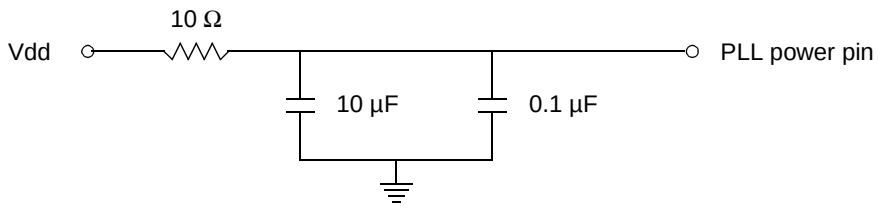


Figure 3. PLL Power Supply Filter Circuit

1.7.3 Decoupling

Place the decoupling caps on the power supply pins for the MCF548*x* as close to the pins as possible:

- 0.1µF and 1nF across each 3.3V supply input.
- 0.1µF and 1nF across each 2.5V supply input.
- 100pF and 1nF across each 1.5V supply input.

1.7.4 Buffering

- Use bus buffers on all data/address lines for all off-board accesses and for all on-board accesses when excessive loading is expected. See Section Appendix A, “Preliminary Electrical Characteristics.”

1.7.5 Pull-up Recommendations

- Use external pull-up resistors on unused inputs.

1.7.6 Clocking Recommendations

The following are general clocking recommendations for the MCF548*x:*

- Use a multi-layer board with a separate ground plane.
- Place the oscillator and all other associated components as close to the CLKIN pin as possible.
- Keep the CLKIN signal isolated from other high frequency signals.
- Ensure that the ground for the bypass capacitors is connected to a solid ground trace/plane.
- Tie the ground trace to the ground pin nearest the oscillator. This prevents large loop currents in the vicinity of the oscillator.
- Tie the ground pin to the most solid ground in the system.
- Do not connect the trace that connects the oscillator and the ground plane to any other circuit element. This tends to make the oscillator unstable.

1.7.7 Interface Recommendations

1.7.7.1 SDRAM Controller

The SDRAM controller has a glueless interface to both SDR and DDR memories. Since different voltages are required for the two memory technologies, the module supports either DDR or SDR but not both. Supported memory clock rate will be up to 133MHz. At this memory clock rate, DDR memory can receive data at an effective rate of 266 MHz.

- Support for up to 13 lines of row address, up to 12 lines of column address, 2 lines of bank address, and up to 4 chip selects. Two memory chip selects are multiplexed with two chip selects for the local bus.
- Memory bus width fixed at 32 bits.

1.7.7.1.1 SDRAM Controller Address Configurations

The SDRAM controller supports up to 13 row addresses and up to 12 column addresses. However, the maximum row and column addresses are not supported at the same time. The number of row and column addresses must be less than 24. In addition to row/column address lines, there are always two row bank address bits. Therefore, the greatest possible address space which can be accessed using a single chip select is (2^{26}) x 32 bit, or 256 Mbytes.

Table 13 shows the address multiplexing used by the MCF548*x* for different configurations. When the SDRAM controller receives the internal module enable, it latches the internal bus address lines A[27:2] and multiplexes them into row, column and row bank addresses. A[9:2] are always used for CA[7:0], A[11:10] are always used for BA[1:0], and A[23:12] are always used for RA[11:0]. A[27:24] can be used for additional row or column address bits, as needed.

Table 13. SDRAM Address Multiplexing

Device	Configuration	Row bit x Col bit x Banks	Internal Address						
			27	26	25	24	23–12	11–10	9–2
64 Mbits	4M x 16 bit	12 x 8 x 4	—	—	—	—	RA11-0	BA1-0	CA7–0
	8M x 8bits	12 x 9 x 4	—	—	—	CA8	RA11–0	BA1–0	CA7–0
		13 x 8 x 4	—	—	—	RA12	RA11–0	BA1–0	CA7–0
	16M x 4 bit	12 x 10 x 4	—	—	CA9	CA8	RA11–0	BA1–0	CA7–0
		13 x 9 x 4	—	—	CA8	RA12	RA11–0	BA1–0	CA7–0
128 Mbits	8M x 16 bit	12 x 9 x 4	—	—	—	CA8	RA11–0	BA1–0	CA7–0
		13 x 8 x 4	—	—	—	RA12	RA11–0	BA1–0	CA7–0
	16M x 8 bit	12 x 10 x 4	—	—	CA9	CA8	RA11–0	BA1–0	CA7–0
		13 x 9 x 4	—	—	CA8	RA12	RA11–0	BA1–0	CA7–0
	32M x 4 bit	12 x 11 x 4	—	CA11	CA9	CA8	RA11–0	BA1–0	CA7–0
		13 x 10 x 4	—	CA9	CA8	RA12	RA11–0	BA1–0	CA7–0

Table 13. SDRAM Address Multiplexing (continued)

Device	Configuration	Row bit x Col bit x Banks	Internal Address						
			27	26	25	24	23–12	11–10	9–2
256 Mbits	16M x 16 bit	12 x 10 x 4	—	—	CA9	CA8	RA11–0	BA1–0	CA7–0
		13 x 9 x 4	—	—	CA8	RA12	RA11–0	BA1–0	CA7–0
	32M x 8 bit	12 x 11 x 4	—	CA11	CA9	CA8	RA11–0	BA1–0	CA7–0
		13 x 10 x 4	—	CA9	CA8	RA12	RA11–0	BA1–0	CA7–0
	64M x 4 bit	12 x 12 x 4	CA12	CA11	CA9	CA8	RA11–0	BA1–0	CA7–0
		13 x 11 x 4	CA11	CA9	CA8	RA12	RA11–0	BA1–0	CA7–0
512 Mbits	32M x 16 bit	12 x 11 x 4	—	CA11	CA9	CA8	RA11–0	BA1–0	CA7–0
		13 x 10x 4	—	CA9	CA8	RA12	RA11–0	BA1–0	CA7–0
	64M x 8bit	12 x 12 x 4	CA12	CA11	CA9	CA8	RA11–0	BA1–0	CA7–0
		13 x 11 x 4	CA11	CA9	CA8	RA12	RA11–0	BA1–0	CA7–0

1.7.7.1.2 SDRAM SDR Connections

Figure 4 shows a block diagram of the connections between the MCF548*x* and SDR SDRAM components. SDR design requires special timing consideration for the SD_DQS[3:0] signals. For reads from DDR SDRAMs, the memory will drive the DQS pins so that the data lines and DQS signals have concurrent edges. The MCF548*x* SDRAMC is designed to latch data 1/4 clock after the SD_DQS[3:0] edge. For DDR SDRAM, this ensures that the latch time is in the middle of the data valid window.

The MCF548*x* also uses the SDDQS[3:0] signals to determine when read data can be latched for SDR SDRAM; however, SDR memories do not provide DQS outputs. Instead the SDRAMC provides an SDRDQS output that is routed back into the controller as SDDQS[3:0]. The SDRDQS signal should be routed such that the valid data from the SDRAM reaches the MCF548*x* at the same time or just before the SDRDQS reaches the SDDQS[3:0] inputs. The appropriate delay for SDRDQS can be generated using a buffer or driver, as shown in Figure 4. Using a buffer or driver will also ensure that the SDRDQS signal can drive all four of the MCF548*x*'s SDDQS[3:0] inputs.

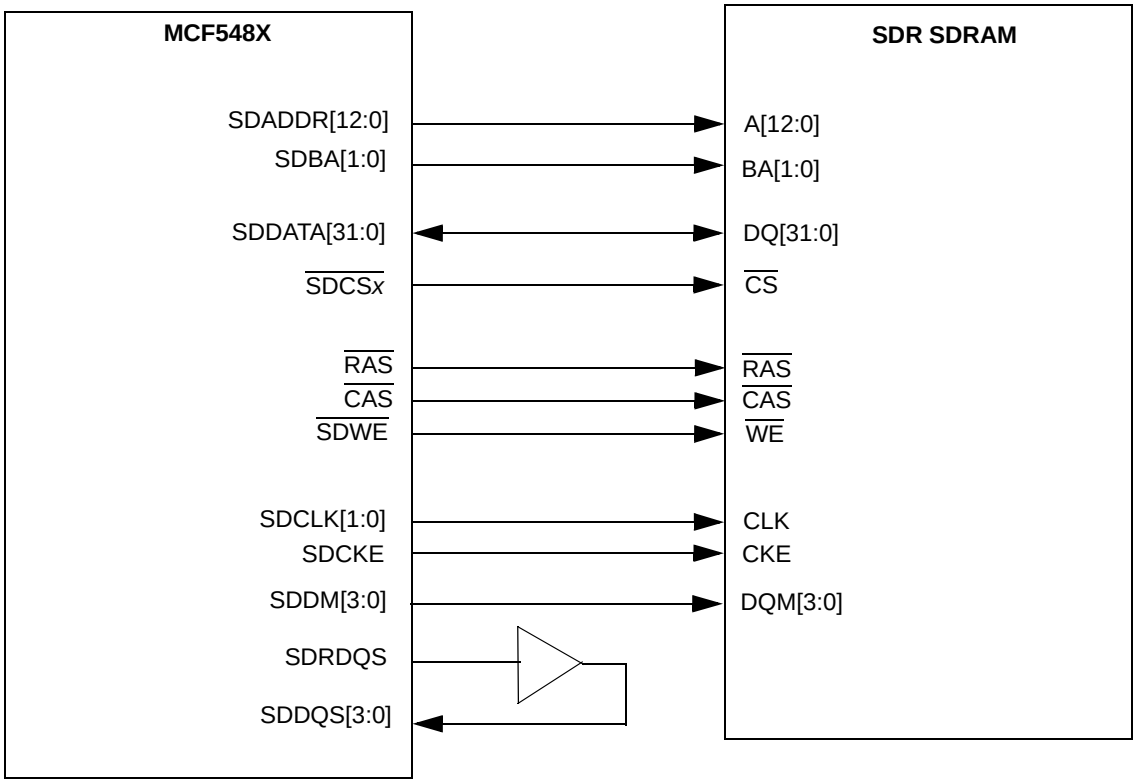


Figure 4. MCF548*x* Connections to SDR SDRAM

1.7.7.1.3 SDRAM DDR Component Connections

Figure 5 shows a block diagram of the connections between the MCF548*x* and DDR SDRAM components.

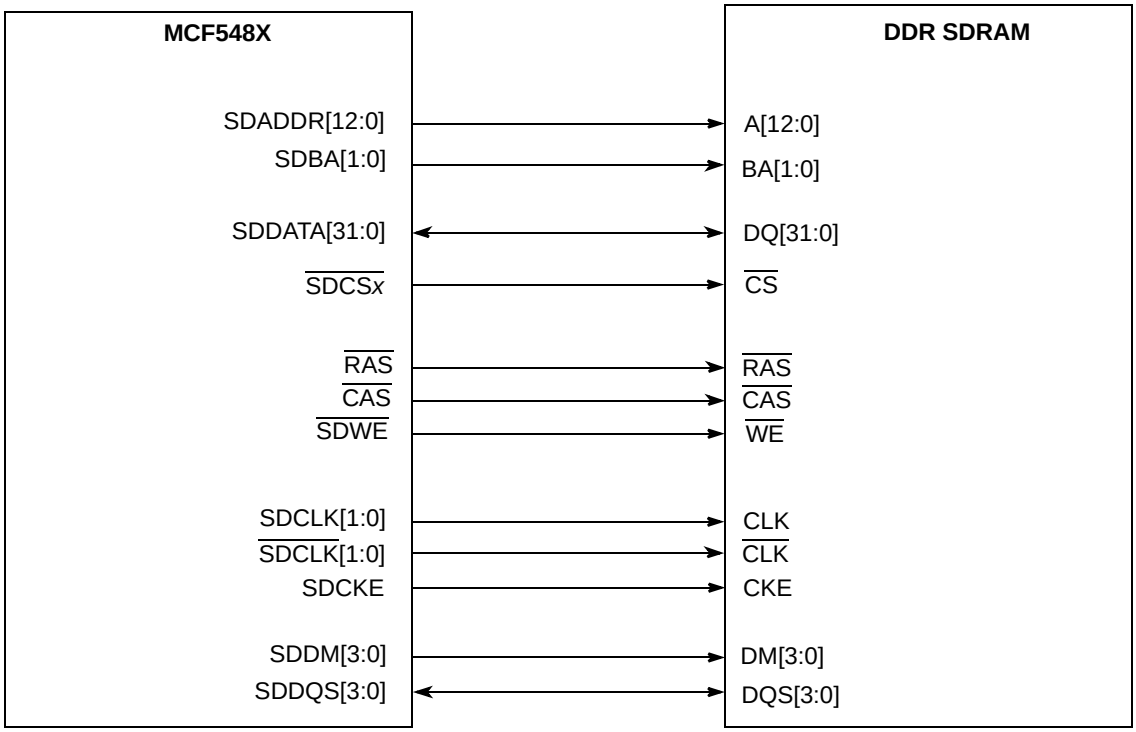


Figure 5. MCF548*x* Connections to DDR SDRAM

1.7.7.1.4 SDRAM DDR DIMM Connections

There is a JEDEC standard for a 100-pin DDR DIMM with a 32-bit wide data bus. This DIMM standard was designed specifically to support 32-bit processors. The MCF548*x* can support current DIMM configurations up to 512 Mbytes.

Figure 6 shows a block diagram of the connections between the MCF548*x* and DDR SDRAM Dims.

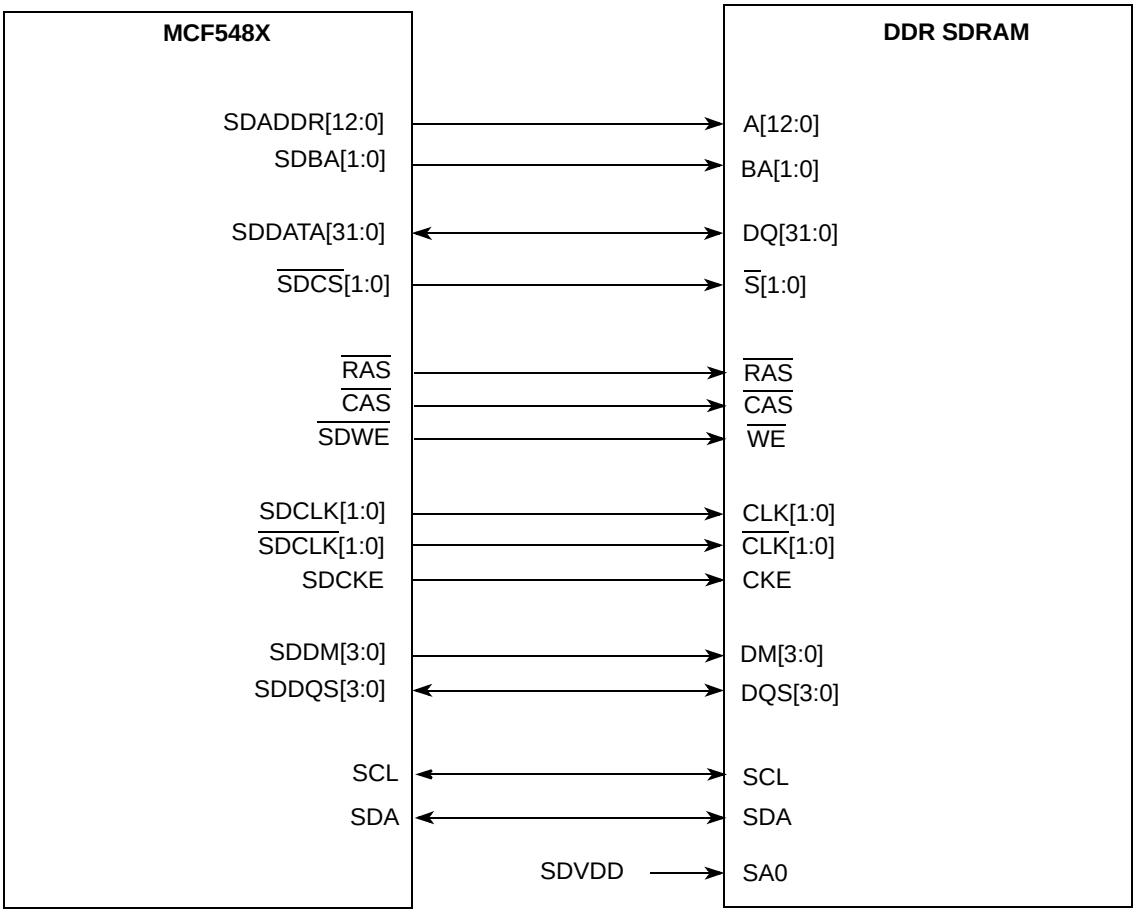


Figure 6. MCF548*x* Connections to 100-pin DDR SDRAM DIMM

1.7.7.1.5 DDR SDRAM Layout Considerations

Due to the critical timing for DDR SDRAM there are a number of considerations that should be taken into account during PCB layout:

- Minimize overall trace lengths.
- Each DQS, DM, and DQ group must have identical loading and similar routing to maintain timing integrity.
- Control and clock signals are routed point-to-point.
- Trace length for clock, address, and command signals should match.
- Route DDR signals on layers adjacent to the ground plane
- Use a VREF plane under the SDRAM.
- VREF is decoupled from both SDVDD and VSS.
- To avoid crosstalk keep address and command signals separate from data and data strobes.
- Use different resistor packs for command/address and data/data strobes.
- Use single series, single parallel termination (25 Ω series, 50 Ω parallel values are recommended, but standard resistor packs with similar values can be substituted.)

- Series termination should be between MCF548*x* and memory, but closest to the processor.
- The parallel termination at end of the signal line.
- 0.1 µF decoupling for every termination resistor pack.

1.7.7.1.6 Termination Example

Figure 7 shows the recommended termination circuitry for DDR SDRAM signals.

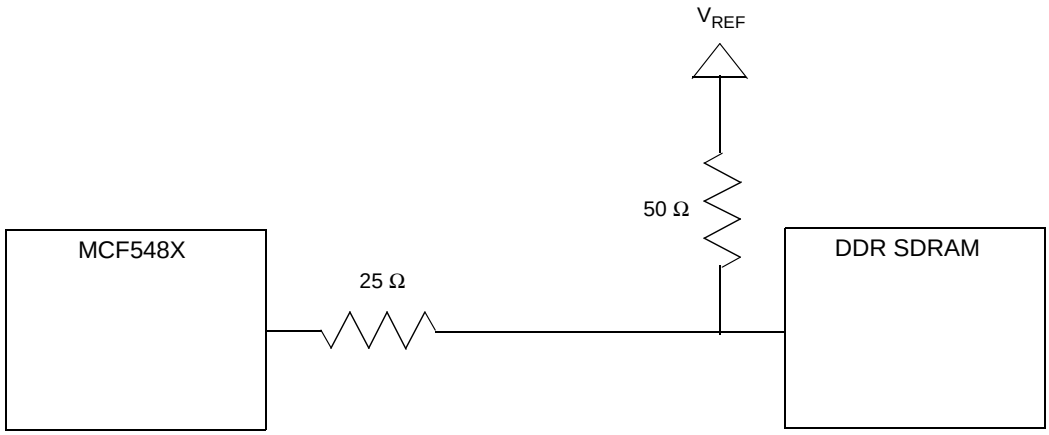


Figure 7. MCF548*x* DDR SDRAM Termination Circuit

1.7.7.2 Ethernet PHY Transceiver Connection

The FEC supports both an MII interface for 10/100 Mbps Ethernet and a 7-wire serial interface for 10 Mbps Ethernet. The interface mode is selected by RCR[MII_MODE]. In MII mode, the 802.3 standard defines and the FEC module supports 18 signals. Table 14 shows the signals used in MII mode.

Table 14. MII Mode

Signal Description	MCF548*x* Pin
Transmit clock	ETXCLK
Transmit enable	ETXEN
Transmit data	ETXD[3:0]
Transmit error	ETXER
Collision	ECOL
Carrier sense	ECRS
Receive clock	ERXCLK
Receive enable	ERXDV
Receive data	ERXD[3:0]
Receive error	ERXER
Management channel clock	EMDC
Management channel serial data	EMDIO

The serial mode interface operates in what is generally referred to as AMD mode. The MCF548*x* configuration for seven-wire serial mode connections to the external transceiver are shown in Table 15.

Table 15. Seven-Wire Mode Configuration

Signal Description	MCF548*x* Pin
Transmit clock	ETXCLK
Transmit enable	ETXEN
Transmit data	ETXD[0]
Collision	ECOL
Receive clock	ERXCLK
Receive enable	ERXDV
Receive data	ERXD[0]
Unused, configure as PB14	ERXER
Unused input, tie to ground	ECRS
Unused, configure as PB[13:11]	ERXD[3:1]
Unused output, ignore	ETXER
Unused, configure as PB[10:8]	ETXD[3:1]
Unused, configure as PB15	EMDC
Input after reset, connect to ground	EMDIO

Refer to the M5282EVB evaluation board user's manual for an example of how to connect an external PHY. Schematics for this board are accessible at the MCF5282 site by navigating from: http://e-www.motorola.com/ following the 32-bit Embedded Processors, 68K/ColdFire, MCF5xxx, MCF5282, and M5282EVB links.

1.7.7.3 FlexCAN

The FlexCAN module interface to the CAN bus is composed of two pins: CANTX and CANRX, which are the serial transmitted data and the serial received data. The use of an external CAN transceiver to interface to the CAN bus is generally required. The transceiver is capable of driving the large current needed for the CAN bus and has current protection, against a defective CAN bus or defective stations.

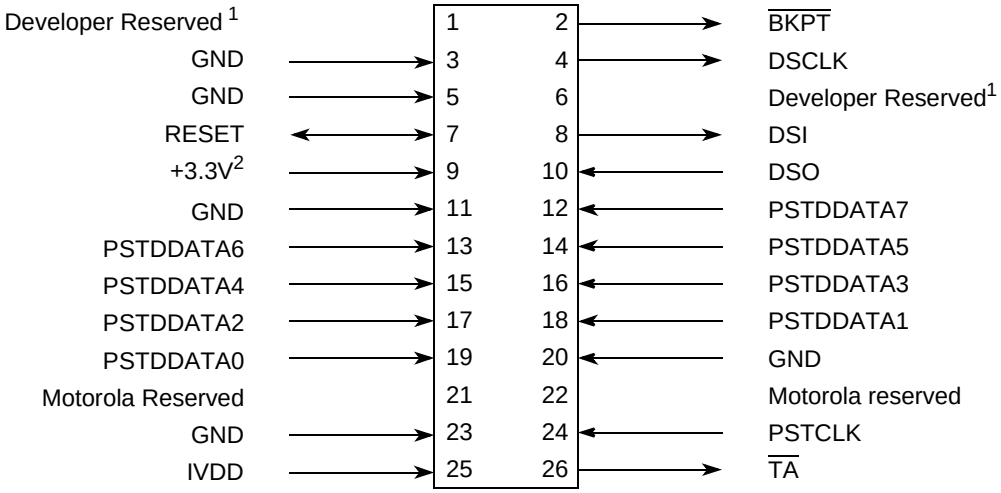
1.7.7.4 BDM

Use the BDM interface as shown in the M5407C3 evaluation board user's manual. The schematics for this board are accessible at the MCF5407 site by navigating from: http://e-www.motorola.com/ following the 32-bit Embedded Processors, 68K/ColdFire, MCF5xxx, MCF5407 and M5407C3 links.

The ColdFire BDM connector, Figure 8, is a 26-pin Berg connector arranged 2 × 13.

NOTE

Some BDM cables tie pin 9 and pin 25 together, even though the official specification lists the two pins at different voltages. A jumper can be added to make the voltage on pin 25 selectable between IVDD and EVDD. This allows the voltage to be changed for compatability with older BDM cables.



1 Pins reserved for BDM developer use
2 Supplied by target

Figure 8. Recommended BDM Connector

1.8 MCF5485/5484 Pinout

Figure 9–Figure 12 show the pinout for the each quadrant of the MCF5485/MCF5484 388 PBGA package. Figure 9 shows the pinout for the upper left quadrant.

	1	2	3	4	5	6	7	8	9	10	11	12	13
A	SDVDD	VSS	SDDM2	SDDATA 23	SDDATA 24	SDDATA 27	SDDQS 3	SDDATA 29	SDADD R0	SDADD R3	SDADD R7	SDADD R11	SDADD R12
B	SDVDD	VSS	SDDDATA18	SDDATA 20	SDDQS 2	SDDATA 21	SDDATA 25	SDDM3	SDDATA 30	SDADD R1	SDADD R5	SDADD R9	$\overline{\text{RSTI}}$
C	SDVDD	$\overline{\text{CAS}}$	VSS	SDDATA 17	SDDATA 19	SDVDD	SDDATA 22	SDDATA 26	SDVDD	SDDATA 31	SDADD R4	SDADD R8	SDVDD
D	SDDATA 14	VREF	SDVDD	SDDATA 16	SDDATA 28	VSS	SDADD R2	SDADD R6	VSS	SDADD R10	IVDD	IVDD	VSS
E	SDDATA 12	SDDATA 15	$\overline{\text{RAS}}$	SDCKE									
F	SDDDATA10	SDDQS 1	SDVDD	VSS									
G	SDDATA 6	SDDATA 9	SDDM1	SDDATA 13									
H	SDDQS 0	SDDATA 5	SDDATA 8	IVDD									
J	SDDATA 3	SDDM0	SDDATA 4	VSS									
K	$\overline{\text{SDWE}}$	SDDATA 0	SDDATA 1	SDDATA 11									
L	SDCLK1	SDRDQS	SDVDD	VSS							VSS	VSS	VSS
M	$\overline{\text{SDCLK1}}$	SDBA1	SDBA0	SDDATA 2							VSS	VSS	VSS
N	SDCLK0	$\overline{\text{SDCLK0}}$	$\overline{\text{SDCS0}}$	SDDATA 7							VSS	VSS	VSS

Figure 9. MCF5485/5484 Upper Left Quadrant Pinout (388 MAPBGA)

Figure 10 shows the pinout for the upper right quadrant of the MCF5485/MCF5484 pinout for the 388 PBGA package.

	14	15	16	17	18	19	20	21	22	23	24	25	26
A	IRQ5	DSI/TDI	TCK	CLKIN	MTMOD1	PLLVDD	RSTO	PSTDDATA1	PSTDDATA3	PSTDDATA7	PCIBR0	PCIBR2	E1RXD1
B	IRQ6	BKPT/TMS	MTMOD0	MTMOD3	PLLVSS	PSTDDATA0	PSTDDATA2	PSTDDATA6	E1RXCLK	PCIBR1	PCIBR3	E1RXDV	E1RXD2
C	MTMOD2	DSCLK/TRST	EVDD	VSS	IVDD	VSS	PSTDDATA4	VSS	EVDD	PCIIDSEL	SDA	SCL	PCITRDY
D	IRQ7	NC	VSS	DSO/TDO	PSTDDATA5	IVDD	PSTCLK	PCIBR4	IVDD	VSS	PCIIRDY	E1RXD3	PCIPERR
E										VSS	EVDD	PCISTOP	PCICXBE1
F										PCIPAR	PCISERR	PCIFRM	PCICXBE3
G										PCIRESET	PCICXBE0	PCICXBE2	PCIAD2
H										IVDD	EVDD	PCIAD1	PCIAD4
J										PCIDEVSEL	PCIAD3	PCIAD5	PCIAD7
K										PCIAD0	PCIAD6	PCIAD8	PCIAD9
L	VSS	VSS	VSS							IVDD	VSS	PCIAD10	PCIAD11
M	VSS	VSS	VSS							VSS	EVDD	PCIAD12	PCIAD13
N	VSS	VSS	VSS							PCIAD16	PCIAD14	PCIAD17	PCIAD15

Figure 10. MCF5485/5484 Upper Right Quadrant Pinout (388 PBGA)

Figure 11 shows the pinout for the lower left quadrant of the MCF5485/MCF5484 pinout for the 388 PBGA package.

	1	2	3	4	5	6	7	8	9	10	11	12	13
P	$\overline{SDCS1}$	$\overline{SDCS2}$	SDVDD	IVDD							VSS	VSS	VSS
R	$\overline{FBCS5}$	$\overline{SDCS3}$	EVDD	VSS							VSS	VSS	VSS
T	$\overline{FBCS2}$	$\overline{FBCS4}$	$\overline{FBCS3}$	AD1							VSS	VSS	VSS
U	$\overline{FBCS0}$	$\overline{FBCS1}$	AD0	VSS									
V	AD3	AD2	AD4	IVDD									
W	AD6	AD5	AD7	AD13									
Y	AD9	AD8	EVDD	VSS									
AA	AD10	AD11	AD14	AD19									
AB	AD12	AD15	EVDD	VSS									
AC	AD17	AD20	AD22	$\overline{BE}/\overline{BW}$ $\overline{E1}$	E1CRS	E0TXD2	VSS	E1TXD3	E0COL	VSS	E1TXD2	IVDD	USB_OSCVDD
AD	AD16	AD21	AD23	AD24	AD26	$\overline{TS}$	EVDD	E0TXD3	E0TXD0	EVDD	E0MDC	VSS	E0RXD0
AE	AD18	AD31	AD28	AD27	R/$\overline{W}$	$\overline{OE}$	$\overline{BE}/\overline{BW}$ $\overline{E0}$	E1RXER	E0TXER	E0TXEN	E1TXD1	E1TXD0	E1TXCLK
AF	AD29	AD25	AD30	$\overline{BE}/\overline{BW}$ $\overline{E3}$	$\overline{BE}/\overline{BW}$ $\overline{E2}$	$\overline{TA}$	E0TXD1	E1COL	E0TXCLK	E0MDIO	E0RXD3	E0RXD2	E0RXD1

Figure 11. MCF5485/5484 Lower Left Quadrant Pinout (388 PBGA)

Figure 12 shows the pinout for the lower left quadrant of the MCF5485/MCF5484 pinout for the 388 PBGA package.

	14	15	16	17	18	19	20	21	22	23	24	25	26
P	VSS	VSS	VSS							PCIAD19	PCIAD20	PCIAD18	PCIAD21
R	VSS	VSS	VSS							IVDD	PCIAD24	PCIAD23	PCIAD22
T	VSS	VSS	VSS							VSS	PCIAD27	PCIAD26	PCIAD25
U										VSS	EVDD	PCIAD29	PCIAD28
V										DSPICS3	$\overline{\text{PCIBG1}}$	PCIAD31	PCIAD30
W										DSPICS5/$\overline{\text{PCSS}}$	$\overline{\text{PCIBG4}}$	$\overline{\text{PCIBG2}}$	$\overline{\text{PCIBG0}}$
Y										$\overline{\text{PSC1RTS}}$	DSPISOUT	DSPICS0/$\overline{\text{SS}}$	$\overline{\text{PCIBG3}}$
AA										IVDD	EVDD	PSC0TXD	DSPICS2
AB										$\overline{\text{PSC3RTS}}$	$\overline{\text{DACK0}}$	PSC1TXD	$\overline{\text{PSC0RTS}}$
AC	E0RXER	NC	USB_PHYVDD	USBVBUS	VSS	$\overline{\text{PSC2CTS}}$	IVDD	PSC0RXD	TOUT2	TOUT1	DSPISIN	$\overline{\text{DACK1}}$	PSC2TXD
AD	E0RXCLK	USB_OSCAVDD	USB_PLLVDD	VSS	EVDD	TIN3	VSS	PSC2RXD	DSPISCK	TOUT3	E1MDC	E1TXEN	$\overline{\text{PSC2RTS}}$
AE	E0RXDV	VSS	VSS	VSS	USBVDD	E0CRS	TIN1	PSC3RXD	PSC1RXD	$\overline{\text{PSC0CTS}}$	E1TXER	E1MDIO	PSC3TXD
AF	USBCLKOUT	USBCLKIN	USBD+	USBD-	USBRBIAS	$\overline{\text{DREQ1}}$	$\overline{\text{DREQ0}}$	TIN2	TIN0	$\overline{\text{PSC3CTS}}$	E1RXD0	$\overline{\text{PSC1CTS}}$	TOUT0

Figure 12. MCF5485/5484 Lower Right Quadrant Pinout (388 PBGA)

1.9 MCF5483/5482 Pinout

Figure 13–Figure 16 show the pinout for the each quadrant of the MCF5483/MCF5482 388 PBGA package. Figure 13 shows the pinout for the upper left quadrant.

	1	2	3	4	5	6	7	8	9	10	11	12	13
A	SDVDD	VSS	SDDM2	SDDATA 23	SDDATA 24	SDDATA 27	SDDQS 3	SDDATA 29	SDADD R0	SDADD R3	SDADD R7	SDADD R11	SDADD R12
B	SDVDD	VSS	SDDDA TA18	SDDATA 20	SDDQS 2	SDDATA 21	SDDATA 25	SDDM3	SDDATA 30	SDADD R1	SDADD R5	SDADD R9	$\overline{\text{RSTI}}$
C	SDVDD	$\overline{\text{CAS}}$	VSS	SDDATA 17	SDDATA 19	SDVDD	SDDATA 22	SDDATA 26	SDVDD	SDDATA 31	SDADD R4	SDADD R8	SDVDD
D	SDDATA 14	VREF	SDVDD	SDDATA 16	SDDATA 28	VSS	SDADD R2	SDADD R6	VSS	SDADD R10	IVDD	IVDD	VSS
E	SDDATA 12	SDDATA 15	$\overline{\text{RAS}}$	SDCKE									
F	SDDDA TA10	SDDQS 1	SDVDD	VSS									
G	SDDATA 6	SDDATA 9	SDDM1	SDDATA 13									
H	SDDQS 0	SDDATA 5	SDDATA 8	IVDD									
J	SDDATA 3	SDDM0	SDDATA 4	VSS									
K	$\overline{\text{SDWE}}$	SDDATA 0	SDDATA 1	SDDATA 11									
L	SDCLK1	SDRDQ S	SDVDD	VSS							VSS	VSS	VSS
M	$\overline{\text{SDCLK1}}$	SDBA1	SDBA0	SDDATA 2							VSS	VSS	VSS
N	SDCLK0	$\overline{\text{SDCLK0}}$	$\overline{\text{SDCS0}}$	SDDATA 7							VSS	VSS	VSS

Figure 13. MCF5483/5482 Upper Left Quadrant Pinout (388 PBGA)

Figure 14 shows the pinout for the upper right quadrant of the MCF5483/MCF5482 pinout for the 388 PBGA package.

	14	15	16	17	18	19	20	21	22	23	24	25	26
A	IRQ5	DSI/TDI	TCK	CLKIN	MTMOD1	PLLVDD	RSTO	PSTDDATA1	PSTDDATA3	PSTDDATA7	PCIBR0	PCIBR2	NC
B	IRQ6	BKPT/TMS	MTMOD0	MTMOD3	PLLVSS	PSTDDATA0	PSTDDATA2	PSTDDATA6	NC	PCIBR1	PCIBR3	NC	NC
C	MTMOD2	DSCLK/TRST	EVDD	VSS	IVDD	VSS	PSTDDATA4	VSS	EVDD	PCIIDSEL	SDA	SCL	PCITRDY
D	IRQ7	NC	VSS	DSO/TDO	PSTDDATA5	IVDD	PSTCLK	PCIBR4	IVDD	VSS	PCIIRDY	NC	PCIPERR
E										VSS	EVDD	PCISTOP	PCICXBE1
F										PCIPAR	PCISERR	PCIFRM	PCICXBE3
G										PCIRESET	PCICXBE0	PCICXBE2	PCIAD2
H										IVDD	EVDD	PCIAD1	PCIAD4
J										PCIDEVSEL	PCIAD3	PCIAD5	PCIAD7
K										PCIAD0	PCIAD6	PCIAD8	PCIAD9
L	VSS	VSS	VSS							IVDD	VSS	PCIAD10	PCIAD11
M	VSS	VSS	VSS							VSS	EVDD	PCIAD12	PCIAD13
N	VSS	VSS	VSS							PCIAD16	PCIAD14	PCIAD17	PCIAD15

Figure 14. MCF5483/5482 Upper Right Quadrant Pinout (388 PBGA)

Figure 15 shows the pinout for the lower left quadrant of the MCF5483/MCF5482 pinout for the 388 PBGA package.

	1	2	3	4	5	6	7	8	9	10	11	12	13
P	$\overline{\text{SDCS1}}$	$\overline{\text{SDCS2}}$	SDVDD	IVDD							VSS	VSS	VSS
R	$\overline{\text{FBCS5}}$	$\overline{\text{SDCS3}}$	EVDD	VSS							VSS	VSS	VSS
T	$\overline{\text{FBCS2}}$	$\overline{\text{FBCS4}}$	$\overline{\text{FBCS3}}$	AD1							VSS	VSS	VSS
U	$\overline{\text{FBCS0}}$	$\overline{\text{FBCS1}}$	AD0	VSS									
V	AD3	AD2	AD4	IVDD									
W	AD6	AD5	AD7	AD13									
Y	AD9	AD8	EVDD	VSS									
AA	AD10	AD11	AD14	AD19									
AB	AD12	AD15	EVDD	VSS									
AC	AD17	AD20	AD22	$\overline{\text{BE}}/\overline{\text{BW}}$ $\overline{\text{E1}}$	NC	E0TXD2	VSS	NC	E0COL	VSS	NC	IVDD	USB_OSCVDD
AD	AD16	AD21	AD23	AD24	AD26	$\overline{\text{TS}}$	EVDD	E0TXD3	E0TXD0	EVDD	E0MDC	VSS	E0RXD0
AE	AD18	AD31	AD28	AD27	R/$\overline{\text{W}}$	$\overline{\text{OE}}$	$\overline{\text{BE}}/\overline{\text{BW}}$ $\overline{\text{E0}}$	NC	E0TXER	E0TXEN	NC	NC	NC
AF	AD29	AD25	AD30	$\overline{\text{BE}}/\overline{\text{BW}}$ $\overline{\text{E3}}$	$\overline{\text{BE}}/\overline{\text{BW}}$ $\overline{\text{E2}}$	$\overline{\text{TA}}$	E0TXD1	NC	E0TXCLK	E0MDIO	E0RXD3	E0RXD2	E0RXD1

Figure 15. MCF5483/5482 Lower Left Quadrant Pinout (388 PBGA)

Figure 16 shows the pinout for the lower left quadrant of the MCF5483/MCF5482 pinout for the 388 PBGA package.

	14	15	16	17	18	19	20	21	22	23	24	25	26
P	VSS	VSS	VSS							PCIAD19	PCIAD20	PCIAD18	PCIAD21
R	VSS	VSS	VSS							IVDD	PCIAD24	PCIAD23	PCIAD22
T	VSS	VSS	VSS							VSS	PCIAD27	PCIAD26	PCIAD25
U										VSS	EVDD	PCIAD29	PCIAD28
V										DSPICS3	$\overline{\text{PCIBG1}}$	PCIAD31	PCIAD30
W										DSPICS5/$\overline{\text{PCSS}}$	$\overline{\text{PCIBG4}}$	$\overline{\text{PCIBG2}}$	$\overline{\text{PCIBG0}}$
Y										$\overline{\text{PSC1RTS}}$	DSPISOUT	DSPICS0/$\overline{\text{SS}}$	$\overline{\text{PCIBG3}}$
AA										IVDD	EVDD	PSC0TXD	DSPICS2
AB										$\overline{\text{PSC3RTS}}$	$\overline{\text{DACK0}}$	PSC1TXD	$\overline{\text{PSC0RTS}}$
AC	E0RXER	NC	USB_PHYVDD	USBVBUS	VSS	$\overline{\text{PSC2CTS}}$	IVDD	PSC0RXD	TOUT2	TOUT1	DSPISIN	$\overline{\text{DACK1}}$	PSC2TXD
AD	E0RXCLK	USB_OSCAVDD	USB_PLLVDD	VSS	EVDD	TIN3	VSS	PSC2RXD	DSPISCK	TOUT3	NC	NC	$\overline{\text{PSC2RTS}}$
AE	E0RXDV	VSS	VSS	VSS	USBVDD	E0CRS	TIN1	PSC3RXD	PSC1RXD	$\overline{\text{PSC0CTS}}$	NC	NC	PSC3TXD
AF	USBCLKOUT	USBCLKIN	USBD+	USBD-	USBRBIAS	$\overline{\text{DREQ1}}$	$\overline{\text{DREQ0}}$	TIN2	TIN0	$\overline{\text{PSC3CTS}}$	NC	$\overline{\text{PSC1CTS}}$	TOUT0

Figure 16. MCF5483/5482 Lower Right Quadrant Pinout (388 PBGA)

1.10 MCF5481/5480 Pinout

Figure 17–Figure 20 show the pinout for the each quadrant of the MCF5481/MCF5480 388 PBGA package. Figure 17 shows the pinout for the upper left quadrant.

	1	2	3	4	5	6	7	8	9	10	11	12	13
A	SDVDD	VSS	SDDM2	SDDATA 23	SDDATA 24	SDDATA 27	SDDQS 3	SDDATA 29	SDADD R0	SDADD R3	SDADD R7	SDADD R11	SDADD R12
B	SDVDD	VSS	SDDDA TA18	SDDATA 20	SDDQS 2	SDDATA 21	SDDATA 25	SDDM3	SDDATA 30	SDADD R1	SDADD R5	SDADD R9	$\overline{\text{RSTI}}$
C	SDVDD	$\overline{\text{CAS}}$	VSS	SDDATA 17	SDDATA 19	SDVDD	SDDATA 22	SDDATA 26	SDVDD	SDDATA 31	SDADD R4	SDADD R8	SDVDD
D	SDDATA 14	VREF	SDVDD	SDDATA 16	SDDATA 28	VSS	SDADD R2	SDADD R6	VSS	SDADD R10	IVDD	IVDD	VSS
E	SDDATA 12	SDDATA 15	$\overline{\text{RAS}}$	SDCKE									
F	SDDDA TA10	SDDQS 1	SDVDD	VSS									
G	SDDATA 6	SDDATA 9	SDDM1	SDDATA 13									
H	SDDQS 0	SDDATA 5	SDDATA 8	IVDD									
J	SDDATA 3	SDDM0	SDDATA 4	VSS									
K	$\overline{\text{SDWE}}$	SDDATA 0	SDDATA 1	SDDATA 11									
L	SDCLK1	SDRDQ S	SDVDD	VSS							VSS	VSS	VSS
M	$\overline{\text{SDCLK1}}$	SDBA1	SDBA0	SDDATA 2							VSS	VSS	VSS
N	SDCLK0	$\overline{\text{SDCLK0}}$	$\overline{\text{SDCS0}}$	SDDATA 7							VSS	VSS	VSS

Figure 17. MCF5481/5480 Upper Left Quadrant Pinout (388 PBGA)

Figure 18 shows the pinout for the upper right quadrant of the MCF5481/MCF5480 pinout for the 388 PBGA package.

	14	15	16	17	18	19	20	21	22	23	24	25	26
A	IRQ5	DSI/TDI	TCK	CLKIN	MTMOD1	PLLVDD	RSTO	PSTDDATA1	PSTDDATA3	PSTDDATA7	PCIBR0	PCIBR2	E1RXD1
B	IRQ6	BKPT/TMS	MTMOD0	MTMOD3	PLLVSS	PSTDDATA0	PSTDDATA2	PSTDDATA6	E1RXCLK	PCIBR1	PCIBR3	E1RXDV	E1RXD2
C	MTMOD2	DSCLK/TRST	EVDD	VSS	IVDD	VSS	PSTDDATA4	VSS	EVDD	PCIIDSEL	SDA	SCL	PCITRDY
D	IRQ7	NC	VSS	DSO/TDO	PSTDDATA5	IVDD	PSTCLK	PCIBR4	IVDD	VSS	PCIIRDY	E1RXD3	PCIPERR
E										VSS	EVDD	PCISTOP	PCICXBE1
F										PCIPAR	PCISERR	PCIFRM	PCICXBE3
G										PCIRESET	PCICXBE0	PCICXBE2	PCIAD2
H										IVDD	EVDD	PCIAD1	PCIAD4
J										PCIDEVSEL	PCIAD3	PCIAD5	PCIAD7
K										PCIAD0	PCIAD6	PCIAD8	PCIAD9
L	VSS	VSS	VSS							IVDD	VSS	PCIAD10	PCIAD11
M	VSS	VSS	VSS							VSS	EVDD	PCIAD12	PCIAD13
N	VSS	VSS	VSS							PCIAD16	PCIAD14	PCIAD17	PCIAD15

Figure 18. MCF5481/5480 Upper Right Quadrant Pinout (388 PBGA)

Figure 19 shows the pinout for the lower left quadrant of the MCF5481/MCF5480 pinout for the 388 PBGA package.

	1	2	3	4	5	6	7	8	9	10	11	12	13
P	$\overline{\text{SDCS1}}$	$\overline{\text{SDCS2}}$	SDVDD	IVDD							VSS	VSS	VSS
R	$\overline{\text{FBCS5}}$	$\overline{\text{SDCS3}}$	EVDD	VSS							VSS	VSS	VSS
T	$\overline{\text{FBCS2}}$	$\overline{\text{FBCS4}}$	$\overline{\text{FBCS3}}$	AD1							VSS	VSS	VSS
U	$\overline{\text{FBCS0}}$	$\overline{\text{FBCS1}}$	AD0	VSS									
V	AD3	AD2	AD4	IVDD									
W	AD6	AD5	AD7	AD13									
Y	AD9	AD8	EVDD	VSS									
AA	AD10	AD11	AD14	AD19									
AB	AD12	AD15	EVDD	VSS									
AC	AD17	AD20	AD22	$\overline{\text{BE}}/\overline{\text{BW}}$ $\overline{\text{E1}}$	E1CRS	E0TXD2	VSS	E1TXD3	E0COL	VSS	E1TXD2	IVDD	USB_OSCVDD [1]
AD	AD16	AD21	AD23	AD24	AD26	$\overline{\text{TS}}$	EVDD	E0TXD3	E0TXD0	EVDD	E0MDC	VSS	E0RXD0
AE	AD18	AD31	AD28	AD27	R/$\overline{\text{W}}$	$\overline{\text{OE}}$	$\overline{\text{BE}}/\overline{\text{BW}}$ $\overline{\text{E0}}$	E1RXER	E0TXER	E0TXEN	E1TXD1	E1TXD0	E1TXCLK
AF	AD29	AD25	AD30	$\overline{\text{BE}}/\overline{\text{BW}}$ $\overline{\text{E3}}$	$\overline{\text{BE}}/\overline{\text{BW}}$ $\overline{\text{E2}}$	$\overline{\text{TA}}$	E0TXD1	E1COL	E0TXCLK	E0MDIO	E0RXD3	E0RXD2	E0RXD1

1 TBD if the USB power pins are connected when the USB is disabled or not used.

Figure 19. MCF5481/5480 Lower Left Quadrant Pinout (388 PBGA)

Figure 20 shows the pinout for the lower left quadrant of the MCF5481/MCF5480 pinout for the 388 PBGA package.

	14	15	16	17	18	19	20	21	22	23	24	25	26
P	VSS	VSS	VSS							PCIAD19	PCIAD20	PCIAD18	PCIAD21
R	VSS	VSS	VSS							IVDD	PCIAD24	PCIAD23	PCIAD22
T	VSS	VSS	VSS							VSS	PCIAD27	PCIAD26	PCIAD25
U										VSS	EVDD	PCIAD29	PCIAD28
V										DSPICS3	$\overline{\text{PCIBG1}}$	PCIAD31	PCIAD30
W										DSPICS5/$\overline{\text{PCSS}}$	$\overline{\text{PCIBG4}}$	$\overline{\text{PCIBG2}}$	$\overline{\text{PCIBG0}}$
Y										$\overline{\text{PSC1RTS}}$	DSPISOUT	DSPICS0/$\overline{\text{SS}}$	$\overline{\text{PCIBG3}}$
AA										IVDD	EVDD	PSC0TXD	DSPICS2
AB										$\overline{\text{PSC3RTS}}$	$\overline{\text{DACK0}}$	PSC1TXD	$\overline{\text{PSC0RTS}}$
AC	E0RXER	NC	USB_PHYVDD[1]	NC	VSS	$\overline{\text{PSC2CTS}}$	IVDD	PSC0RXD	TOUT2	TOUT1	DSPISIN	$\overline{\text{DACK1}}$	PSC2TXD
AD	E0RXCLK	USB_OSCAVDD[1]	USB_PLLVDD[1]	VSS	EVDD	TIN3	VSS	PSC2RXD	DSPISCK	TOUT3	E1MDC	E1TXEN	$\overline{\text{PSC2RTS}}$
AE	E0RXDV	VSS	VSS	VSS	USBVDD[1]	E0CRS	TIN1	PSC3RXD	PSC1RXD	$\overline{\text{PSC0CTS}}$	E1TXER	E1MDIO	PSC3TXD
AF	NC	NC	NC	NC	NC	$\overline{\text{DREQ1}}$	$\overline{\text{DREQ0}}$	TIN2	TIN0	$\overline{\text{PSC3CTS}}$	E1RXD0	$\overline{\text{PSC1CTS}}$	TOUT0

1 TBD if the USB power pins are connected when the USB is disabled or not used.

Figure 20. MCF5485/5484 Lower Right Quadrant Pinout (388 PBGA)

1.11 Mechanicals

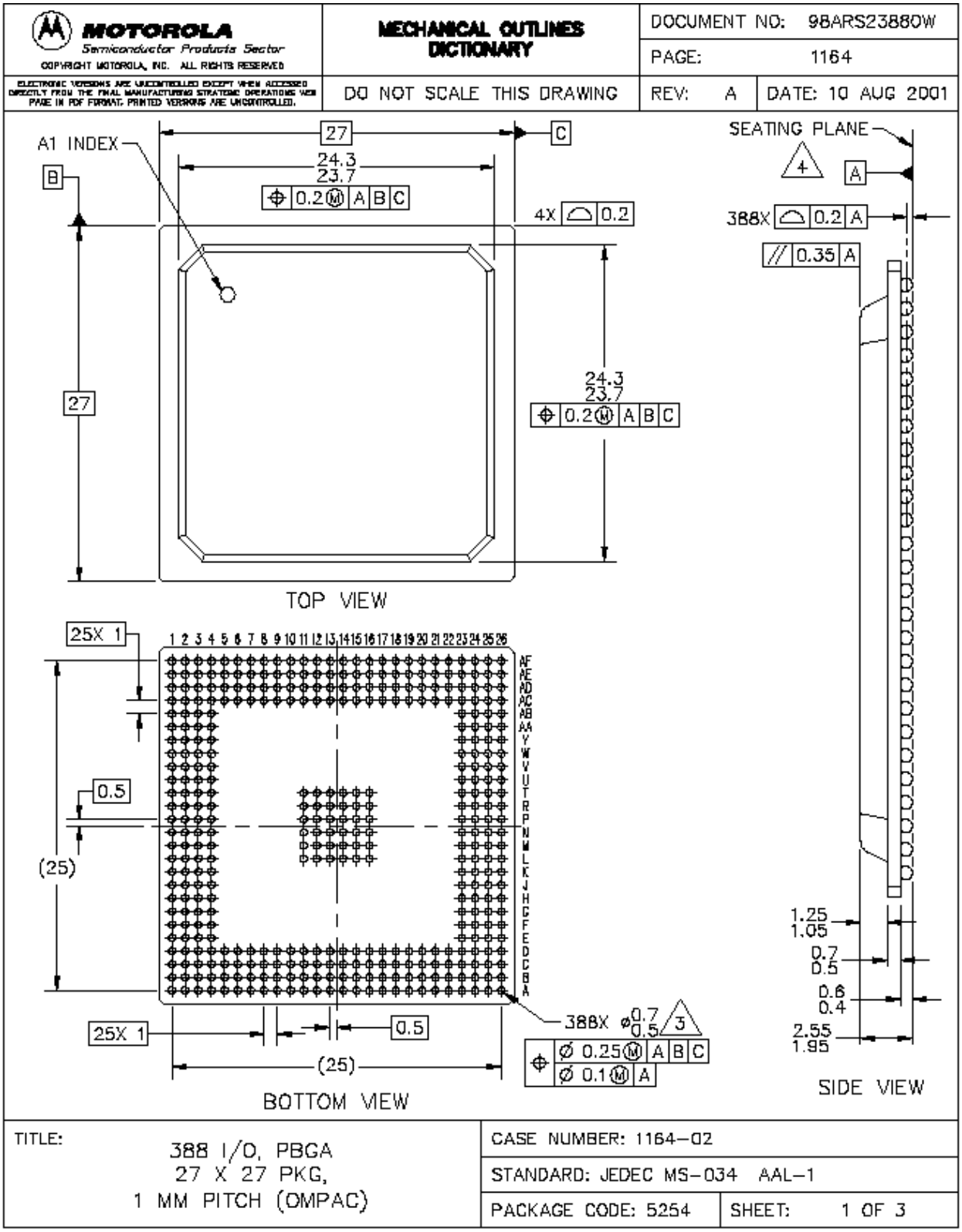


Figure 21. 388-pin PBGA Package Outline

1.12 Ordering Information

Table 16. Orderable Part Numbers

Motorola Part Number	Description	Package	Speed	Temperature
MCF5485CZP200	MCF5485 RISC Microprocessor	388 PBGA	200MHz	–40° to +85° C
MCF5484CZP200	MCF5484 RISC Microprocessor	388 PBGA	200MHz	–40° to +85° C
MCF5483CZP166	MCF5483 RISC Microprocessor	388 PBGA	166MHz	–40° to +85° C
MCF5482CZP166	MCF5482 RISC Microprocessor	388 PBGA	166MHz	–40° to +85° C
MCF5481CZP166	MCF5481 RISC Microprocessor	388 PBGA	166MHz	–40° to +85° C
MCF5480CZP166	MCF5480 RISC Microprocessor	388 PBGA	166MHz	–40° to +85° C

1.13 Device/Family Documentation List

Table 17. MCF548X Documentation

Motorola Document Number	Title	Revision	Status
MCF5485EC/D	MCF548x Integrated Microprocessor Hardware Specifications	1.0	This Document
V4ECFUM/D	ColdFire CF4e Core User's Manual	0	Available
MCF5485UM/D	MCF548X Advance Information Manual	0	In Process
MCF5485PB/D	MCF548X Product Brief	0	Available
CFPRODFACT/D	The ColdFire Family of 32-Bit Microprocessors Family Overview and Technology Roadmap	0	Available
MCF5XXXWP	MCF5XXXWP WHITE PAPER: Motorola ColdFire VL RISC Processors	0	Available
CFPRM/D	ColdFire Family Programmer's Reference Manual	2	Available

1.14 Document Revision History

Table 18 provides a revision history for the MCF548*x* hardware specification.

Table 18. Document Revision History

Rev. No.	Substantive Change(s)
0.1	Initial release.
1.0	Updated pinout information and signal names.
1.1	Updated VREFsignal description.
1.2	• Changed MAPBGA to PBGA throughout. • In Section 1.12, "Ordering Information," changed VF suffix to ZP.

Appendix A
Preliminary Electrical Characteristics

This section contains electrical specification tables and reference timing diagrams for the MCF548X microprocessor. This section contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications of MCF548X.

The electrical specifications are preliminary and are from previous designs or design simulations. These specifications may not be fully tested or guaranteed at this early stage of the product life cycle. Finalized specifications will be published after complete characterization and device qualifications have been completed.

NOTE

The parameters specified in this MPU document supersede any values found in the module specifications.

A.1 Maximum Ratings

Table 19 lists maximum and minimum ratings for supply and operating voltages and storage temperature. Operating outside of these ranges may cause erratic behavior or damage to the processor.

Table 19. Absolute Maximum Ratings

Rating	Symbol	Value	Units
External (I/O pads) supply voltage (3.3-V power pins)	EV_{DD}	-0.3 to +4.0	V
Internal logic supply voltage	IV_{DD}	-0.5 to +2.0	V
Memory (I/O pads) supply voltage (2.5-V power pins)	SD V_{DD}	-0.3 to +4.0 SDR Memory -0.3 to +2.8 DDR Memory	V
PLL supply voltage	PLL V_{DD}	-0.5 to +2.0	V
Internal logic supply voltage, input voltage level	V_{in}	-0.5 to +3.6	V
Storage temperature range	T_{stg}	-55 to +150	^{o}C

A.2 Thermal Characteristics

A.2.1 Operating Temperatures

Table 20 lists junction and ambient operating temperatures.

Table 20. Operating Temperatures

Characteristic	Symbol	Value	Units
Maximum operating junction temperature	T_j	105	^{o}C
Maximum operating ambient temperature	T_{Amax}	<85 [1]	^{o}C
Minimum operating ambient temperature	T_{Amin}	- 40	^{o}C

[1] This published maximum operating ambient temperature should be used only as a system design guideline. All device operating parameters are guaranteed only when the junction temperature lies within the specified range.

A.2.2 Thermal Resistance

Table 21 lists thermal resistance values.

Table 21. Thermal Resistance

Characteristic		Symbol	Value	Unit
388 pin TEPBGA — Junction to ambient, natural convection	Four layer board (2s2p)	θ_{JMA}	20–22[1,2]	°C/W
Junction to ambient (@200 ft/min)	Four layer board (2s2p)	θ_{JMA}	23[1,2]	°C/W
Junction to board		θ_{JB}	15 [1]	°C/W
Junction to case		θ_{JC}	10 [2]	°C/W
Junction to top of package	Natural convection	Ψ_{jt}	2[1, 3]	°C/W

1 Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

2 Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

3 Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

A.3 DC Electrical Specifications

Table 22 lists DC electrical operating temperatures. This table is based on an operating voltage of EV_{DD} = 3.3 V_{DC} ± 0.3 V_{DC} and IV_{DD} of 1.5 ± 0.07 V_{DC}.

Table 22. DC Electrical Specifications

Characteristic	Symbol	Min	Max	Units
External (I/O pads) operation voltage range	EV_{DD}	3.0	3.6	V
Memory (I/O pads) operation voltage range (DDR Memory)	SD V_{DD}	2.30	2.70	V
Internal logic operation voltage range [1]	IV_{DD}	1.43	1.58	V
PLL Analog operation voltage range [1]	PLL V_{DD}	1.43	1.58	V
USB oscillator operation voltage range	USB_OSV_{DD}	3.0	3.6	V
USB digital logic operation voltage range	$USBV_{DD}$	3.0	3.6	V
USB PHY operation voltage range	USB_PHYV_{DD}	3.0	3.6	V
USB oscillator analog operation voltage range	USB_OSCAV_{DD}	1.43	1.58	V
USB PLL operation voltage range	USB_PLLV_{DD}	1.43	1.58	V
Input high voltage SSTL 3.3V (SDR DRAM)	V_{IH}	2.0	3.6	V
Input low voltage SSTL 3.3V (SDR DRAM)	V_{IL}	-0.5	0.8	V
Input high voltage SSTL 2.5V (DDR DRAM)	V_{IH}	2.0	2.8	V
Input low voltage SSTL 2.5V (DDR DRAM)	V_{IL}	-0.5	0.8	V
Output high voltage I_{OH} = 8 mA, 16 mA ,24 mA	V_{OH}	2.4	—	V

Table 22. DC Electrical Specifications

Characteristic	Symbol	Min	Max	Units
Output low voltage I_{OL} = 8 mA , 16 mA ,24 mA[5]	V_{OL}	—	0.5	V
Capacitance [2], V_{in} = 0 V, f = 1 MHz	C_{IN}	—	TBD	pF

1 IV_{DD} and PLL V_{DD} should be at the same voltage. PLL V_{DD} should have a filtered input. Please see Figure 22 for an example circuit. Note: There are three PLL V_{DD} inputs. A filter circuit should used on each PLL V_{DD} input.

2 Capacitance C_{IN} is periodically sampled rather than 100% tested.

A.3.1 PLL Power Filtering

To further enhance noise isolation, an external filter is strongly recommended for PLL analog V_{DD} pins. The filter shown in Figure 22 should be connected between the board V_{DD} and the PLL V_{DD} pins. The resistor and capacitors should be placed as close to the dedicated PLL V_{DD} pin as possible.

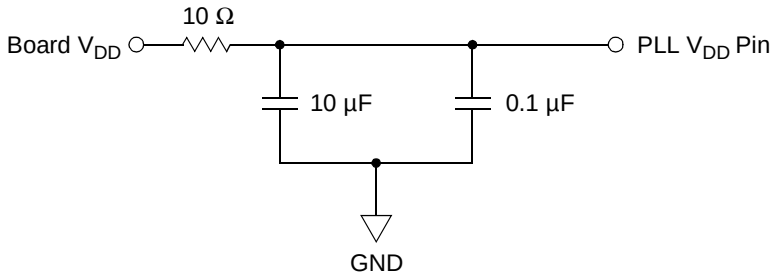


Figure 22. System PLL V_{DD} Power Filter

A.3.2 USB Power Filtering

To minimize noise, a external filters are required for each of the USB power pins. The filter shown in Figure 23 should be connected between the board EV_{DD} or $IV_{DD}$and each of the USB V_{DD} pins. The resistor and capacitors should be placed as close to the dedicated USB V_{DD} pin as possible. A separate filter circuit should be included for each USB V_{DD} pin, a total of five circuits.

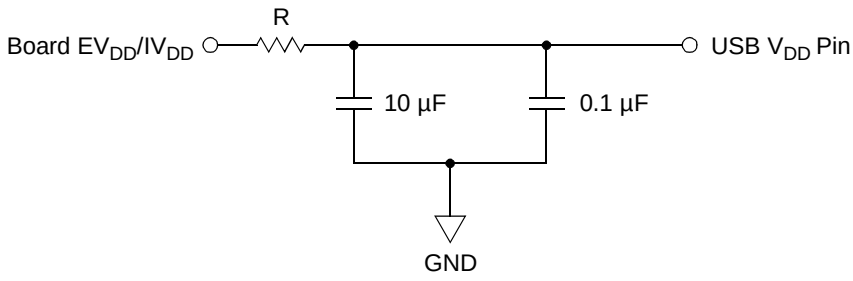


Figure 23. USB V_{DD} Power Filter

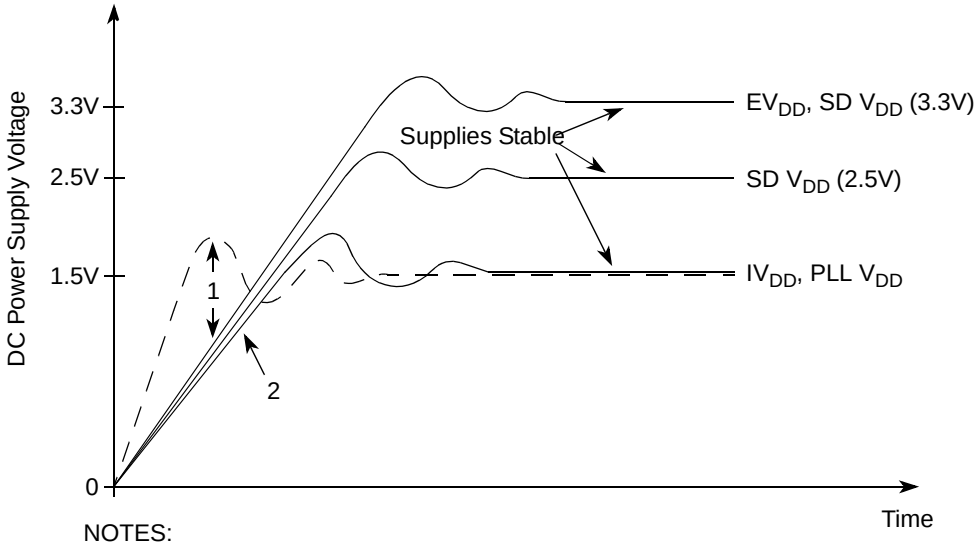
Lists the resistor values and supply voltages to be used in the circuit for each of the USB V_{DD} pins.

Table 23. USB Filter Circuit Values

USB V_{DD} Pin	Nominal Voltage	Resistor Value (R)
USB_OSCV_{DD}	3.3V	0Ω
$USBV_{DD}$	3.3V	0Ω
USB_PHYV_{DD}	3.3V	0Ω
USB_OSCAV_{DD}	1.5V	0Ω
USB_PHYV_{DD}	1.5V	10Ω

A.4 Supply Voltage Sequencing and Separation Cautions

Figure 24 shows situations in sequencing the I/O V_{DD} (EV_{DD}), SDRAM V_{DD} (SD V_{DD}), PLL V_{DD} (PLL V_{DD}), and Core V_{DD} (IV_{DD}).



NOTES:
1. IV_{DD} should not exceed EV_{DD}, SD V_{DD} or PLL V_{DD} by more than 0.4V at any time, including power-up.
2. Recommended that IV_{DD}/PLL V_{DD} should track EV_{DD}/SD V_{DD} up to 0.9V, then separate for completion of ramps.
3. Input voltage must not be greater than the supply voltage (EV_{DD}, SD V_{DD}, IV_{DD}, or PLL V_{DD}) by more than 0.5V at any time, including during power-up.
4. Use 1 microsecond or slower rise time for all supplies.

Figure 24. Supply Voltage Sequencing and Separation Cautions

The relationship between SD V_{DD} and EV_{DD} is non-critical during power-up and power-down sequences. Both SD V_{DD} (2.5V or 3.3V) and EV_{DD} are specified relative to IV_{DD}.

A.4.1 Power Up Sequence

If EV_{DD}/SD V_{DD} are powered up with the IV_{DD} at 0V, then the sense circuits in the I/O pads will cause all pad output drivers connected to the EV_{DD}/SD V_{DD} to be in a high impedance state. There is no limit on how long after EV_{DD}/SD V_{DD} powers up before IV_{DD} must power up. IV_{DD} should not lead the EV_{DD}, SD V_{DD} or PLL V_{DD} by more than 0.4V during power ramp up or there will be high current in the internal ESD protection diodes. The rise times on the power supplies should be slower than 1 microsecond to avoid turning on the internal ESD protection clamp diodes.

The recommended power up sequence is as follows:

1. Use 1 microsecond or slower rise time for all supplies.
2. IV_{DD}/PLL V_{DD} and EV_{DD}/SD V_{DD} should track up to 0.9V and then separate for the completion of ramps with EV_{DD}/SD V_{DD} going to the higher external voltages. One way to accomplish this is to use a low drop-out voltage regulator.

A.4.2 Power Down Sequence

If IV_{DD}PLL V_{DD} are powered down first, then sense circuits in the I/O pads will cause all output drivers to be in a high impedance state. There is no limit on how long after IV_{DD} and PLL V_{DD} power down before EV_{DD} or SD V_{DD} must power down. IV_{DD} should not lag EV_{DD}, SD V_{DD}, or PLL V_{DD} going low by more than 0.4V during power down or there will be undesired high current in the ESD protection diodes. There are no requirements for the fall times of the power supplies.

The recommended power down sequence is as follows:

1. Drop IV_{DD}/PLL V_{DD} to 0V.
2. Drop EV_{DD}/SD V_{DD} supplies.

A.5 Output Driver Capability and Loading

Table 24 lists values for drive capability and output loading.

Table 24. I/O Driver Capability

Signal	Drive Capability	Output Load (C_L)
SDRAMC (SDADDR[12:0], SDDATA[31:0], $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, SDDM[3:0], $\overline{\text{SDWE}}$, SDBA[1:0]	24 mA	15 pF
SDRAMC DQS and clocks (SDDQS[3:0], SDRDQS, SDCLK[1:0], $\overline{\text{SDCLK}}$[1:0], SDCKE)	24 mA	15 pF
SDRAMC chip selects ($\overline{\text{SDCS}}$[3:0])	24 mA	15 pF
FlexBus (AD[31:0], $\overline{\text{FBCS}}$[5:0], $\overline{\text{TS}}$, R/$\overline{\text{W}}$, $\overline{\text{BE}}$/$\overline{\text{BWE}}$[3:0], $\overline{\text{OE}}$)	16 mA	20 pF
FEC (E*n*MDIO, E*n*MDC, E*n*TXEN, E*n*TXD[3:0], E*n*TXER	8 mA	15 pF
Timer (TOUT[3:0])	8 mA	50 pF
FlexCAN (CANTX)	8 mA	30 pF
$\overline{\text{DACK}}$[1:0]	8 mA	30 pF
PSC (PSC*n*TXD[3:0], $\overline{\text{PSC}n\text{RTS}}$/PSC*n*FSYNC,	8 mA	30 pF
DSPI (DSPISOUT, DSPICS0/SS, DSPICS[2:3], DSPICS5/PCSS)	24 mA	50 pF

Table 24. I/O Driver Capability

Signal	Drive Capability	Output Load (C_L)
PCI (PCIAD[31:0], PCIBG[4:1], PCIBG0/PCIREQOUT, PCIDEVSEL, PCICXBE[3:0], PCIFRM, PCIPERR, PCIRESET, PCISERR, PCISTOP, PCIPAR, PCITRDY, PCIIRDY	16 mA	50 pF
I2C (SCL, SDA)	8 mA	50 pF
BDM (PSTCLK, PSTDDATA[7:0], DSO/TDO,	8 mA	25 pF
RSTO	8 mA	50 pF

A.6 PLL Timing Specifications

The specifications in Table 25 are for the CLKIN pin.

Table 25. Clock Timing Specification

Num	Characteristic	Min	Max	Units
C1	Cycle time	15.15	33.3	ns
C2	Rise time (20% of Vdd to 80% of vdd)	—	2	ns
C3	Fall time (80% of Vdd to 20% of Vdd)	—	2	ns
C4	Duty cycle (at 50% of Vdd)	40	60	%

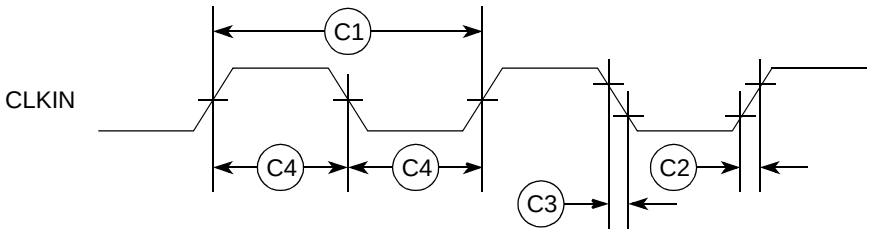


Figure 25. Input Clock Timing Diagram

Table 6 shows the supported PLL encodings.

Table 26. MCF548X Divide Ratio Encodings

AD[12:8] [1]	Clock Ratio	CLKIN—PCI and FlexBus Frequency Range (MHz)	Internal XLB and SDRAM Bus Frequency Range (MHz)	Core Frequency Range (MHz)
00011	1:2	41.6–50.0	83.33–100	166.66–200
00101	1:2	30.0–41.5	60.0–83.0	120.0–166.66

1 All other values of AD[12:8] are reserved.

Figure 26 correlates CLKIN, internal bus, and core clock frequencies for the 1x–2x multipliers.

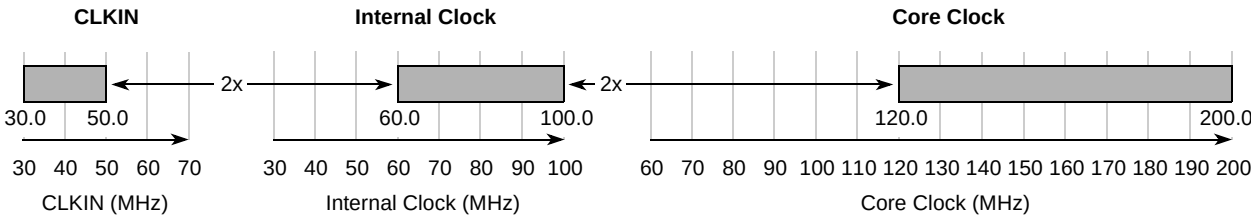


Figure 26. CLKIN, Internal Bus, and Core Clock Ratios

A.7 Reset Timing Specifications

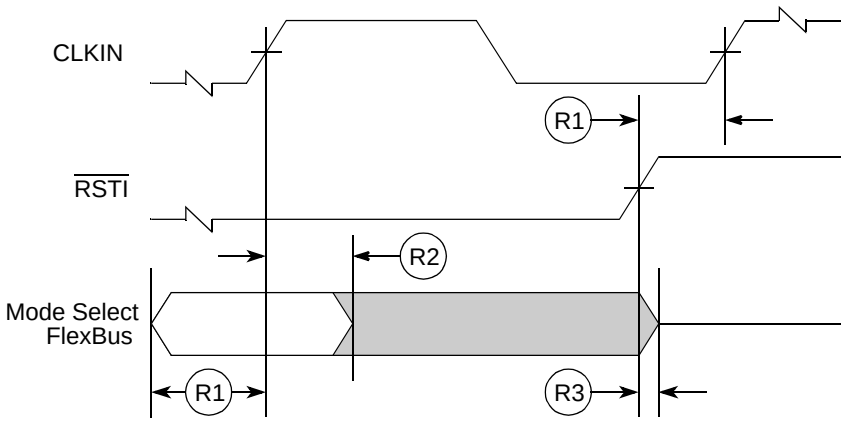
Table 27 lists specifications for the reset timing parameters shown in Figure 27

Table 27. Reset Timing Specification

Num	Characteristic	66 MHz CLKIN		Units
		Min	Max	
R1 [1]	Valid to CLKIN (setup)	8	—	nS
R2	CLKIN to invalid (hold)	1.0	—	nS
R3	$\overline{\text{RSTI}}$ to invalid (hold)	1.0	—	nS

[1] $\overline{\text{RESET}}$ and FlexBus data lines are synchronized internally. Setup and hold times must be met only if recognition on a particular clock is required.

Figure 27 shows reset timing for the values in Table 27.



NOTE:
Mode selects are registered on the rising clock edge before the cycle in which $\overline{\text{RSTI}}$ is recognized as being negated.

Figure 27. Reset Timing

A.8 FlexBus

A multi-function external bus interface called FlexBus is provided on MCF5482 with basic functionality to interface to slave-only devices up to a maximum bus frequency of 66 MHz. It can be directly connected to asynchronous or synchronous devices such as external boot ROMs, flash memories, gate-array logic, or other simple target (slave) devices with little or no additional circuitry. For asynchronous devices a simple chip-select based interface can be used. The FlexBus interface has six general purpose chip-selects ($\overline{\text{FBCS}}$[5:0]). Chip-select $\overline{\text{FBCS0}}$ can be dedicated to boot ROM access and can be programmed to be byte (8 bits), word (16 bits), or longword (32 bits) wide. Control signal timing is compatible with common ROM / flash memories.

A.8.1 FlexBus AC Timing Characteristics

The following timing numbers indicate when data will be latched or driven onto the external bus, relative to the system clock.

Table 28. FlexBus AC Timing Specifications

Num	Characteristic	Min	Max	Unit	Notes
	Frequency of Operation	30	66	Mhz	1
FB1	Clock Period (CLKIN)	15.15	33.33	ns	2
FB2	Address, Data, and Control Output Valid (AD[31:0], $\overline{\text{FBCS}}$[5:0], R/$\overline{\text{W}}$, $\overline{\text{TS}}$, TSIZ[1:0], $\overline{\text{BE}}$/$\overline{\text{BWE}}$[3:0], $\overline{\text{OE}}$, and $\overline{\text{TBST}}$)	—	7.0	ns	3
FB3	Address, Data, and Control Output Hold ((AD[31:0], $\overline{\text{FBCS}}$[5:0], R/$\overline{\text{W}}$, $\overline{\text{TS}}$, TSIZ[1:0], $\overline{\text{BE}}$/$\overline{\text{BWE}}$[3:0], $\overline{\text{OE}}$, and $\overline{\text{TBST}}$)	1	—	ns	3, 4
FB4	Data Input Setup	3.5	—	ns	
FB5	Data Input Hold	0	—	ns	
FB6	Transfer Acknowledge ($\overline{\text{TA}}$) Input Setup	4	—	ns	
FB7	Transfer Acknowledge ($\overline{\text{TA}}$) Input Hold	0	—	ns	
FB8	Address Output Valid (PCIAD[31:0])	—	6.0	ns	5
FB9	Address Output Hold (PCIAD[31:0])	0	—	ns	5

1 The frequency of operation is the same as the PCI frequency of operation. The MCF548X supports a single external reference clock (CLKIN). This signal defines the frequency of operation for both FlexBus and PCI.
2 Max cycle rate is determined by CLKIN and how the user has the system PLL configured.
3 Timing for chip selects only applies to the FBCS[5:0] signals. Please see Section A.9.2, “DDR SDRAM AC Timing Characteristics” for SDCS[3:0] timing.
4 The FlexBus supports programming an extension of the address hold. Please consult the MCF548X specification manual for more information.
5 These specs are used when the PCIAD[31:0] signals are configured as 32-bit, non-muxed FlexBus address signals.

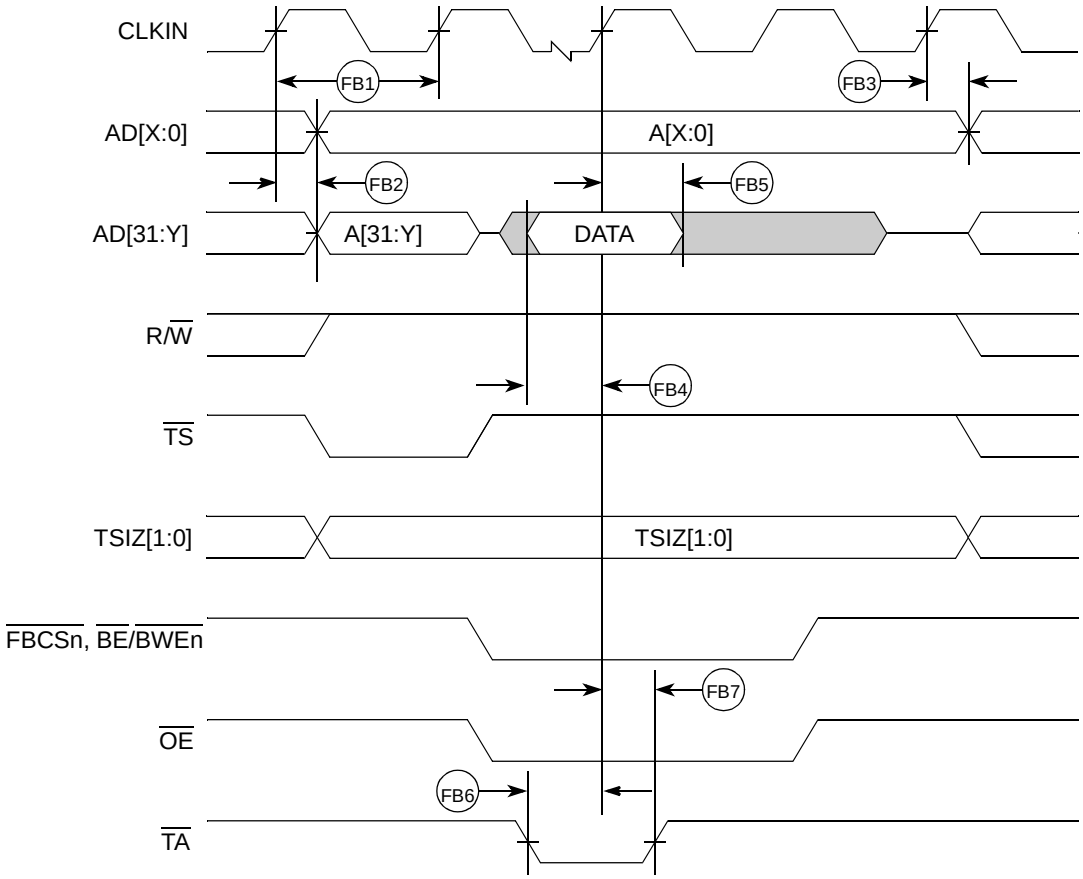


Figure 28. FlexBus Read Timing

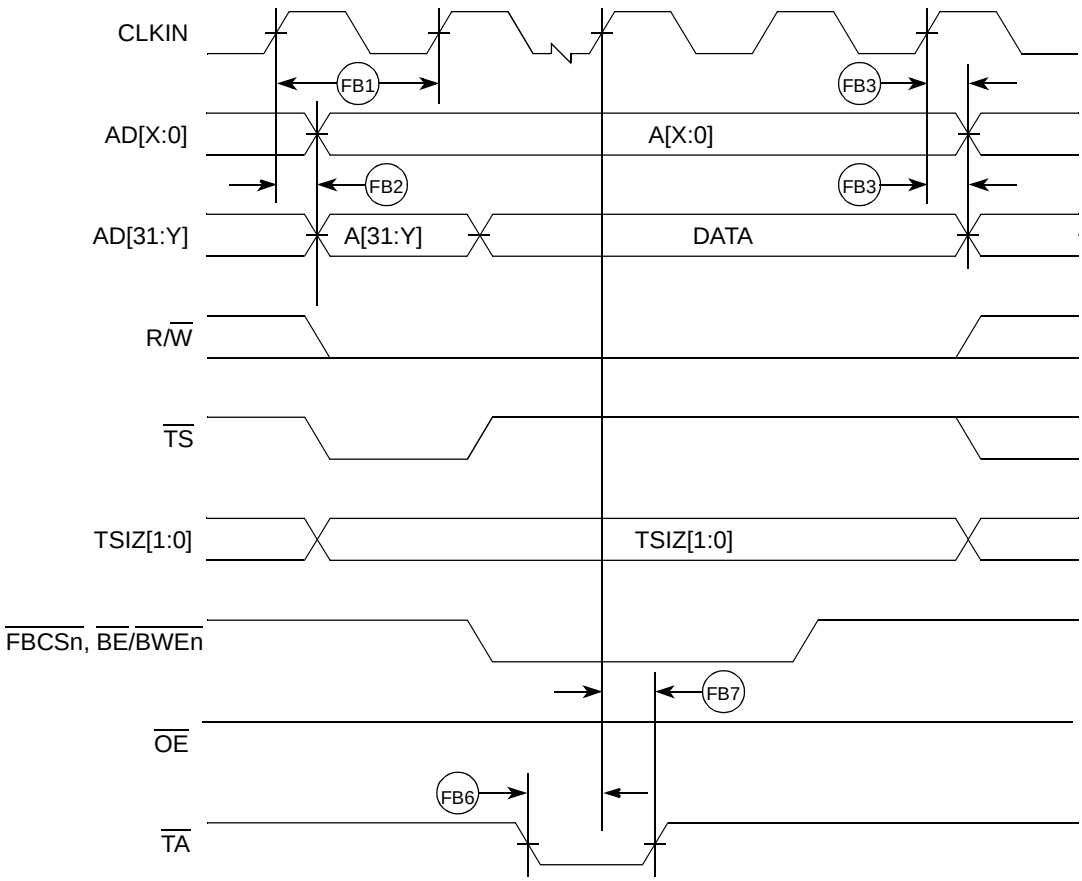


Figure 29. FlexBus Write Timing

A.9 SDRAM Bus

The SDRAM controller supports accesses to main SDRAM memory from any internal master. It supports either standard SDRAM or double data rate (DDR) SDRAM, but it does not support both at the same time. The SDRAM controller uses SSTL2 and SSTL3 I/O drivers. Both SSTL drive modes are programmable for either Class I or Class II drive strength.

A.9.1 SDR SDRAM AC Timing Characteristics

The following timing numbers indicate when data will be latched or driven onto the external bus, relative to the memory bus clock, when operating in SDR mode on write cycles and relative to SDR_DQS on read cycles. The MCF548X SDRAM controller is a DDR controller that has an SDR mode. Because it is designed to support DDR, a DQS pulse must still be supplied to MCF548X for each data beat of an SDR read. MCF548X accomplishes this by asserting a signal called SDR_DQS during read cycles. Care must be taken during board design to adhere to the following guidelines and specs with regard to the SDR_DQS signal and its usage.

Table 29. SDR Timing Specifications

Symbol	Characteristic	Min	Max	Unit	Notes
	Frequency of Operation	83	133	Mhz	1
SD1	Clock Period (t_{CK})	7.52	12	ns	2
SD2	Clock Skew (t_{SK})		TBD		
SD3	Pulse Width High (t_{CKH})	0.45	0.55	SDCLK	3
SD4	Pulse Width Low (t_{CKL})	0.45	0.55	SDCLK	4
SD5	Address, CKE, CAS, RAS, WE, BA, CS - Output Valid (t_{CMV})		0.5*SDCLK + 1.0ns	ns	
SD6	Address, CKE, CAS, RAS, WE, BA, CS - Output Hold (t_{CMH})	2.0		ns	
SD7	SDRDQS Output Valid (t_{DQSOV})		Self timed	ns	5
SD8	SDDQS[3:0] input setup relative to SDCLK (t_{DQSIS})	0.25*SDCLK	0.40*SDCLK	ns	6
SD9	SDDQS[3:0] input hold relative to SDCLK (t_{DQSIH})	Does not apply. 0.5 SDCLK fixed width.			7
SD10	Data Input Setup relative to SDCLK (reference only) (t_{DIS})	0.25*SDCLK		ns	8
SD11	Data Input Hold relative to SDCLK (reference only) (t_{DIH})	1.0		ns	
SD12	Data and Data Mask Output Valid (t_{DV})		0.75*SDCLK +0.500ns	ns	
SD13	Data and Data Mask Output Hold (t_{DH})	1.5		ns	

1 The frequency of operation is either 2x or 4x the CLKIN frequency of operation. MCF548X supports a single external reference clock (CLKIN). This signal defines the frequency of operation for both FlexBus and PCI, but SDRAM clock operates at the same frequency as the internal bus clock. Please see the PLL chapter of the MCF548X Specification for more information on setting the SDRAM clock rate.

2 SDCLK is one SDRAM clock in (ns).

3 Pulse width high plus pulse width low cannot exceed min and max clock period.

4 Pulse width high plus pulse width low cannot exceed min and max clock period.

5 SDR_DQS is designed to pulse 0.25 clock before the rising edge of the memory clock. This is a guideline only. Subtle variation from this guideline is expected. SDR_DQS will only pulse during a read cycle and one pulse will occur for each data beat.

6 SDR_DQS is designed to pulse 0.25 clock before the rising edge of the memory clock. This spec is a guideline only. Subtle variation from this guideline is expected. SDR_DQS will only pulse during a read cycle and one pulse will occur for each data beat.

7 The SDR_DQS pulse is designed to be 0.5 clock in width. The timing of the rising edge is most important. The falling edge does not affect the memory controller.

8 Since a read cycle in SDR mode still uses the DQS circuit within MCF548X, it is most critical that the data valid window be centered 1/4 clk after the rising edge of DQS. Ensuring that this happens will result in successful SDR reads. The input setup spec is just provided as guidance.

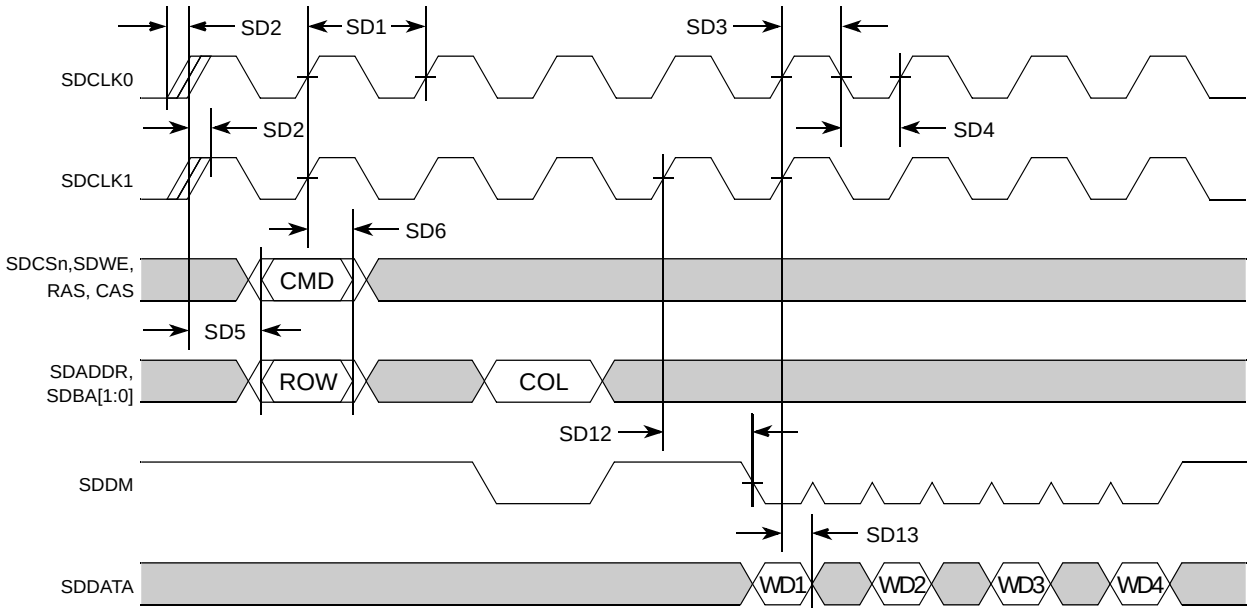


Figure 30. SDR Write Timing

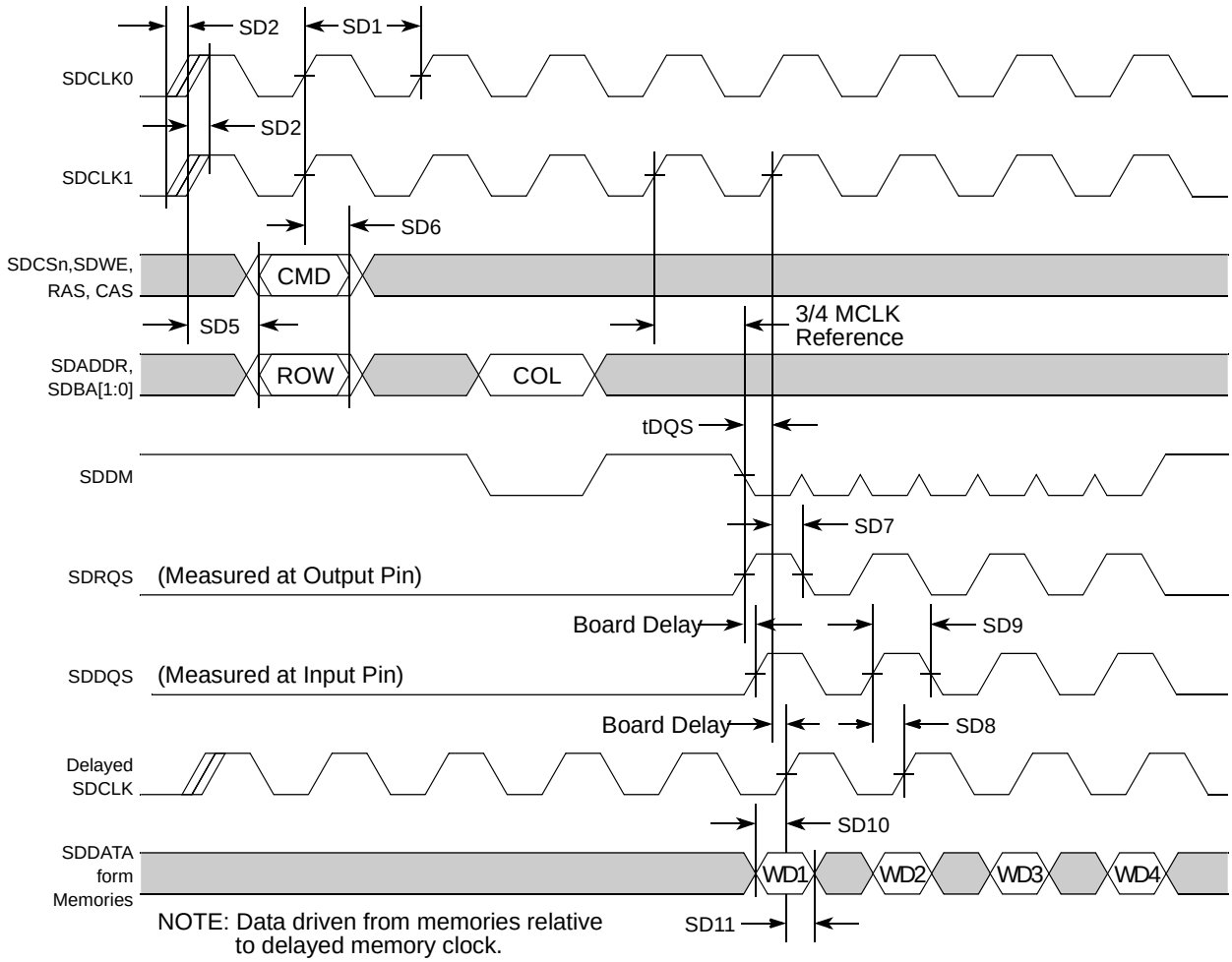


Figure 31. SDR Read Timing

A.9.2 DDR SDRAM AC Timing Characteristics

When using the DDR SDRAM controller the following timing numbers must be followed to properly latch or drive data onto the memory bus. All timing numbers are relative to the four DQS byte lanes.

Table 30. DDR Clock Timing Specifications

Symbol	Characteristic	Min	Max	Unit
V_{MP}	Clock output mid-point voltage	1.05	1.45	V
V_{OUT}	Clock output voltage level	-0.3	SD_VDD + 0.3	V
V_{ID}	Clock output differential voltage (peak to peak swing)	0.7	SD_VDD + 0.6	V
V_{IX}	Clock crossing point voltage	1.05	1.45	V

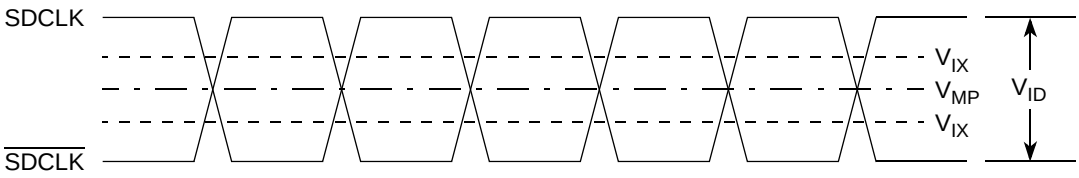


Figure 32. DDR Clock Timing Diagram

Table 31. DDR Timing Specifications

Symbol	Characteristic	Min	Max	Unit	Notes
	Frequency of Operation	83	133	MHz	1
DD1	Clock Period (t_{CK})	7.52	12	ns	2
DD2	Pulse Width High (t_{CKH})	0.45	0.55	SDCLK	3
DD3	Pulse Width Low (t_{CKL})	0.45	0.55	SDCLK	4
DD4	Address, SDCKE, $\overline{CAS}$, $\overline{RAS}$, $\overline{WE}$, SDBA, $\overline{SDCS}$ - Output Valid (t_{CMV})	—	0.5*SDCLK+ 1.0 ns	ns	
DD5	Address, SDCKE, $\overline{CAS}$, $\overline{RAS}$, $\overline{WE}$, SDBA, $\overline{SDCS}$ - Output Hold (t_{CMH})	2.0	—	ns	
DD6	Write Command to first DQS Latching Transition (t_{DQSS})	—	1.25	SDCLK	
DD7	Data and Data Mask Output Setup (DQ-->DQS) Relative to DQS (DDR Write Mode) (t_{QS})	1.5	—	ns	5 6
DD8	Data and Data Mask Output Hold (DQS-->DQ) Relative to DQS (DDR Write Mode) (t_{QH})	1.0	—	ns	7
DD9	Input Data Skew Relative to DQS (Input Setup) (t_{IS})		1	ns	8
DD10	Input Data Hold Relative to DQS (t_{IH})	0.25*SDCLK +0.5ns	—	ns	9
DD11	DQS falling edge to SDCLK rising (output setup time) (t_{DSS})	0.5	—	ns	
DD12	DQS falling edge from SDCLK rising (output hold time) (t_{DSH})	0.5	—	ns	
DD13	DQS input read preamble width (t_{RPRE})	0.9	1.1	SDCLK	
DD14	DQS input read postamble width (t_{RPST})	0.4	0.6	SDCLK	
DD15	DQS output write preamble width (t_{WPRE})	0.25	—	SDCLK	
DD16	DQS output write postamble width (t_{WPST})	0.4	0.6	SDCLK	

1 The frequency of operation is either 2x or 4x the CLKIN frequency of operation. The MCF548X supports a single external reference clock (CLKIN). This signal defines the frequency of operation for both FlexBus and PCI, but SDRAM clock operates at the same frequency as the internal bus clock. Please see the PLL chapter for more information on setting the SDRAM clock rate.

2 SDCLK is one memory clock in (ns).

3 Pulse width high plus pulse width low cannot exceed max clock period.

4 Pulse width high plus pulse width low cannot exceed max clock period.

5 This specification relates to the required input setup time of today's DDR memories. SDDATA[31:24] is relative to SDDQS3, SDDATA[23:16] is relative to SDDQS2, SDDATA[15:8] is relative to SDDQS1, and SDDATA[7:0] is relative SDDQS0.

6 The first data beat will be valid before the first rising edge of SDDQS and after the SDDQS write preamble. The remaining data beats will be valid for each subsequent SDDQS edge.

7 This specification relates to the required hold time of today's DDR memories. SDDATA[31:24] is relative to SDDQS3, SDDATA[23:16] is relative to SDDQS2, SDDATA[15:8] is relative to SDDQS1, and SDDATA[7:0] is relative SDDQS0.

8 Data input skew is derived from each SDDQS clock edge. It begins with a SDDQS transition and ends when the last data line becomes valid. This input skew must include DDR memory output skew and system level board skew (due to routing or other factors).

9 Data input hold is derived from each SDDQS clock edge. It begins with a SDDQS transition and ends when the first data line becomes invalid.

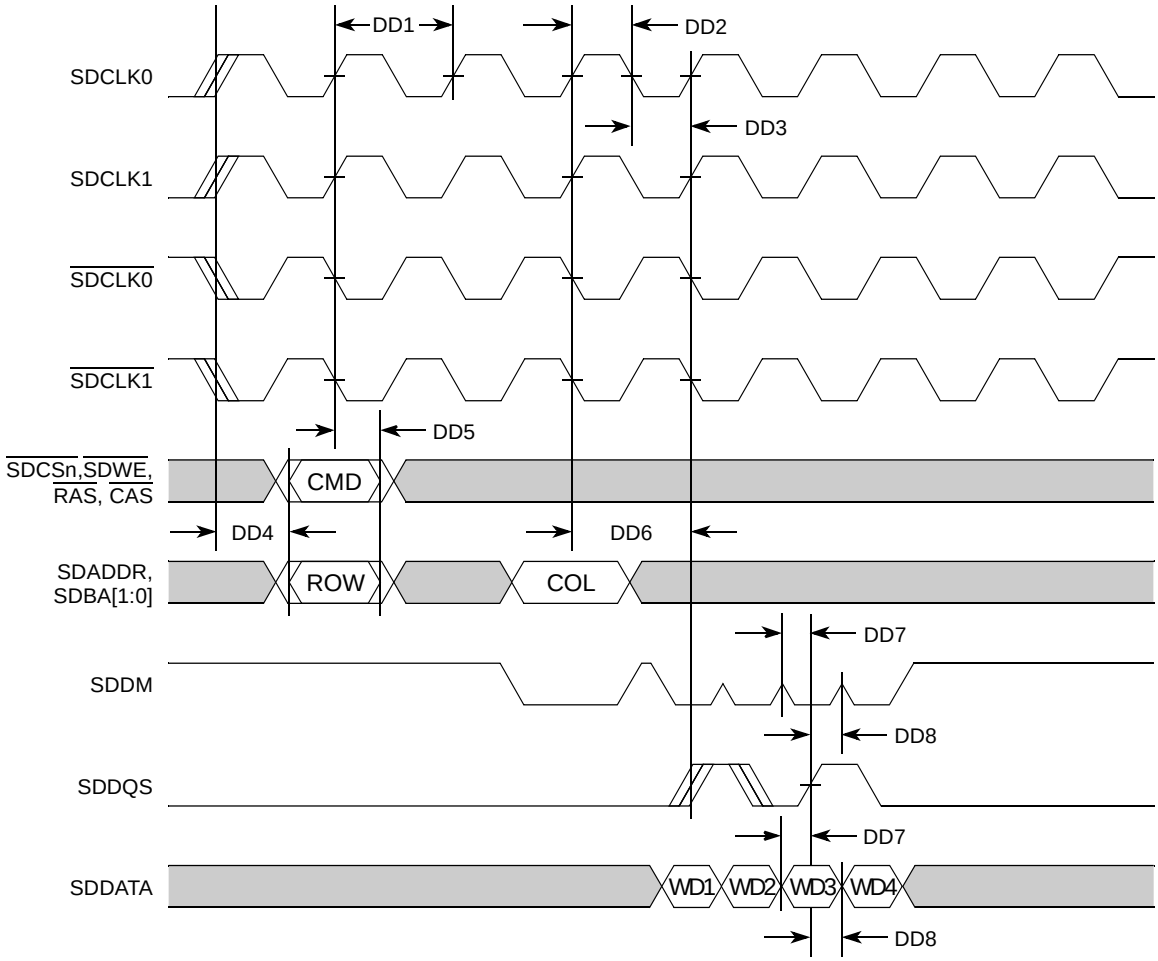


Figure 33. DDR Write Timing

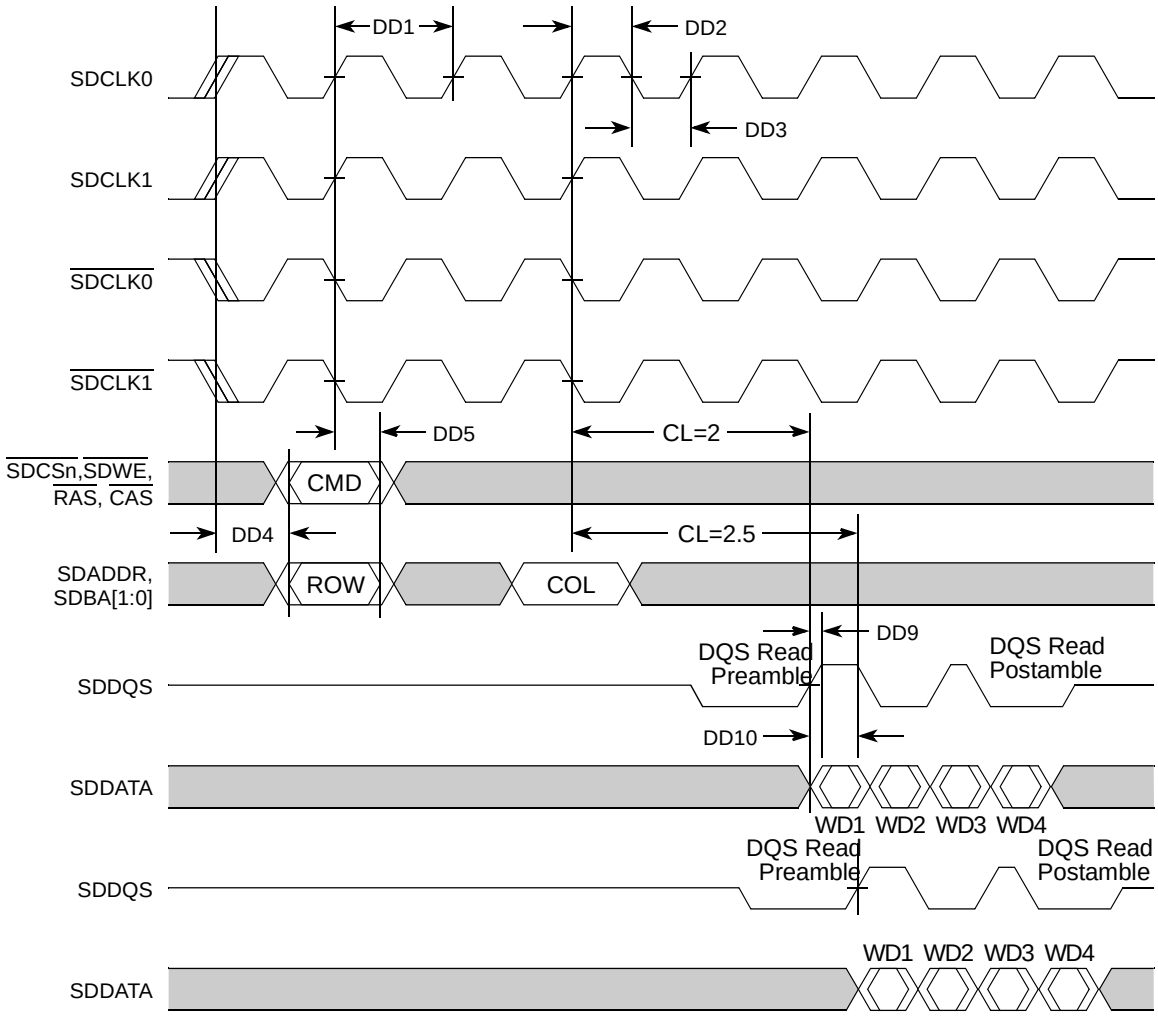


Figure 34. DDR Read Timing

A.10 PCI Bus

The PCI bus on the MCF548X is PCI 2.2 compliant. The following timing numbers are mostly from the PCI 2.2 spec. Please refer to the PCI 2.2 spec for a more detailed timing analysis.

Table 32. PCI Timing Specifications

Num	Characteristic	Min	Max	Unit	Notes
	Frequency of Operation	30	66	Mhz	1
P1	Clock Period (t_{CK})	15.15	33.33	ns	2
P2	Address, Data, and Command (33< PCI <= 66 Mhz) - Input Setup (t_{IS})	3.0	—	ns	
P2	Address, Data, and Command (0 < PCI <= 33 Mhz) - Input Setup (t_{IS})	7.0	—	ns	
P3	Address, Data, and Command (33-66 Mhz) - Output Valid (t_{DV})	—	6.0	ns	3

Num	Characteristic	Min	Max	Unit	Notes
P3	Address, Data, and Command (0 -33 Mhz) - Output Valid (t_{DV})	—	11.0	ns	
P4	PCI signals (0 - 66 Mhz) - Output Hold (t_{DH})	0	—	ns	4
P5	PCI signals (0 - 66 Mhz) - Input Hold (t_{IH})	0	—	ns	5
P6	PCI REQ/GNT (33 < PCI <= 66Mhz) - Output valid (t_{DV})	—	6	ns	6
P7	PCI REQ/GNT (0 < PCI <= 33Mhz) - Output valid (t_{DV})	—	12	ns	
P8	PCI REQ/GNT (33 < PCI <= 66Mhz) - Input Setup (t_{IS})	—	5	ns	
P9	PCI REQ (0 < PCI <= 33Mhz) - Input Setup (t_{IS})	12	—	ns	
P10	PCI GNT (0 < PCI <= 33Mhz) - Input Setup (t_{IS})	10	—	ns	

1 Please see the PLL chapter for more information on setting the PCI clock rate. Also specific guidelines may need to be followed when operating the system PLL below certain frequencies.
2 Max cycle rate is determined by CLKIN and how the user has the system PLL configured.
3 All signals defined as PCI bused signals. Does not include PTP (point-to-point) signals.
4 PCI 2.2 spec does not require an output hold time. Although the MCF548X may provide a slight amount of hold, it is not required or guaranteed.
5 PCI 2.2 spec requires zero input hold.
6 These signals are defined at PTP (Point-to-point) in the PCI 2.2 spec.

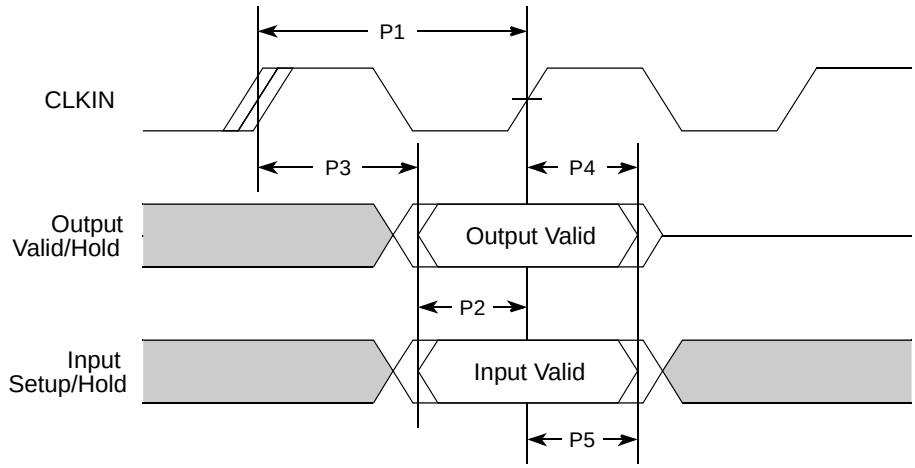


Figure 35. PCI Timing

A.11 Fast Ethernet AC Timing Specifications

A.11.1 MII/7-WIRE Interface Timing Specs

The following timing specs meet the requirements for both MII and 7-Wire style interfaces for a range of transceiver devices. If this interface is to be used with a specific transceiver device the timing specs may be altered to match that specific transceiver.

Table 33. MII Receive Signal Timing

NUM	Characteristic	MIN	MAX	UNIT
M1	RXD[3:0], RXDV, RXER to RXCLK setup	5	—	ns
M2	RXCLK to RXD[3:0], RXDV, RXER hold	5	—	ns
M3	RXCLK pulse width high	35%	65%	RXCLK period
M4	RXCLK pulse width low	35%	65%	RXCLK period

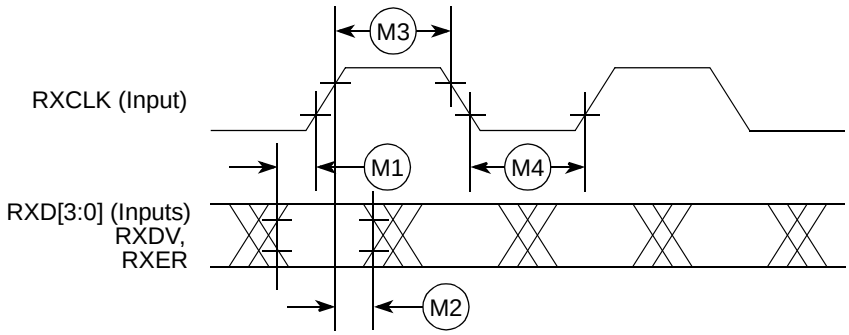


Figure 36. MII Receive Signal Timing Diagram

A.11.2 MII Transmit Signal Timing

Table 34. MII Transmit Signal Timing

NUM	Characteristic	MIN	MAX	UNIT
M5	TXCLK to TXD[3:0], TXEN, TXER invalid	0	—	ns
M6	TXCLK to TXD[3:0], TXEN, TXER valid	—	25	ns
M7	TXCLK pulse width high	35%	65%	TXCLK period
M8	TXCLK pulse width low	35%	65%	TXCLK period

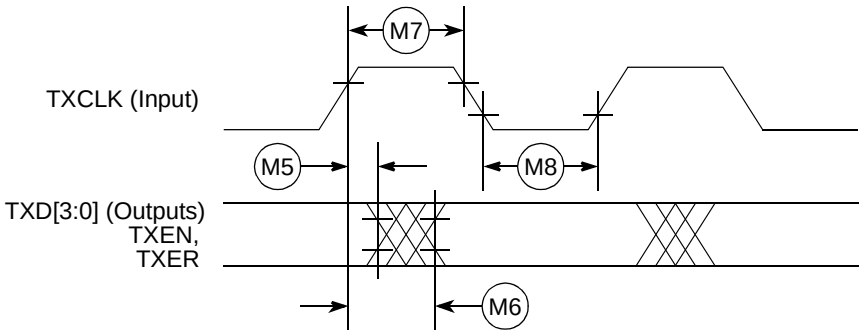


Figure 37. MII Transmit Signal Timing Diagram

A.11.3 MII Async Inputs Signal Timing (CRS, COL)

Table 35. MII Transmit Signal Timing

NUM	Characteristic	MIN	MAX	UNIT
M9	CRS, COL minimum pulse width	1.5	—	TX_CLK period

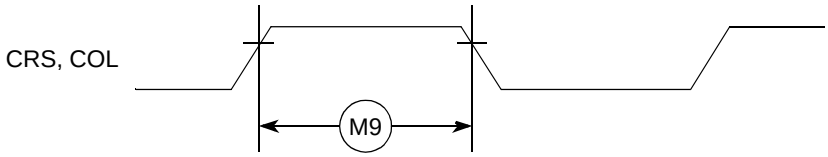


Figure 38. MII Async Inputs Timing Diagram

A.11.4 MII Serial Management Channel Timing (MDIO,MDC)

Table 36. MII Serial Management Channel Signal Timing

NUM	Characteristic	MIN (nS)	MAX (nS)	UNIT
M10	MDC falling edge to MDIO output invalid (min prop delay)	0	—	ns
M11	MDC falling edge to MDIO output valid (max prop delay)	—	25	ns
M12	MDIO (input) to MDC rising edge setup	10	—	ns
M13	MDIO (input) to MDC rising edge hold	0	—	ns
M14	MDC pulse width high	40%	60%	MDC period
M15	MDC pulse width low	40%	60%	MDC period

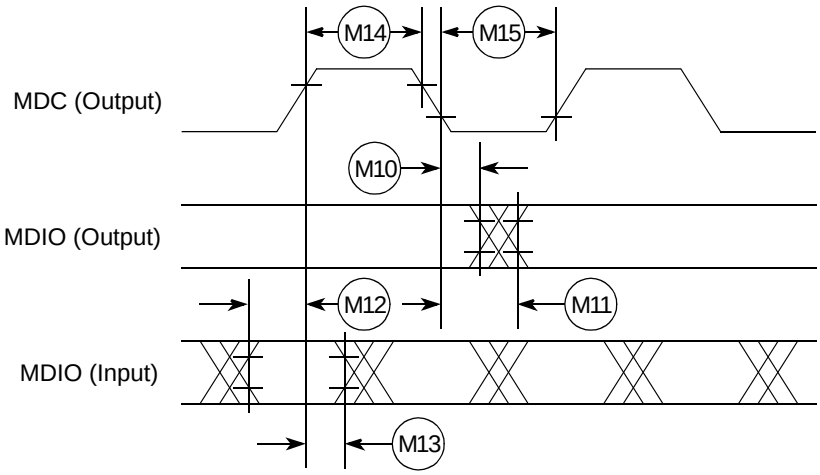


Figure 39. MII Serial Management Channel TIming Diagram

A.12 General Timing Specifications

Table 37 lists timing specifications for the GPIO, PSC, FlexCAN, $\overline{\text{DREQ}}$, $\overline{\text{DACK}}$, and external interrupts.

Table 37. General AC Timing Specifications

Name	Characteristic	Min	Max	Unit
G1	CLKIN high to signal output valid	—	2	PSTCLK
G2	CLKIN high to signal invalid (output hold)	0	—	ns
G3	Signal input pulse width	2	—	PSTCLK

A.13 I^2C Input/Output Timing Specifications

Table 38 lists specifications for the I^2C input timing parameters shown in Figure 40.

Table 38. I^2C Input Timing Specifications between SCL and SDA

Num	Characteristic	Min	Max	Units
I1	Start condition hold time	2	—	Bus clocks
I2	Clock low period	8	—	Bus clocks
I3	SCL/SDA rise time (V_{IL} = 0.5 V to V_{IH} = 2.4 V)	—	1	mS
I4	Data hold time	0	—	ns
I5	SCL/SDA fall time (V_{IH} = 2.4 V to V_{IL} = 0.5 V)	—	1	mS
I6	Clock high time	4	—	Bus clocks
I7	Data setup time	0	—	ns
I8	Start condition setup time (for repeated start condition only)	2	—	Bus clocks
I9	Stop condition setup time	2	—	Bus clocks

Table 39 lists specifications for the I^2C output timing parameters shown in Figure 40.

Table 39. I^2C Output Timing Specifications between SCL and SDA

Num	Characteristic	Min	Max	Units
I1 [1]	Start condition hold time	6	—	Bus clocks
I2 [1]	Clock low period	10	—	Bus clocks
I3 [2]	SCL/SDA rise time (V_{IL} = 0.5 V to V_{IH} = 2.4 V)	—	—	µS
I4 [1]	Data hold time	7	—	Bus clocks
I5 [3]	SCL/SDA fall time (V_{IH} = 2.4 V to V_{IL} = 0.5 V)	—	3	ns
I6 [1]	Clock high time	10	—	Bus clocks
I7 [1]	Data setup time	2	—	Bus clocks
I8 [1]	Start condition setup time (for repeated start condition only)	20	—	Bus clocks
I9 [1]	Stop condition setup time	10	—	Bus clocks

1 Note: Output numbers depend on the value programmed into the IFDR; an IFDR programmed with the maximum frequency (IFDR = 0x20) results in minimum output timings as shown in Table 39. The I^2C interface is designed to scale the actual data transition time to move it to the middle of the SCL low period. The actual position is affected by the prescale and division values programmed into the IFDR; however, the numbers given in Table 39 are minimum values.

2 Because SCL and SDA are open-collector-type outputs, which the processor can only actively drive low, the time SCL or SDA take to reach a high level depends on external signal capacitance and pull-up resistor values.

3 Specified at a nominal 50-pF load.

Figure 40 shows timing for the values in Table 38 and Table 39.

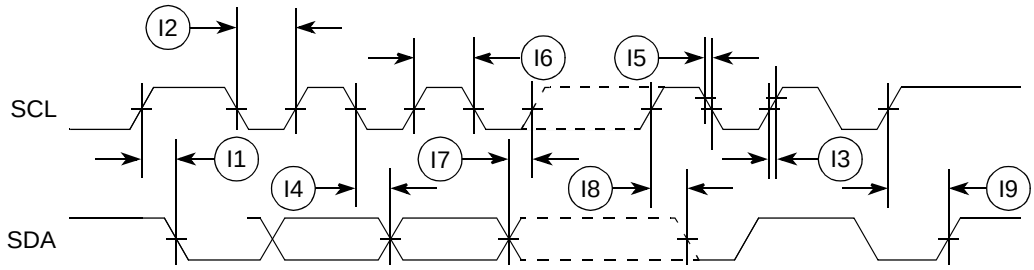


Figure 40. I^2C Input/Output Timings

A.14 JTAG and Boundary Scan Timing

Table 40. JTAG and Boundary Scan Timing

Num	Characteristics [1]	Symbol	Min	Max	Unit
J1	TCLK Frequency of Operation	f_{JCYC}	DC	10	MHz
J2	TCLK Cycle Period	t_{JCYC}	2	—	t_{CK}
J3	TCLK Clock Pulse Width	t_{JCW}	15.15	—	ns
J4	TCLK Rise and Fall Times	t_{JCRF}	0.0	3.0	ns

Table 40. JTAG and Boundary Scan Timing (continued)

Num	Characteristics [1]	Symbol	Min	Max	Unit
J5	Boundary Scan Input Data Setup Time to TCLK Rise	t_{BSDST}	5.0	—	ns
J6	Boundary Scan Input Data Hold Time after TCLK Rise	t_{BSDHT}	24.0	—	ns
J7	TCLK Low to Boundary Scan Output Data Valid	t_{BSDV}	0.0	15.0	ns
J8	TCLK Low to Boundary Scan Output High Z	t_{BSDZ}	0.0	15.0	ns
J9	TMS, TDI Input Data Setup Time to TCLK Rise	t_{TAPBST}	5.0	—	ns
J10	TMS, TDI Input Data Hold Time after TCLK Rise	t_{TAPBHT}	10.0	—	ns
J11	TCLK Low to TDO Data Valid	t_{TDODV}	0.0	15.0	ns
J12	TCLK Low to TDO High Z	t_{TDODZ}	0.0	15.0	ns
J13	$\overline{\text{TRST}}$ Assert Time	t_{TRSTAT}	100.0	—	ns
J14	$\overline{\text{TRST}}$ Setup Time (Negation) to TCLK High	t_{TRSTST}	10.0	—	ns

1 MTMOD is expected to be a static signal. Hence, it is not associated with any timing

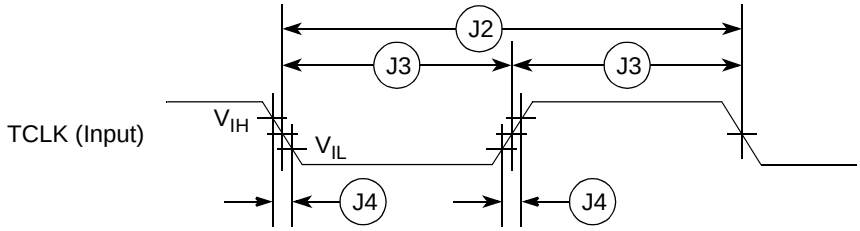


Figure 41. Test Clock Input Timing

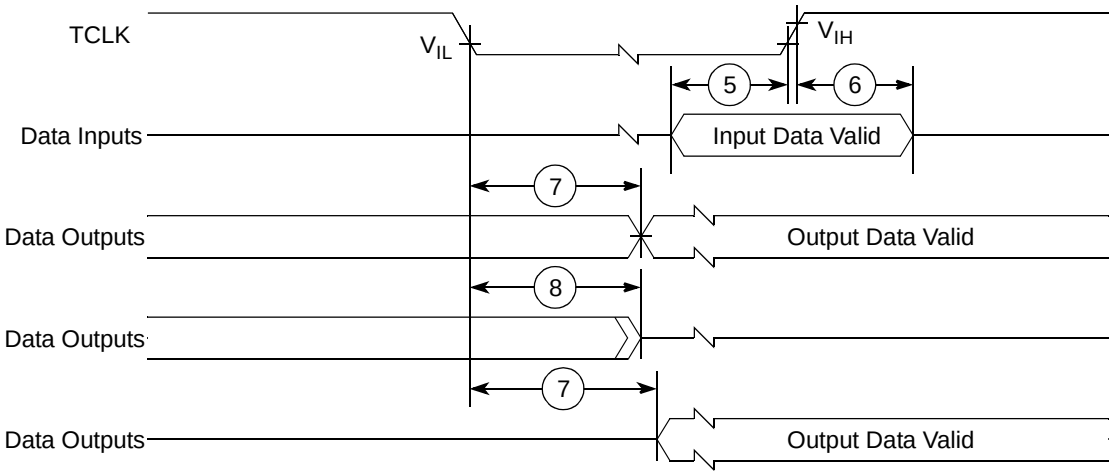


Figure 42. Boundary Scan (JTAG) Timing

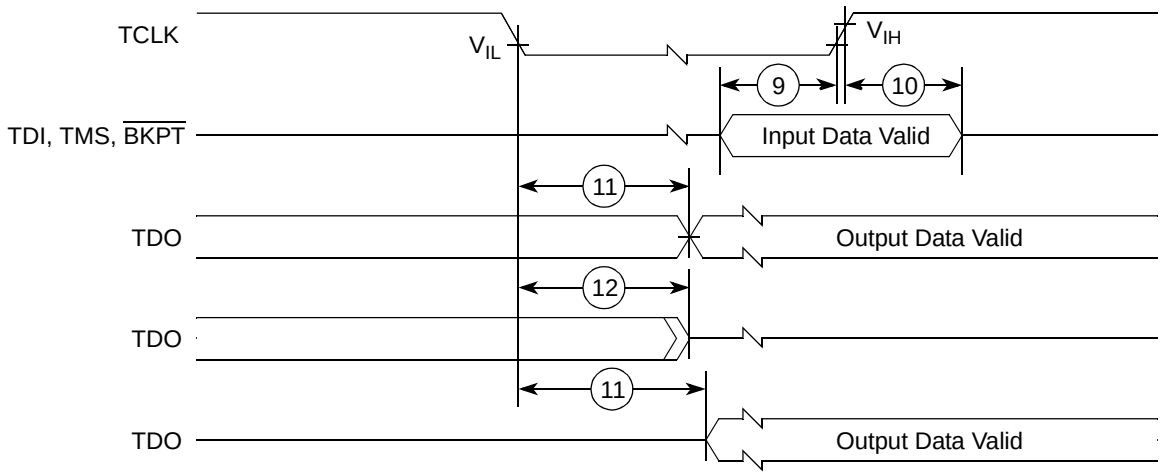


Figure 43. Test Access Port Timing

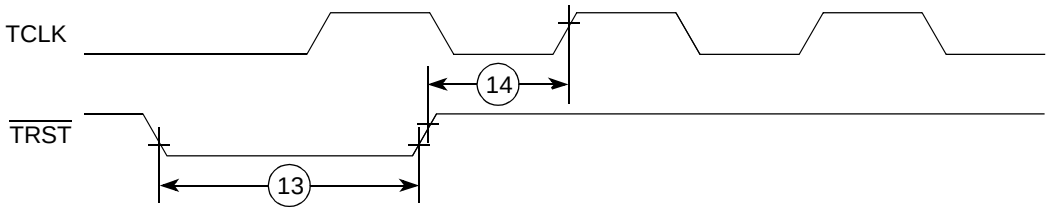


Figure 44. TRST TimingDebug AC Timing Specifications

Table 41 lists specifications for the debug AC timing parameters shown in Figure 46.

Table 41. Debug AC Timing Specification

Num	Characteristic	66 MHz		Units
		Min	Max	
D1	PSTDDATA to PSTCLK setup	4.5		ns
D2	PSTCLK to PSTDDATA hold	4.5		ns
D3	DSI-to-DSCLK setup	1		PSTCLKs
D4 [1]	DSCLK-to-DSO hold	4		PSTCLKs
D5	DSCLK cycle time	5		PSTCLKs

[1] DSCLK and DSI are synchronized internally. D4 is measured from the synchronized DSCLK input relative to the rising edge of CLKOUT.

Figure 45 shows real-time trace timing for the values in Table 41.

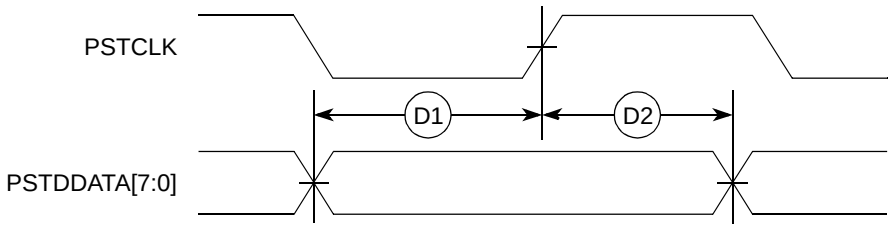


Figure 45. Real-Time Trace AC Timing

Figure 46 shows BDM serial port AC timing for the values in Table 41.

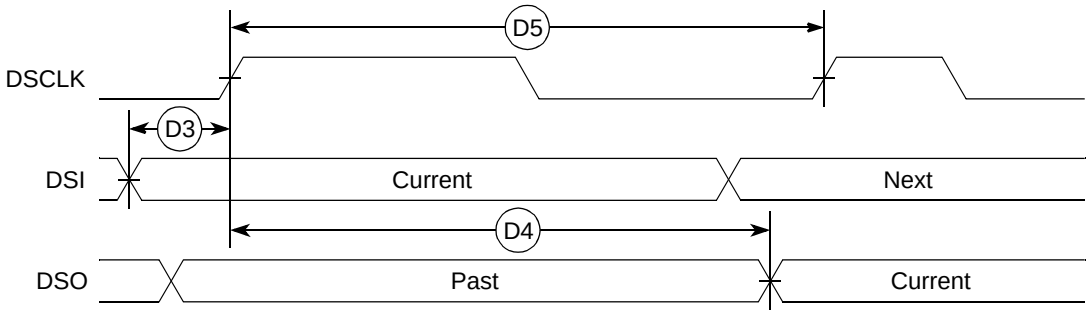


Figure 46. BDM Serial Port AC Timing

A.15 DSPI Electrical Specifications

Table 42 lists DSPI timings.

Table 42. DSPI Modules AC Timing Specifications

Name	Characteristic	Min	Max	Unit
DS1	DSPI_CS[3:0] to DSPI_CLK	1 × tck	510 × tck	ns
DS2	DSPI_CLK high to DSPI_DOUT valid.	—	12	ns
DS3	DSPI_CLK high to DSPI_DOUT invalid. (Output hold)	2	—	ns
DS4	DSPI_DIN to DSPI_CLK (Input setup)	10	—	ns
DS5	DSPI_DIN to DSPI_CLK (Input hold)	10	—	ns

The values in Table 42 correspond to Figure 47.

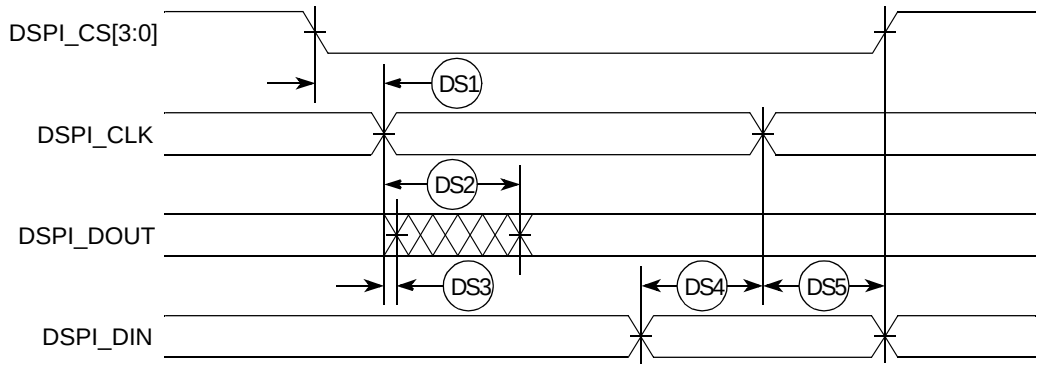


Figure 47. DSPI Timing

A.16 Timer Module AC Timing Specifications

Table 43 lists timer module AC timings.

Table 43. Timer Module AC Timing Specifications

Name	Characteristic	0–66 MHz		Unit
		Min	Max	
T1	TIN0 / TIN1 / TIN2 / TIN3 cycle time	3	—	PSTCLK
T2	TIN0 / TIN1 / TIN2 / TIN3 pulse width	1	—	PSTCLK

THIS PAGE INTENTIONALLY LEFT BLANK

THIS PAGE INTENTIONALLY LEFT BLANK

HOW TO REACH US:

USA / EUROPE / Locations Not Listed:

Motorola Literature Distribution
P.O. Box 5405
Denver, Colorado 80217
1-800-521-6274 or 480-768-2130

JAPAN:

Motorola Japan Ltd.
SPS, Technical Information Center
3-20-1, Minami-Azabu Minato-ku
Tokyo, 106-8573 Japan
81-3-3440-3569

ASIA/PACIFIC:

Motorola Semiconductors H.K. Ltd.
Silicon Harbour Centre
2 Dai King Street
Tai Po Industrial Estate
Tai Po, N.T., Hong Kong
852-26668334

HOME PAGE:

http://motorola.com/semiconductors

MOTOROLA

MCF5485EC/D, **Rev. 1.2, 3/2004**