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Continuity of document content

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Continuity of ordering part numbers

Infineon continues to support existing part numbers. Please continue to use the ordering part numbers listed in the datasheet for ordering.

CY25200

Programmable Spread Spectrum Clock Generator for EMI Reduction

Features

- Wide Operating Output (SSCLK) Frequency Range
  - 3 to 200 MHz
- Programmable Spread Spectrum with nominal 31.5-kHz modulation frequency
- Center Spread: ±0.25% to ±2.5%
- Down Spread: –0.5% to –5.0%
- Input frequency range
  - External crystal: 8 to 30 MHz fundamental crystals
  - External reference: 8 to 166 MHz clock
- Integrated phase-locked loop (PLL)
- Programmable crystal load capacitor tuning array
- Low cycle-to-cycle jitter
- 3.3-V operation with 2.5-V Output Clock Drive Option
- Spread Spectrum On and Off function
- Power Down or Output Enable function
- Output Frequency Select option
- Field-Programmable
- Package: 16-pin TSSOP

Functional Description

The CY25200 is a programmable clock generator with spread spectrum capability. Spread spectrum modulates the output clock frequency over a small range, spreading the energy and reducing the energy peak. This is a powerful technique to reduce EMI in a variety of applications.

It uses either an external reference clock or a crystal for an input. It also uses a PLL to generate a spread spectrum output clock that can be a different frequency than the input. Up to six output clocks are available and up to two of them can be REFCLKs (copies of the input clock, without spread).

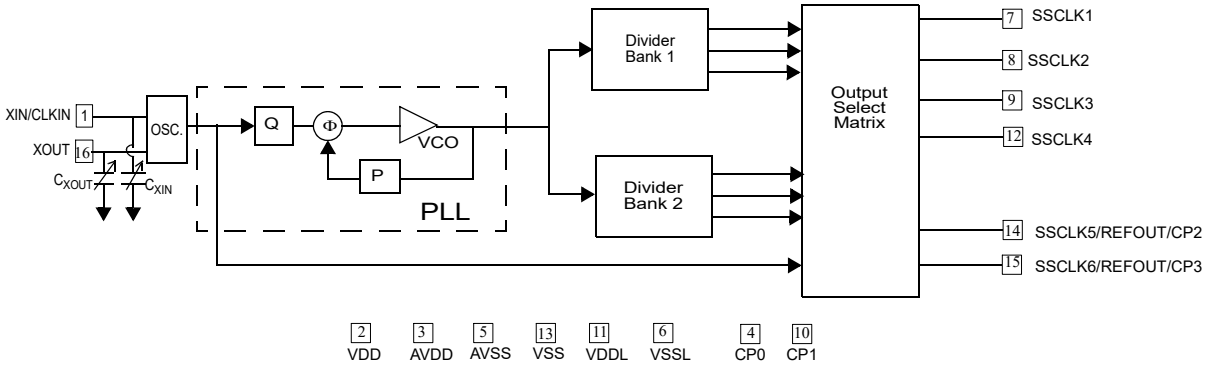
The CY25200 is highly configurable. Programmable variables include the input and output frequencies, spread percentage, center spread or down spread, and control pin functions. The oscillator pin capacitance can also be programmed to match the load capacitance requirement (C_L) of the crystal, eliminating the need for external capacitors.

Available features include Output Enable, Power Down, Spread On/Off, Frequency Select, and the option to power some output clocks at 2.5 V.

Programmability enables fast prototyping, which is particularly useful when doing EMC testing and determining the optimal spread settings.

For a complete list of related documentation, click here.

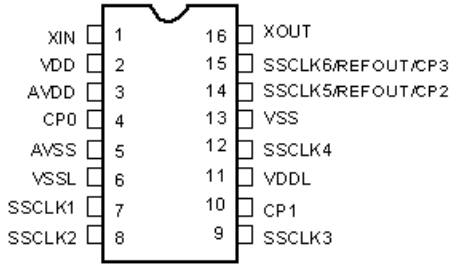
Logic Block Diagram



Contents

Pin Configuration

Figure 1. 16-pin TSSOP pinout



Pin Description

Table 1. Pin Summary

Name	Pin Number	Description
XIN	1	Crystal input or Reference Clock input
XOUT	16	Crystal output. Leave this pin floating if external clock is used
VDD	2	3.3-V power supply for digital logic and SSCLK5 and 6 clock outputs
AVDD	3	3.3-V analog–PLL power supply
VSS	13	Ground
AVSS	5	Analog ground
VDDL	11	2.5-V or 3.3-V power supply for SSCLK1/2/3/4 clock outputs
VSSL	6	VDDL power supply ground
SSCLK1	7	Programmable spread spectrum clock output at VDDL level (2.5 V or 3.3 V)
SSCLK2	8	Programmable spread spectrum clock output at VDDL level (2.5 V or 3.3 V)
SSCLK3	9	Programmable spread spectrum clock output at VDDL level (2.5 V or 3.3 V)
SSCLK4	12	Programmable spread spectrum clock output at VDDL level (2.5 V or 3.3 V)
SSCLK5/REFOUT/CP2	14	Programmable spread spectrum clock or buffered reference output at VDD level (3.3 V) or control pin, CP2
SSCLK6/REFOUT/CP3	15	Programmable spread spectrum clock or buffered reference output at VDD level (3.3 V) or control pin, CP3
CP0[1]	4	Control pin 0
CP1[1]	10	Control pin 1

Note
1. Pins are programmed to be any of the following control signals: OE: Output Enable, OE = 1, all the SSCLK outputs are enabled; PD#: Power down, PD# = 0, all the SSCLK outputs are three-stated and the part enters a low power state; SSON: Spread Spectrum Control (SSON = 0, No Spread and SSON = 1, Spread Signal), CLKSEL: SSCLK Output Frequency Select.See Control Pins (CP0, CP1, CP2 and CP3) for control pins programming options.

Table 2. Fixed Function Pins

Pin Function	Output Clock Frequency	Input Frequency	C_{XIN} and C_{XOUT}	Spread Percent	Modulation Frequency
Pin Name	SSCLK[1:6]	XIN and XOUT	XIN and XOUT	SSCLK[1:6]	SSCLK[1:6]
Pin#	7, 8, 9, 12, 14, 15	1 and 16	1 and 16	7, 8, 9, 12, 14, 15	7, 8, 9, 12, 14, 15
Units	MHz	MHz	pF	% and Center- or Down-spread	kHz
Program Value CLKSEL = 0	USER SPECIFIED	USER SPECIFIED	USER SPECIFIED	USER SPECIFIED	USER SPECIFIED
Program Value CLKSEL = 1	USER SPECIFIED				

Table 3. Multi-Function Pins

Pin Function	Output Clock/REFOUT/OE/SSON/CLKSEL		OE/PD#/SSON/CLKSEL	
Pin Name	SSCLK5/REFOUT/CP2	SSCLK6/REFOUT/CP3	CP0	CP1
Pin#	14	15	4	10
Units	Function	Function	Function	Function
	USER SPECIFIED	USER SPECIFIED	USER SPECIFIED	USER SPECIFIED

General Description

The CY25200 is a Spread Spectrum Clock Generator (SSCG) IC used to reduce Electro Magnetic Interference (EMI) found in today's high speed digital electronic systems.

The device uses a Cypress proprietary Phase-Locked Loop (PLL) and Spread Spectrum Clock (SSC) technology to synthesize and modulate the frequency of the input clock. By frequency modulating the clock, the measured EMI at the fundamental and harmonic frequencies are reduced. This reduction in radiated energy significantly reduces the cost of complying with regulatory agency requirements (EMC) and improves time to market, without degrading system performance.

The CY25200 uses a factory and field-programmable configuration memory array to synthesize output frequency, spread percentage, crystal load capacitor, clock control pins, PD#, and OE options.

The spread percentage is factory and field-programmed to either center spread or down spread with various spread percentages. The range for center spread is from ±0.25% to ±2.50%. The range for down spread is from –0.5% to –5.0%. Contact the factory for smaller or larger spread percentage amounts, if required.

The input to the CY25200 is either a crystal or a clock signal. The input frequency range for crystals is 8 to 30 MHz and for clock signals is 8 to 166 MHz.

The CY25200 has six clock outputs, SSCLK1 to SSCLK6. The frequency modulated SSCLK outputs are programmed from 3 to 200 MHz.

The CY25200 products are available in a 16-pin TSSOP package with a commercial operating temperature range of 0 to 70 °C.

Programming Description

Field-Programmable CY25200

The CY25200 is programmed at the package level, and must be programmed prior to installation on a circuit board. Field programmable devices are denoted by an "F" in the ordering code, and are blank when shipped. The CY25200 is Flash technology based, which allows it to be reprogrammed up to 100 times. This allows for fast and easy design changes and product updates, and eliminates issues with old and out of date inventory.

Samples and small prototype quantities are programmed on the CY3672 programmer with the CY3695 socket adapter.

Factory-Programmed CY25200

Factory programming by Cypress is available for high volume orders. All requests must be submitted to the local Cypress Field Application Engineer (FAE) or sales representative. After the request is processed, you will receive a new part number, samples, and data sheet with the programmed values. This part number is used for additional sample requests and production orders.

Product Functions

Control Pins (CP0, CP1, CP2 and CP3)

Four control signals are available through programming of pins 4, 10, 14, and 15.

CP0 (pin 4) and CP1 (pin10) are specifically designed to function as control pins. However, pins 14 (SSCLK5/REFOUT/CP2) and 15 (SSCLK6/REFOUT/CP3) are multi-functional and can be programmed to be either a control signal or an output clock (SSCLK or REFOUT). All of the control pins, CP0, CP1, CP2, and CP3 are programmable to one of the following functions:

- OE (Output Enable): if OE = 1, all SSCLK and REFOUT outputs are enabled.
- SSON (Spread spectrum control): if SSON = 1, spread is on; if SSON = 0, spread is off.
- CLKSEL (Clock select): frequency select for all SSCLK outputs.
- PD# (Power Down; active low): if PD# = 0, all the outputs are three-stated and the part enters a low power state.

Note that the PD# function is available only on CP0 or CP1; it is not available on CP2 or CP3.

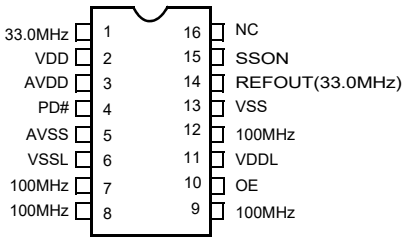
Example

Here is an example with three control pins:

- CLKIN = 33 MHz
- SSCLK1/2/3/4 = 100 MHz with ±1% spread
- SSCLK 5 = REFOUT(33 MHz)
- CP0 (pin 4) = PD#
- CP1 (pin 10) = OE
- CP3 (pin 15) = SSON

The pinout for the above example is shown in Figure 2.

Figure 2. Example Pin Diagram



CLKSEL

The CLKSEL control pin enables you to select between two different SSCLK output frequencies. These must be related frequencies that are derived off of a common PLL frequency. Specifically, CLKSEL does not change the PLL frequency. It only changes the output divider. For instance, 33.333 MHz and 66.666 MHz are both derived from a PLL frequency of 400 MHz, by dividing it down by 12 and 6 respectively. Table 4 on page 6 shows an example of how this is implemented. The PLL frequency range is 100 to 400 MHz. The two output dividers in the CY25200 can be any integer between 2 and 130, providing two different but related frequencies as explained above.

Table 4 on page 6 and Figure 3 on page 6 show an example configuration using the frequencies just described. In this example, the configurable pins SSCLK5 (pin 14) and SSCLK6 (pin 15) are used as output clocks.

Input Frequency (XIN, Pin 1 and XOUT, Pin 16)

The input to the CY25200 is a crystal or a clock. The input frequency range for crystals is 8 to 30 MHz, and for clock signal is 8 to 166 MHz.

C_{XIN} and C_{XOUT} (Pin 1 and Pin 16)

The CY25200 has internal load capacitors at pin 1 (C_{XIN}) and pin 16 (C_{XOUT}). C_{XIN} always equals C_{XOUT}, and they are programmable from 12 pF to 60 pF, in 0.5 pF increments. This feature eliminates the need for external crystal load capacitors.

The following formula is used to calculate the value of C_{XIN} and C_{XOUT} for matching the crystal load (C_L):

$C_{XIN} = C_{XOUT} = 2C_L – C_P$

Where C_L is the crystal load capacitor as specified by the crystal manufacturer and C_P is the parasitic PCB capacitance on each node of the crystal.

For example, if a crystal with C_L of 16 pF is used, and C_P is 2 pF, C_{XIN} and C_{XOUT} is calculated as:

$C_{XIN} = C_{XOUT} = (2 \times 16) – 2 = 30$ pF.

If using a driven reference clock, set C_{XIN} and C_{XOUT} to the minimum value 12 pF, connect the reference to XIN/CLKIN, and leave XOUT unconnected.

Output Frequency (SSCLK1 through SSCLK6 Outputs)

All the SSCLK outputs are produced by synthesizing the input reference frequency using a PLL and modulating the VCO frequency. SSCLK[1:4] are fixed function output clocks (SSCLK). SSCLK5 and SSCLK6 are also programmable to function the same as SSCLK[1:4], or as buffered copies of the input reference (REFOUT), or as control pin as discussed in Control Pins (CP0, CP1, CP2 and CP3). To use the 2.5-V output drive option on SSCLK[1:4], VDDL must be connected to a 2.5-V power supply (SSCLK[1:4] outputs are powered by VDDL). When using the 2.5-V output drive option, the maximum output frequency on SSCLK[1:4] is 166 MHz.

Spread Percentage (SSCLK1 to SSCLK6 Outputs)

The SSCLK frequency is programmed to a percentage value from ±0.25% to ±2.5% for center spread and from –0.5% to –5.0% down spread. The granularity is 0.25%.

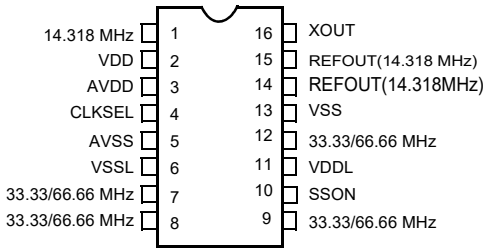
Modulation Frequency

The default modulation frequency is 31.5 kHz. Other modulation frequencies available via the configuration software are 30.1 kHz and 32.9 kHz.

Table 4. Using Clock Select, CLKSEL Control Pin

Input Frequency (MHz)	CLKSEL (Pin 4)	SSCLK1 (Pin 7)	SSCLK2 (Pin 8)	SSCLK3 (Pin 9)	SSCLK4 (Pin 12)	REFOUT (Pin 14)	REFOUT (Pin 15)
14.318	CLKSEL = 0	33.33	33.33	33.33	33.33	14.318	14.318
	CLKSEL = 1	66.66	66.66	66.66	66.66	14.318	14.318

Figure 3. Using Clock Select, CLKSEL Control Pin Configuration pinout



Absolute Maximum Ratings

Supply voltage (V_{DD}) ..... –0.5 to +7.0 V
DC input voltage ..... –0.5 V to V_{DD} + 0.5 V
Storage temperature (non-condensing) ..... –55 °C to +125 °C
Junction temperature ..... –40 °C to +125 °C
Data retention at Tj = 125 °C .....> 10 years
Package power dissipation ..... 350 mW
Static discharge voltage (per MIL-STD-883, Method 3015) ..... ≥ 2000 V

Recommended Crystal Specifications

Parameter	Description	Comments	Min	Typ	Max	Unit
F_{NOM}	Nominal crystal frequency	Parallel resonance, fundamental mode, AT cut	8	–	30	MHz
C_{LNOM}	Nominal load capacitance	Internal load caps	6	–	30	pF
R_1	Equivalent series resistance (ESR)	Fundamental mode	–	–	25	Ω
R_3/R_1	Ratio of third overtone mode ESR to Fundamental Mode ESR	Ratio used because typical R_1 values are much less than the maximum specification	3	–	–	Ω
DL	Crystal drive level	No external series resistor assumed	–	0.5	2	mW

Recommended Operating Conditions

Parameter	Description	Min	Typ	Max	Unit
V_{DD}	Operating voltage	3.135	3.3	3.465	V
V_{DDLHI}	Operating voltage	3.135	3.3	3.465	V
V_{DDLLO}	Operating voltage	2.375	2.5	2.625	V
T_{AC}	Ambient commercial temp	0	–	70	°C
C_{LOAD}	Maximum load capacitance V_{DD}/V_{DDL} = 3.3 V	–	–	15	pF
C_{LOAD}	Maximum load capacitance V_{DDL} = 2.5 V	–	–	15	pF
$F_{SSCLK\text{-}HighVoltage}$	SSCLK1/2/3/4/5/6 when $V_{DD} = A_{VDD} = V_{DDL}$ = 3.3 V	3	–	200	MHz
$F_{SSCLK\text{-}LowVoltage}$	SSCLK1/2/3/4 when $V_{DD} = A_{VDD}$ = 3.3 V and V_{DDL} = 2.5 V	3	–	166	MHz
R_{EFOUT}	REFOUT when $V_{DD} = A_{VDD}$ = 3.3 V and V_{DDL} = 3.3 V or 2.5 V	8	–	166	MHz
f_{REF1}	Clock Input	8	–	166	MHz
f_{REF2}	Crystal Input	8	–	30	MHz
t_{PU}	Power up time for all V_{DD}s to reach minimum specified voltage (power ramps must be monotonic)	0.05	–	500	ms

DC Electrical Specifications

Parameter [2]	Name	Description	Min	Typ	Max	Unit
$I_{OH3.3}$	Output High Current	$V_{OH} = V_{DD} – 0.5$ V, $V_{DD}/V_{DDL} = 3.3$ V	12	24	–	mA
$I_{OL3.3}$	Output Low Current	$V_{OL} = 0.5$ V, $V_{DD}/V_{DDL} = 3.3$ V	12	24	–	mA
$I_{OH2.5}$	Output High Current	$V_{OH} = V_{DDL} – 0.5$ V, $V_{DDL} = 2.5$ V	8	16	–	mA
$I_{OL2.5}$	Output Low Current	$V_{OL} = 0.5$ V, $V_{DDL} = 2.5$ V	8	16	–	mA
V_{IH}	Input High Voltage	CMOS levels, 70% of V_{DD}	0.7	–	1.0	V_{DD}
V_{IL}	Input Low Voltage	CMOS levels, 30% of V_{DD}	0	–	0.3	V_{DD}
I_{VDD} [3]	Supply Current	AV_{DD}/V_{DD} Current	–	–	33	mA
$I_{VDDL2.5}$ [3]	Supply Current	V_{DDL} Current ($V_{DDL} = 2.625$ V)	–	–	20	mA
$I_{VDDL3.3}$ [3]	Supply Current	V_{DDL} Current ($V_{DDL} = 3.465$ V)	–	–	26	mA
I_{DDS}	Power Down Current	$V_{DD} = V_{DDL} = AV_{DD} = 3.465$ V	–	–	50	µA
I_{OHZ} I_{OLZ}	Output Leakage	$V_{DD} = V_{DDL} = AV_{DD} = 3.465$ V	–	–	10	µA

Thermal Resistance

Parameter [4]	Description	Test Conditions	16-pin TSSOP	Unit
θ_{JA}	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, in accordance with EIA/JESD51.	90	°C/W
θ_{JC}	Thermal resistance (junction to case)		14	°C/W

Notes
2. Not 100% tested, guaranteed by design.
3. I_{VDD} currents specified for SSCLK1/2/3/4/5/6 = 33.33 MHz with CLKIN = 14.318 MHz and 15 pF on all the output clocks.
4. These parameters are guaranteed by design and are not tested.

AC Electrical Specifications

Parameter	Description	Condition	Min	Typ	Max	Unit
DC	Output Duty Cycle	SSCLK, Measured at $V_{DD}/2$	45	50	55	%
	Output Duty Cycle	REFCLK, Measured at $V_{DD}/2$ Duty Cycle of CLKIN = 50%.	40	50	60	%
SR1	Rising/Falling Edge Slew Rate	SSCLK1/2/3/4 < 100 MHz, $V_{DD} = V_{DDL} = 3.3$ V	0.6	–	2.0	V/ns
SR2	Rising/Falling Edge Slew Rate	SSCLK1/2/3/4 ≥ 100 MHz, $V_{DD} = V_{DDL} = 3.3$ V	0.8	–	3.5	V/ns
SR3	Rising/Falling Edge Slew Rate	SSCLK1/2/3/4 < 100 MHz, $V_{DD} = V_{DDL} = 2.5$ V	0.5	–	2.2	V/ns
SR4	Rising/Falling Edge Slew Rate	SSCLK1/2/3/4 ≥ 100 MHz, $V_{DD} = V_{DDL} = 2.5$ V	0.6	–	3.0	V/ns
SR5	Rising/Falling Edge Slew Rate	SSCLK5/6 < 100 MHz, $V_{DD} = V_{DDL} = 3.3$ V	0.6	–	1.9	V/ns
SR6	Rising/Falling Edge Slew Rate	SSCLK5/6 ≥ 100 MHz, $V_{DD} = V_{DDL} = 3.3$ V	1.0	–	2.9	V/ns
T_{CCJ1}	Cycle-to-Cycle Jitter SSCLK1/2/3/4	CLKIN = SSCLK1/2/3/4 = 166 MHz, ±2% spread and SSCLK5/6 = REFOUT, $V_{DD} = V_{DDL} = 3.3$ V	–	–	110	ps
		CLKIN = SSCLK1/2/3/4 = 66.66 MHz, ±2% spread and SSCLK5/6 = REFOUT, $V_{DD} = V_{DDL} = 3.3$ V	–	–	170	ps
		CLKIN = SSCLK1/2/3/4 = 33.33 MHz, ±2% spread and SSCLK5/6 = REFOUT, $V_{DD} = V_{DDL} = 3.3$ V	–	–	140	ps
		CLKIN = SSCLK1/2/3/4 = 14.318 MHz, ±2% spread and SSCLK5/6 = REFOUT, $V_{DD} = V_{DDL} = 3.3$ V	–	–	290	ps
T_{CCJ2}	Cycle-to-Cycle Jitter SSCLK5/6=REFOUT	CLKIN = SSCLK1/2/3/4 = 166 MHz, ±2% spread and SSCLK5/6 = REFOUT, $V_{DD} = V_{DDL} = 3.3$ V	–	–	100	ps
		CLKIN = SSCLK1/2/3/4 = 66.66 MHz, ±2% spread and SSCLK5/6 = REFOUT, $V_{DD} = V_{DDL} = 3.3$ V	–	–	120	ps
		CLKIN = SSCLK1/2/3/4 = 33.33 MHz, ±2% spread and SSCLK5/6 = REFOUT, $V_{DD} = V_{DDL} = 3.3$ V	–	–	180	ps
		CLKIN = SSCLK1/2/3/4 = 14.318 MHz, ±2% spread and SSCLK5/6 = REFOUT, $V_{DD} = V_{DDL} = 3.3$ V	–	–	180	ps

AC Electrical Specifications *(continued)*

Parameter	Description	Condition	Min	Typ	Max	Unit
T_{CCJ3}	Cycle-to-Cycle Jitter SSCLK1/2/3/4	CLKIN = SSCLK1/2/3/4 = 166 MHz, ±2% spread and SSCLK5/6 = REFOUT, V_{DD} = 3.3 V, V_{DDL} = 2.5 V	–	–	110	ps
		CLKIN = SSCLK1/2/3/4 = 66.66 MHz, ±2% spread and SSCLK5/6 = REFOUT, V_{DD} = 3.3 V, V_{DDL} = 2.5 V	–	–	170	ps
		CLKIN = SSCLK1/2/3/4 = 33.33 MHz, ±2% spread and SSCLK5/6 = REFOUT, V_{DD} = 3.3 V, V_{DDL} = 2.5 V	–	–	190	ps
		CLKIN = SSCLK1/2/3/4 = 14.318 MHz, ±2% spread and SSCLK5/6 = REFOUT, V_{DD} = 3.3 V, V_{DDL} = 2.5 V	–	–	330	ps
T_{STP}	Power Down Time	Time from falling edge on PD# to stopped outputs (Asynchronous)	–	150	300	ns
T_{OE1}	Output Disable Time	Time from falling edge on OE to stopped outputs (Asynchronous)	–	150	300	ns
T_{OE2}	Output Enable Time	Time from rising edge on OE to outputs at a valid frequency (Asynchronous)	–	150	300	ns
F_{MOD}	Spread Spectrum Modulation Frequency	SSCLK1/2/3/4/5/6	30.0	31.5	33.0	kHz
T_{PU1}	Power Up Time, Crystal is used	Time from rising edge on PD# to outputs at valid frequency (Asynchronous)	–	3	5	ms
T_{PU2}	Power Up Time, Reference clock is used	Time from rising edge on PD# to outputs at valid frequency (Asynchronous)	–	2	3	ms
T_{SKEW} [5]	Clock Skew	Output to output skew between related clock outputs. Measured at $V_{DD}/2$.	–	–	250	ps

Note
5. Skew and phase alignment is guaranteed within all SSCLK outputs and within both REFOUT outputs. All SSCLK outputs are related, and all REOUT outputs are related, but SSCLK and REFOUT outputs are not related to each other.

Switching Waveforms

Figure 4. Duty Cycle Timing (DC = t_{1A}/t_{1B})

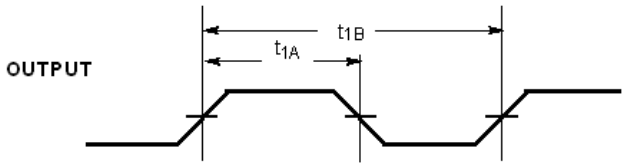
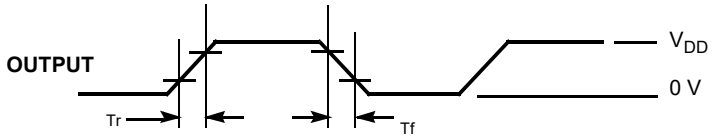


Figure 5. Output Rise and Fall Time (SSCLK and REFCLK)



Output Rise time (Tr) = (0.6 x V_{DD})/SR1 (or SR3)
Output Fall time (Tf) = (0.6 x V_{DD})/SR2 (or SR4)
Refer to AC Electrical Characteristics table for SR (Slew Rate) values.

Figure 6. Power Down and Power Up Timing

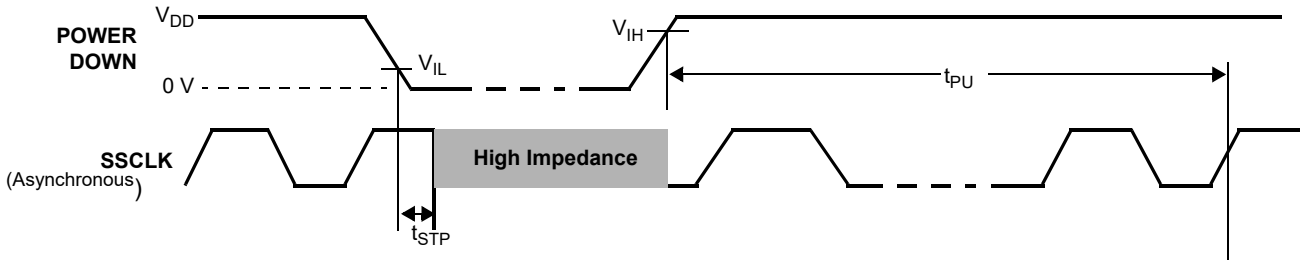
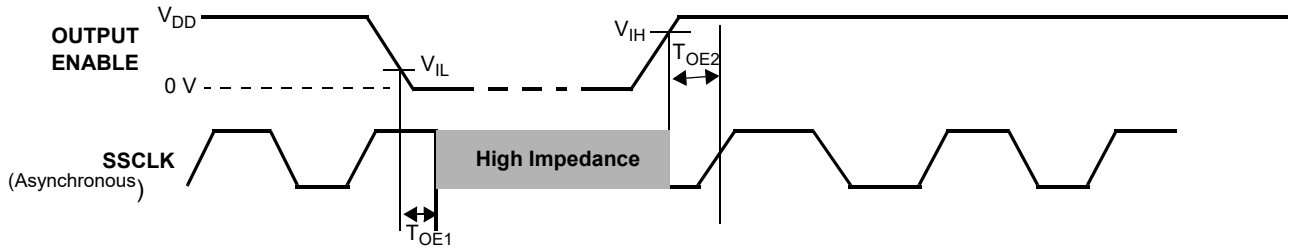
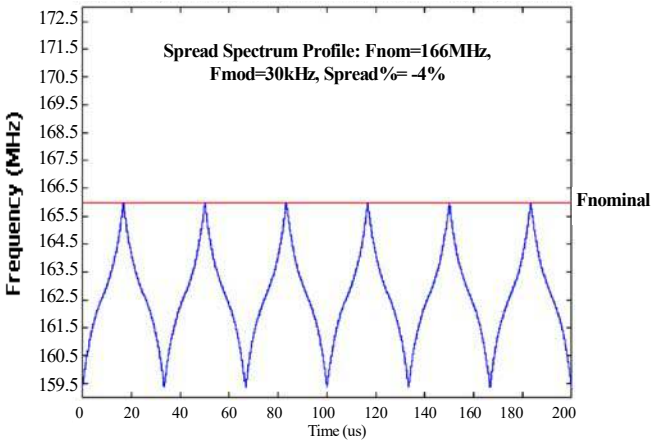


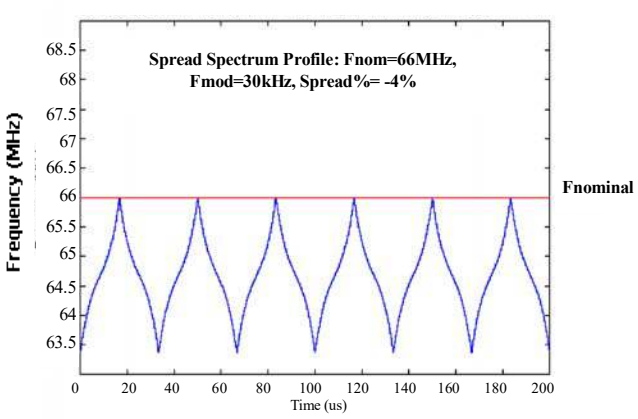
Figure 7. Output Enable and Disable Timing

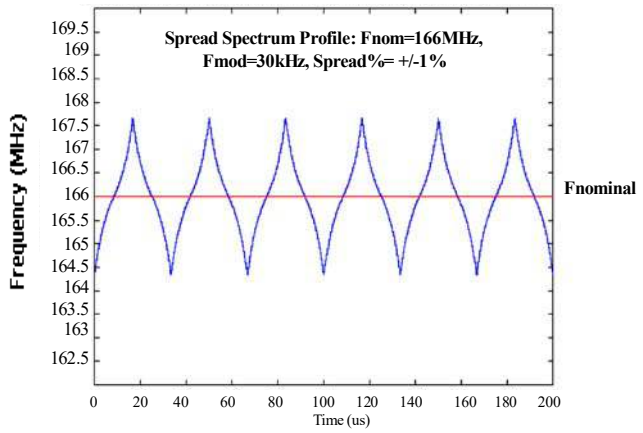


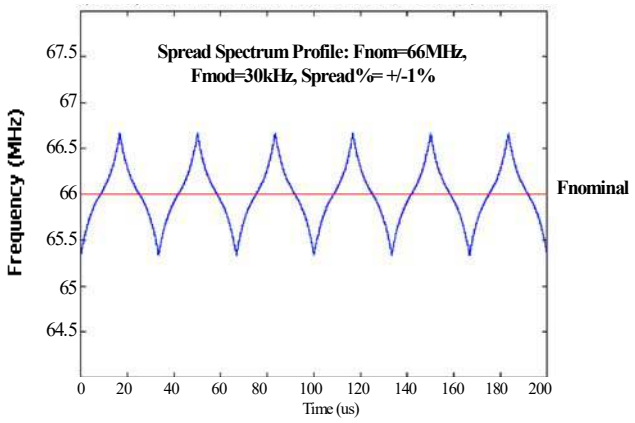
Informational Graphs

The informational graphs are meant to convey the typical performance levels. No performance specification is implied or guaranteed.









Ordering Information

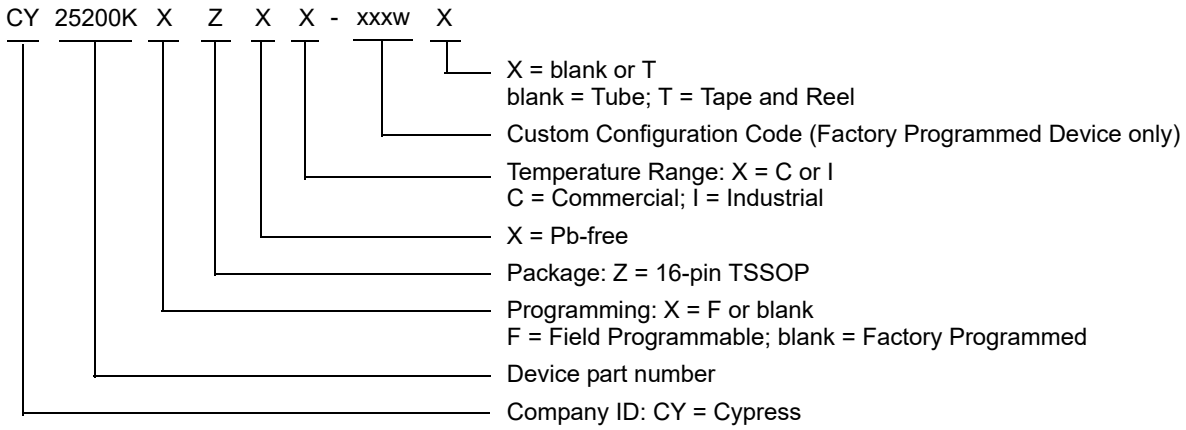
Ordering Code	Package Type	Programming	Operating Temperature Range
CY25200KFZXC	16-pin TSSOP (Pb-free)	Field	Commercial, 0 °C to 70 °C
CY25200KFZXCT	16-pin TSSOP – Tape and Reel (Pb-free)	Field	Commercial, 0 °C to 70 °C
CY25200KFZXI	16-pin TSSOP (Pb-free)	Field	Industrial, –40 °C to 85 °C
CY25200KFZXIT	16-pin TSSOP – Tape and Reel (Pb-free)	Field	Industrial, –40 °C to 85 °C
Programmer			
CY3672-USB	Programmer for Field Programmable Devices	N/A	N/A
CY3695	CY22050/CY22150/CY25200 Socket Adapter for CY3672-USB	N/A	N/A

Some product offerings are factory programmed customer specific devices with customized part numbers. The Possible Configurations table shows the available device types, but not complete part numbers. Contact your local Cypress FAE or Sales Representative for more information.

Possible Configurations

Ordering Code [6]	Package Type	Programming	Operating Temperature Range
CY25200ZXC-xxx	16-pin TSSOP (Pb-free)	Factory	Commercial, 0 °C to 70 °C
CY25200ZXC-xxxT	16-pin TSSOP – Tape and Reel (Pb-free)	Factory	Commercial, 0 °C to 70 °C
CY25200ZXI-xxx	16-pin TSSOP (Pb-free)	Factory	Industrial, –40 °C to 85 °C
CY25200ZXI-xxxT	16-pin TSSOP – Tape and Reel (Pb-free)	Factory	Industrial, –40 °C to 85 °C

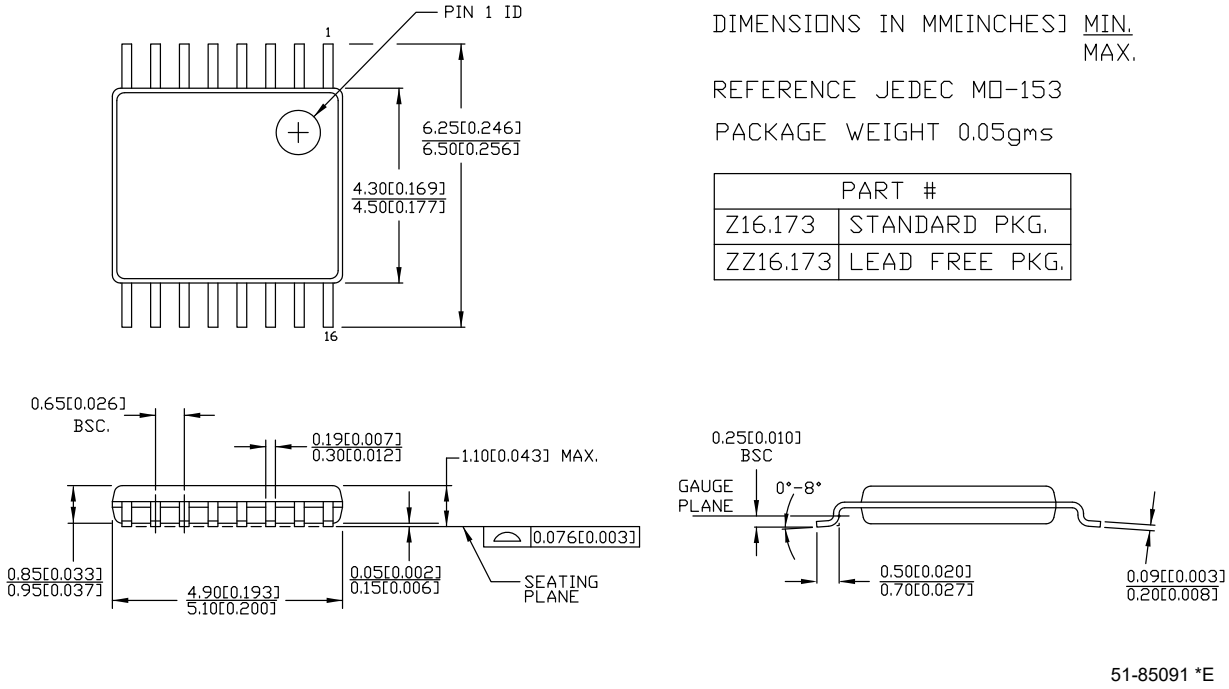
Ordering Code Definitions



Note
6. "xxx" denotes a specific device configuration, and is referred to as the "dash number". "w" denotes the configuration revision.

Package Drawing and Dimensions

Figure 8. 16-pin TSSOP (4.40 mm Body) Z16.173/ZZ16.173 Package Outline, 51-85091



Acronyms

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interference
FAE	Field Application Engineer
OE	Output Enable
OSC	Oscillator
PLL	Phase Locked Loop
SSC	Spread Spectrum Clock
SSCG	Spread Spectrum Clock Generator
TSSOP	Thin Shrunk Small Outline Package

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
kΩ	kilohm
kHz	kilohertz
MHz	megahertz
µA	microampere
ms	millisecond
mW	milliwatt
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
ps	picosecond
V	volt

Document History Page

Document Title: CY25200, Programmable Spread Spectrum Clock Generator for EMI Reduction Document Number: 38-07633				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	204243	RGL	See ECN	New data sheet.
*A	220043	RGL	See ECN	Updated Ordering Information: No change in part numbers. Minor Change: Replaced Z with X in MPNs in ordering information for Pb free.
*B	267832	RGL	See ECN	Added Field Programmable Devices related information in all instances across the document. Updated Ordering Information: Updated part numbers.
*C	291094	RGL	See ECN	Updated AC Electrical Specifications: Added t_{SKEW} parameter and its details.
*D	1821908	DPF / AESA	See ECN	Updated Recommended Operating Conditions: Updated details in “Description” column corresponding to $F_{SSCLK-Low\ Voltage}$ parameter (Replaced SSCLK5/6 with SSCLK1/2/3/4). Updated AC Electrical Specifications: Removed T_{CCJ4} parameter and its details.
*E	2442066	KVM / AESA	See ECN	Updated Ordering Information: Updated part numbers. Added Note “Not recommended for new designs.” and referred the same note in CY25200ZXC_XXXW, CY25200ZXC_XXXWT, CY25200FZXC and CY25200FZXCT. Updated Package Drawing and Dimensions. No change in revisions. Updated caption of spec 51-85091 *A (Replaced Z16.173 with ZZ16). Updated to new template.
*F	2758387	KVM / AESA	09/01/2009	Extensive text edits in all instances across the document. Removed Benefits. Added Description. Updated Pin Description: Updated Table 2. Updated Table 3. Updated Programming Description: Updated Modulation Frequency: Updated description. Updated DC Electrical Specifications: Updated minimum and typical values of $I_{OH3.3}$ and $I_{OL3.3}$ parameters. Updated AC Electrical Specifications: Updated details in “Unit” column (Filled all missing units). Updated details in “Description” column corresponding to T_{STP}, T_{OE1} and T_{OE2} parameters. Updated Note 5 (for clarity). Standardized all parameter names to upper case. Updated Ordering Information: Updated part numbers. Updated existing Note “Not recommended for new designs.” as “Not recommended for new designs. Part numbers without a “K” are being replaced by part numbers with a “K”. There are no changes to device specifications as a result of the part number change.”

Document History Page *(continued)*

Document Title: CY25200, Programmable Spread Spectrum Clock Generator for EMI Reduction Document Number: 38-07633				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
*G	2897246	KVM	03/22/10	Updated Ordering Information: Removed inactive parts. Removed Note “Not recommended for new designs. Part numbers without a “K” are being replaced by part numbers with a “K”. There are no changes to device specifications as a result of the part number change.” and its references. Added Possible Configurations. Referred Note 6 in “Ordering Code” column. Updated Package Drawing and Dimensions: spec 51-85091 – Changed revision from *A to *B.
*H	3103982	BASH	07/12/2010	Added Ordering Code Definitions. Updated Package Drawing and Dimensions: spec 51-85091 – Changed revision from *B to *C. Added Acronyms and Units of Measure. Minor edits. Updated to new template.
*I	4209874	CINM	12/16/2013	Updated Ordering Information: Updated part numbers. Updated Possible Configurations: Updated part numbers. Updated Package Drawing and Dimensions: spec 51-85091 – Changed revision from *C to *D. Updated to new template. Completing Sunset Review.
*J	4581659	AJU	11/28/2014	Updated Functional Description: Added “For a complete list of related documentation, click here.” at the end. Updated Package Drawing and Dimensions: spec 51-85093 – Changed revision from *D to *E.
*K	4623539	TAVA	01/14/2015	Updated Ordering Information: Updated Possible Configurations: Updated details in “Ordering Code” column.
*L	5532023	PSR	11/24/2016	Updated Functional Description: Updated description. Updated Programming Description: Removed “CyberClocks™ Online Software”. Added Thermal Resistance. Updated Package Drawing and Dimensions: Removed table “16-pin TSSOP Package Characteristics”. Updated to new template. Completing Sunset Review.
*M	6453987	XHT	01/21/2019	Updated the template.

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