

1-Mbit (64K x 16) Static RAM

Features

- **Temperature Ranges**
 - **Commercial:** 0°C to 70°C
 - **Industrial:** -40°C to 85°C
 - **Automotive:** -40°C to 125°C
- **Pin- and function-compatible with CY7C1021BV33**
- **High speed**
 - $t_{AA} = 8$ ns (Commercial & Industrial)
 - $t_{AA} = 12$ ns (Automotive)
- **CMOS for optimum speed/power**
- **Low active power: 360 mW (max.)**
- **Automatic power-down when deselected**
- **Independent control of upper and lower bits**
- **Available in 44-pin TSOP II, 400-mil SOJ, 48-ball FBGA**
- **Also available in Lead-Free 44-pin TSOP II, 400-mil SOJ packages**

Functional Description^[1]

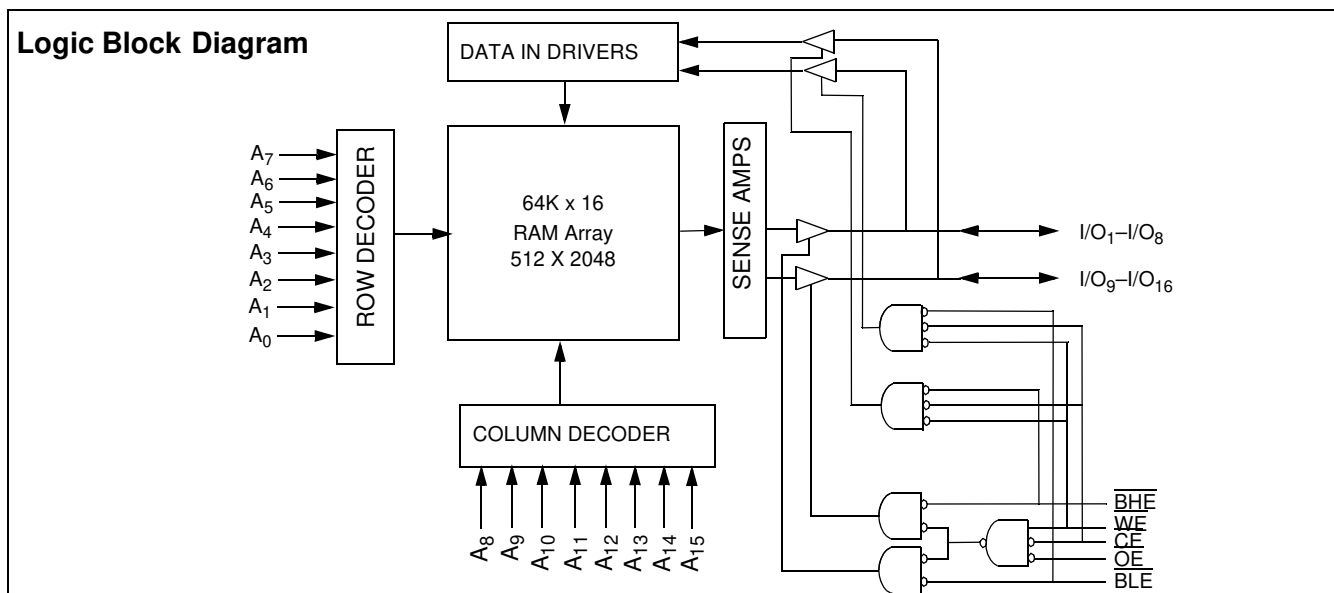
The CY7C1021CV33 is a high-performance CMOS static RAM organized as 65,536 words by 16 bits. This device has an automatic power-down feature that significantly reduces power consumption when deselected.

Writing to the device is accomplished by taking Chip Enable (\overline{CE}) and Write Enable (\overline{WE}) inputs LOW. If Byte Low Enable (\overline{BLE}) is LOW, then data from I/O pins (I/O_1 through I/O_8), is written into the location specified on the address pins (A_0 through A_{15}). If Byte High Enable (\overline{BHE}) is LOW, then data from I/O pins (I/O_9 through I/O_{16}) is written into the location specified on the address pins (A_0 through A_{15}).

Reading from the device is accomplished by taking Chip Enable (\overline{CE}) and Output Enable (\overline{OE}) LOW while forcing the Write Enable (\overline{WE}) HIGH. If Byte Low Enable (\overline{BLE}) is LOW, then data from the memory location specified by the address pins will appear on I/O_1 to I/O_8 . If Byte High Enable (\overline{BHE}) is LOW, then data from memory will appear on I/O_9 to I/O_{16} . See the truth table at the end of this data sheet for a complete description of Read and Write modes.

The input/output pins (I/O_1 through I/O_{16}) are placed in a high-impedance state when the device is deselected (\overline{CE} HIGH), the outputs are disabled (\overline{OE} HIGH), the \overline{BHE} and \overline{BLE} are disabled (\overline{BHE} , \overline{BLE} HIGH), or during a Write operation (\overline{CE} LOW, and \overline{WE} LOW).

The CY7C1021CV33 is available in standard 44-pin TSOP Type II, 400-mil-wide SOJ packages, as well as a 48-ball FBGA.

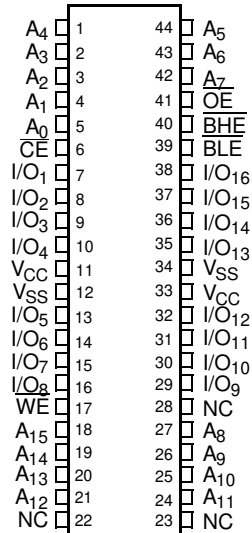
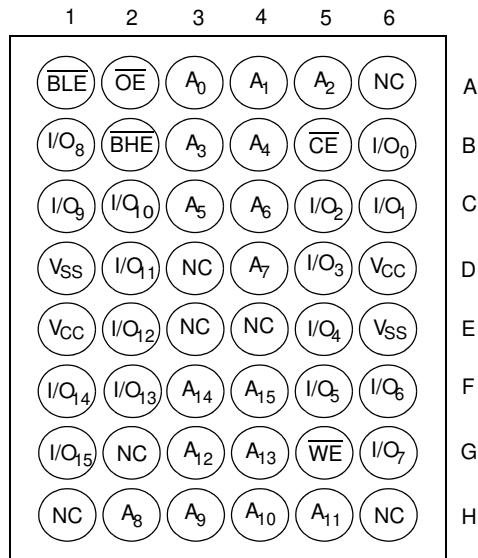


Note:

1. For best-practice recommendations, please refer to the Cypress application note "System Design Guidelines" on <http://www.cypress.com>.

Selection Guide

	CY7C1021CV33-8	CY7C1021CV33-10	CY7C1021CV33-12	CY7C1021CV33-15	Unit
Maximum Access Time	8	10	12	15	ns
Maximum Operating Current	95	90	85	80	mA
	Automotive	-	-	90	mA
Maximum CMOS Standby Current	5	5	5	5	mA
	Automotive	-	-	10	mA

Pin Configurations
**SOJ / TSOP II
Top View**

48-ball FBGA
(Top View)


Pin Definitions

Pin Name	SOJ, TSOP Pin Number	BGA Pin Number	I/O Type	Description
A ₀ -A ₁₅	1-5, 18-21, 24-27, 42-44	A3, A4, A5, B3, B4, C3, C4, D4, H2, H3, H4, H5, G3, G4, F3, F4	Input	Address Inputs used to select one of the address locations.
I/O ₀ -I/O ₁₅ ^[2]	7-10, 13-16, 29-32, 35-38	B6, C6, C5, D5, E5, F5, F6, G6, B1, C1, C2, D2, E2, F2, F1, G1	Input/Output	Bidirectional Data I/O lines. Used as input or output lines depending on operation.
NC	22, 23, 28	A6, D3, E3, E4, G2, H1, H6	No Connect	No Connects. Not connected to the die.
$\overline{\text{WE}}$	17	G5	Input/Control	Write Enable Input, active LOW. When selected LOW, a Write is conducted. When deselected HIGH, a Read is conducted.
$\overline{\text{CE}}$	6	B5	Input/Control	Chip Enable Input, active LOW. When LOW, selects the chip. When HIGH, deselects the chip.
$\overline{\text{BHE}}$, $\overline{\text{BLE}}$	39, 40	A1, B2	Input/Control	Byte Write Select Inputs, active LOW. $\overline{\text{BLE}}$ controls I/O ₈ -I/O ₁ , $\overline{\text{BHE}}$ controls I/O ₁₆ -I/O ₉ .
$\overline{\text{OE}}$	41	A2	Input/Control	Output Enable, active LOW. Controls the direction of the I/O pins. When LOW, the I/O pins are allowed to behave as outputs. When deasserted HIGH, I/O pins are three-stated, and act as input data pins.
V _{SS}	12,34	D1, E6	Ground	Ground for the device. Should be connected to ground of the system.
V _{CC}	11,33	D6, E1	Power Supply	Power Supply inputs to the device.

Note:

2. I/O₁-I/O₁₆ for SOJ/TSOP and I/O₀-I/O₁₅ for BGA packages.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to +150°C
 Ambient Temperature with Power Applied -55°C to +125°C
 Supply Voltage on V_{CC} to Relative GND^[3] -0.5V to +4.6V
 DC Voltage Applied to Outputs in High-Z State^[3] -0.5V to V_{CC}+0.5V
 DC Input Voltage^[3] -0.5V to V_{CC}+0.5V
 Current into Outputs (LOW) 20 mA

Static Discharge Voltage >2001V (per MIL-STD-883, Method 3015)

Latch-up Current >200 mA

Operating Range

Range	Ambient Temperature (T _A)	V _{CC}
Commercial	0°C to +70°C	3.3V ± 10%
Industrial	-40°C to +85°C	3.3V ± 10%
Automotive	-40°C to +125°C	3.3V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	1021CV33-8		1021CV33-10		1021CV33-12		1021CV33-15		Unit	
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = -4.0 mA	2.4		2.4		2.4		2.4		V	
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 8.0 mA		0.4		0.4		0.4		0.4	V	
V _{IH}	Input HIGH Voltage		2.0	V _{CC} + 0.3	2.0	V _{CC} + 0.3	2.0	V _{CC} + 0.3	2.0	V _{CC} + 0.3	V	
V _{IL}	Input LOW Voltage ^[3]		-0.3	0.8	-0.3	0.8	-0.3	0.8	-0.3	0.8	V	
I _{IX}	Input Load Current	GND ≤ V _I ≤ V _{CC}	Com'l / Ind'l	-1	+1	-1	+1	-1	+1	-1	+1	μA
			Automotive					-12	+12			μA
I _{OZ}	Output Leakage Current	GND ≤ V _I ≤ V _{CC} , Output Disabled	Com'l / Ind'l	-1	+1	-1	+1	-1	+1	-1	+1	μA
			Automotive	-	-	-	-	-12	+12	-	-	μA
I _{OS}	Output Short Circuit Current ^[4]	V _{CC} = Max., V _{OUT} = GND		-300		-300		-300		-300	mA	
I _{CC}	V _{CC} Operating Supply Current	V _{CC} = Max., I _{OUT} = 0 mA, f = f _{MAX} = 1/t _{RC}	Com'l / Ind'l		95		90		85		80	mA
			Automotive		-		-		90		-	mA
I _{SB1}	Automatic CE Power-Down Current — TTL Inputs	Max. V _{CC} , CE ≥ V _{IH} , V _{IN} ≥ V _{IH} or V _{IN} ≤ V _{IL} , f = f _{MAX}	Com'l / Ind'l		15		15		15		15	mA
			Automotive		-		-		20		-	mA
I _{SB2}	Automatic CE Power-Down Current — CMOS Inputs	Max. V _{CC} , CE ≥ V _{CC} - 0.3V, V _{IN} ≥ V _{CC} - 0.3V, or V _{IN} ≤ 0.3V, f = 0	Com'l / Ind'l		5		5		5		5	mA
			Automotive		-		-		10		-	mA

Notes:

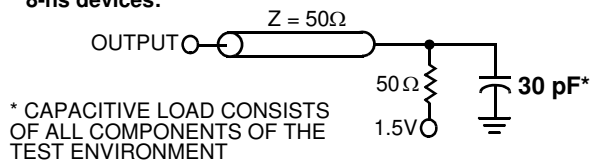
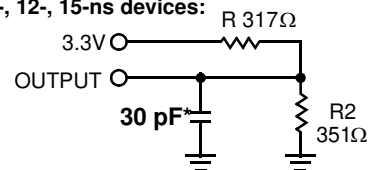
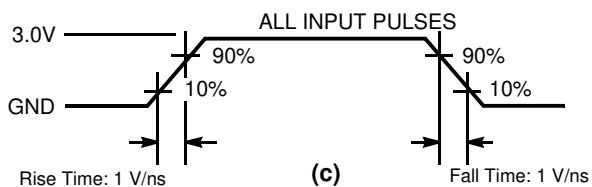
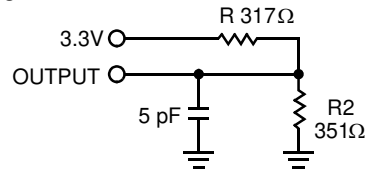
- V_{IL} (min.) = -2.0V and V_{IH} (max) = V_{CC} + 0.5V for pulse durations of less than 20 ns.
- Not more than one output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.

Thermal Resistance^[5]

Parameter	Description	Test Conditions	48-ball FBGA	44-lead SOJ	44-lead TSOP-II	Unit
Θ_{JA}	Thermal Resistance (Junction to Ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA / JESD51.	95.32	65.06	76.92	°C/W
Θ_{JC}	Thermal Resistance (Junction to Case)		10.68	34.21	15.86	°C/W

Capacitance^[5]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	$T_A = 25^\circ\text{C}$, $f = 1\text{ MHz}$, $V_{CC} = 3.3\text{V}$	8	pF
C_{OUT}	Output Capacitance		8	pF

AC Test Loads and Waveforms^[6]
8-ns devices:

(a)
10-, 12-, 15-ns devices:

(b)

(c)
High-Z characteristics:

(d)
Note:

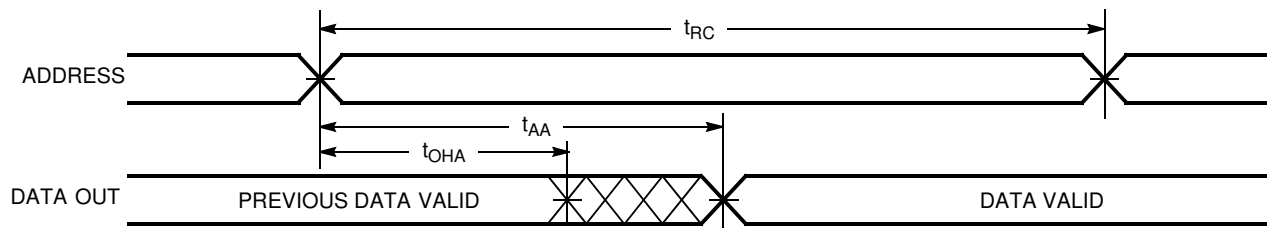
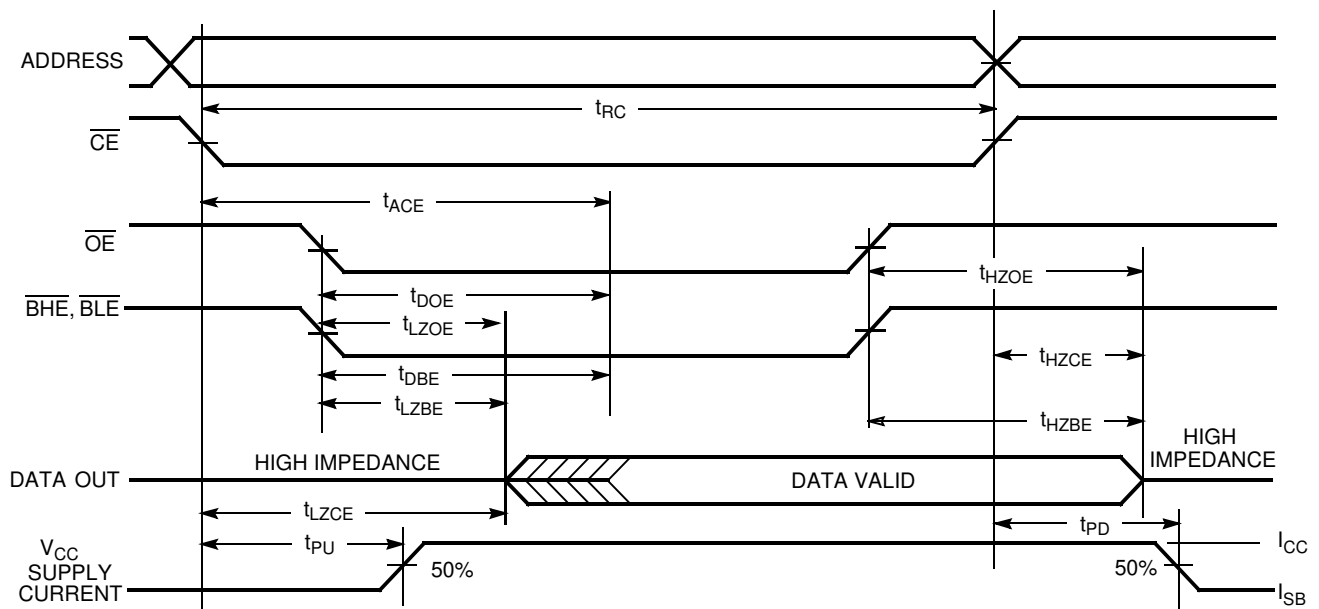
5. Tested initially and after any design or process changes that may affect these parameters.
6. AC characteristics (except High-Z) for all 8-ns parts are tested using the load conditions shown in Figure (a). All other speeds are tested using the Thevenin load shown in Figure (b). High-Z characteristics are tested for all speeds using the test load shown in Figure (d).

Switching Characteristics Over the Operating Range^[7]

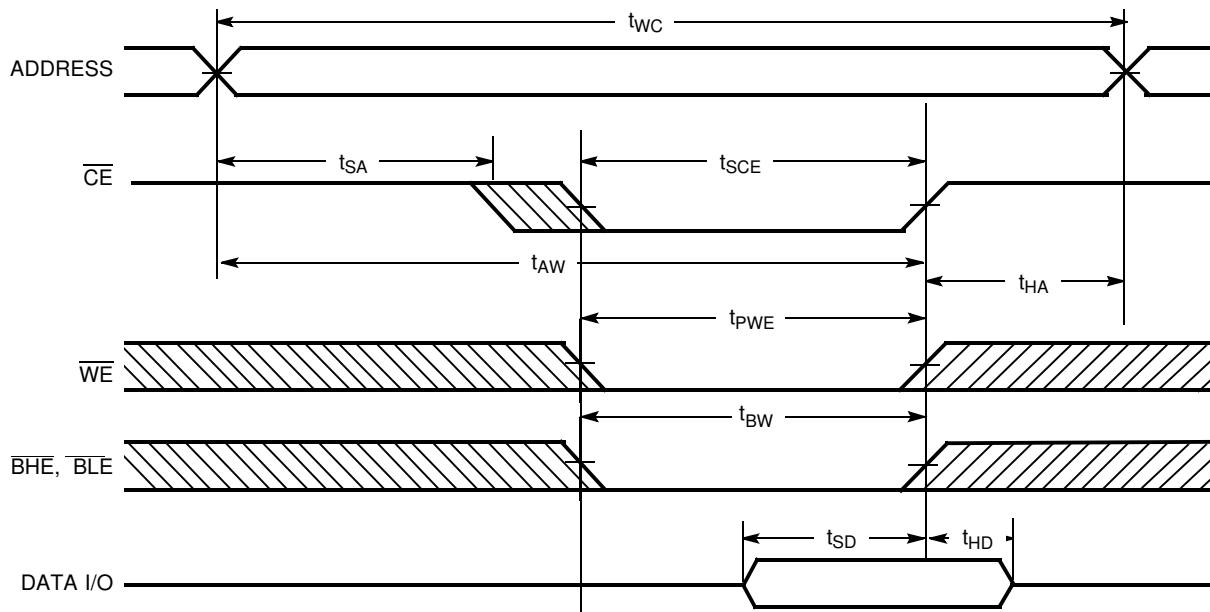
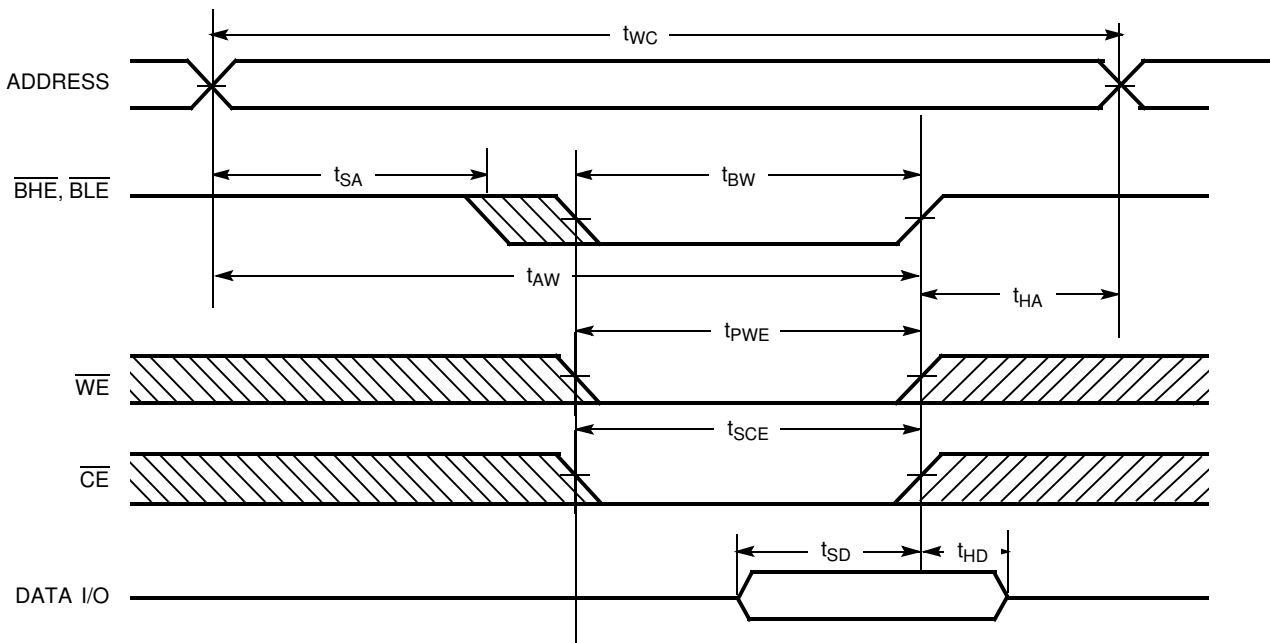
Parameter	Description	1021CV33-8		1021CV33-10		1021CV33-12		1021CV33-15		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle										
t_{RC}	Read Cycle Time	8		10		12		15		ns
t_{AA}	Address to Data Valid		8		10		12		15	ns
t_{OHA}	Data Hold from Address Change	3		3		3		3		ns
t_{ACE}	\overline{CE} LOW to Data Valid		8		10		12		15	ns
t_{DOE}	\overline{OE} LOW to Data Valid		5		5		6		7	ns
t_{LZOE}	\overline{OE} LOW to Low-Z ^[8]	0		0		0		0		ns
t_{HZOE}	\overline{OE} HIGH to High-Z ^[8, 9]		4		5		6		7	ns
t_{LZCE}	\overline{CE} LOW to Low-Z ^[8]	3		3		3		3		ns
t_{HZCE}	\overline{CE} HIGH to High-Z ^[8, 9]		4		5		6		7	ns
$t_{PU}^{[10]}$	\overline{CE} LOW to Power-Up	0		0		0		0		ns
$t_{PD}^{[10]}$	\overline{CE} HIGH to Power-Down		8		10		12		15	ns
t_{DBE}	Byte Enable to Data Valid		5		5		6		7	ns
t_{LZBE}	Byte Enable to Low-Z	0		0		0		0		ns
t_{HZBE}	Byte Disable to High-Z		4		5		6		7	ns
Write Cycle^[11]										
t_{WC}	Write Cycle Time	8		10		12		15		ns
t_{SCE}	\overline{CE} LOW to Write End	7		8		9		10		ns
t_{AW}	Address Set-up to Write End	7		8		9		10		ns
t_{HA}	Address Hold from Write End	0		0		0		0		ns
t_{SA}	Address Set-up to Write Start	0		0		0		0		ns
t_{PWE}	\overline{WE} Pulse Width	6		7		8		10		ns
t_{SD}	Data Set-up to Write End	5		5		6		8		ns
t_{HD}	Data Hold from Write End	0		0		0		0		ns
t_{LZWE}	\overline{WE} HIGH to Low-Z ^[8]	3		3		3		3		ns
t_{HZWE}	\overline{WE} LOW to High-Z ^[8, 9]		4		5		6		7	ns
t_{BW}	Byte Enable to End of Write	6		7		8		9		ns

Notes:

7. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V.
8. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any given device.
9. t_{HZOE} , t_{HZBE} , t_{HZCE} , and t_{HZWE} are specified with a load capacitance of 5 pF as in part (d) of AC Test Loads. Transition is measured ± 500 mV from steady-state voltage.
10. This parameter is guaranteed by design and is not tested.
11. The internal Write time of the memory is defined by the overlap of \overline{CE} LOW, \overline{WE} LOW and $\overline{BHE}/\overline{BLE}$ LOW. \overline{CE} , \overline{WE} and $\overline{BHE}/\overline{BLE}$ must be LOW to initiate a Write, and the transition of these signals can terminate the Write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the Write.

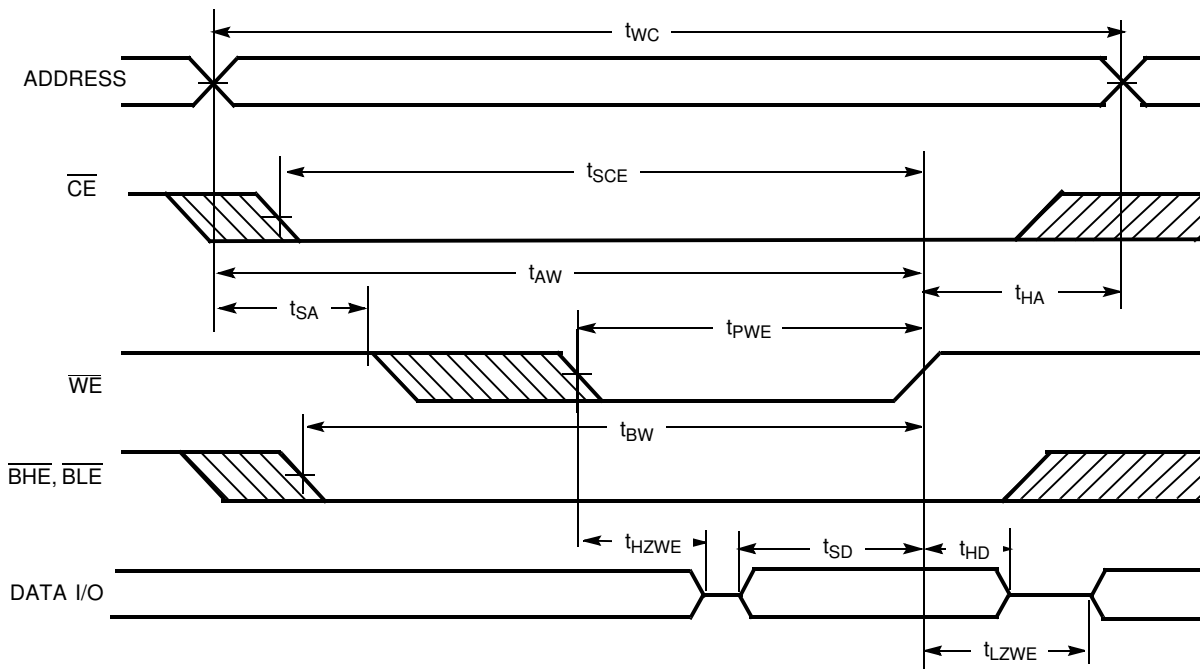
Switching Waveforms
Read Cycle No. 1^[12, 13]

Read Cycle No. 2 (\overline{OE} Controlled)^[13, 14]

Notes:

- 12. Device is continuously selected. \overline{OE} , \overline{CE} , \overline{BHE} and/or \overline{BLE} = V_{IL} .
- 13. \overline{WE} is HIGH for Read cycle.
- 14. Address valid prior to or coincident with \overline{CE} transition LOW.

Switching Waveforms (continued)
Write Cycle No. 1 ($\overline{\text{CE}}$ Controlled)^[15, 16]

Write Cycle No. 2 ($\overline{\text{BLE}}$ or $\overline{\text{BHE}}$ Controlled)

Notes:

15. Data I/O is high impedance if $\overline{\text{OE}}$ or $\overline{\text{BHE}}$ and/or $\overline{\text{BLE}} = V_{\text{IH}}$.
 16. If $\overline{\text{CE}}$ goes HIGH simultaneously with $\overline{\text{WE}}$ going HIGH, the output remains in a high-impedance state.

Switching Waveforms (continued)

Write Cycle No. 3 (\overline{WE} Controlled, LOW)

Truth Table

CE	OE	WE	BLE	BHE	I/O ₁ -I/O ₈	I/O ₉ -I/O ₁₆	Mode	Power
H	X	X	X	X	High-Z	High-Z	Power-down	Standby (I_{SB})
L	L	H	L	L	Data Out	Data Out	Read – All bits	Active (I_{CC})
			L	H	Data Out	High-Z	Read – Lower bits only	Active (I_{CC})
			H	L	High-Z	Data Out	Read – Upper bits only	Active (I_{CC})
L	X	L	L	L	Data In	Data In	Write – All bits	Active (I_{CC})
			L	H	Data In	High-Z	Write – Lower bits only	Active (I_{CC})
			H	L	High-Z	Data In	Write – Upper bits only	Active (I_{CC})
L	H	H	X	X	High-Z	High-Z	Selected, Outputs Disabled	Active (I_{CC})
L	X	X	H	H	High-Z	High-Z	Selected, Outputs Disabled	Active (I_{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
8	CY7C1021CV33-8VC	V34	44-lead (400-Mil) Molded SOJ	Commercial
	CY7C1021CV33-8ZC	Z44	44-lead TSOP Type II	
	CY7C1021CV33-8BAC	BA48A	48-ball FBGA	
10	CY7C1021CV33-10VC	V34	44-lead (400-Mil) Molded SOJ	Commercial
	CY7C1021CV33-10VI	V34	44-lead (400-Mil) Molded SOJ	Industrial
	CY7C1021CV33-10ZC	Z44	44-lead TSOP Type II	Commercial
	CY7C1021CV33-10ZI		44-lead TSOP Type II	Industrial
	CY7C1021CV33-10BAC	BA48A	48-ball FBGA	Commercial
	CY7C1021CV33-10BAI			Industrial

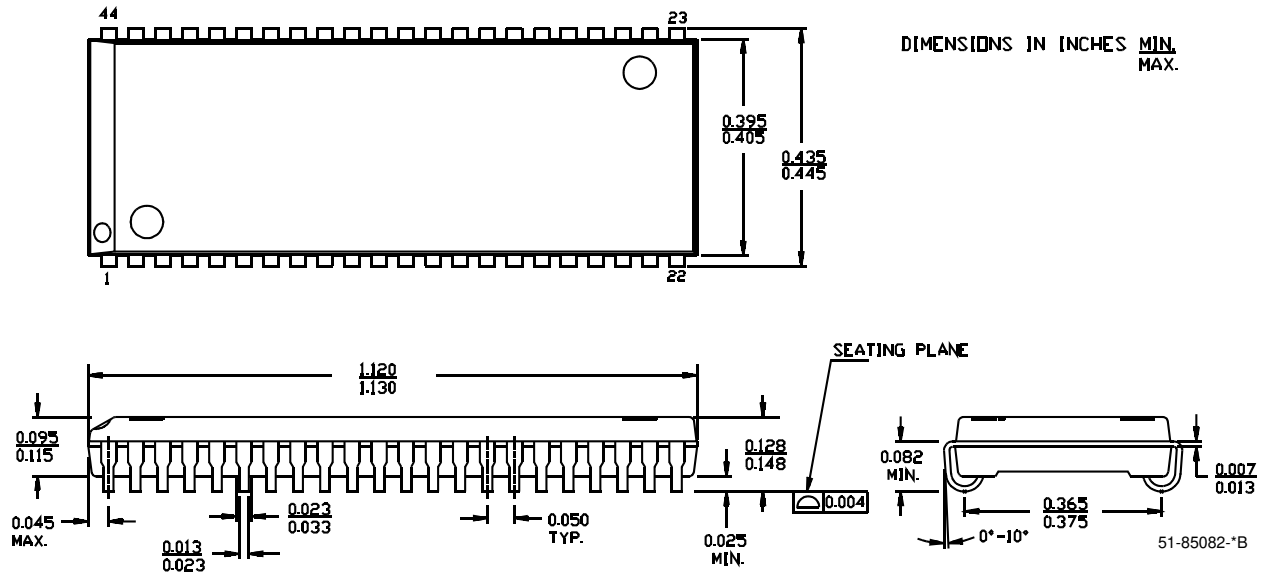
Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
12	CY7C1021CV33-12VC	V34	44-pin (400-Mil) Molded SOJ	Commercial
	CY7C1021CV33-12VI			Industrial
	CY7C1021CV33-12VE			Automotive
	CY7C1021CV33-12ZC	Z44	44-pin TSOP Type II	Commercial
	CY7C1021CV33-12ZI			Industrial
	CY7C1021CV33-12ZSE			Automotive
	CY7C1021CV33-12BAC	BA48A	48-ball FBGA	Commercial
	CY7C1021CV33-12BAI			Industrial
	CY7C1021CV33-12BAE			Automotive
15	CY7C1021CV33-15VC	V34	44-pin (400-Mil) Molded SOJ	Commercial
	CY7C1021CV33-15VI			Industrial
	CY7C1021CV33-15ZC	Z44	44-pin TSOP Type II	Commercial
	CY7C1021CV33-15ZI			Industrial
	CY7C1021CV33-15BAC	BA48A	48-ball FBGA	Commercial
	CY7C1021CV33-15BAI			Industrial
8	CY7C1021CV33-8VXC	V34	44-lead (400-Mil) Molded SOJ (Pb-Free)	Commercial
	CY7C1021CV33-8ZXC	Z44	44-lead TSOP Type II (Pb-Free)	Commercial
	CY7C1021CV33-8BAXC	BA48A	48-ball FBGA (Pb-Free)	Commercial
10	CY7C1021CV33-10VXC	V34	44-lead (400-Mil) Molded SOJ (Pb-Free)	Commercial
	CY7C1021CV33-10VXI	V34	44-lead (400-Mil) Molded SOJ (Pb-Free)	Industrial
	CY7C1021CV33-10ZXC	Z44	44-lead TSOP Type II (Pb-Free)	Commercial
	CY7C1021CV33-10ZXI	Z44	44-lead TSOP Type II (Pb-Free)	Industrial
	CY7C1021CV33-10BAXC	BA48A	48-ball FBGA (Pb-Free)	Commercial
	CY7C1021CV33-10BAXI			Industrial
12	CY7C1021CV33-12VXC	V34	44-pin (400-Mil) Molded SOJ (Pb-Free)	Commercial
	CY7C1021CV33-12VXI	V34	44-pin (400-Mil) Molded SOJ (Pb-Free)	Industrial
	CY7C1021CV33-12VXE	V34	44-pin (400-Mil) Molded SOJ (Pb-Free)	Automotive
	CY7C1021CV33-12ZXC	Z44	44-lead TSOP Type II (Pb-Free)	Commercial
	CY7C1021CV33-12ZXI	Z44	44-lead TSOP Type II (Pb-Free)	Industrial
	CY7C1021CV33-12ZSXE	Z44	44-pin TSOP Type II (Pb-Free)	Automotive
	CY7C1021CV33-12BAXC	BA48A	48-ball FBGA (Pb-Free)	Commercial
	CY7C1021CV33-12BAXI	BA48A	48-ball FBGA (Pb-Free)	Industrial
	CY7C1021CV33-12BAXE	BA48A	48-ball FBGA (Pb-Free)	Automotive
15	CY7C1021CV33-15VXC	V34	44-pin (400-Mil) Molded SOJ (Pb-Free)	Commercial
	CY7C1021CV33-15VXI	V34	44-pin (400-Mil) Molded SOJ (Pb-Free)	Industrial
	CY7C1021CV33-15ZXC	Z44	44-lead TSOP Type II (Pb-Free)	Commercial
	CY7C1021CV33-15ZXI	Z44	44-lead TSOP Type II (Pb-Free)	Industrial
	CY7C1021CV33-15BAXC	BA48A	48-ball FBGA (Pb-Free)	Commercial
	CY7C1021CV33-15BAXI			Industrial

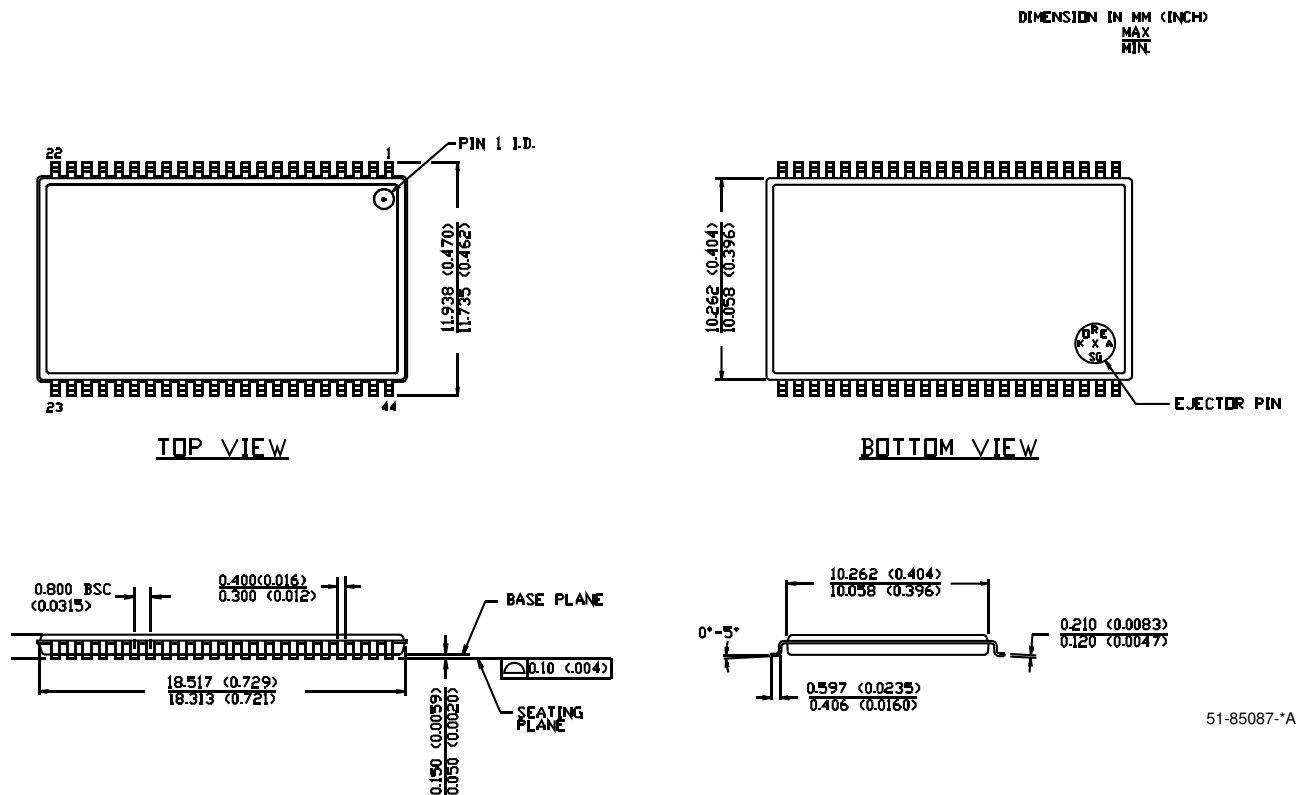
Shaded areas contain advance information. Please contact your local Cypress sales representative for availability of these parts.

Package Diagrams (continued)

44-Lead (400-Mil) Molded SOJ V34



44-pin TSOP II Z44



All products and company names mentioned in this document are the trademarks of their respective holders.

Document History Page

Document Title: CY7C1021CV33 1-Mbit (64K x 16) Static RAM Document Number: 38-05132				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	109472	12/06/01	HGK	New Data Sheet
*A	115044	05/08/02	HGK	Ram7 version C4K x 16 Async. Remove "Preliminary"
*B	115808	06/25/02	HGK	I _{SB1} and I _{CC} values changed
*C	120413	10/31/02	DFP	Updated BGA pin E4 to NC.
*D	238454	See ECN	RKF	1) Added Automotive Specs to Datasheet 2) Added Pb-Free devices in the Ordering information
*E	334398	See ECN	SYT	Added Pb-Free on page# 9 and 10