ADC32J4x Dual-Channel, 14-Bit, 50-MSPS to 160-MSPS, Analog-to-Digital Converters with JESD204B Interface

1 Features

- Dual Channel
- 14-Bit Resolution
- Single Supply: 1.8 V
- Flexible Input Clock Buffer with Divide-by-1, -2, -4
- SNR = 72.2 dBFS, SFDR = 87 dBc at f_{IN} = 70 MHz
- Ultralow Power Consumption:
  – 227 mW/Ch at 160 MSPS
- Channel Isolation: 105 dB
- Internal Dither
- JESD204B Serial Interface:
  – Subclass 0, 1, 2 Compliant up to 3.2 Gbps
  – Supports One Lane per ADC up to 160 MSPS
- Support for Multichip Synchronization
- Pin-to-Pin Compatible with 12-Bit Version (ADC32J2X)
- Package: VQFN-48 (7 mm × 7 mm)

2 Applications

- Multi-Carrier, Multi-Mode Cellular Base Stations
- Radar and Smart Antenna Arrays
- Munitions Guidance
- Motor Control Feedback
- Network and Vector Analyzers
- Communications Test Equipment
- Nondestructive Testing
- Microwave Receivers
- Software-Defined Radios (SDRs)
- Quadrature and Diversity Radio Receivers

3 Description

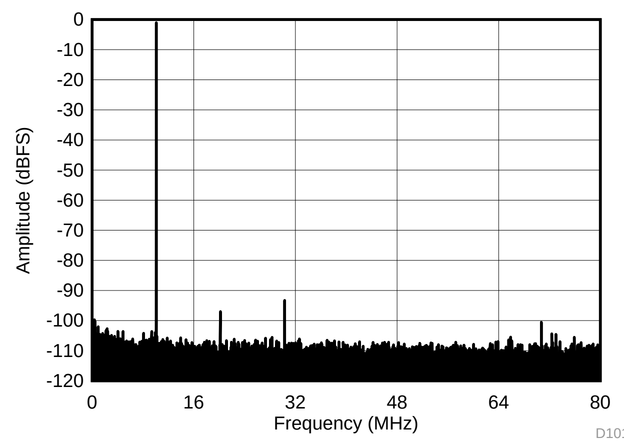
The ADC32J4x are a high-linearity, ultra-low power, dual-channel, 14-bit, 50-MSPS to 160-MSPS, analog-to-digital converter (ADC) family. The devices are designed specifically to support demanding, high input frequency signals with large dynamic range requirements. A clock input divider allows more flexibility for system clock architecture design and the SYSREF input enables complete system synchronization. The ADC32J4x family supports JESD204B interface in order to reduce the number of interface lines, thus allowing high system integration density. The JESD204B interface is a serial interface, where the data of each ADC are serialized and output over only one differential pair. An internal phase-locked loop (PLL) multiplies the incoming ADC sampling clock by 20 to derive the bit clock, which is used to serialize the 14-bit data from each channel. The devices support subclass 1 with interface speeds up to 3.2 Gbps.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
ADC32J4x	VQFN (48)	7.00 mm × 7.00 mm

(1) For all available packages, see the package option addendum at the end of the datasheet.

Performance at f_S = 160 MSPS, f_{IN} = 10 MHz (SNR = 72.5 dBFS, SFDR = 92 dBc)



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4 Revision History

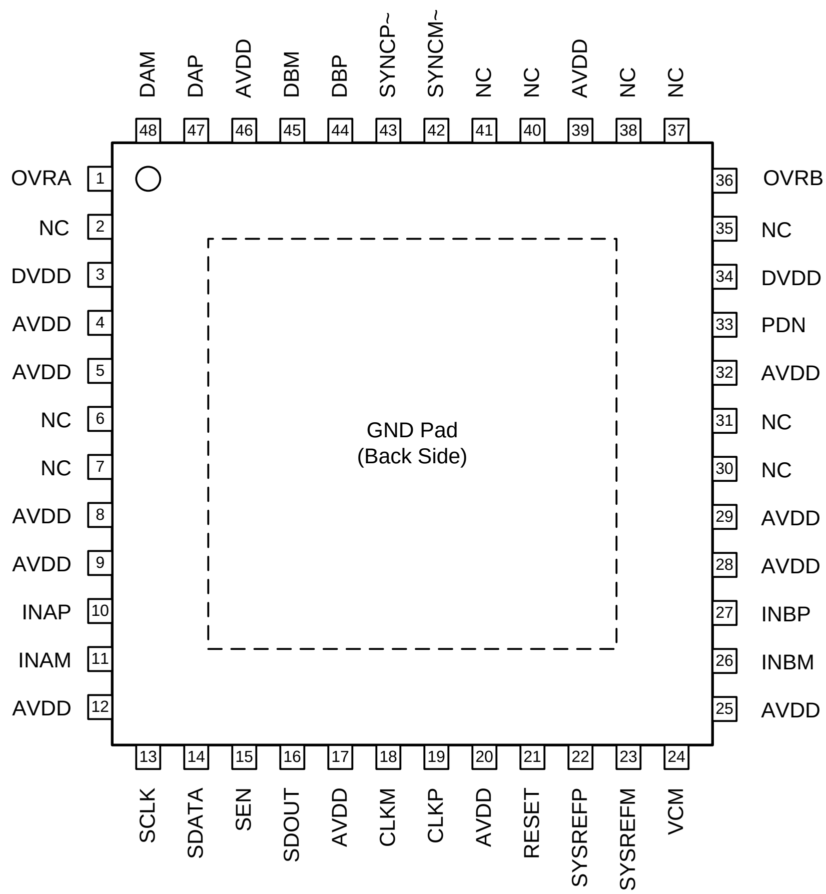
Changes from Original (May 2014) to Revision A	Page
• Changed from product preview to production data	1

5 Device Comparison Table

INTERFACE	RESOLUTION (Bits)	25 MSPS	50 MSPS	80 MSPS	125 MSPS	160 MSPS
Serial LVDS	12	ADC3221	ADC3222	ADC3223	ADC3224	—
	14	ADC3241	ADC3242	ADC3243	ADC3244	—
JESD204B	12	—	ADC32J22	ADC32J23	ADC32J24	ADC32J25
	14	—	ADC32J42	ADC32J43	ADC32J44	ADC32J45

6 Pin Configuration and Functions

RGZ Package
48-Pin VQFN
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
AVDD	4, 5, 8, 9, 12, 17, 20, 25, 28, 29, 32, 39, 46	I	Analog 1.8-V power supply
CLKM	18	I	Negative differential clock input for the ADC
CLKP	19	I	Positive differential clock input for the ADC
DAM	48	O	Negative serial JESD204B output for channel A
DAP	47	O	Positive serial JESD204B output for channel A
DBM	45	O	Negative serial JESD204B output for channel B
DBP	44	O	Positive serial JESD204B output for channel B
DVDD	3,34	I	Digital 1.8-V power supply
GND	PowerPAD™	I	Ground, 0 V
INAM	11	I	Negative differential analog input for channel A
INAP	10	I	Positive differential analog input for channel A
INBM	26	I	Negative differential analog input for channel B
INBP	27	I	Positive differential analog input for channel B
NC	2, 6, 7, 30, 31, 35, 37, 38, 40, 41	—	Do not connect
OVRA	1	O	Overrange indicator for channel A
OVRB	36	O	Overrange indicator for channel B
PDN	33	I	Power-down control. This pin has an internal 150-kΩ pulldown resistor.
RESET	21	I	Hardware reset; active high. This pin has an internal 150-kΩ pulldown resistor.
SCLK	13	I	Serial interface clock input. This pin has an internal 150-kΩ pulldown resistor.
SDATA	14	I	Serial Interface data input. This pin has an internal 150-kΩ pulldown resistor.
SDOUT	16	O	Serial interface data output
SEN	15	I	Serial interface enable. This pin has an internal 150-kΩ pullup resistor to AVDD.
SYNCM~	42	I	Positive JESD204B SYNC~ input
SYNCP~	43	I	Negative JESD204B SYNC~ input
SYSREFM	23	I	Negative external SYSREF input
SYSREFP	22	I	Positive external SYSREF input
VCM	24	O	Common-mode voltage output for analog inputs

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
Supply voltage range, AVDD		–0.3	2.1	V
Supply voltage range, DVDD		–0.3	2.1	V
Voltage applied to input pins:	INAP, INBP, INCP, INDP, INAM, INBM, INCM, INDM	–0.3	Minimum (AVDD + 0.3, 2.1)	V
	CLKP, CLKM[2]	–0.3	Minimum (AVDD + 0.3, 2.1)	V
	SYSREFP, SYSREFM, SYNCP~, SYNCM~	–0.3	Minimum (AVDD + 0.3, 2.1)	V
	SCLK, SEN, SDATA, RESET, PDN	–0.3	3.6	V
Temperature	Operating free-air, T_A	–40	85	°C
	Operating junction, T_J		125	°C
	Storage, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) When AVDD is turned off, TI recommends switching off the input clock (or ensuring the voltage on CLKP, CLKM is less than |0.3 V|). This configuration prevents the ESD protection diodes at the clock input pins from turning on.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1]	±2000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions[1]

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
SUPPLIES						
AVDD	Analog supply voltage range		1.7	1.8	1.9	V
DVDD	Digital supply voltage range		1.7	1.8	1.9	V
ANALOG INPUT						
V_{ID}	Differential input voltage	For input frequencies < 450 MHz		2		V_{PP}
		For input frequencies < 600 MHz		1		V_{PP}
V_{IC}	Input common-mode voltage			VCM ± 0.025		V
CLOCK INPUT						
	Input clock frequency	Sampling clock frequency	15		160[2]	MSPS
	Input clock amplitude (differential)	Sine wave, ac-coupled	0.2	1.5		V
		LVPECL, ac-coupled		1.6		V
		LVDS, ac-coupled		0.7		V
	Input clock duty cycle		35%	50%	65%	
	Input clock common-mode voltage			0.95		V
DIGITAL OUTPUTS						
C_{LOAD}	Maximum external load capacitance from each output pin to GND			3.3		pF
R_{LOAD}	Single-ended load resistance			50		Ω

(1) After power-up, to reset the device for the first time, only use the RESET pin; see the *Register Initialization* section.
(2) With the clock divider enabled by default for divide-by-1. Maximum sampling clock frequency for the divide-by-4 option is 640 MSPS.

7.4 Thermal Information

THERMAL METRIC(1)		ADC32J4x RGZ (VQFN) 48 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	25.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	18.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	3.0	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

Typical values are over the operating free-air temperature range, at T_A = 25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = 85°C, maximum sampling rate, 50% clock duty cycle, AVDD = DVDD = 1.8 V, and –1-dBFS differential input, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUT						
	Differential input full-scale			2.0		V_{PP}
r_i	Input resistance	Differential at dc		6.5		kΩ
c_i	Input capacitance	Differential at dc		5.2		pF
$V_{OC(VCM)}$	VCM common-mode voltage output			0.95		V
	VCM output current capability			10		mA
	Input common-mode current	Per analog input pin		1.5		µA/MSPS
	Analog input bandwidth (3 dB)	50-Ω differential source driving a 50-Ω termination across INP, INM		450		MHz
DC ACCURACY						
E_O	Offset error		–20		20	mV
$E_{G(REF)}$	Gain error as a result of internal reference inaccuracy alone		–3		3	%FS
$E_{G(CHAN)}$	Gain error of channel alone			±1		%FS
$\alpha_{(EGCHAN)}$	Temperature coefficient of $E_{G(CHAN)}$			–0.017		Δ%FS/Ch
CHANNEL-TO-CHANNEL ISOLATION						
	Crosstalk(1)	f_{IN} = 10 MHz		105		dB
		f_{IN} = 100 MHz		105		dB
		f_{IN} = 200 MHz		105		dB
		f_{IN} = 230 MHz		105		dB
		f_{IN} = 300 MHz		105		dB

(1) Crosstalk is measured with a –1-dBFS input signal on aggressor channel and no input on victim channel.

7.6 Electrical Characteristics: ADC32J44, ADC32J45

Typical values are over the operating free-air temperature range, at T_A = 25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = 85°C, maximum sampling rate, 50% clock duty cycle, AVDD = DVDD = 1.8 V, and –1-dBFS differential input, unless otherwise noted.

PARAMETER	ADC32J44			ADC32J45			UNIT
	MIN	TYP	MAX	MIN	TYP	MAX	
ADC clock frequency			125			160	MSPS
Resolution	14			14			Bits
1.8-V analog supply current		177	292		192	302	mA
1.8-V digital supply current		46	65		56	80	mA
Total power dissipation		401	535		454	560	mW
Global power-down dissipation		5			5		mW
Wake-up time from global power-down		85			85		us
Standby power-down dissipation		112			118		mW
Wake-up time from standby power-down		35			35		µs

7.7 Electrical Characteristics: ADC32J42, ADC32J43

Typical values are over the operating free-air temperature range, at T_A = 25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = 85°C, maximum sampling rate, 50% clock duty cycle, AVDD = DVDD = 1.8 V, and –1-dBFS differential input, unless otherwise noted.

PARAMETER	ADC32J42			ADC32J43			UNIT
	MIN	TYP	MAX	MIN	TYP	MAX	
ADC clock frequency			50			80	MSPS
Resolution	14			14			Bits
1.8-V analog supply current		134	267		152	272	mA
1.8-V digital supply current		22	45		31	46	mA
Total power dissipation		281	435		329	450	mW
Global power-down dissipation		5			5		mW
Wake-up time from global power-down		85			85		us
Standby power-down dissipation		99			105		mW
Wake-up time from standby power-down		35			35		µs

7.8 AC Performance: ADC32J45

Typical values are over the operating free-air temperature range, at T_A = 25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = 85°C, ADC sampling rate = 160 MSPS, 50% clock duty cycle, AVDD = DVDD = 1.8 V, and –1-dBFS differential input, unless otherwise noted.

PARAMETER		TEST CONDITIONS	ADC32J45 (f_S = 160 MSPS) DITHER ON MIN	DITHER ON TYP	DITHER ON MAX	DITHER OFF MIN	DITHER OFF TYP	DITHER OFF MAX	UNIT
DYNAMIC AC CHARACTERISTICS									
SNR	Signal-to-noise ratio	f_{IN} = 10 MHz		72.5			72.8		dBFS
		f_{IN} = 70 MHz	70.2	71.7			72.0		
		f_{IN} = 100 MHz		71.3			71.6		
		f_{IN} = 170 MHz		70.1			70.7		
		f_{IN} = 230 MHz		68.9			69.5		
NSD	Noise spectral density (averaged across Nyquist zone)	f_{IN} = 10 MHz		151.5			151.8		dBFS/Hz
		f_{IN} = 70 MHz	–149.5	150.7			151.0		
		f_{IN} = 100 MHz		150.3			150.6		
		f_{IN} = 170 MHz		149.1			149.7		
		f_{IN} = 230 MHz		147.9			148.5		
SINAD	Signal-to-noise and distortion ratio	f_{IN} = 10 MHz		72.3			72.6		dBFS
		f_{IN} = 70 MHz	68.3	71.5			71.8		
		f_{IN} = 100 MHz		71.0			71.2		
		f_{IN} = 170 MHz		69.6			70.1		
		f_{IN} = 230 MHz		68.3			68.4		
ENOB	Effective number of bits	f_{IN} = 10 MHz		11.7			11.8		Bits
		f_{IN} = 70 MHz	11.1	11.6			11.6		
		f_{IN} = 100 MHz		11.5			11.5		
		f_{IN} = 170 MHz		11.3			11.3		
		f_{IN} = 230 MHz		11.0			11.1		
SFDR	Spurious-free dynamic range	f_{IN} = 10 MHz		90			88		dBc
		f_{IN} = 70 MHz	81	85			85		
		f_{IN} = 100 MHz		85			84		
		f_{IN} = 170 MHz		84			83		
		f_{IN} = 230 MHz		81			80		
HD2	Second-order harmonic distortion	f_{IN} = 10 MHz		90			91		dBc
		f_{IN} = 70 MHz	81	91			92		
		f_{IN} = 100 MHz		88			86		
		f_{IN} = 170 MHz		84			83		
		f_{IN} = 230 MHz		81			80		
HD3	Third-order harmonic distortion	f_{IN} = 10 MHz		91			88		dBc
		f_{IN} = 70 MHz	81	85			84		
		f_{IN} = 100 MHz		85			84		
		f_{IN} = 170 MHz		91			86		
		f_{IN} = 230 MHz		86			87		
Non HD2, HD3	Spurious-free dynamic range (excluding HD2, HD3)	f_{IN} = 10 MHz		98			95		dBc
		f_{IN} = 70 MHz	87	99			95		
		f_{IN} = 100 MHz		97			94		
		f_{IN} = 170 MHz		92			91		
		f_{IN} = 230 MHz		91			89		

AC Performance: ADC32J45 (continued)

Typical values are over the operating free-air temperature range, at T_A = 25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = 85°C, ADC sampling rate = 160 MSPS, 50% clock duty cycle, AVDD = DVDD = 1.8 V, and –1-dBFS differential input, unless otherwise noted.

PARAMETER		TEST CONDITIONS	ADC32J45 (f_S = 160 MSPS)						UNIT
			DITHER ON			DITHER OFF			
			MIN	TYP	MAX	MIN	TYP	MAX	
THD	Total harmonic distortion	f_{IN} = 10 MHz		87			84		dBc
		f_{IN} = 70 MHz	78	84			83		
		f_{IN} = 100 MHz		83			82		
		f_{IN} = 170 MHz		82			80		
		f_{IN} = 230 MHz		79			77		
IMD3	Two-tone, third-order intermodulation distortion	f_{IN1} = 45 MHz, f_{IN2} = 50 MHz		90			90		dBFS
		f_{IN1} = 185 MHz, f_{IN2} = 190 MHz		86			86		
DNL	Differential nonlinearity	f_{IN} = 70 MHz		±0.3			±0.3		LSBs
INL	Integrated nonlinearity	f_{IN} = 70 MHz		±1.5			±1.5		LSBs

7.9 AC Performance: ADC32J44

Typical values are over the operating free-air temperature range, at T_A = 25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = 85°C, ADC sampling rate = 125 MSPS, 50% clock duty cycle, AVDD = DVDD = 1.8 V, and –1-dBFS differential input, unless otherwise noted.

PARAMETER		TEST CONDITIONS	ADC32J44 (f_S = 125 MSPS)						UNIT
			DITHER ON			DITHER OFF			
			MIN	TYP	MAX	MIN	TYP	MAX	
DYNAMIC AC CHARACTERISTICS									
SNR	Signal-to-noise ratio	f_{IN} = 10 MHz		72.6			72.8		dBFS
		f_{IN} = 70 MHz	70.8	72.3			72.5		
		f_{IN} = 100 MHz		72.1			72.3		
		f_{IN} = 170 MHz		70.1			71.7		
		f_{IN} = 230 MHz		70.0			70.8		
NSD	Noise spectral density (averaged across Nyquist zone)	f_{IN} = 10 MHz		150.6			150.8		dBFS/Hz
		f_{IN} = 70 MHz	–148.8	150.3			150.5		
		f_{IN} = 100 MHz		150.1			150.3		
		f_{IN} = 170 MHz		148.1			149.7		
		f_{IN} = 230 MHz		148.0			148.8		
SINAD	Signal-to-noise and distortion ratio	f_{IN} = 10 MHz		72.5			72.7		dBFS
		f_{IN} = 70 MHz	68.6	72.2			72.4		
		f_{IN} = 100 MHz		72.0			72.2		
		f_{IN} = 170 MHz		70.7			71.4		
		f_{IN} = 230 MHz		69.5			70.2		
ENOB	Effective number of bits	f_{IN} = 10 MHz		11.8			11.8		Bits
		f_{IN} = 70 MHz	11.1	11.7			11.7		
		f_{IN} = 100 MHz		11.7			11.7		
		f_{IN} = 170 MHz		11.4			11.6		
		f_{IN} = 230 MHz		11.2			11.4		
SFDR	Spurious-free dynamic range	f_{IN} = 10 MHz		94			92		dBc
		f_{IN} = 70 MHz	81	93			91		
		f_{IN} = 100 MHz		93			90		
		f_{IN} = 170 MHz		85			84		
		f_{IN} = 230 MHz		82			81		
HD2	Second-order harmonic distortion	f_{IN} = 10 MHz		95			92		dBc
		f_{IN} = 70 MHz	81	94			94		
		f_{IN} = 100 MHz		93			91		
		f_{IN} = 170 MHz		85			84		
		f_{IN} = 230 MHz		82			81		
HD3	Third-order harmonic distortion	f_{IN} = 10 MHz		96			92		dBc
		f_{IN} = 70 MHz	82	93			90		
		f_{IN} = 100 MHz		93			90		
		f_{IN} = 170 MHz		88			88		
		f_{IN} = 230 MHz		91			93		
Non HD2, HD3	Spurious-free dynamic range (excluding HD2, HD3)	f_{IN} = 10 MHz		99			96		dBc
		f_{IN} = 70 MHz	87	99			96		
		f_{IN} = 100 MHz		98			96		
		f_{IN} = 170 MHz		98			95		
		f_{IN} = 230 MHz		96			91		

AC Performance: ADC32J44 (continued)

Typical values are over the operating free-air temperature range, at T_A = 25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = 85°C, ADC sampling rate = 125 MSPS, 50% clock duty cycle, AVDD = DVDD = 1.8 V, and –1-dBFS differential input, unless otherwise noted.

PARAMETER		TEST CONDITIONS	ADC32J44 (f_S = 125 MSPS)						UNIT
			DITHER ON			DITHER OFF			
			MIN	TYP	MAX	MIN	TYP	MAX	
THD	Total harmonic distortion	f_{IN} = 10 MHz		91			87		dBc
		f_{IN} = 70 MHz	78	90			87		
		f_{IN} = 100 MHz		90			87		
		f_{IN} = 170 MHz		83			82		
		f_{IN} = 230 MHz		80			79		
IMD3	Two-tone, third-order intermodulation distortion	f_{IN1} = 45 MHz, f_{IN2} = 50 MHz		91			91		dBFS
		f_{IN1} = 185 MHz, f_{IN2} = 190 MHz		86			86		
DNL	Differential nonlinearity	f_{IN} = 70 MHz		±0.3			±0.3		LSBs
INL	Integrated nonlinearity	f_{IN} = 70 MHz		±1.5			±1.5		LSBs

7.10 AC Performance: ADC32J43

Typical values are over the operating free-air temperature range, at T_A = 25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = 85°C, ADC sampling rate = 80 MSPS, 50% clock duty cycle, AVDD = DVDD = 1.8 V, and –1-dBFS differential input, unless otherwise noted.

PARAMETER		TEST CONDITIONS	ADC32J43 (f_S = 80 MSPS) DITHER ON MIN	DITHER ON TYP	DITHER ON MAX	DITHER OFF MIN	DITHER OFF TYP	DITHER OFF MAX	UNIT
DYNAMIC AC CHARACTERISTICS									
SNR	Signal-to-noise ratio	f_{IN} = 10 MHz		72.3			72.6		dBFS
		f_{IN} = 70 MHz	70.8	72.2			72.4		
		f_{IN} = 100 MHz		72.0			72.2		
		f_{IN} = 170 MHz		71.4			71.8		
		f_{IN} = 230 MHz		70.6			71.0		
NSD	Noise spectral density (averaged across Nyquist zone)	f_{IN} = 10 MHz		148.4			148.7		dBFS/Hz
		f_{IN} = 70 MHz	–146.8	148.2			148.4		
		f_{IN} = 100 MHz		148.0			148.2		
		f_{IN} = 170 MHz		147.4			147.8		
		f_{IN} = 230 MHz		146.6			147.0		
SINAD	Signal-to-noise and distortion ratio	f_{IN} = 10 MHz		72.3			72.5		dBFS
		f_{IN} = 70 MHz	68.6	72.2			72.2		
		f_{IN} = 100 MHz		71.9			72.0		
		f_{IN} = 170 MHz		71.0			71.4		
		f_{IN} = 230 MHz		69.9			70.2		
ENOB	Effective number of bits	f_{IN} = 10 MHz		11.7			11.8		Bits
		f_{IN} = 70 MHz	11.1	11.7			11.7		
		f_{IN} = 100 MHz		11.6			11.7		
		f_{IN} = 170 MHz		11.5			11.6		
		f_{IN} = 230 MHz		11.3			11.4		
SFDR	Spurious-free dynamic range	f_{IN}= 10 MHz		96			91		dBc
		f_{IN} = 70 MHz	82	95			90		
		f_{IN} = 100 MHz		91			88		
		f_{IN} = 170 MHz		85			84		
		f_{IN} = 230 MHz		81			80		
HD2	Second-order harmonic distortion	f_{IN} = 10 MHz		96			95		dBc
		f_{IN} = 70 MHz	81	98			96		
		f_{IN} = 100 MHz		93			91		
		f_{IN} = 170 MHz		85			84		
		f_{IN} = 230 MHz		81			80		
HD3	Third-order harmonic distortion	f_{IN} = 10 MHz		95			93		dBc
		f_{IN} = 70 MHz	83	92			92		
		f_{IN} = 100 MHz		91			88		
		f_{IN} = 170 MHz		92			91		
		f_{IN} = 230 MHz		83			83		
Non HD2, HD3	Spurious-free dynamic range (excluding HD2, HD3)	f_{IN} = 10 MHz		99			93		dBc
		f_{IN} = 70 MHz	87	99			93		
		f_{IN} = 100 MHz		97			92		
		f_{IN} = 170 MHz		97			93		
		f_{IN} = 230 MHz		95			92		

AC Performance: ADC32J43 (continued)

Typical values are over the operating free-air temperature range, at T_A = 25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = 85°C, ADC sampling rate = 80 MSPS, 50% clock duty cycle, AVDD = DVDD = 1.8 V, and –1-dBFS differential input, unless otherwise noted.

PARAMETER		TEST CONDITIONS	ADC32J43 (f_S = 80 MSPS)						UNIT
			DITHER ON			DITHER OFF			
			MIN	TYP	MAX	MIN	TYP	MAX	
THD	Total harmonic distortion	f_{IN} = 10 MHz		93			87		dBc
		f_{IN} = 70 MHz	78	93			87		
		f_{IN} = 100 MHz		87			85		
		f_{IN} = 170 MHz		83			82		
		f_{IN} = 230 MHz		79			77		
IMD3	Two-tone, third-order intermodulation distortion	f_{IN1} = 45 MHz, f_{IN2} = 50 MHz		90			90		dBFS
		f_{IN1} = 185 MHz, f_{IN2} = 190 MHz		89			89		
DNL	Differential nonlinearity	f_{IN} = 70 MHz		±0.3			±0.3		LSBs
INL	Integrated nonlinearity	f_{IN} = 70 MHz		±1.5			±1.5		LSBs

7.11 AC Performance: ADC32J42

Typical values are over the operating free-air temperature range, at T_A = 25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = 85°C, ADC sampling rate = 50 MSPS, 50% clock duty cycle, AVDD = DVDD = 1.8 V, and –1-dBFS differential input, unless otherwise noted.

PARAMETER		TEST CONDITIONS	ADC32J42 (f_S = 50 MSPS)						UNIT
			DITHER ON			DITHER OFF			
			MIN	TYP	MAX	MIN	TYP	MAX	
DYNAMIC AC CHARACTERISTICS									
SNR	Signal-to-noise ratio	f_{IN} = 10 MHz	71.3	72.2			72.5		dBFS
		f_{IN} = 70 MHz		71.8			72.1		
		f_{IN} = 100 MHz		71.8			72.0		
		f_{IN} = 170 MHz		71.1			71.5		
		f_{IN} = 230 MHz		69.1			69.4		
NSD	Noise spectral density (averaged across Nyquist zone)	f_{IN} = 10 MHz		146.1			146.5		dBFS/Hz
		f_{IN} = 70 MHz		145.8			146.1		
		f_{IN} = 100 MHz		145.8			146.0		
		f_{IN} = 170 MHz		145.1			145.5		
		f_{IN} = 230 MHz		143.1			143.4		
SINAD	Signal-to-noise and distortion ratio	f_{IN} = 10 MHz	69.1	72.1			72.3		dBFS
		f_{IN} = 70 MHz		71.8			71.9		
		f_{IN} = 100 MHz		71.7			71.8		
		f_{IN} = 170 MHz		70.8			71.1		
		f_{IN} = 230 MHz		68.4			68.7		
ENOB	Effective number of bits	f_{IN} = 10 MHz	11.2	11.7			11.7		Bits
		f_{IN} = 70 MHz		11.6			11.7		
		f_{IN} = 100 MHz		11.6			11.6		
		f_{IN} = 170 MHz		11.5			11.5		
		f_{IN} = 230 MHz		11.1			11.1		
SFDR	Spurious-free dynamic range	f_{IN} = 10 MHz	84.5	95			93		dBc
		f_{IN} = 70 MHz		95			90		
		f_{IN} = 100 MHz		91			89		
		f_{IN} = 170 MHz		85			84		
		f_{IN} = 230 MHz		81			80		
HD2	Second-order harmonic distortion	f_{IN} = 10 MHz	84.5	95			94		dBc
		f_{IN} = 70 MHz		97			96		
		f_{IN} = 100 MHz		92			92		
		f_{IN} = 170 MHz		85			84		
		f_{IN} = 230 MHz		81			80		
HD3	Third-order harmonic distortion	f_{IN} = 10 MHz	84.5	102			93		dBc
		f_{IN} = 70 MHz		95			90		
		f_{IN} = 100 MHz		91			89		
		f_{IN} = 170 MHz		88			88		
		f_{IN} = 230 MHz		82			83		
Non HD2, HD3	Spurious-free dynamic range (excluding HD2, HD3)	f_{IN} = 10 MHz	87	98			91		dBc
		f_{IN} = 70 MHz		94			92		
		f_{IN} = 100 MHz		91			91		
		f_{IN} = 170 MHz		96			92		
		f_{IN} = 230 MHz		93			91		

AC Performance: ADC32J42 (continued)

Typical values are over the operating free-air temperature range, at T_A = 25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = 85°C, ADC sampling rate = 50 MSPS, 50% clock duty cycle, AVDD = DVDD = 1.8 V, and –1-dBFS differential input, unless otherwise noted.

PARAMETER		TEST CONDITIONS	ADC32J42 (f_S = 50 MSPS) DITHER ON MIN	DITHER ON TYP	DITHER ON MAX	DITHER OFF MIN	DITHER OFF TYP	DITHER OFF MAX	UNIT
THD	Total harmonic distortion	f_{IN} = 10 MHz	79.5	92			90		dBc
		f_{IN} = 70 MHz		91			87		
		f_{IN} = 100 MHz		88			85		
		f_{IN} = 170 MHz		83			82		
		f_{IN} = 230 MHz		78			78		
IMD3	Two-tone, third-order intermodulation distortion	f_{IN1} = 45 MHz, f_{IN2} = 50 MHz		90			90		dBFS
		f_{IN1} = 185 MHz, f_{IN2} = 190 MHz		86			86		
DNL	Differential nonlinearity	f_{IN} = 70 MHz		±0.3			±0.3		LSBs
INL	Integrated nonlinearity	f_{IN} = 70 MHz		±1.5			±1.5		LSBs

7.12 Digital Characteristics

The dc specifications refer to the condition where the digital outputs are not switching, but are permanently at a valid logic level 0 or 1. AVDD = DVDD = 1.8 V and –1-dBFS differential input, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL INPUTS (RESET, SCLK, SEN, SDATA, PDN)(1)						
V_{IH}	High-level input voltage	All digital inputs support 1.8-V and 3.3-V logic levels	1.2			V
V_{IL}	Low-level input voltage	All digital inputs support 1.8-V and 3.3-V logic levels			0.4	V
I_{IH}	High-level input current	SEN		0		µA
		RESET, SCLK, SDATA, PDN		10		µA
I_{IL}	Low-level input current	SEN		10		µA
		RESET, SCLK, SDATA, PDN		0		µA
DIGITAL INPUTS (SYNCP~, SYNCM~, SYSREFP, SYSREFM)						
V_{IH}	High-level input voltage			1.3		V
V_{IL}	Low-level input voltage			0.5		V
$V_{(CM\_DIG)}$	Common-mode voltage for SYNC~ and SYSREF			0.95		V
DIGITAL OUTPUTS (SDOUT, OVRA, OVRB)						
V_{OH}	High-level output voltage		DVDD – 0.1	DVDD		V
V_{OL}	Low-level output voltage				0.1	V
DIGITAL OUTPUTS (JESD204B Interface: DxP, DxM)(2)						
V_{OH}	High-level output voltage			AVDD		V
V_{OL}	Low-level output voltage			AVDD – 0.4		V
V_{OD}	Output differential voltage			0.4		V
V_{OC}	Output common-mode voltage			AVDD – 0.2		V
	Transmitter short-circuit current	Transmitter pins shorted to any voltage between –0.25 V and 1.45 V	–100		100	mA
z_{os}	Single-ended output impedance			50		Ω
	Output capacitance	Output capacitance inside the device, from either output to ground		2		pF

(1) The RESET, SCLK, SDATA, and PDN pins have a 150-kΩ (typical) internal pulldown resistor to ground, and the SEN pin has a 150-kΩ (typical) pullup resistor to AVDD.
(2) 50-Ω, single-ended external termination to 1.8 V.

7.13 Timing Requirements

Typical values are at 25°C, AVDD = DVDD = 1.8 V, and –1-dBFS differential input, unless otherwise noted. Minimum and maximum values are across the full temperature range: T_{MIN} = –40°C to T_{MAX} = 85°C. See Figure 143.

			MIN	TYP	MAX	UNITS
SAMPLE TIMING REQUIREMENTS						
	Aperture delay		0.85	1.25	1.65	ns
	Aperture delay matching	Between four channels on the same device		±70		ps
		Between two devices at the same temperature and supply voltage		±150		ps
	Aperture jitter			200		f_S rms
	Wake-up time	Time to valid data after coming out of STANDBY mode		35	100	µs
		Time to valid data after coming out of global power-down		85	300	µs
$t_{SU\_SYNC\sim}$	Setup time for SYNC~ referenced to input clock rising edge		1			ns
$t_{H\_SYNC\sim}$	Hold time for SYNC~ referenced to input clock rising edge		100			ps
t_{SU_SYSREF}	Setup time for SYSREF referenced to input clock rising edge		1			ns
t_{H_SYSREF}	Hold time for SYSREF referenced to input clock rising edge		100			ps
CML OUTPUT TIMING REQUIREMENTS						
	Unit interval		312.5		1667	ps
	Serial output data rate				3.2	Gbps
	Total jitter: 3.125 Gbps (20X mode, f_S = 156.25 MSPS)			0.3		$_{P-P}$UI
t_R, t_F	Data rise time, data fall time: rise and fall times measured from 20% to 80%, differential output waveform, 600 Mbps ≤ bit rate ≤ 3.125 Gbps			105		ps

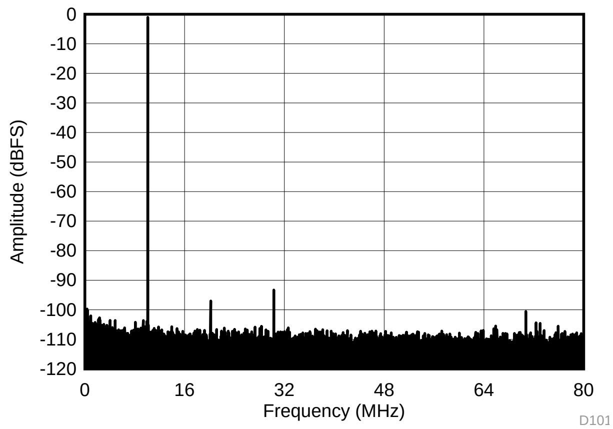
Table 1. Latency in Different Modes(1)(2)

MODE	PARAMETER	LATENCY (N Cycles)	TYPICAL DATA DELAY (t_D, ns)
20X	ADC latency	17	0.29 × t_S + 3
	Normal OVR latency	9	0.5 × t_S + 2
	Fast OVR latency	7	0.5 × t_S + 2
	From SYNC~ falling edge to CGS phase(3)	15	0.3 × t_S + 4
	From SYNC~ rising edge to ILA sequence(4)	17	0.3 × t_S + 4
40X	ADC latency	16	0.85 × t_S + 3.9
	Normal OVR latency	9	0.5 × t_S + 2
	Fast OVR latency	7	0.5 × t_S + 2
	From SYNC~ falling edge to CGS phase(3)	14	0.9 × t_S + 4
	From SYNC~ rising edge to ILA sequence(4)	12	0.9 × t_S + 4

(1) Overall latency = latency + t_D.
(2) t_S is the time period of the ADC conversion clock.
(3) Latency is specified for subclass 2. In subclass 0, the SYNC~ falling edge to CGS phase latency is 16 clock cycles in 10X mode and 15 clock cycles in 20X mode.
(4) Latency is specified for subclass 2. In subclass 0, the SYNC~ rising edge to ILA sequence latency is 11 clock cycles in 10X mode and 11 clock cycles in 20X mode.

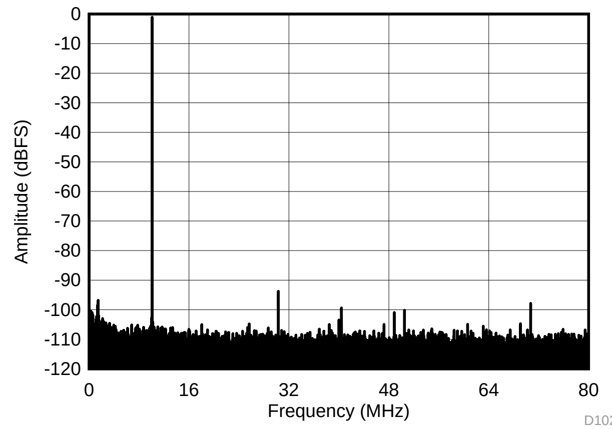
7.14 Typical Characteristics: ADC32J45

Typical values are at T_A= 25°C, ADC sampling rate = 160 MSPS, 50% clock duty cycle, AVDD = DVDD = 1.8 V, –1-dBFS differential input, 2-V_{PP} full-scale, 32k-point FFT, dither enabled, and special modes written, unless otherwise noted.



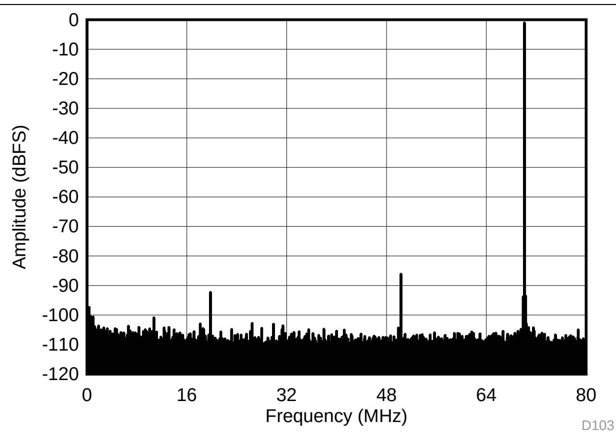
f_S = 160 MSPS, SNR = 72.4 dBFS, f_{IN} = 10 MHz, SFDR = 92.3 dBc

Figure 1. FFT for 10-MHz Input Signal (Dither On)



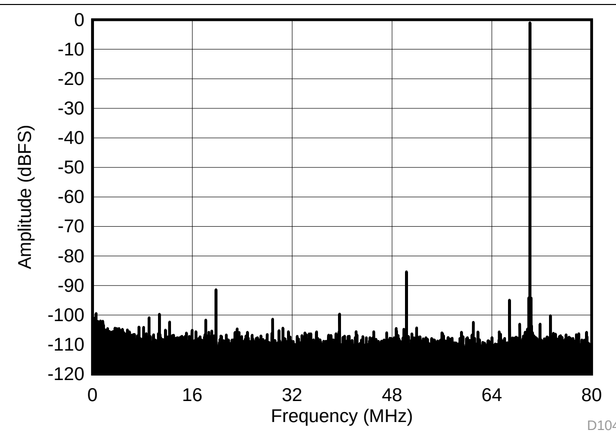
f_S = 160 MSPS, SNR = 72.7 dBFS, f_{IN} = 10 MHz, SFDR = 92.7 dBc

Figure 2. FFT for 10-MHz Input Signal (Dither Off)



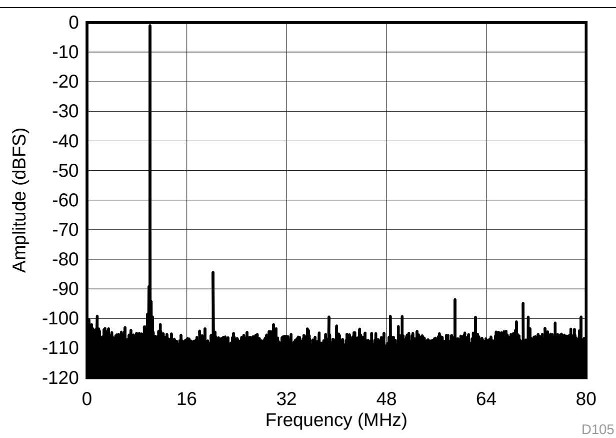
f_S = 160 MSPS, SNR = 71.7 dBFS, f_{IN} = 70 MHz, SFDR = 86 dBc

Figure 3. FFT for 70-MHz Input Signal (Dither On)



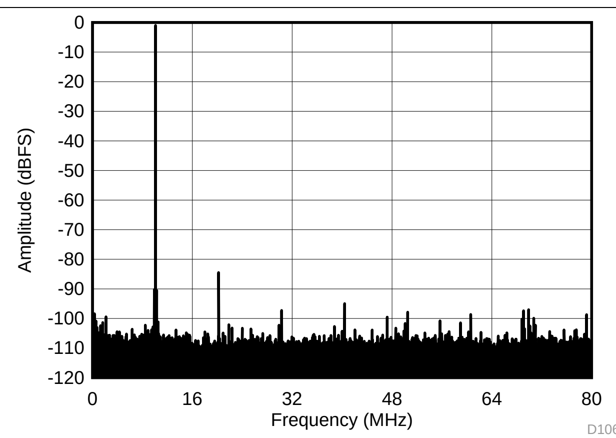
f_S = 160 MSPS, SNR = 72.1 dBFS, f_{IN} = 70 MHz, SFDR = 85 dBc

Figure 4. FFT for 70-MHz Input Signal (Dither Off)



f_S = 160 MSPS, SNR = 70.6 dBFS, f_{IN} = 170 MHz, SFDR = 85 dBc

Figure 5. FFT for 170-MHz Input Signal (Dither On)

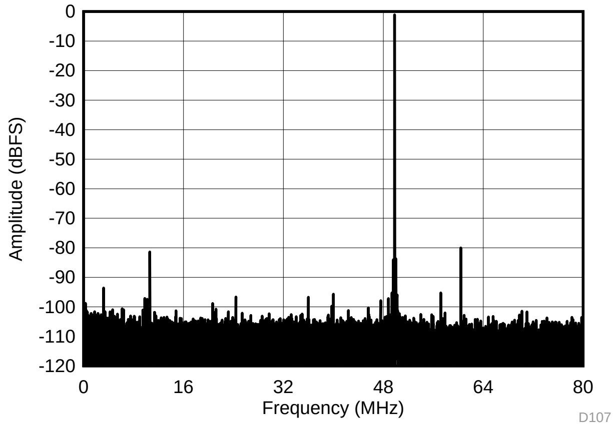


f_S = 160 MSPS, SNR = 71.4 dBFS, f_{IN} = 170 MHz, SFDR = 84 dBc

Figure 6. FFT for 170-MHz Input Signal (Dither Off)

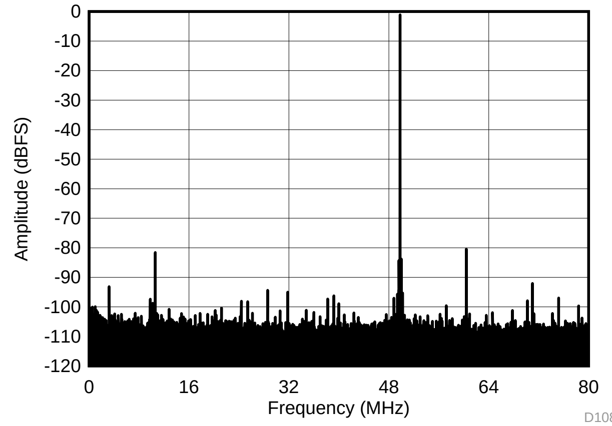
Typical Characteristics: ADC32J45 (continued)

Typical values are at T_A= 25°C, ADC sampling rate = 160 MSPS, 50% clock duty cycle, AVDD = DVDD = 1.8 V, –1-dBFS differential input, 2-V_{PP} full-scale, 32k-point FFT, dither enabled, and special modes written, unless otherwise noted.



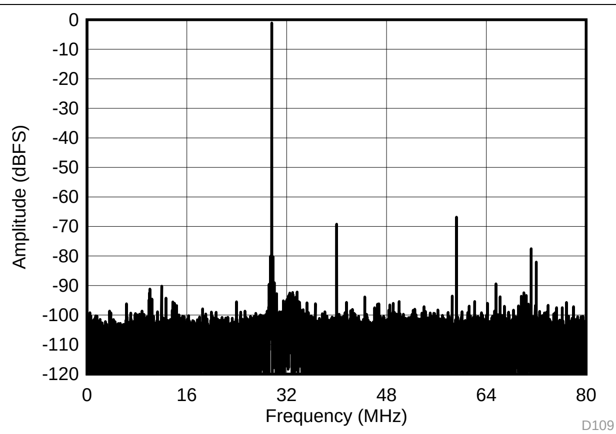
f_S = 160 MSPS, SNR = 69.3 dBFS, f_{IN} = 270 MHz, SFDR = 78.9 dBc

Figure 7. FFT for 270-MHz Input Signal (Dither On)



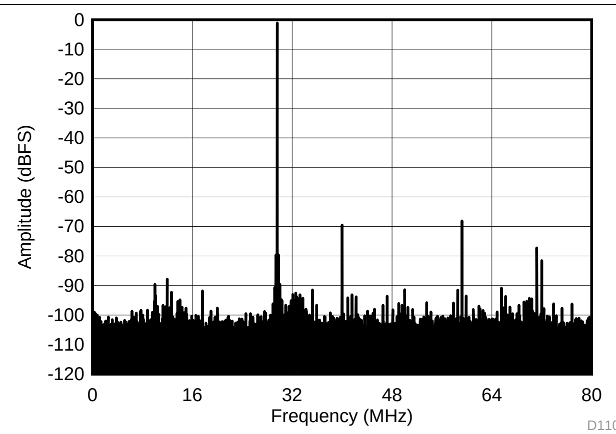
f_S = 160 MSPS, SNR = 69.9 dBFS, f_{IN} = 270 MHz, SFDR = 79.3 dBc

Figure 8. FFT for 270-MHz Input Signal (Dither Off)



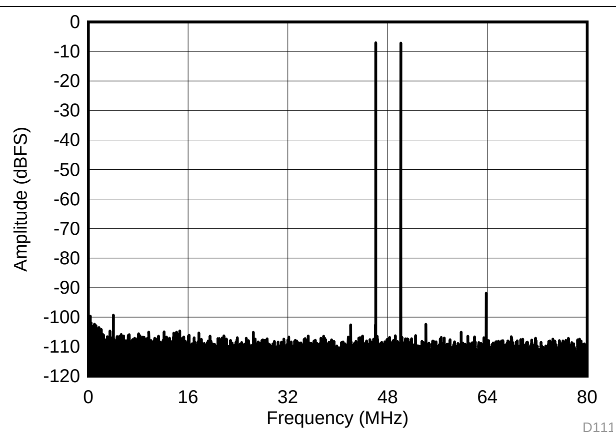
f_S = 160 MSPS, SNR = 63.2 dBFS, f_{IN} = 450 MHz, SFDR = 65.7 dBc

Figure 9. FFT for 450-MHz Input Signal (Dither On)



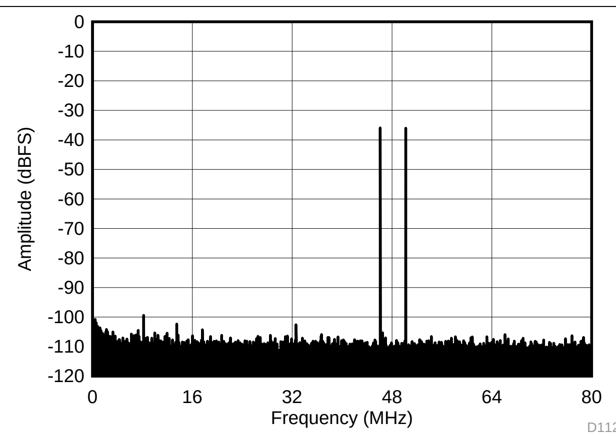
f_S = 160 MSPS, SNR = 63.8 dBFS, f_{IN} = 450 MHz, SFDR = 67 dBc

Figure 10. FFT for 450-MHz Input Signal (Dither Off)



f_S = 160 MSPS, IMD = 92 dBFS, f_{IN1} = 46 MHz, f_{IN2} = 50 MHz

Figure 11. FFT for Two-Tone Input Signal (–7 dBFS at 46 MHz and 50 MHz)

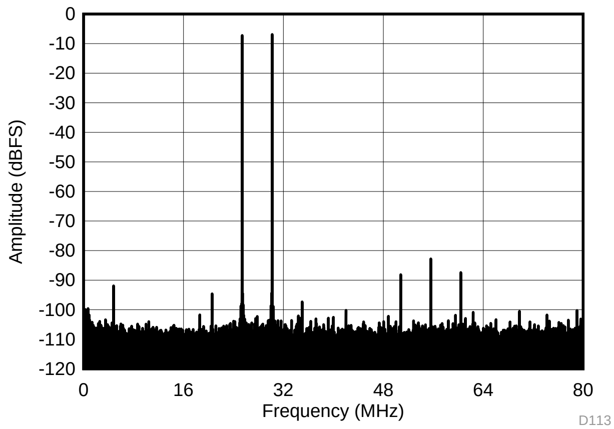


f_S = 160 MSPS, IMD = 99 dBFS, f_{IN1} = 46 MHz, f_{IN2} = 50 MHz

Figure 12. FFT for Two-Tone Input Signal (–36 dBFS at 46 MHz and 50 MHz)

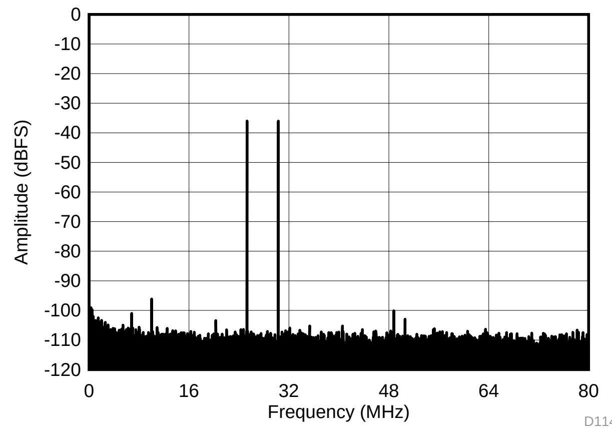
Typical Characteristics: ADC32J45 (continued)

Typical values are at T_A= 25°C, ADC sampling rate = 160 MSPS, 50% clock duty cycle, AVDD = DVDD = 1.8 V, –1-dBFS differential input, 2-V_{PP} full-scale, 32k-point FFT, dither enabled, and special modes written, unless otherwise noted.



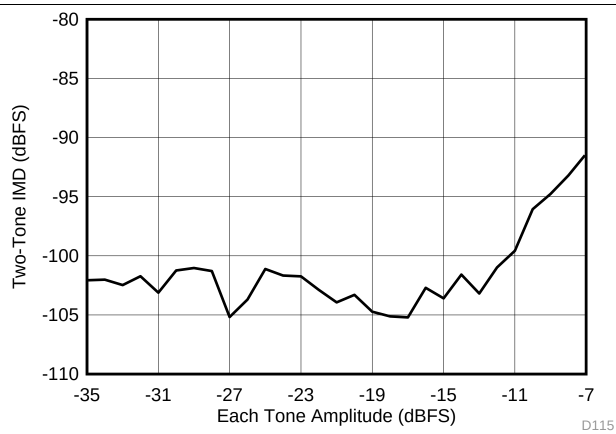
f_S = 160 MSPS, IMD = 87 dBFS, f_{IN1} = 185 MHz, f_{IN2} = 190 MHz

Figure 13. FFT for Two-Tone Input Signal (–7 dBFS at 185 MHz and 190 MHz)



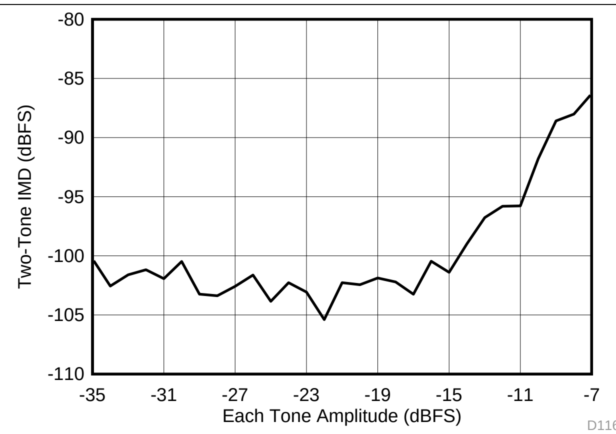
f_S = 160 MSPS, IMD = 100 dBFS, f_{IN1} = 185 MHz, f_{IN2} = 190 MHz

Figure 14. FFT for Two-Tone Input Signal (–36 dBFS at 185 MHz and 190 MHz)



f_S = 160 MSPS, f_{IN1} = 46 MHz, f_{IN2} = 50 MHz

Figure 15. Intermodulation Distortion vs Input Amplitude (46 MHz and 50 MHz)



f_S = 160 MSPS, f_{IN1} = 185 MHz, f_{IN2} = 190 MHz

Figure 16. Intermodulation Distortion vs Input Amplitude (185 MHz and 190 MHz)

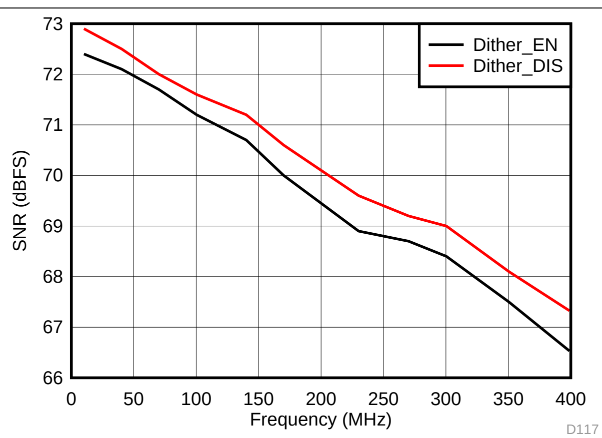


Figure 17. Signal-to-Noise Ratio vs Input Frequency

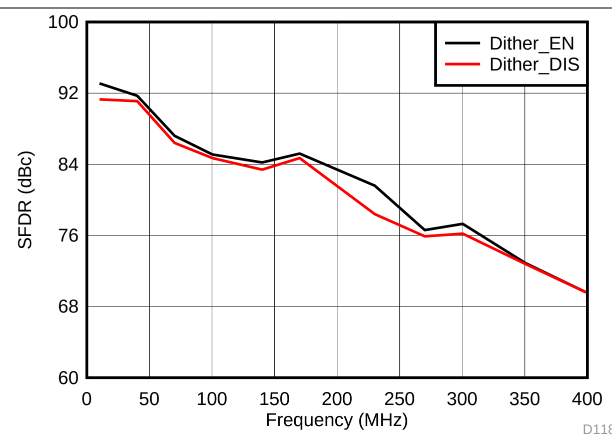


Figure 18. Spurious-Free Dynamic Range vs Input Frequency

Typical Characteristics: ADC32J45 (continued)

Typical values are at T_A= 25°C, ADC sampling rate = 160 MSPS, 50% clock duty cycle, AVDD = DVDD = 1.8 V, –1-dBFS differential input, 2-V_{PP} full-scale, 32k-point FFT, dither enabled, and special modes written, unless otherwise noted.

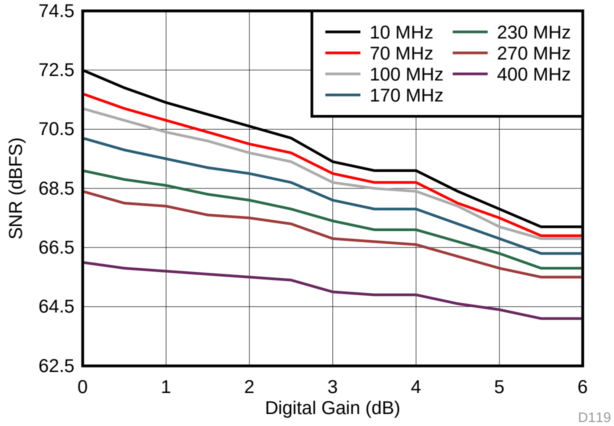


Figure 19. Signal-to-Noise Ratio vs Digital Gain and Input Frequency

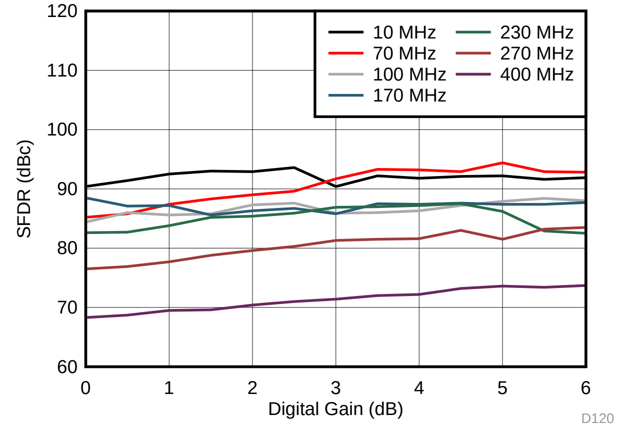


Figure 20. Spurious-Free Dynamic Range vs Digital Gain and Input Frequency

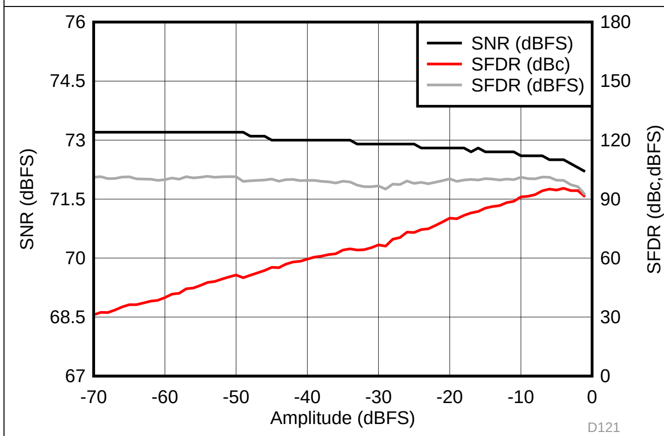


Figure 21. Performance vs Input Amplitude (30 MHz)

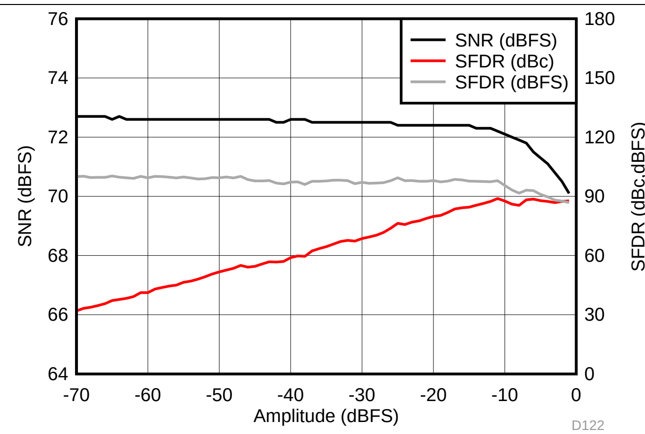


Figure 22. Performance vs Input Amplitude (170 MHz)

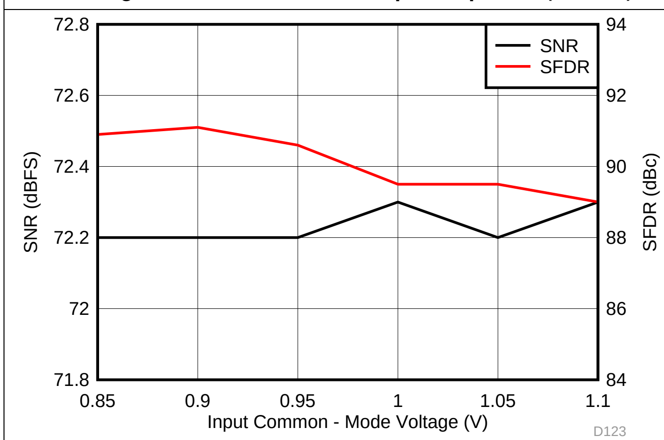


Figure 23. Performance vs Input Common-Mode Voltage (30 MHz)

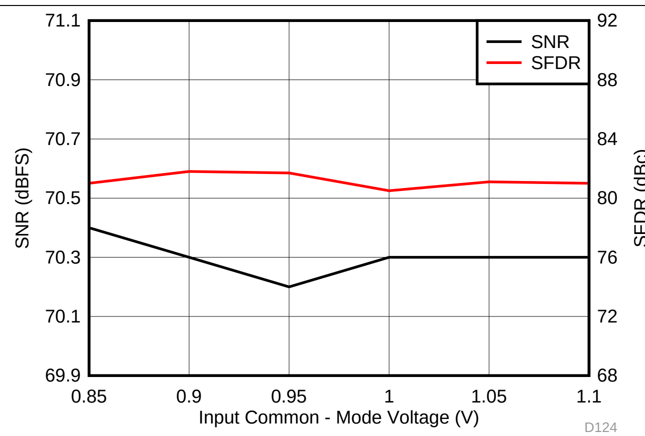


Figure 24. Performance vs Input Common-Mode Voltage (170 MHz)

Typical Characteristics: ADC32J45 (continued)

Typical values are at T_A= 25°C, ADC sampling rate = 160 MSPS, 50% clock duty cycle, AVDD = DVDD = 1.8 V, –1-dBFS differential input, 2-V_{PP} full-scale, 32k-point FFT, dither enabled, and special modes written, unless otherwise noted.

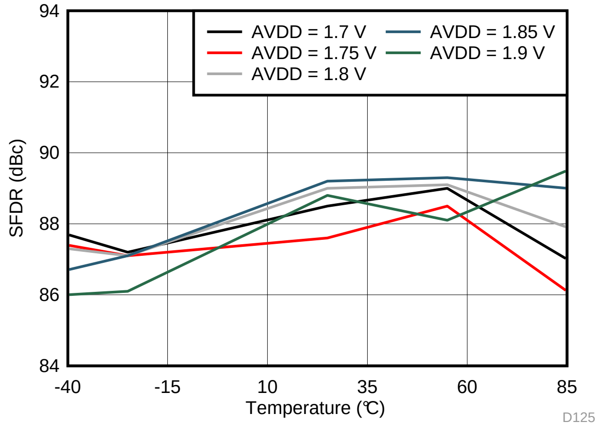


Figure 25. Spurious-Free Dynamic Range vs AVDD Supply and Temperature

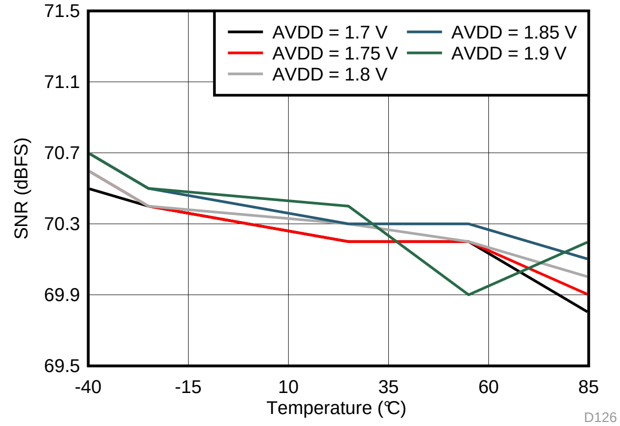


Figure 26. Signal-to-Noise Ratio vs AVDD Supply and Temperature

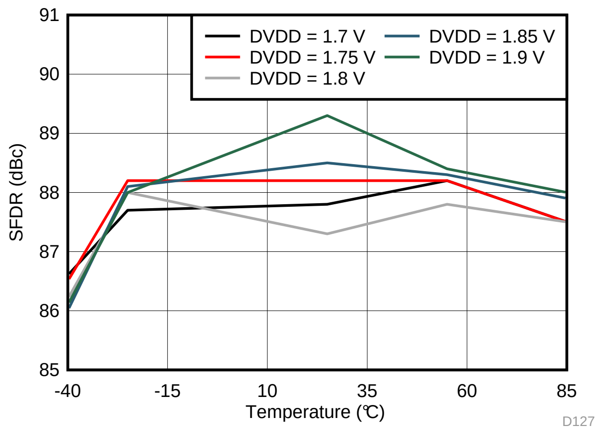


Figure 27. Spurious-Free Dynamic Range vs DVDD Supply and Temperature

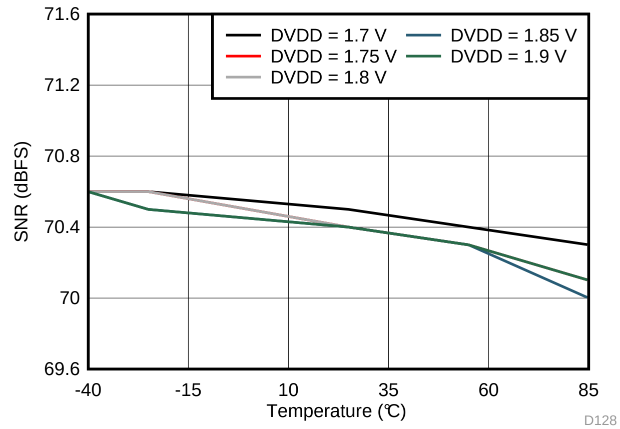


Figure 28. Signal-to-Noise Ratio vs DVDD Supply and Temperature

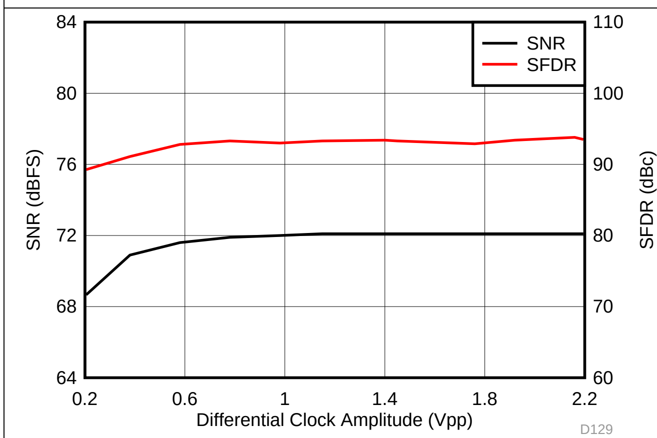


Figure 29. Performance vs Clock Amplitude (40 MHz)

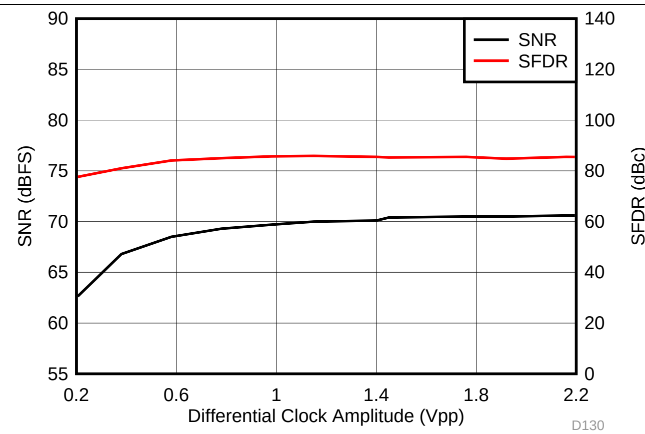


Figure 30. Performance vs Clock Amplitude (150 MHz)

Typical Characteristics: ADC32J45 (continued)

Typical values are at T_A= 25°C, ADC sampling rate = 160 MSPS, 50% clock duty cycle, AVDD = DVDD = 1.8 V, –1-dBFS differential input, 2-V_{PP} full-scale, 32k-point FFT, dither enabled, and special modes written, unless otherwise noted.

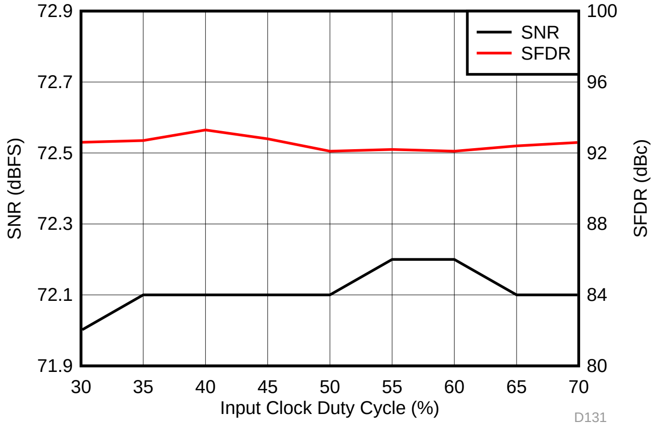


Figure 31. Performance vs Clock Duty Cycle (40 MHz)

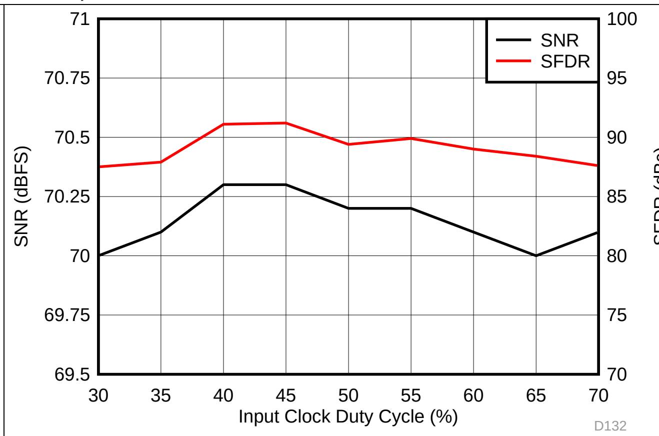
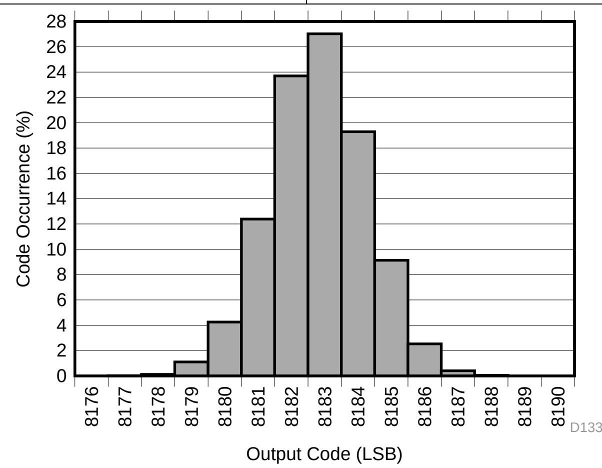


Figure 32. Performance vs Clock Duty Cycle (150 MHz)

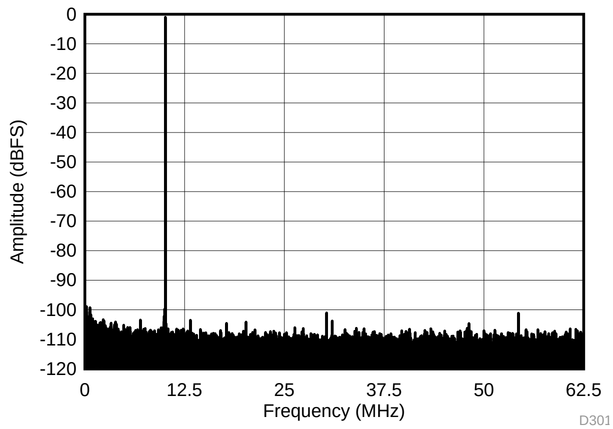


RMS noise = 1.3 LSBs

Figure 33. Idle Channel Histogram

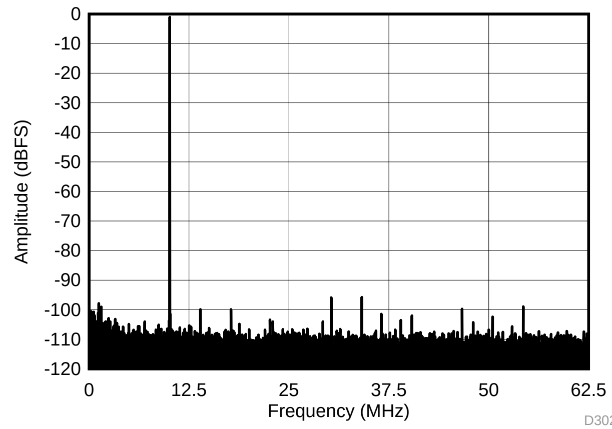
7.15 Typical Characteristics: ADC32J44

Typical values are at T_A= 25°C, ADC sampling rate = 125 MSPS, 50% clock duty cycle, AVDD = DVDD = 1.8 V, –1-dBFS differential input, 2-V_{PP} full-scale, and 32k-point FFT, unless otherwise noted.



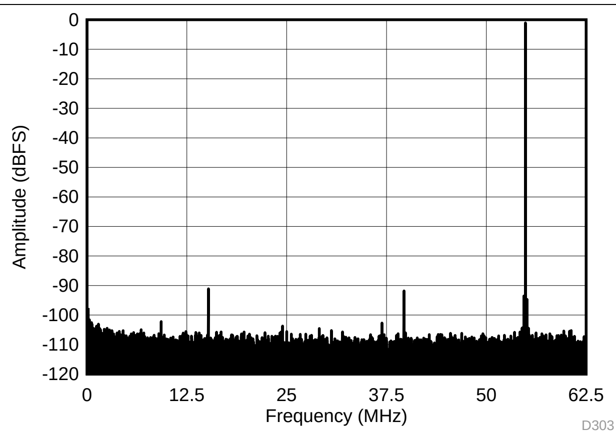
f_S = 125 MSPS, SNR = 72.4 dBFS, f_{IN} = 10 MHz, SFDR = 98.3 dBc

Figure 34. FFT for 10-MHz Input Signal (Dither On)



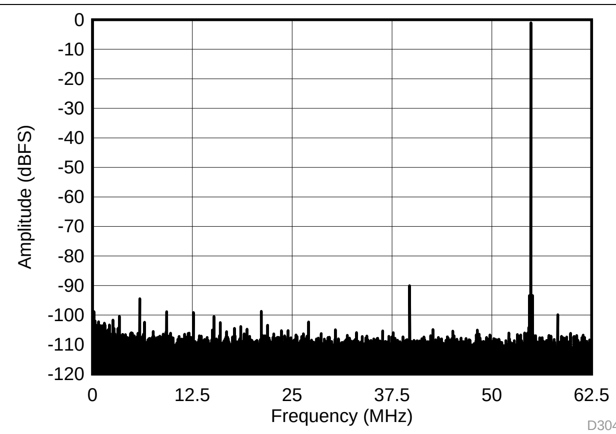
f_S = 125 MSPS, SNR = 72.7 dBFS, f_{IN} = 10 MHz, SFDR = 94.7 dBc

Figure 35. FFT for 10-MHz Input Signal (Dither Off)



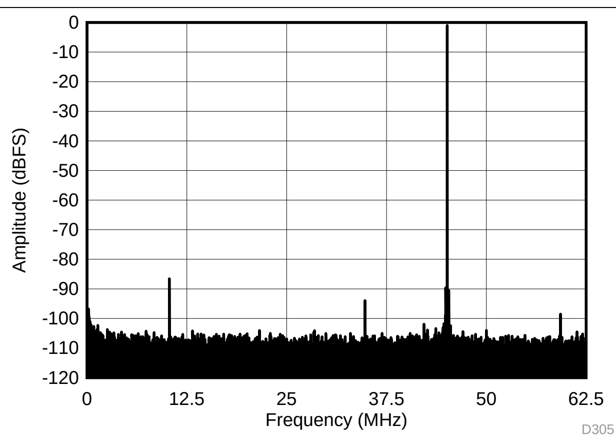
f_S = 125 MSPS, SNR = 71.9 dBFS, f_{IN} = 70 MHz, SFDR = 91 dBc

Figure 36. FFT for 70-MHz Input Signal (Dither On)



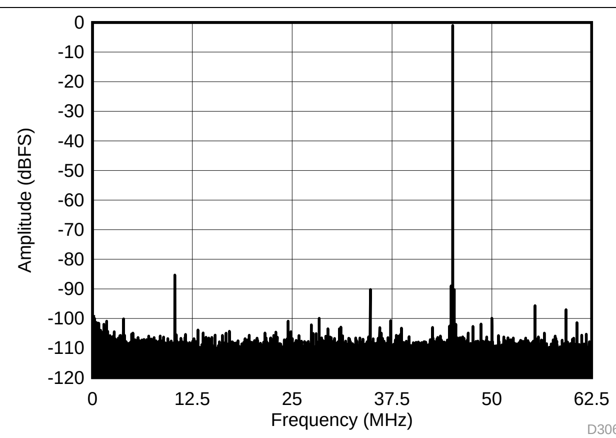
f_S = 125 MSPS, SNR = 72.3 dBFS, f_{IN} = 70 MHz, SFDR = 90 dBc

Figure 37. FFT for 70-MHz Input Signal (Dither Off)



f_S = 125 MSPS, SNR = 71 dBFS, f_{IN} = 170 MHz, SFDR = 86 dBc

Figure 38. FFT for 170-MHz Input Signal (Dither On)

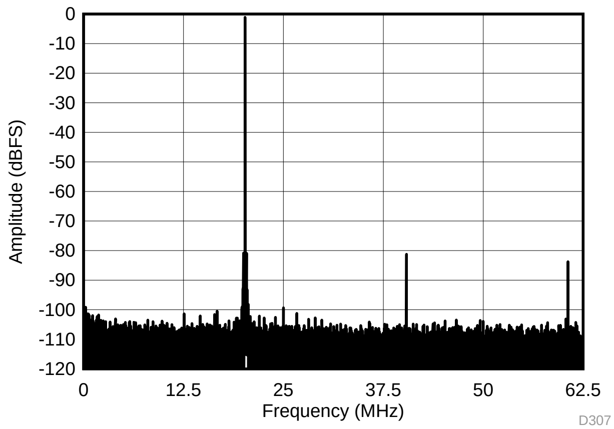


f_S = 125 MSPS, SNR = 71.9 dBFS, f_{IN} = 70 MHz, SFDR = 85 dBc

Figure 39. FFT for 170-MHz Input Signal (Dither Off)

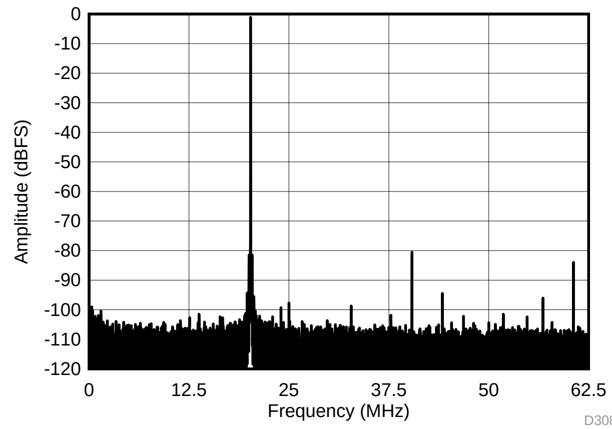
Typical Characteristics: ADC32J44 (continued)

Typical values are at T_A= 25°C, ADC sampling rate = 125 MSPS, 50% clock duty cycle, AVDD = DVDD = 1.8 V, –1-dBFS differential input, 2-V_{PP} full-scale, and 32k-point FFT, unless otherwise noted.



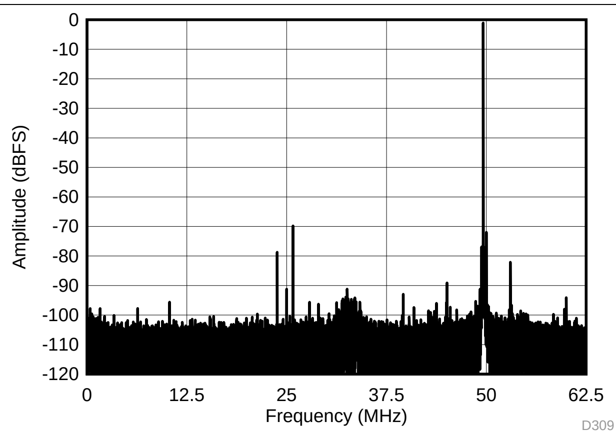
f_S = 125 MSPS, SNR = 70.4 dBFS, f_{IN} = 270 MHz, SFDR = 80.1 dBc

Figure 40. FFT for 270-MHz Input Signal (Dither On)



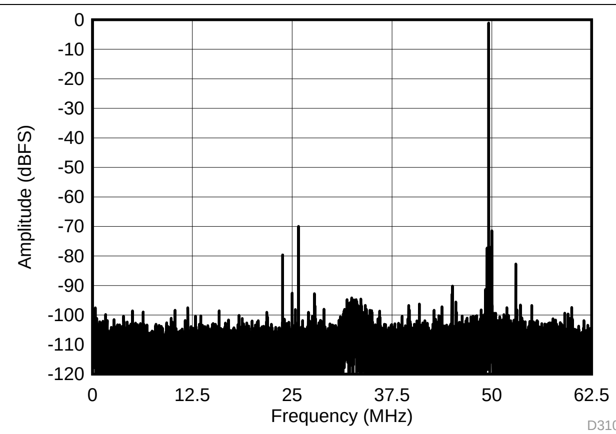
f_S = 125 MSPS, SNR = 70.5 dBFS, f_{IN} = 270 MHz, SFDR = 79.4 dBc

Figure 41. FFT for 270-MHz Input Signal (Dither Off)



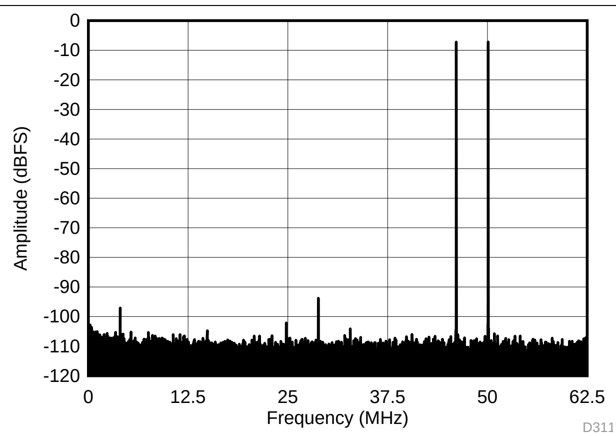
f_S = 125 MSPS, SNR = 64.2 dBFS, f_{IN} = 450 MHz, SFDR = 68.7 dBc

Figure 42. FFT for 450-MHz Input Signal (Dither On)



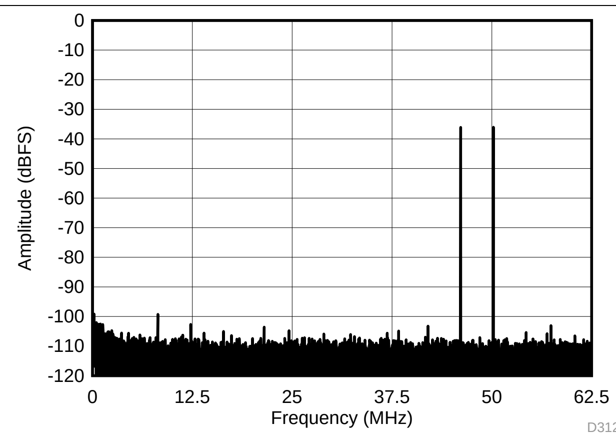
f_S = 125 MSPS, SNR = 64.6 dBFS, f_{IN} = 450 MHz, SFDR = 68.9 dBc

Figure 43. FFT for 450-MHz Input Signal (Dither Off)



f_S = 125 MSPS, IMD = 93 dBFS, f_{IN1} = 46 MHz, f_{IN2} = 50 MHz

Figure 44. FFT for Two-Tone Input Signal (–7 dBFS at 46 MHz and 50 MHz)

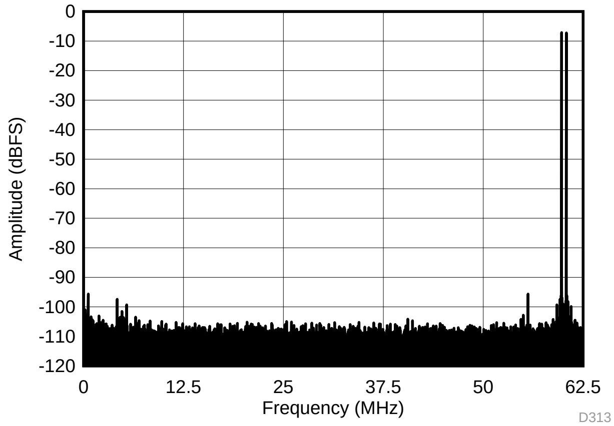


f_S = 125 MSPS, IMD = 101 dBFS, f_{IN1} = 46 MHz, f_{IN2} = 50 MHz

Figure 45. FFT for Two-Tone Input Signal (–36 dBFS at 46 MHz and 50 MHz)

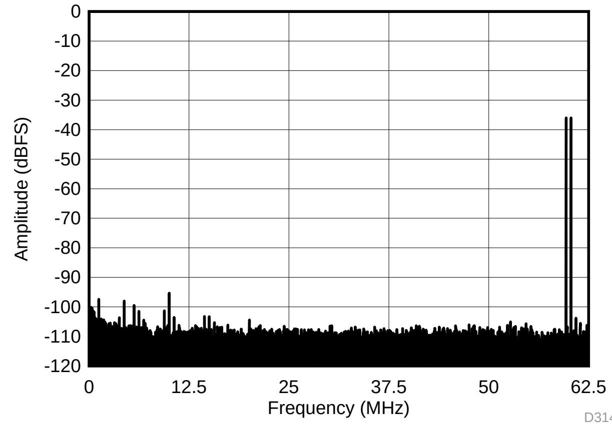
Typical Characteristics: ADC32J44 (continued)

Typical values are at T_A= 25°C, ADC sampling rate = 125 MSPS, 50% clock duty cycle, AVDD = DVDD = 1.8 V, –1-dBFS differential input, 2-V_{PP} full-scale, and 32k-point FFT, unless otherwise noted.



f_S = 125 MSPS, IMD = 88 dBFS, f_{IN1} = 185 MHz, f_{IN2} = 190 MHz

Figure 46. FFT for Two-Tone Input Signal (–7 dBFS at 185 MHz and 190 MHz)



f_S = 125 MSPS, IMD = 99 dBFS, f_{IN1} = 46 MHz, f_{IN2} = 50 MHz

Figure 47. FFT for Two-Tone Input Signal (–36 dBFS at 185 MHz and 190 MHz)

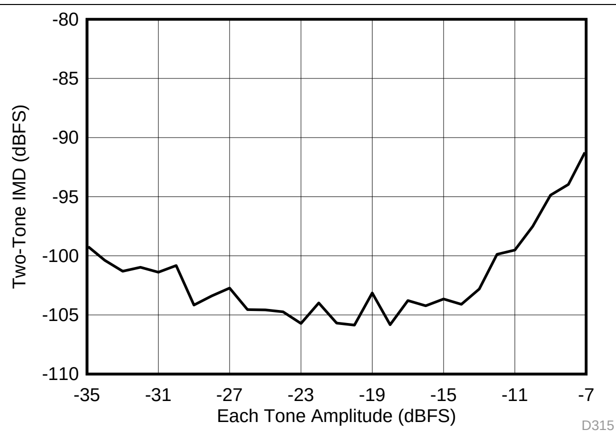


Figure 48. Intermodulation Distortion vs Input Amplitude (46 MHz and 50 MHz)

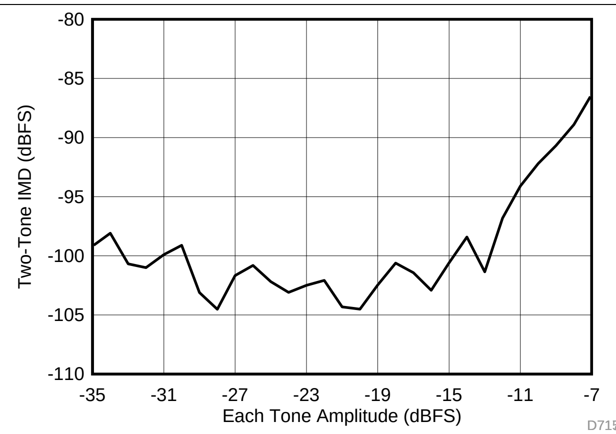


Figure 49. Intermodulation Distortion vs Input Amplitude (185 MHz and 190 MHz)

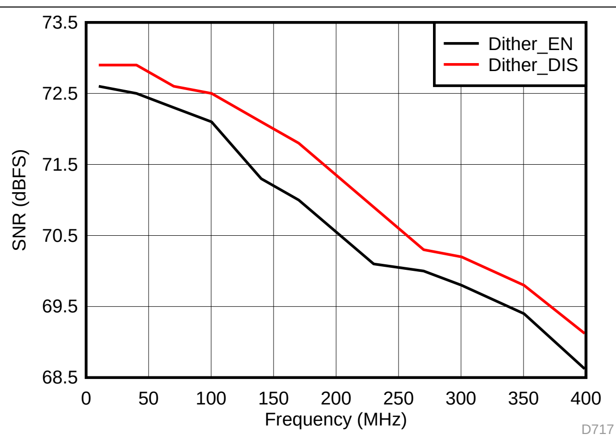


Figure 50. Signal-to-Noise Ratio vs Input Frequency

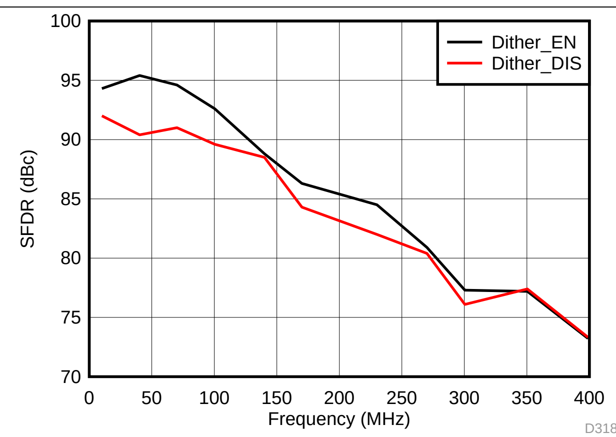


Figure 51. Spurious-Free Dynamic Range vs Input Frequency

Typical Characteristics: ADC32J44 (continued)

Typical values are at T_A= 25°C, ADC sampling rate = 125 MSPS, 50% clock duty cycle, AVDD = DVDD = 1.8 V, –1-dBFS differential input, 2-V_{PP} full-scale, and 32k-point FFT, unless otherwise noted.

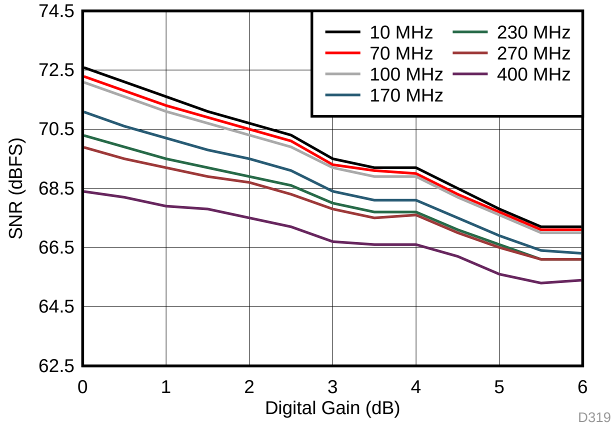


Figure 52. Signal-to-Noise Ratio vs Digital Gain and Input Frequency

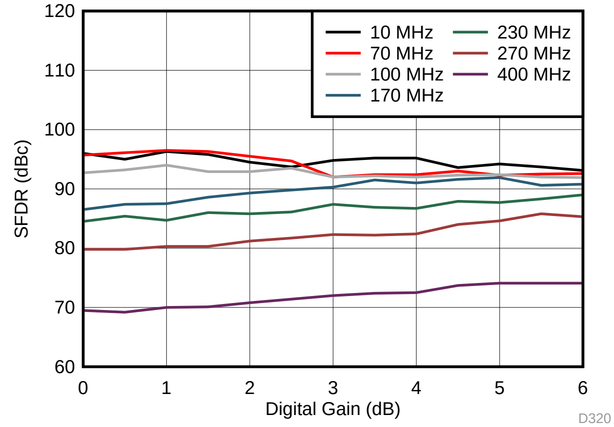


Figure 53. Spurious-Free Dynamic Range vs Digital Gain and Input Frequency

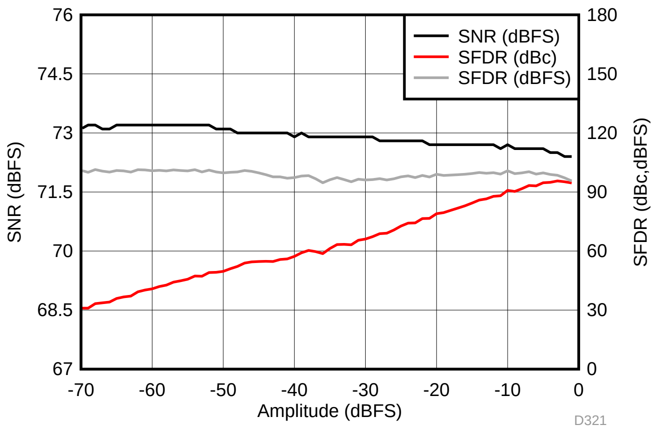


Figure 54. Performance vs Input Amplitude (30 MHz)

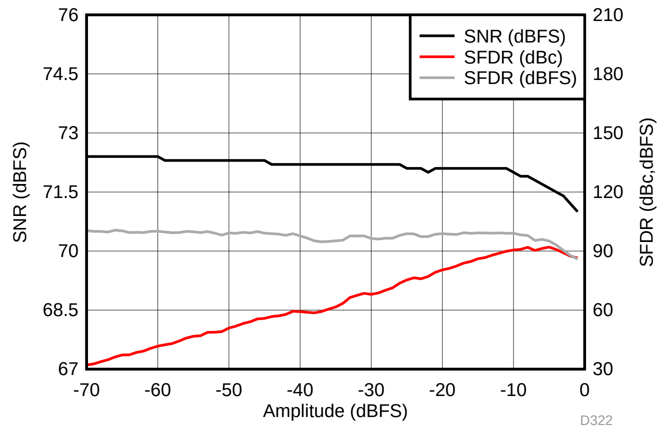


Figure 55. Performance vs Input Amplitude (170 MHz)

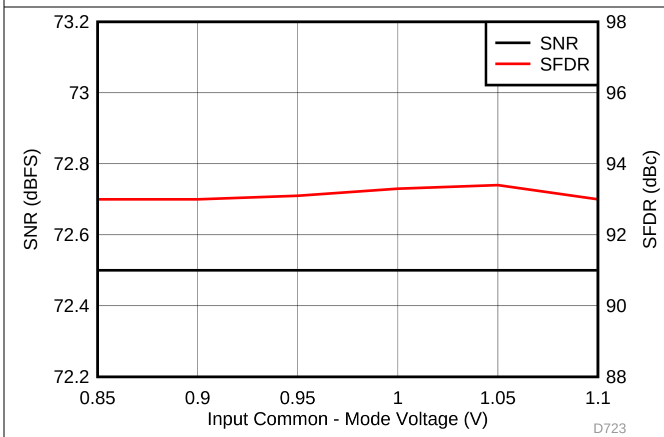


Figure 56. Performance vs Input Common-Mode Voltage (30 MHz)

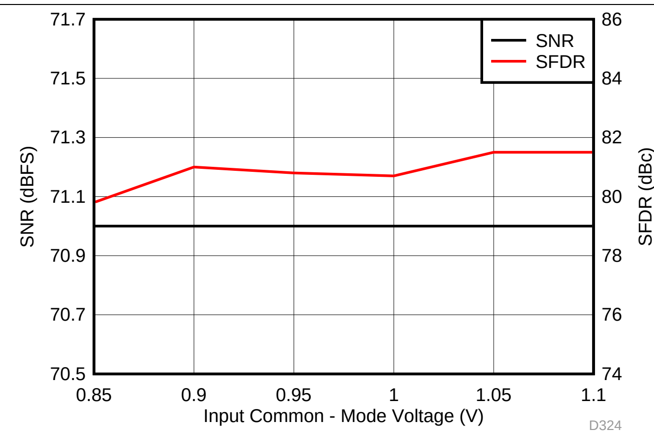


Figure 57. Performance vs Input Common-Mode Voltage (170 MHz)

Typical Characteristics: ADC32J44 (continued)

Typical values are at T_A= 25°C, ADC sampling rate = 125 MSPS, 50% clock duty cycle, AVDD = DVDD = 1.8 V, –1-dBFS differential input, 2-V_{PP} full-scale, and 32k-point FFT, unless otherwise noted.

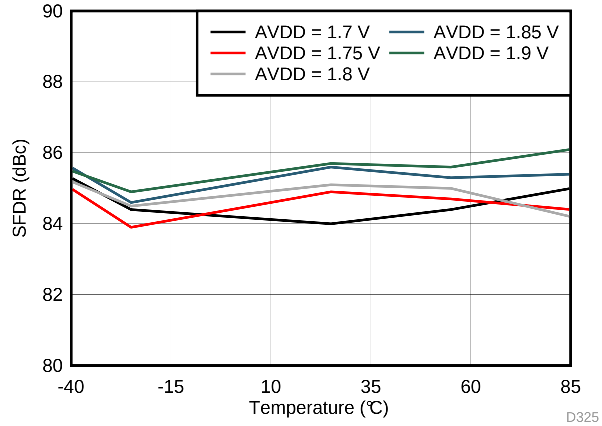


Figure 58. Spurious-Free Dynamic Range vs AVDD Supply and Temperature

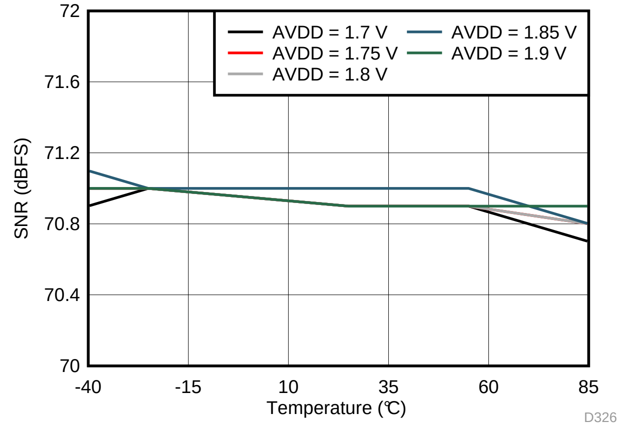


Figure 59. Signal-to-Noise Ratio vs AVDD Supply and Temperature

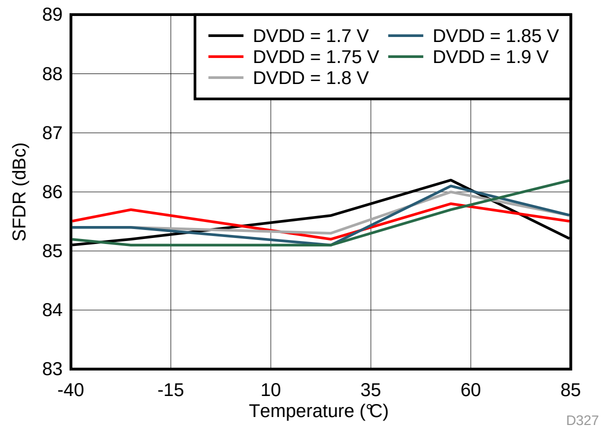


Figure 60. Spurious-Free Dynamic Range vs DVDD Supply and Temperature

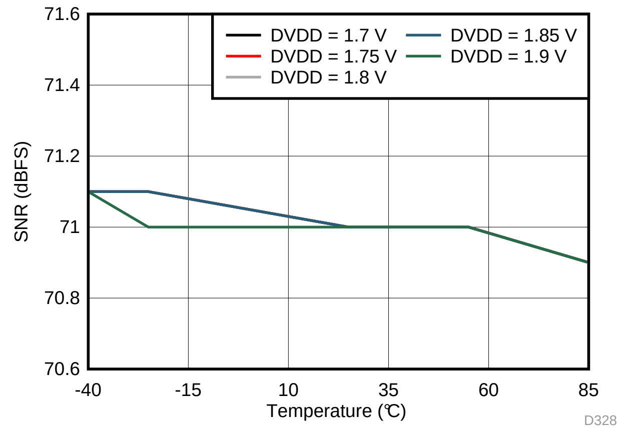


Figure 61. Signal-to-Noise Ratio vs DVDD Supply and Temperature

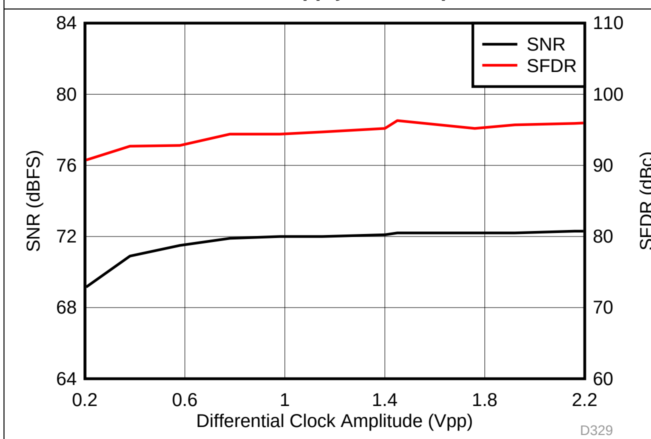


Figure 62. Performance vs Clock Amplitude (40 MHz)

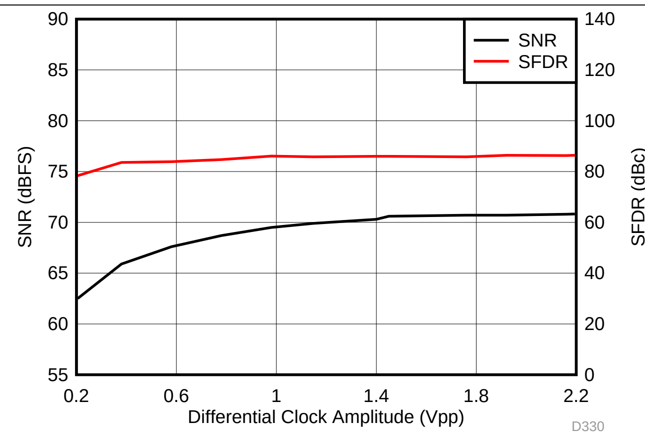


Figure 63. Performance vs Clock Amplitude (150 MHz)

Typical Characteristics: ADC32J44 (continued)

Typical values are at T_A= 25°C, ADC sampling rate = 125 MSPS, 50% clock duty cycle, AVDD = DVDD = 1.8 V, –1-dBFS differential input, 2-V_{PP} full-scale, and 32k-point FFT, unless otherwise noted.

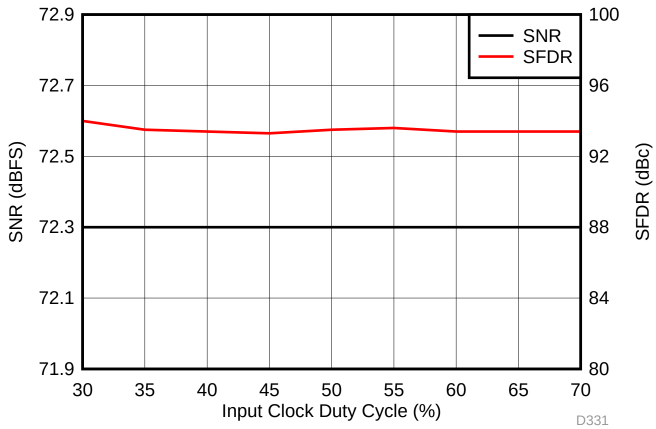


Figure 64. Performance vs Clock Duty Cycle (40 MHz)

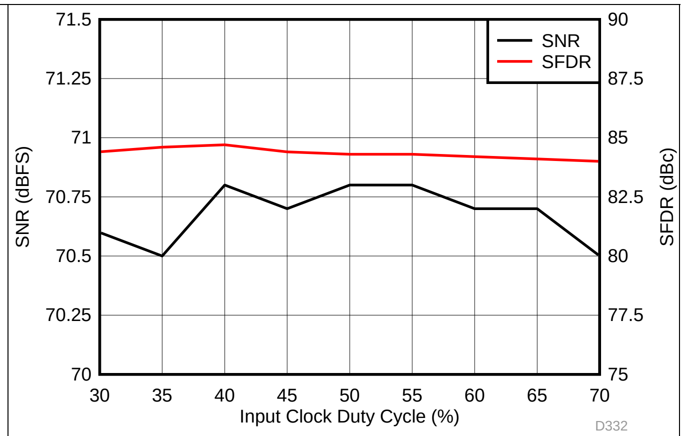
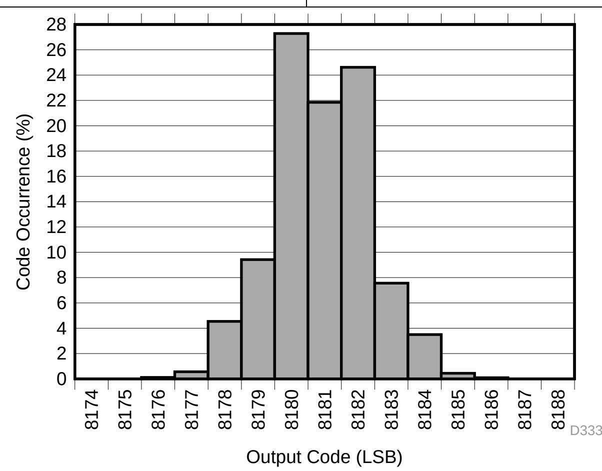


Figure 65. Performance vs Clock Duty Cycle (150 MHz)

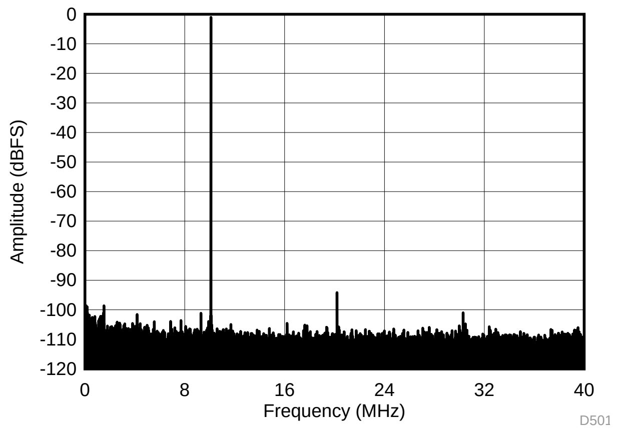


RMS noise = 1.4 LSBs

Figure 66. Idle Channel Histogram

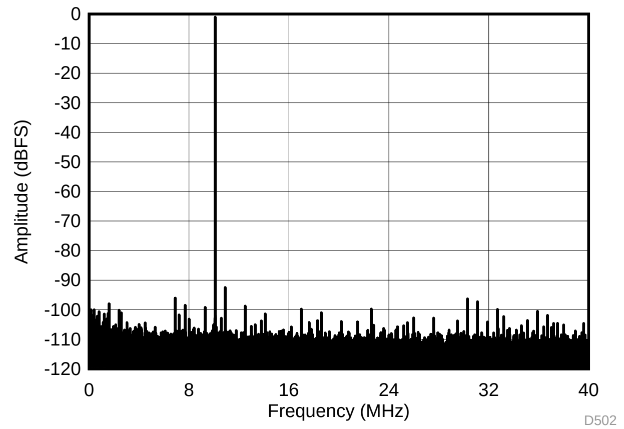
7.16 Typical Characteristics: ADC32J43

Typical values are at T_A= 25°C, ADC sampling rate = 80 MSPS, 50% clock duty cycle, AVDD = DVDD = 1.8 V, –1-dBFS differential input, 2-V_{PP} full-scale, and 32k-point FFT, unless otherwise noted.



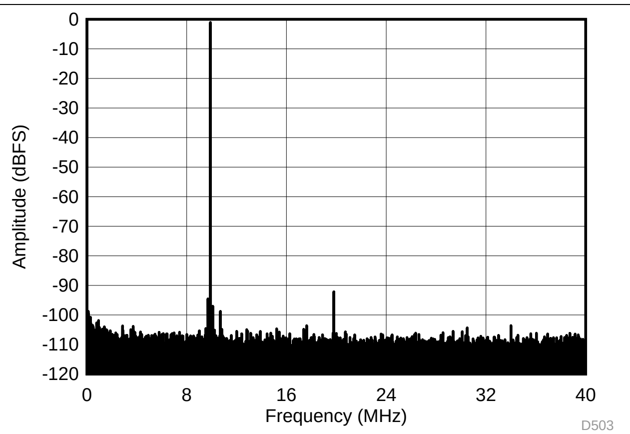
f_S = 80 MSPS, SNR = 72.2 dBFS, f_{IN} = 10 MHz, SFDR = 93.1 dBc

Figure 67. FFT for 10-MHz Input Signal (Dither On)



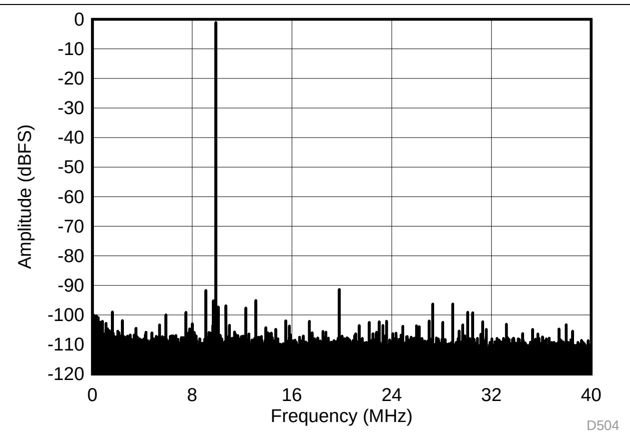
f_S = 80 MSPS, SNR = 72.6 dBFS, f_{IN} = 10 MHz, SFDR = 91.4 dBc

Figure 68. FFT for 10-MHz Input Signal (Dither Off)



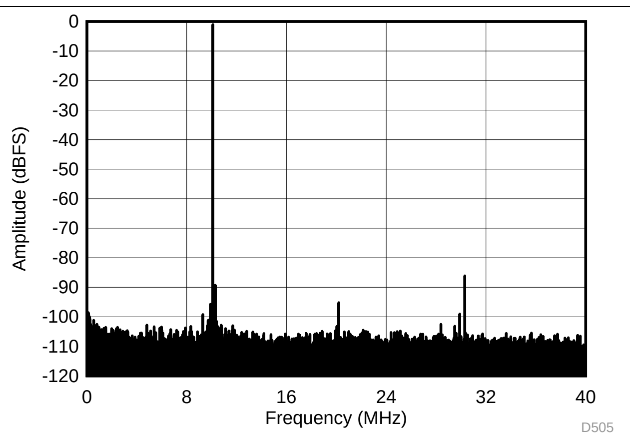
f_S = 80 MSPS, SNR = 72.1 dBFS, f_{IN} = 70 MHz, SFDR = 92 dBc

Figure 69. FFT for 70-MHz Input Signal (Dither On)



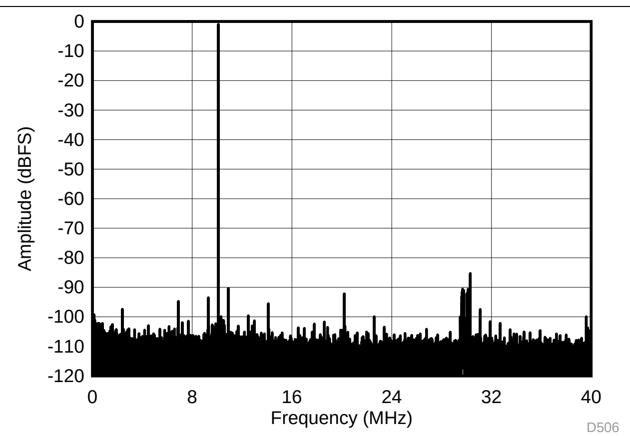
f_S = 80 MSPS, SNR = 72.5 dBFS, f_{IN} = 70 MHz, SFDR = 91 dBc

Figure 70. FFT for 70-MHz Input Signal (Dither Off)



f_S = 80 MSPS, SNR = 71 dBFS, f_{IN} = 170 MHz, SFDR = 86 dBc

Figure 71. FFT for 170-MHz Input Signal (Dither On)

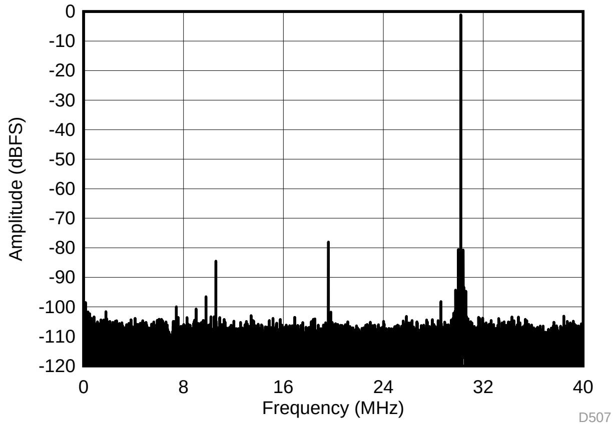


f_S = 80 MSPS, SNR = 69.7 dBFS, f_{IN} = 10 MHz, SFDR = 85 dBc

Figure 72. FFT for 170-MHz Input Signal (Dither Off)

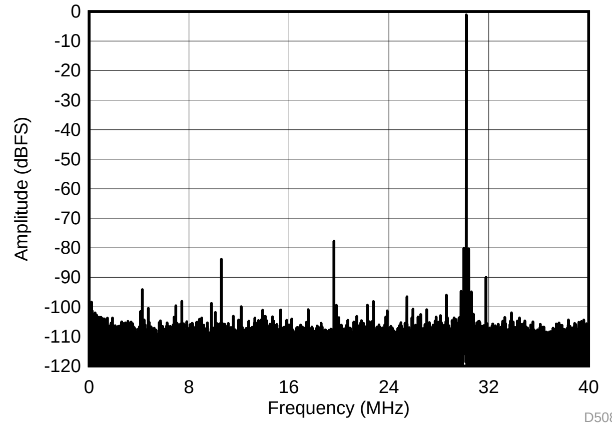
Typical Characteristics: ADC32J43 (continued)

Typical values are at T_A= 25°C, ADC sampling rate = 80 MSPS, 50% clock duty cycle, AVDD = DVDD = 1.8 V, –1-dBFS differential input, 2-V_{PP} full-scale, and 32k-point FFT, unless otherwise noted.



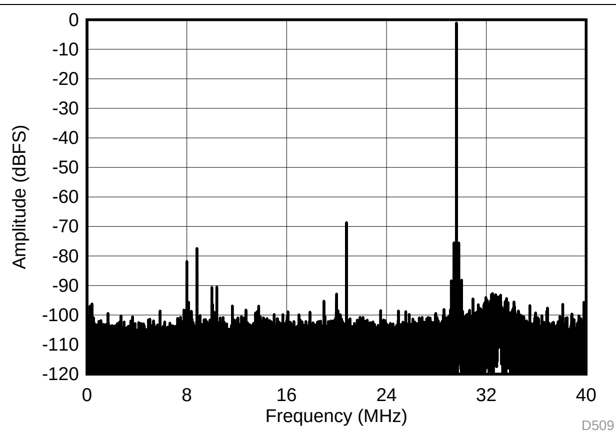
f_S = 80 MSPS, SNR = 70.2 dBFS, f_{IN} = 270 MHz, SFDR = 76.9 dBc

Figure 73. FFT for 270-MHz Input Signal (Dither On)



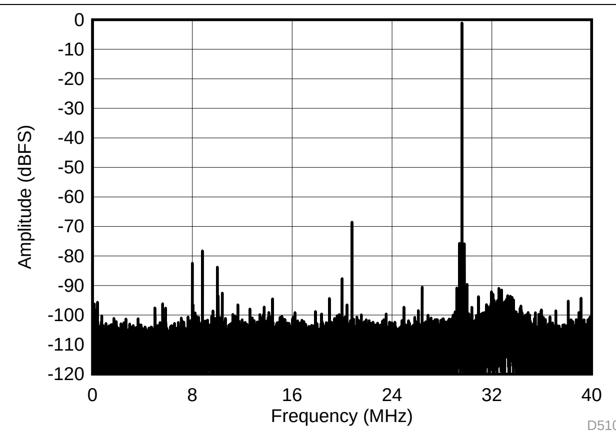
f_S = 80 MSPS, SNR = 70.5 dBFS, f_{IN} = 270 MHz, SFDR = 76.7 dBc

Figure 74. FFT for 270-MHz Input Signal (Dither Off)



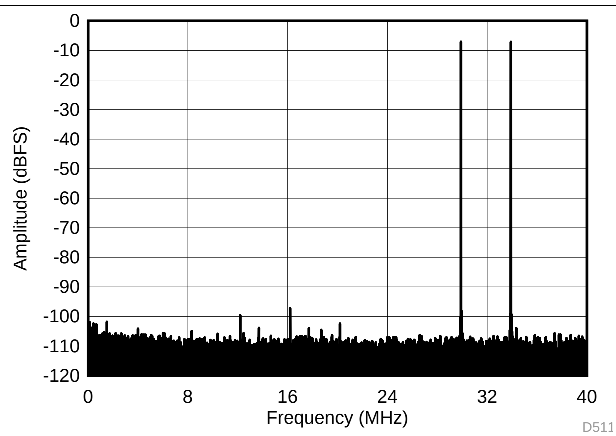
f_S = 80 MSPS, SNR = 64.5 dBFS, f_{IN} = 450 MHz, SFDR = 67.6 dBc

Figure 75. FFT for 450-MHz Input Signal (Dither On)



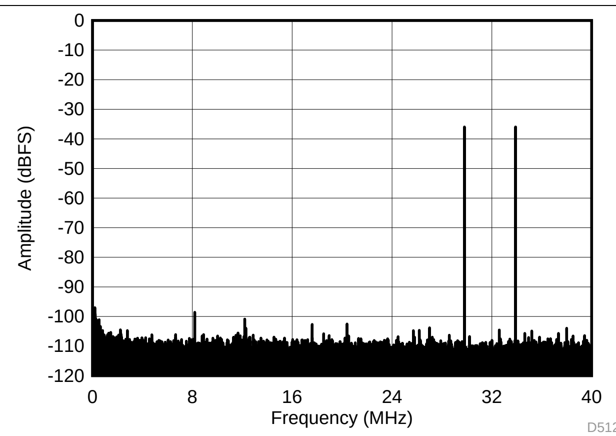
f_S = 80 MSPS, SNR = 63.8 dBFS, f_{IN} = 450 MHz, SFDR = 67.4 dBc

Figure 76. FFT for 450-MHz Input Signal (Dither Off)



f_S = 80 MSPS, IMD = 93 dBFS, f_{IN1} = 46 MHz, f_{IN2} = 50 MHz

Figure 77. FFT for Two-Tone Input Signal (–7 dBFS at 46 MHz and 50 MHz)

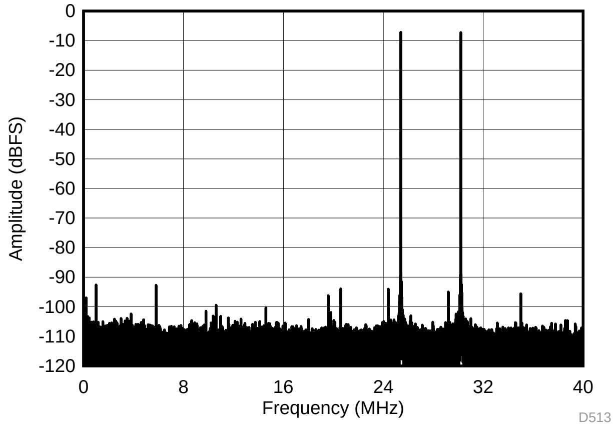


f_S = 80 MSPS, IMD = 101 dBFS, f_{IN1} = 46 MHz, f_{IN2} = 50 MHz

Figure 78. FFT for Two-Tone Input Signal (–36 dBFS at 46 MHz and 50 MHz)

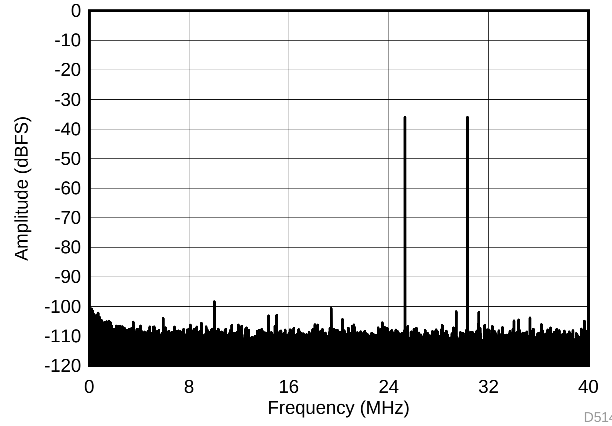
Typical Characteristics: ADC32J43 (continued)

Typical values are at T_A= 25°C, ADC sampling rate = 80 MSPS, 50% clock duty cycle, AVDD = DVDD = 1.8 V, –1-dBFS differential input, 2-V_{PP} full-scale, and 32k-point FFT, unless otherwise noted.



f_S = 80 MSPS, IMD = 88 dBFS, f_{IN1} = 185 MHz, f_{IN2} = 190 MHz

Figure 79. FFT for Two-Tone Input Signal (–7 dBFS at 185 MHz and 190 MHz)



f_S = 80 MSPS, IMD = 99 dBFS, f_{IN1} = 185 MHz, f_{IN2} = 190 MHz

Figure 80. FFT for Two-Tone Input Signal (–36 dBFS at 185 MHz and 190 MHz)

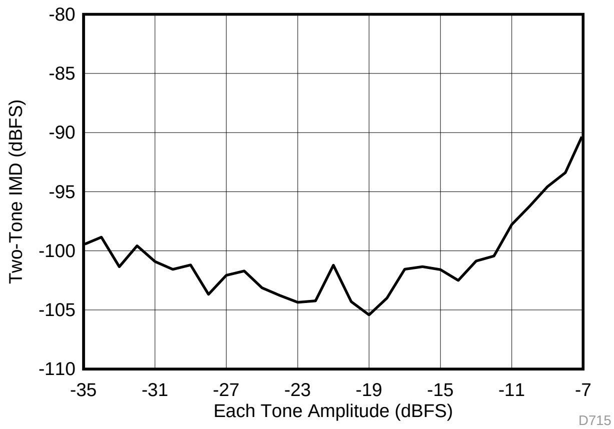


Figure 81. Intermodulation Distortion vs Input Amplitude (46 MHz and 50 MHz)

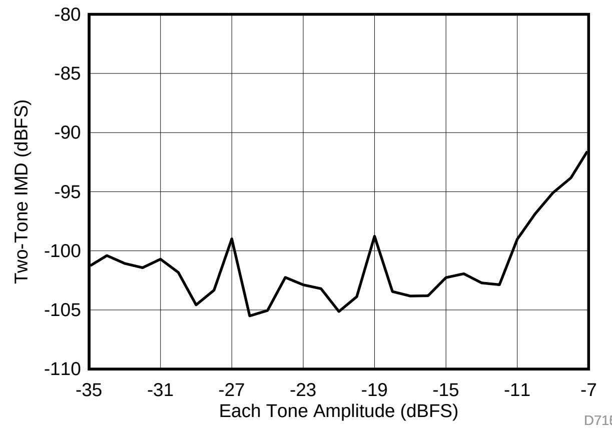


Figure 82. Intermodulation Distortion vs Input Amplitude (185 MHz and 190 MHz)

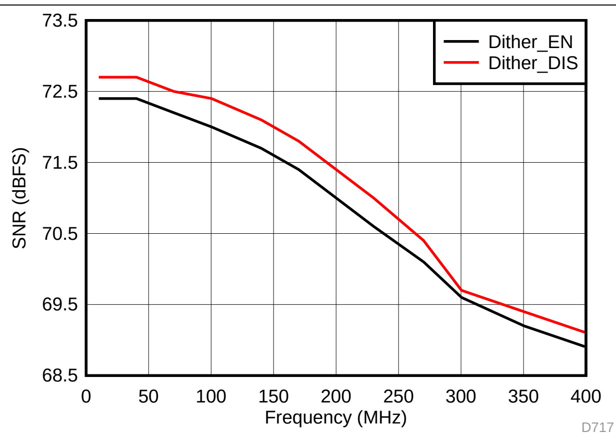


Figure 83. Signal-to-Noise Ratio vs Input Frequency

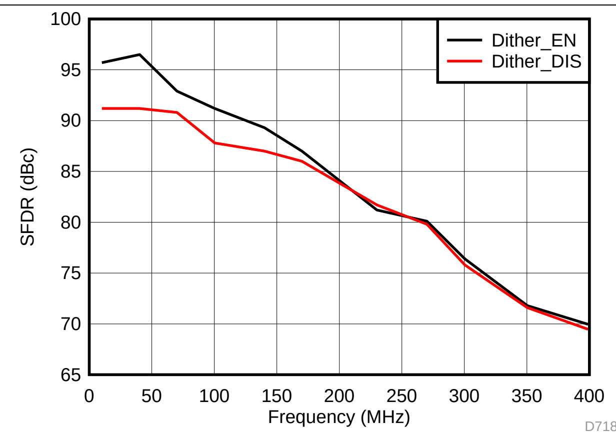


Figure 84. Spurious-Free Dynamic Range vs Input Frequency

Typical Characteristics: ADC32J43 (continued)

Typical values are at T_A= 25°C, ADC sampling rate = 80 MSPS, 50% clock duty cycle, AVDD = DVDD = 1.8 V, –1-dBFS differential input, 2-V_{PP} full-scale, and 32k-point FFT, unless otherwise noted.

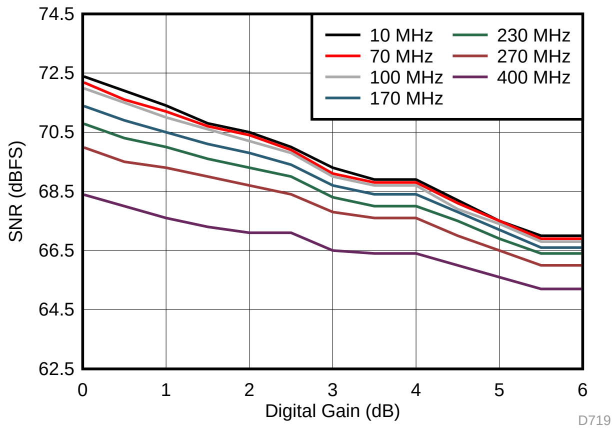


Figure 85. Signal-to-Noise Ratio vs Digital Gain and Input Frequency

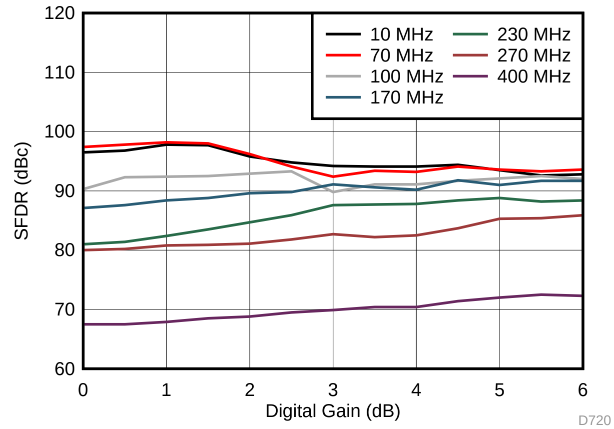


Figure 86. Spurious-Free Dynamic Range vs Digital Gain and Input Frequency

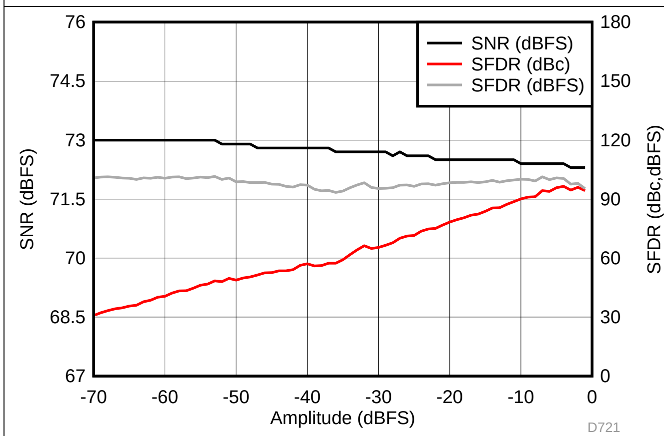


Figure 87. Performance vs Input Amplitude (30 MHz)

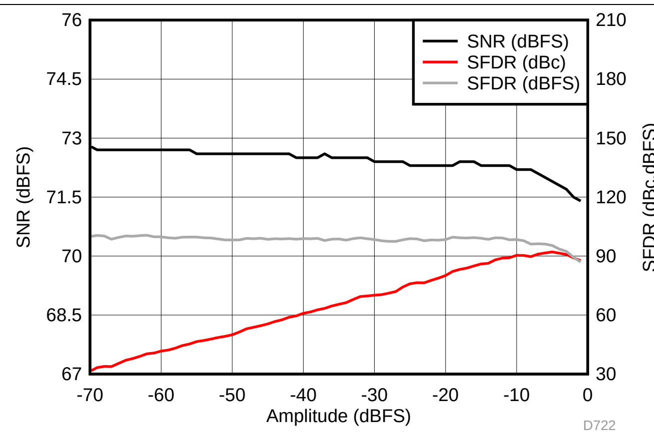


Figure 88. Performance vs Input Amplitude (170 MHz)

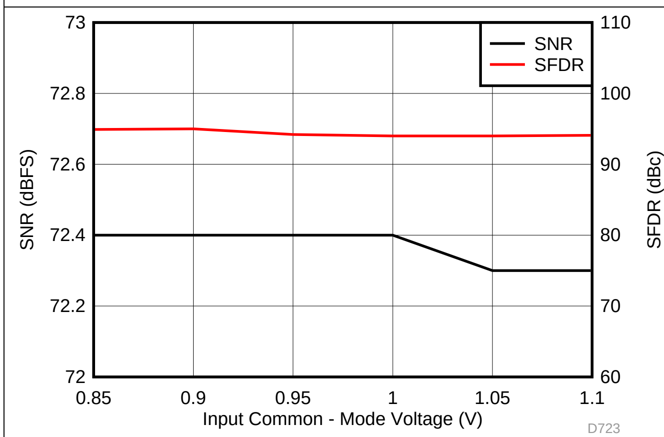


Figure 89. Performance vs Input Common-Mode Voltage (30 MHz)

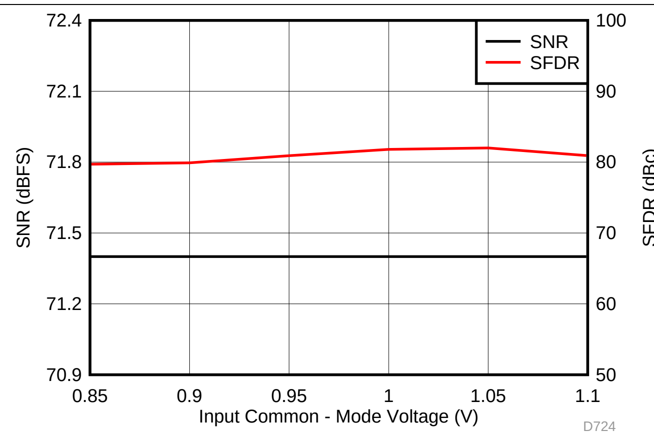


Figure 90. Performance vs Input Common-Mode Voltage (170 MHz)

Typical Characteristics: ADC32J43 (continued)

Typical values are at T_A= 25°C, ADC sampling rate = 80 MSPS, 50% clock duty cycle, AVDD = DVDD = 1.8 V, –1-dBFS differential input, 2-V_{PP} full-scale, and 32k-point FFT, unless otherwise noted.

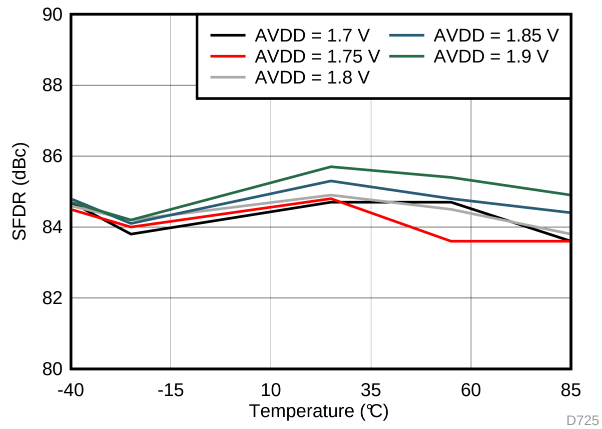


Figure 91. Spurious-Free Dynamic Range vs AVDD Supply and Temperature

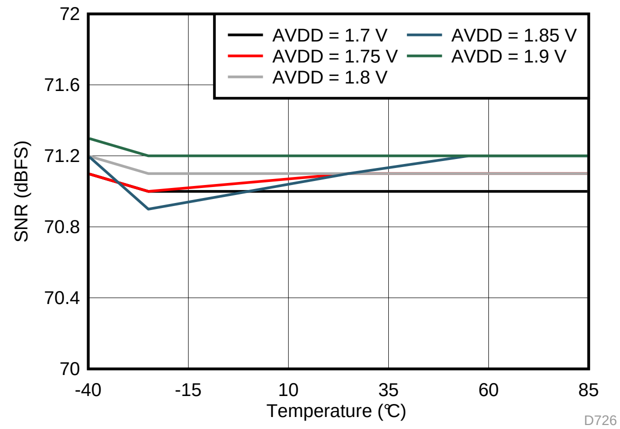


Figure 92. Signal-to-Noise Ratio vs AVDD Supply and Temperature

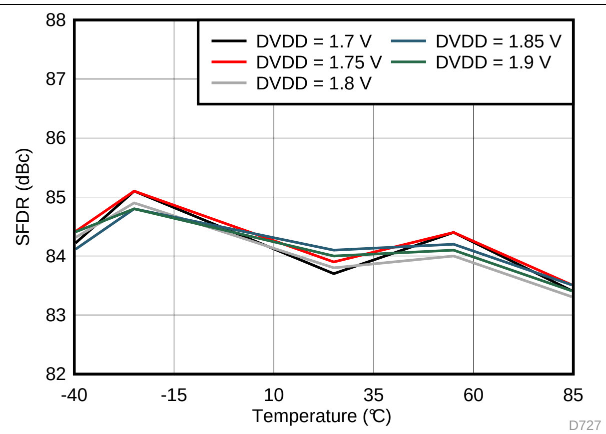


Figure 93. Spurious-Free Dynamic Range vs DVDD Supply and Temperature

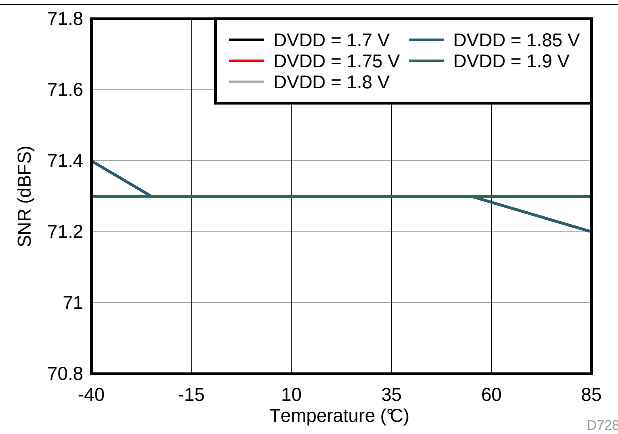


Figure 94. Signal-to-Noise Ratio vs DVDD Supply and Temperature

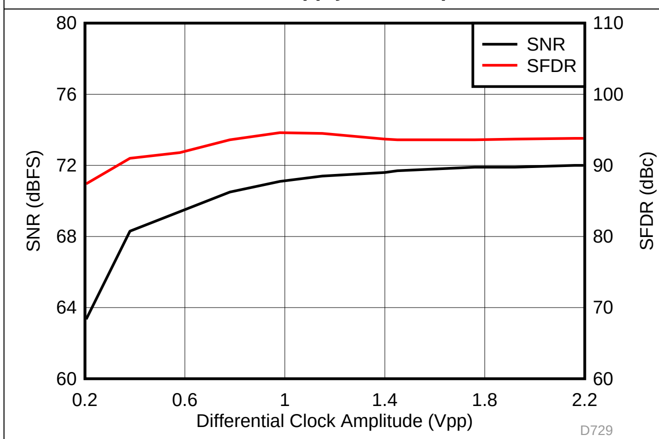


Figure 95. Performance vs Clock Amplitude (40 MHz)

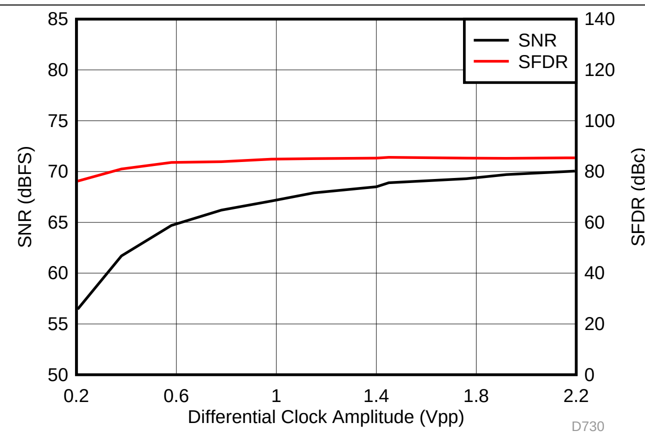


Figure 96. Performance vs Clock Amplitude (150 MHz)

Typical Characteristics: ADC32J43 (continued)

Typical values are at T_A = 25°C, ADC sampling rate = 80 MSPS, 50% clock duty cycle, AVDD = DVDD = 1.8 V, –1-dBFS differential input, 2-V_{PP} full-scale, and 32k-point FFT, unless otherwise noted.

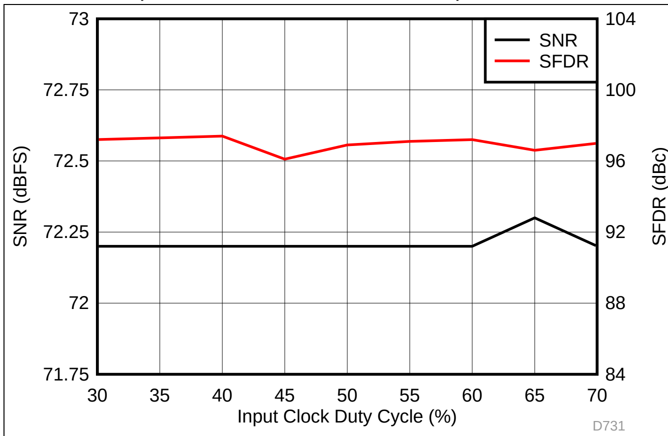


Figure 97. Performance vs Clock Duty Cycle (40 MHz)

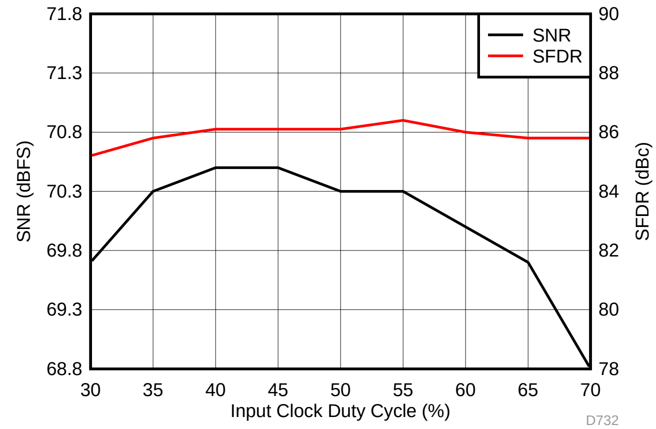
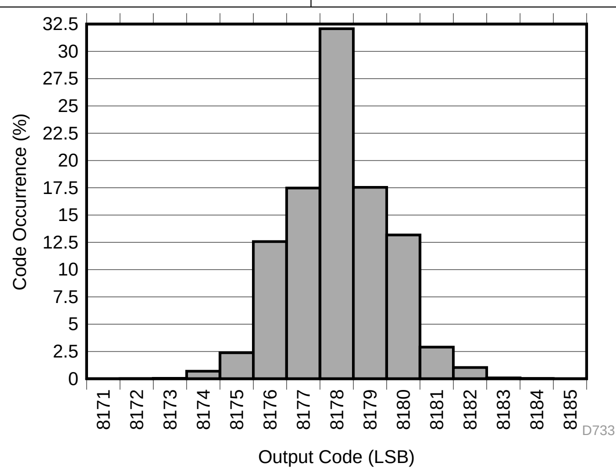


Figure 98. Performance vs Clock Duty Cycle (150 MHz)

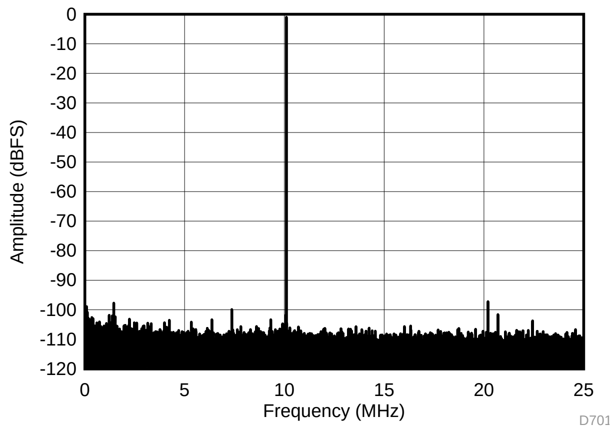


RMS noise = 1.4 LSBs

Figure 99. Idle Channel Histogram

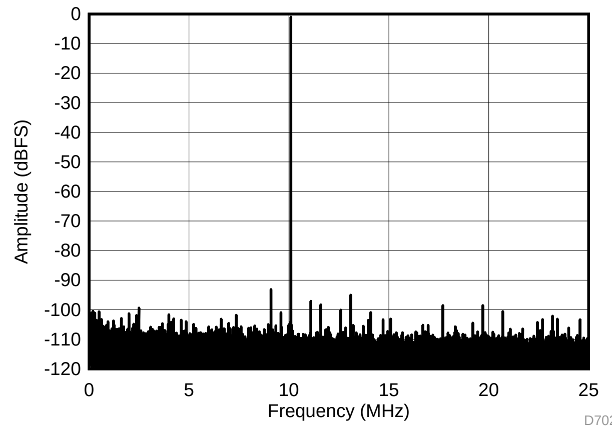
7.17 Typical Characteristics: ADC32J42

Typical values are at T_A= 25°C, ADC sampling rate = 50 MSPS, 50% clock duty cycle, AVDD = DVDD = 1.8 V, –1-dBFS differential input, 2-V_{PP} full-scale, and 32k-point FFT, unless otherwise noted.



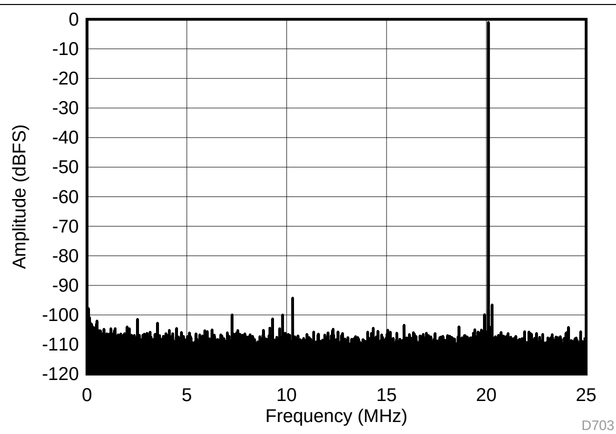
f_S = 50 MSPS, SNR = 72.1 dBFS, f_{IN} = 10 MHz, SFDR = 96.2 dBc

Figure 100. FFT for 10-MHz Input Signal (Dither On)



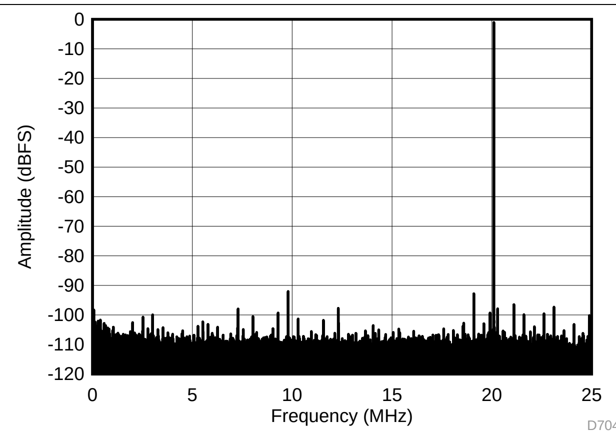
f_S = 50 MSPS, SNR = 72.6 dBFS, f_{IN} = 10 MHz, SFDR = 92.1 dBc

Figure 101. FFT for 10-MHz Input Signal (Dither Off)



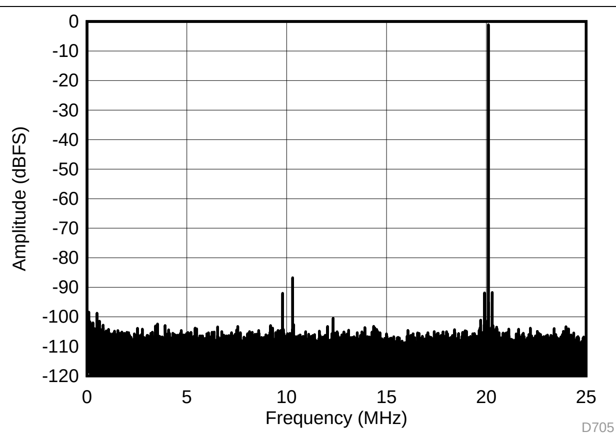
f_S = 50 MSPS, SNR = 71.7 dBFS, f_{IN} = 70 MHz, SFDR = 93.2 dBc

Figure 102. FFT for 70-MHz Input Signal (Dither On)



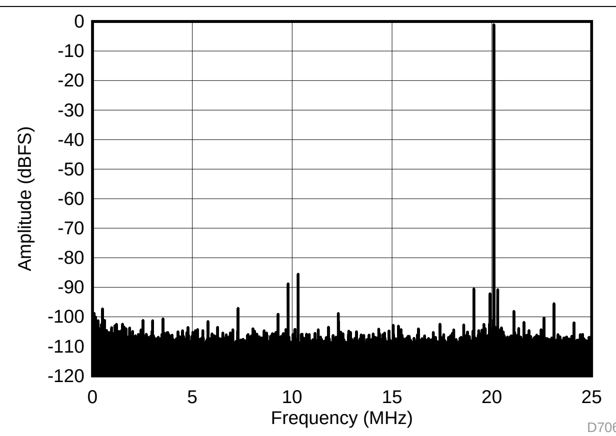
f_S = 50 MSPS, SNR = 72 dBFS, f_{IN} = 70 MHz, SFDR = 92 dBc

Figure 103. FFT for 70-MHz Input Signal (Dither Off)



f_S = 50 MSPS, SNR = 70.4 dBFS, f_{IN} = 170 MHz, SFDR = 86 dBc

Figure 104. FFT for 170-MHz Input Signal (Dither On)

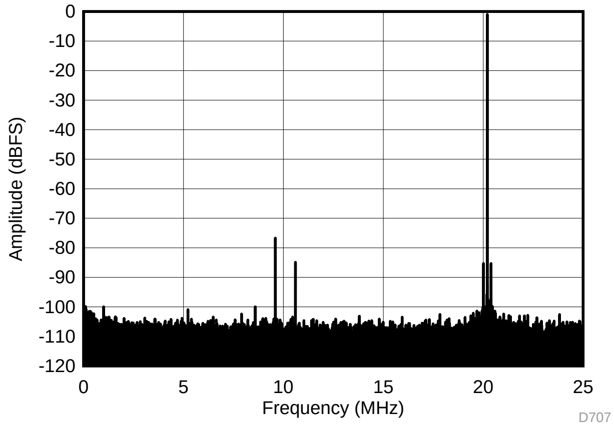


f_S = 50 MSPS, SNR = 70.9 dBFS, f_{IN} = 170 MHz, SFDR = 85 dBc

Figure 105. FFT for 170-MHz Input Signal (Dither Off)

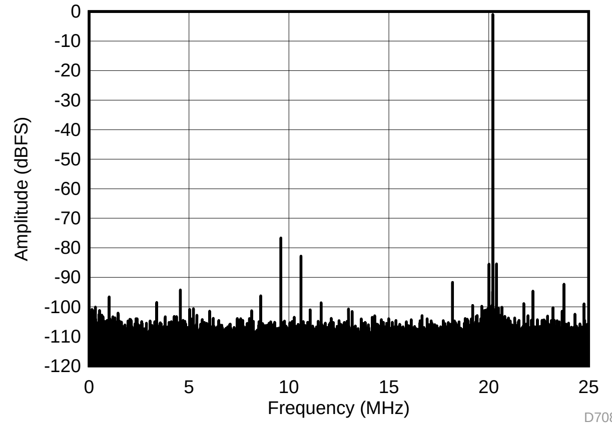
Typical Characteristics: ADC32J42 (continued)

Typical values are at T_A= 25°C, ADC sampling rate = 50 MSPS, 50% clock duty cycle, AVDD = DVDD = 1.8 V, –1-dBFS differential input, 2-V_{PP} full-scale, and 32k-point FFT, unless otherwise noted.



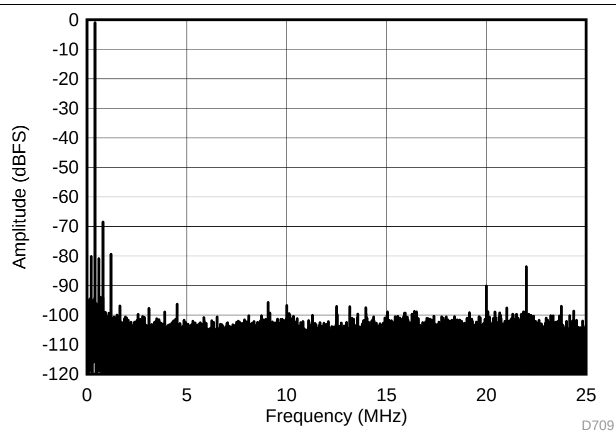
f_S = 50 MSPS, SNR = 69.5 dBFS, f_{IN} = 270 MHz, SFDR = 75.7 dBc

Figure 106. FFT for 270-MHz Input Signal (Dither On)



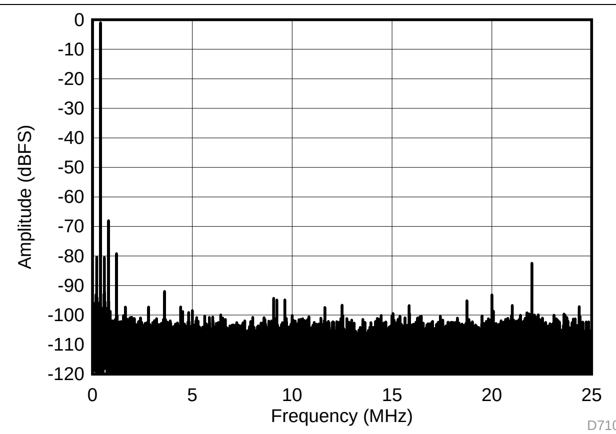
f_S = 50 MSPS, SNR = 69.5 dBFS, f_{IN} = 270 MHz, SFDR = 75.7 dBc

Figure 107. FFT for 270-MHz Input Signal (Dither Off)



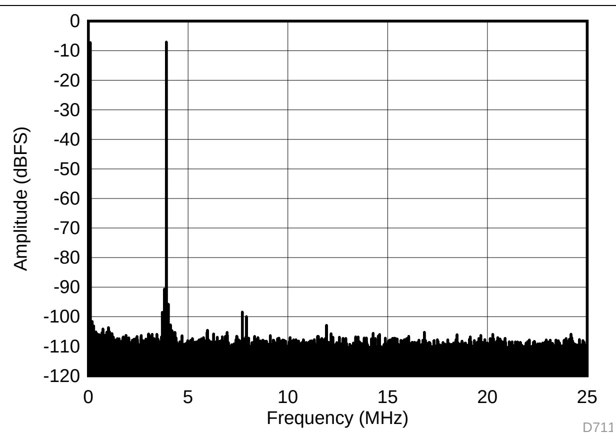
f_S = 50 MSPS, SNR = 65.9 dBFS, f_{IN} = 450 MHz, SFDR = 67.4 dBc

Figure 108. FFT for 450-MHz Input Signal (Dither On)



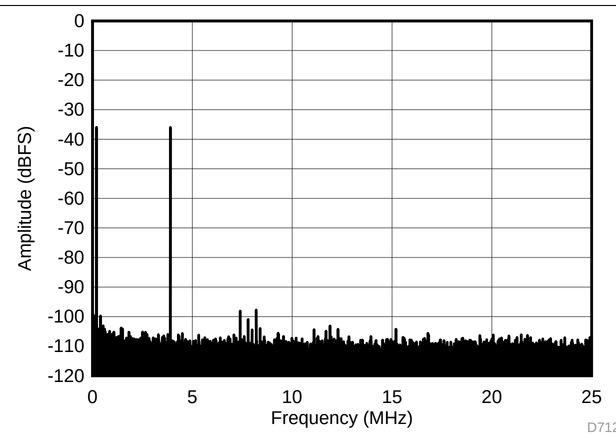
f_S = 50 MSPS, SNR = 66.4 dBFS, f_{IN} = 450 MHz, SFDR = 67 dBc

Figure 109. FFT for 450-MHz Input Signal (Dither Off)



f_S = 50 MSPS, IMD = 93 dBFS, f_{IN1} = 46 MHz, f_{IN2} = 50 MHz

Figure 110. FFT for Two-Tone Input Signal (–7 dBFS at 46 MHz and 50 MHz)

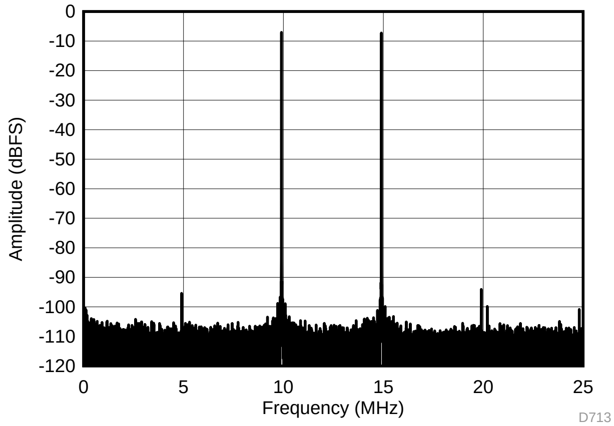


f_S = 50 MSPS, IMD = 101 dBFS, f_{IN1} = 46 MHz, f_{IN2} = 50 MHz

Figure 111. FFT for Two-Tone Input Signal (–36 dBFS at 46 MHz and 50 MHz)

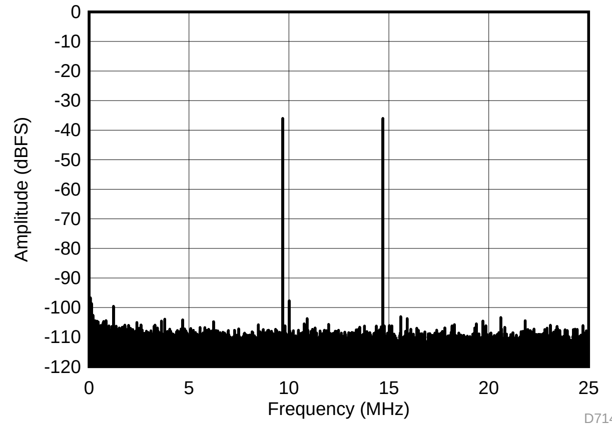
Typical Characteristics: ADC32J42 (continued)

Typical values are at T_A= 25°C, ADC sampling rate = 50 MSPS, 50% clock duty cycle, AVDD = DVDD = 1.8 V, –1-dBFS differential input, 2-V_{PP} full-scale, and 32k-point FFT, unless otherwise noted.



f_S = 50 MSPS, IMD = 86 dBFS, f_{IN1} = 185 MHz, f_{IN2} = 190 MHz

Figure 112. FFT for Two-Tone Input Signal (–7 dBFS at 185 MHz and 190 MHz)



f_S = 50 MSPS, IMD = 99 dBFS, f_{IN1} = 185 MHz, f_{IN2} = 190 MHz

Figure 113. FFT for Two-Tone Input Signal (–36 dBFS at 185 MHz and 190 MHz)

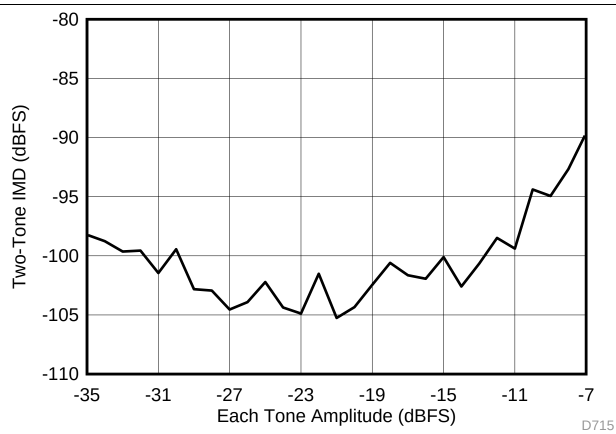


Figure 114. Intermodulation Distortion vs Input Amplitude (46 MHz and 50 MHz)

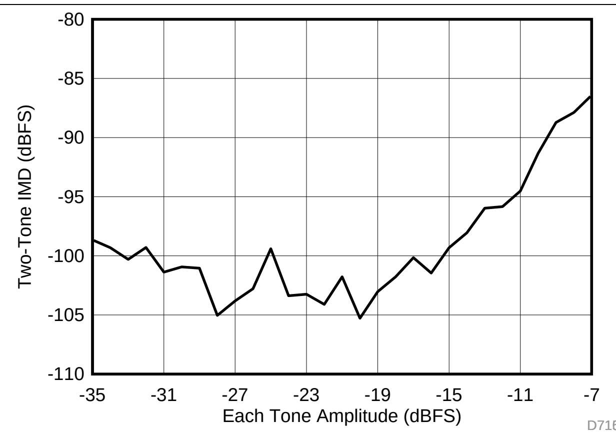


Figure 115. Intermodulation Distortion vs Input Amplitude (185 MHz and 190 MHz)

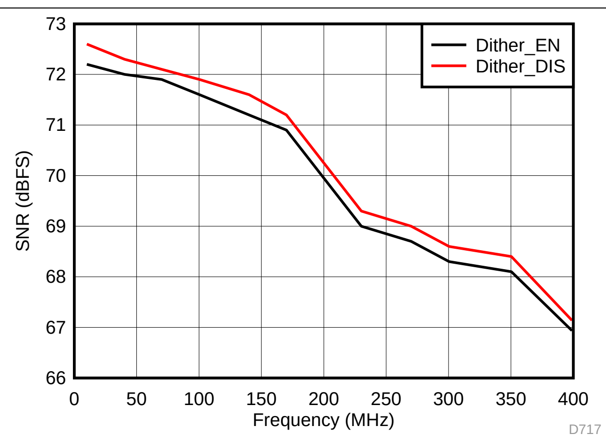


Figure 116. Signal-to-Noise Ratio vs Input Frequency

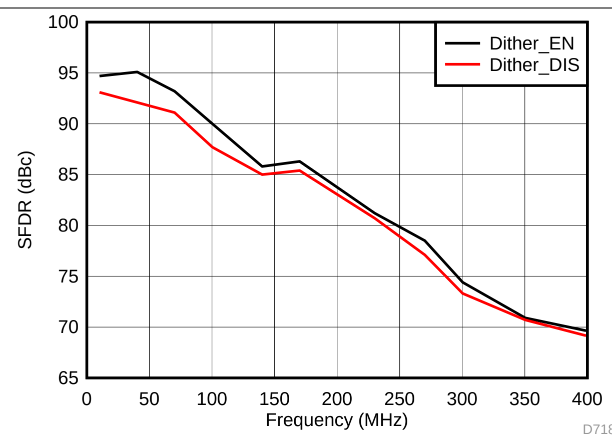


Figure 117. Spurious-Free Dynamic Range vs Input Frequency

Typical Characteristics: ADC32J42 (continued)

Typical values are at T_A= 25°C, ADC sampling rate = 50 MSPS, 50% clock duty cycle, AVDD = DVDD = 1.8 V, –1-dBFS differential input, 2-V_{PP} full-scale, and 32k-point FFT, unless otherwise noted.

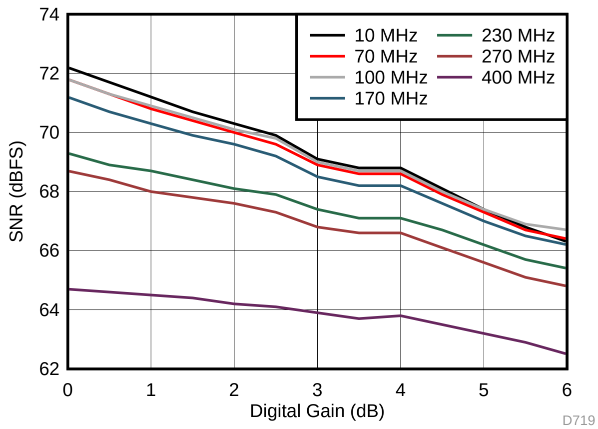


Figure 118. Signal-to-Noise Ratio vs Digital Gain and Input Frequency

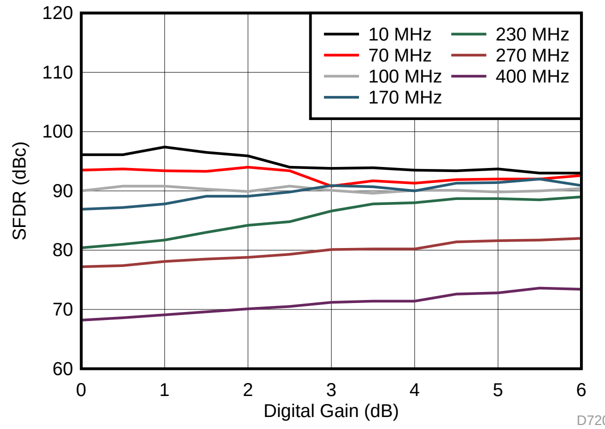


Figure 119. Spurious-Free Dynamic Range vs Digital Gain and Input Frequency

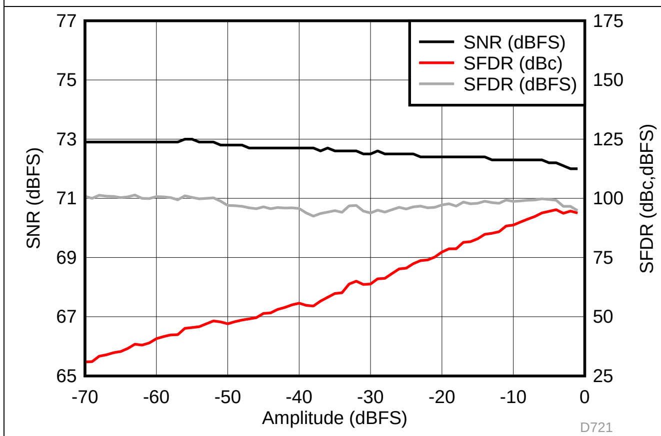


Figure 120. Performance vs Input Amplitude (30 MHz)

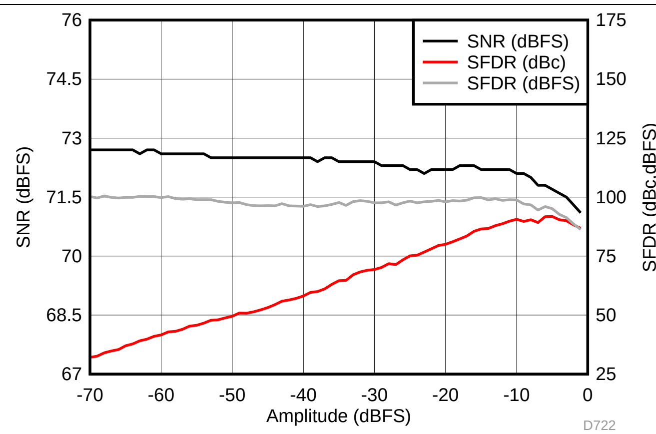


Figure 121. Performance vs Input Amplitude (170 MHz)

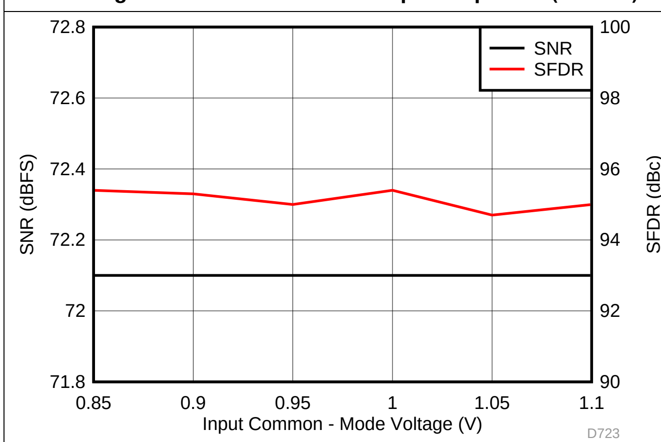


Figure 122. Performance vs Input Common-Mode Voltage (30 MHz)

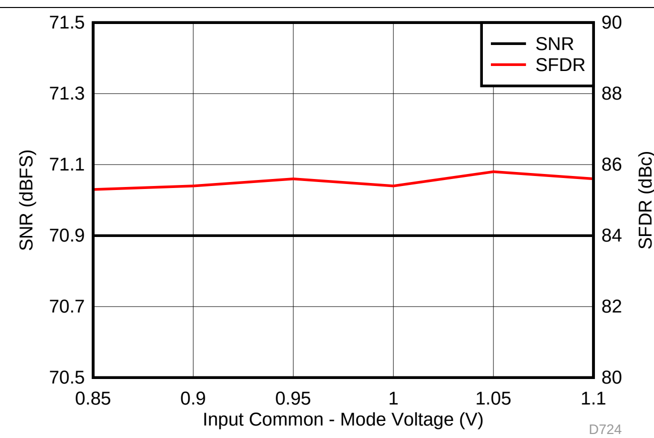


Figure 123. Performance vs Input Common-Mode Voltage (170 MHz)

Typical Characteristics: ADC32J42 (continued)

Typical values are at T_A= 25°C, ADC sampling rate = 50 MSPS, 50% clock duty cycle, AVDD = DVDD = 1.8 V, –1-dBFS differential input, 2-V_{PP} full-scale, and 32k-point FFT, unless otherwise noted.

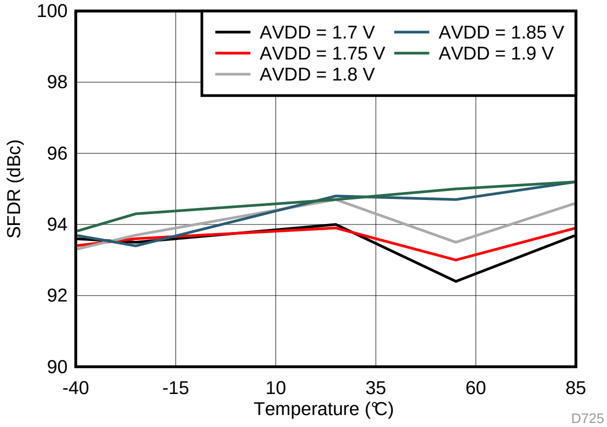


Figure 124. Spurious-Free Dynamic Range vs AVDD Supply and Temperature

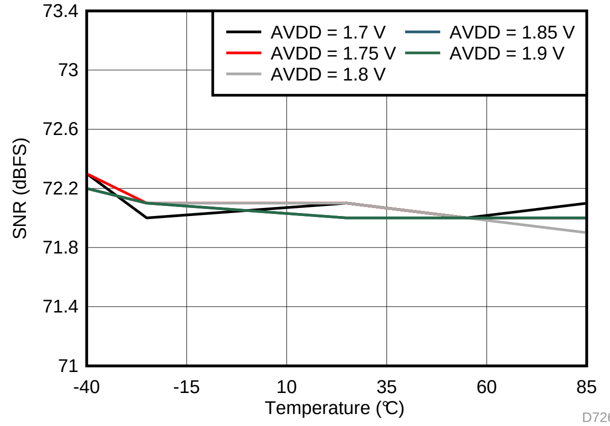


Figure 125. Signal-to-Noise Ratio vs AVDD Supply and Temperature

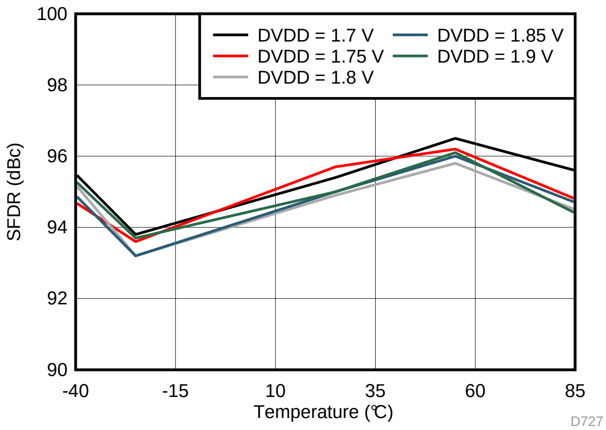


Figure 126. Spurious-Free Dynamic Range vs DVDD Supply and Temperature

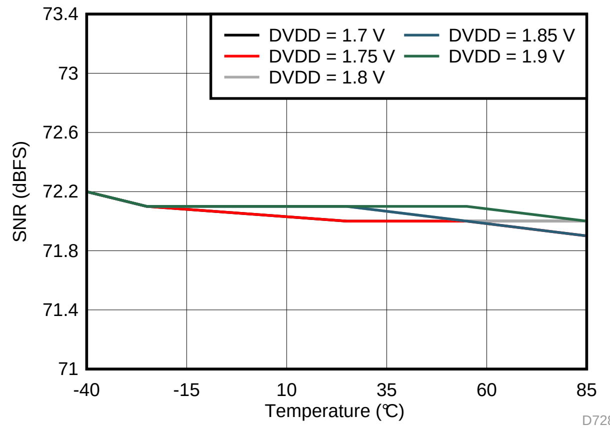


Figure 127. Signal-to-Noise Ratio vs DVDD Supply and Temperature

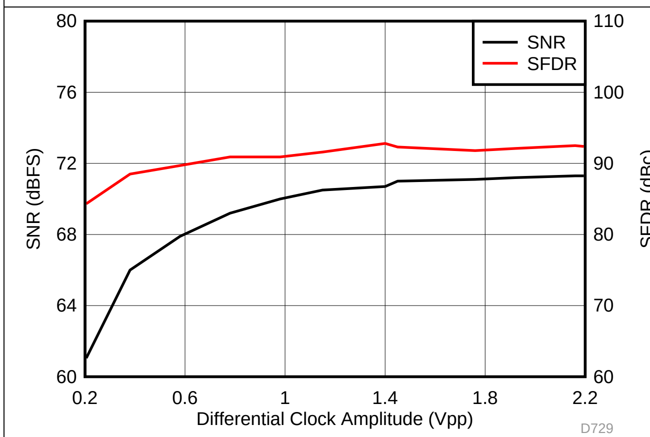


Figure 128. Performance vs Clock Amplitude (40 MHz)

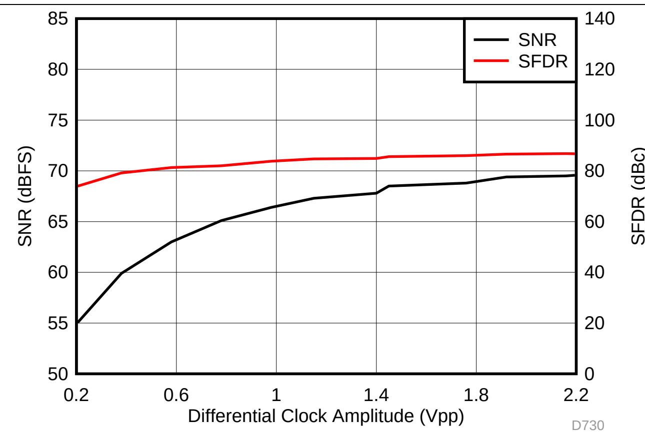


Figure 129. Performance vs Clock Amplitude (150 MHz)

Typical Characteristics: ADC32J42 (continued)

Typical values are at T_A= 25°C, ADC sampling rate = 50 MSPS, 50% clock duty cycle, AVDD = DVDD = 1.8 V, –1-dBFS differential input, 2-V_{PP} full-scale, and 32k-point FFT, unless otherwise noted.

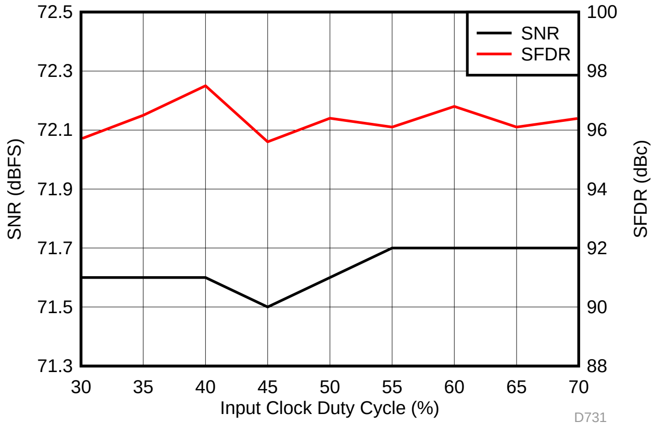


Figure 130. Performance vs Clock Duty Cycle (40 MHz)

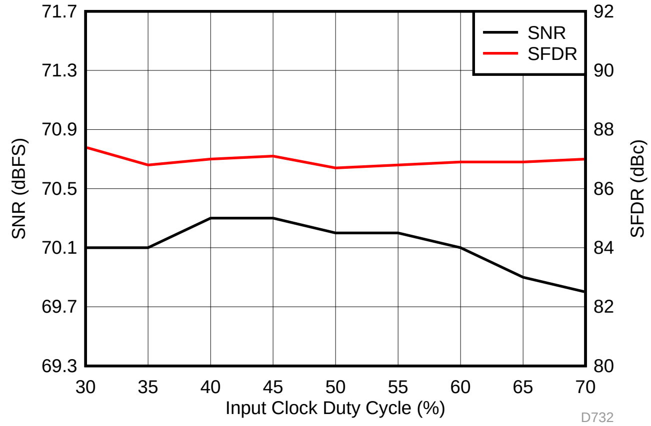
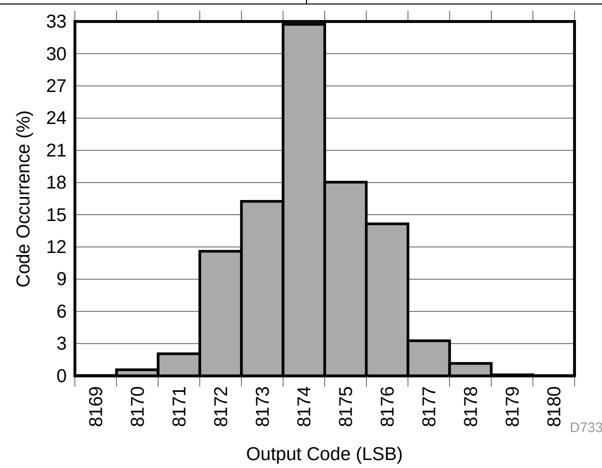


Figure 131. Performance vs Clock Duty Cycle (150 MHz)

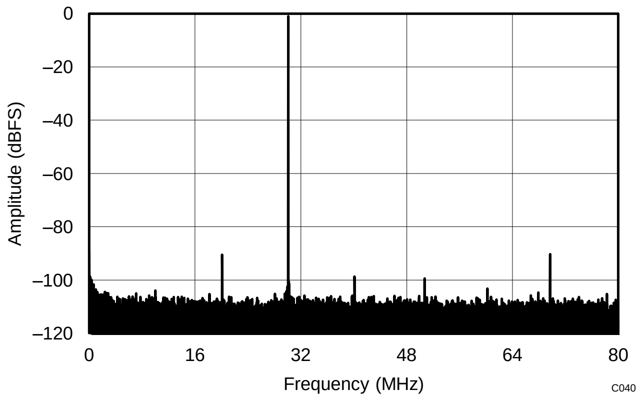


RMS noise = 1.3 LSBs

Figure 132. Idle Channel Histogram

7.18 Typical Characteristics: Common Plots

Typical values are at T_A= 25°C, ADC sampling rate = 160 MSPS, 50% clock duty cycle, AVDD = DVDD = 1.8 V, –1-dBFS differential input, 2-V_{PP} full-scale, and 32k-point FFT, unless otherwise noted.



f_S = 160 MSPS, f_{CM} = 10 MHz, 50 mV_{PP}, f_{IN} = 30 MHz, Amplitude (f_{IN} + f_{CM}) = –98 dBFS, Amplitude (f_{IN} – f_{CM}) = –91 dBFS

Figure 133. CMRR FFT

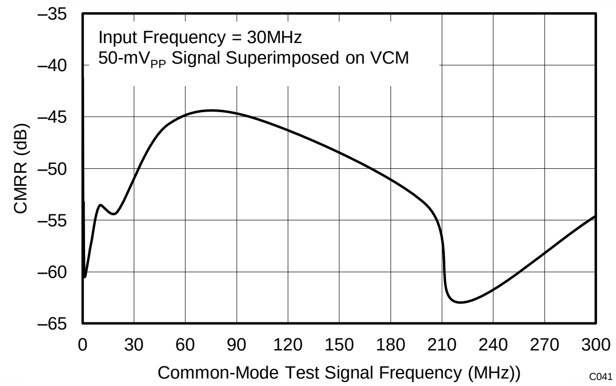
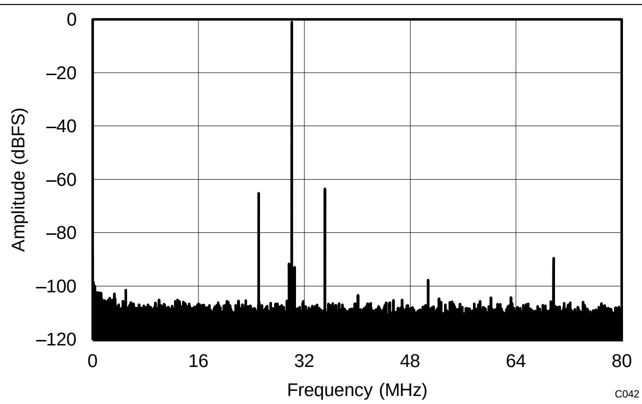


Figure 134. CMRR vs Test Signal Frequency



f_S = 160 MSPS, f_{PSRR} = 5 MHz, 50 mV_{PP}, f_{IN} = 30 MHz, Amplitude (f_{IN} + f_{PSRR}) = –65 dBFS, Amplitude (f_{IN} – f_{PSRR}) = –67 dBFS

Figure 135. PSRR FFT for AVDD Supply

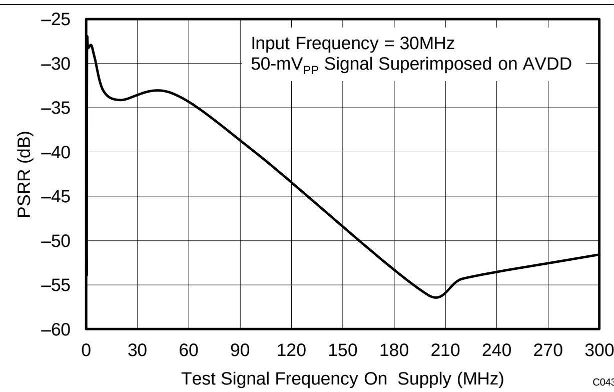


Figure 136. PSRR vs Test Signal Frequency

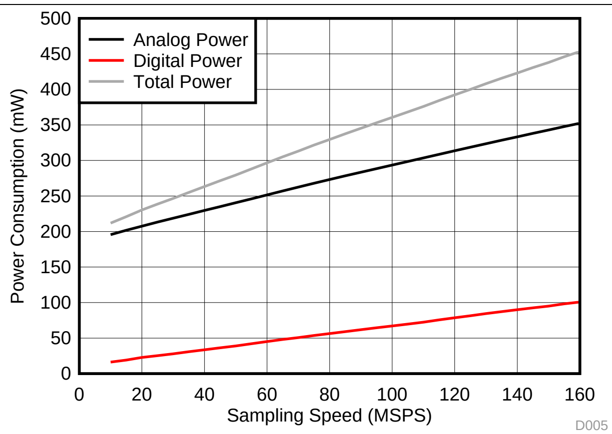


Figure 137. Power vs Sampling Frequency 20X Mode

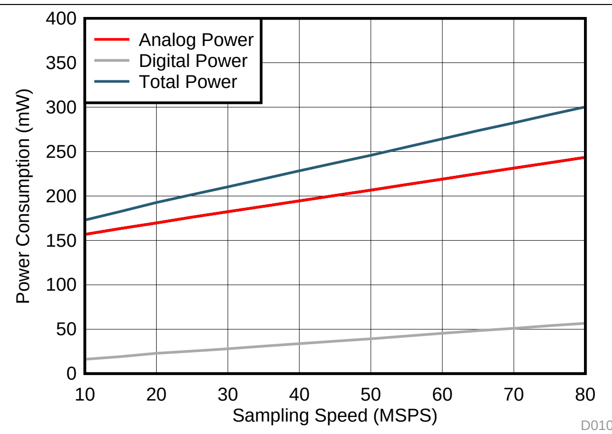


Figure 138. Power vs Sampling Frequency 40X Mode

7.19 Typical Characteristics: Contour Plots

Typical values are at T_A= 25°C, 50% clock duty cycle, AVDD = DVDD = 1.8 V, –1-dBFS differential input, 2-V_{PP} full-scale, and 32k-point FFT, unless otherwise noted.

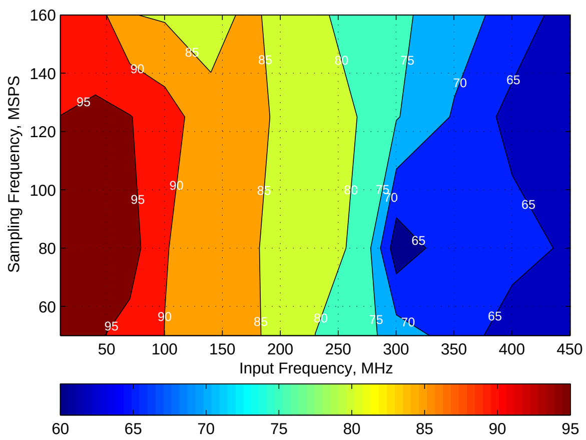


Figure 139. Spurious-Free Dynamic Range (SFDR) for 0-dB Gain

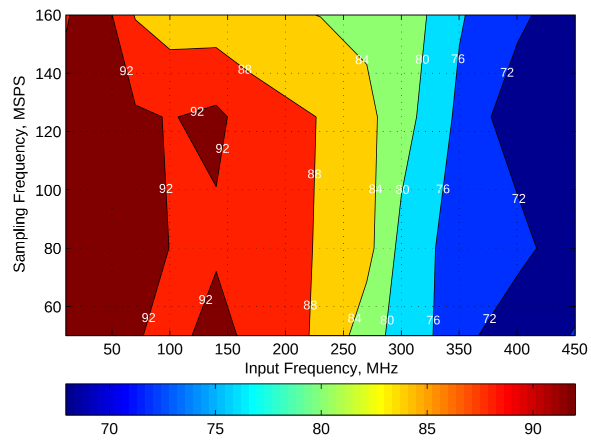


Figure 140. Spurious-Free Dynamic Range (SFDR) for 6-dB Gain

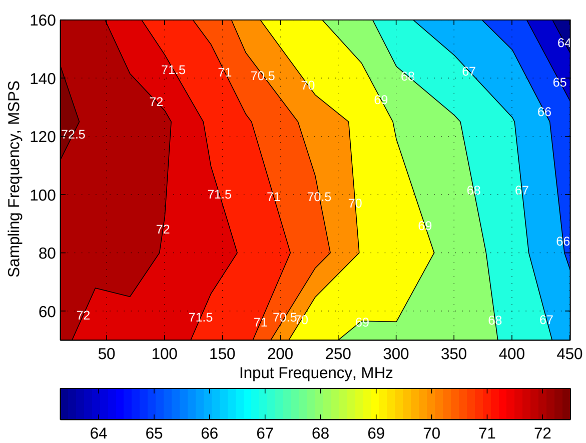


Figure 141. Signal-to-Noise Ratio (SNR) for 0-dB Gain

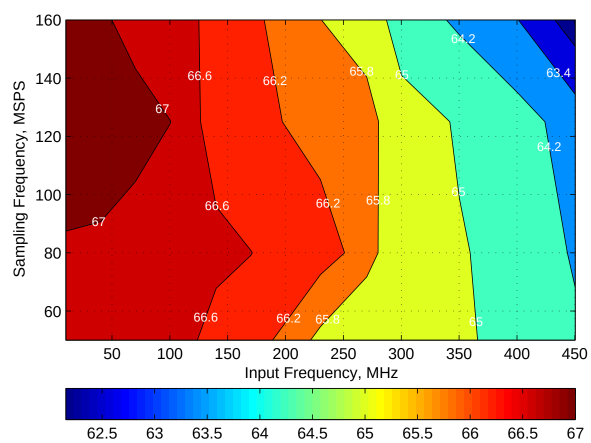
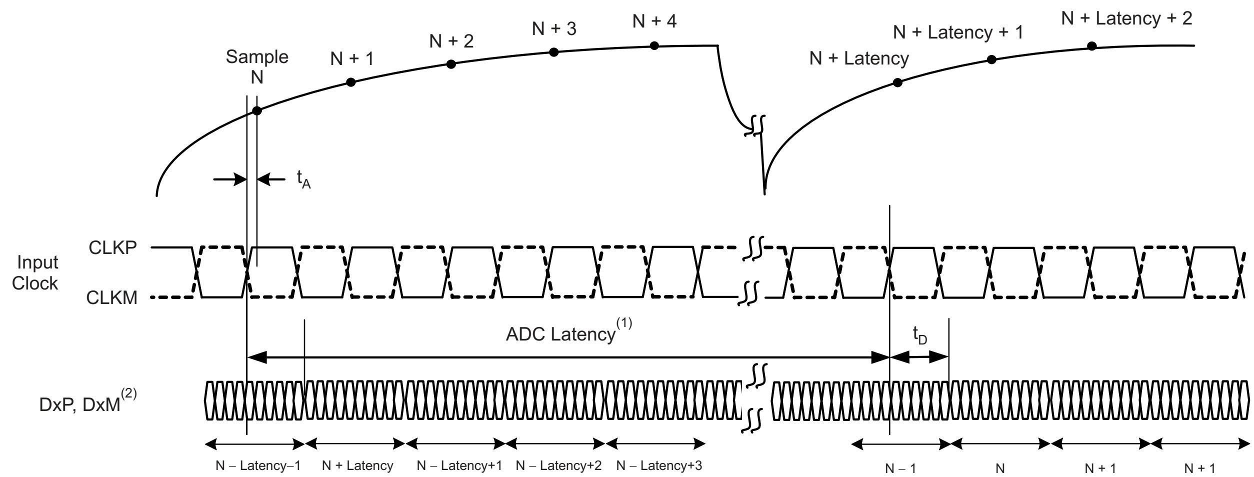


Figure 142. Signal-to-Noise Ratio (SNR) for 6-dB Gain

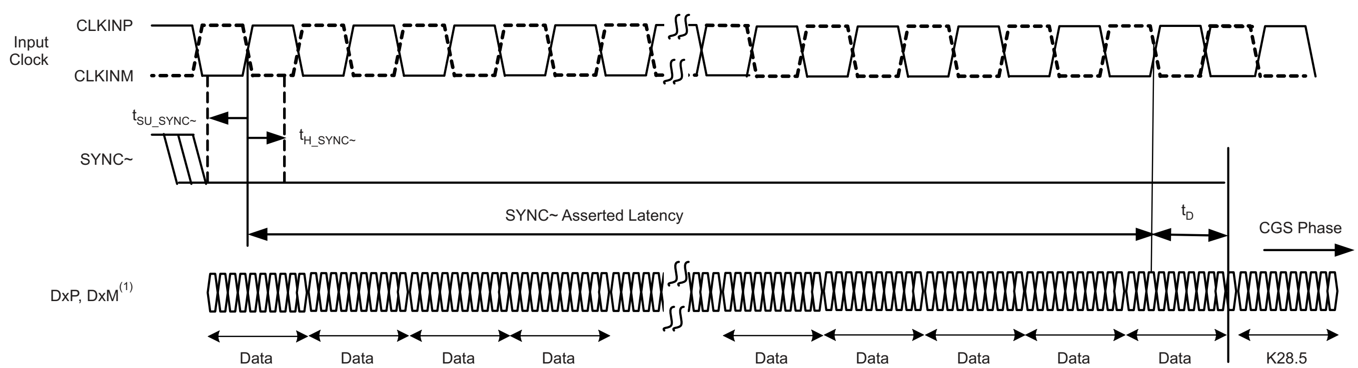
8 Parameter Measurement Information

8.1 Timing Diagrams



(1) Overall latency = ADC latency + t_D.
(2) x = A for channel A and B for channel B.

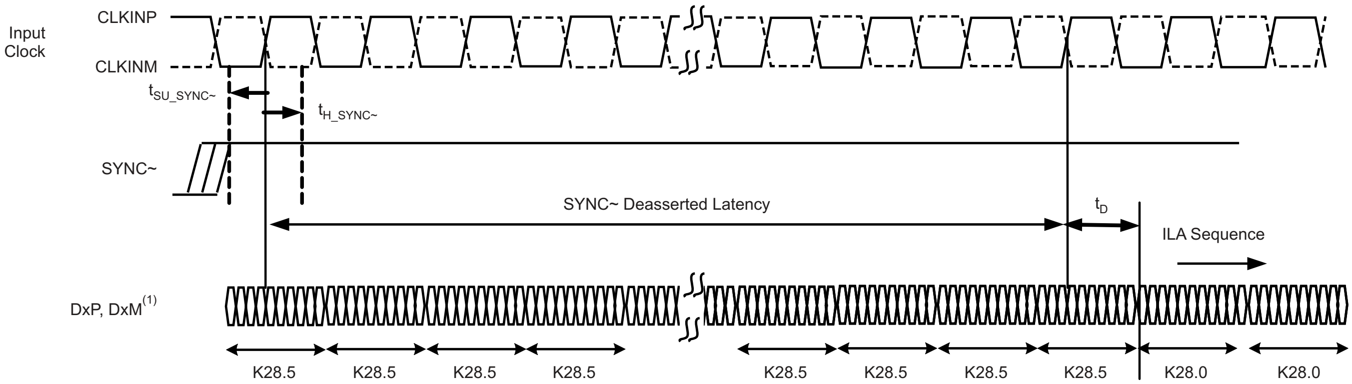
Figure 143. ADC Latency



(1) x = A for channel A and B for channel B.

Figure 144. SYNC~ Latency in CGS Phase

Timing Diagrams (continued)



(1) x = A for channel A and B for channel B.

Figure 145. SYNC~ Latency in ILAS Phase

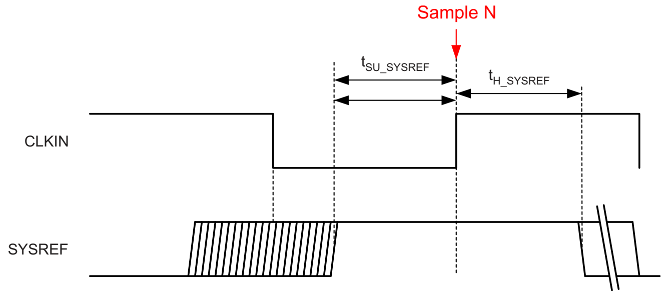


Figure 146. SYSREF Timing (Subclass 1)

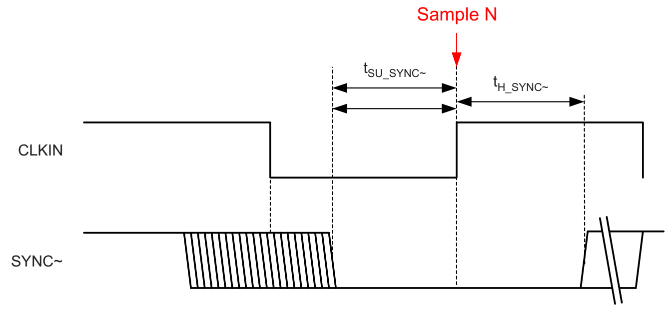


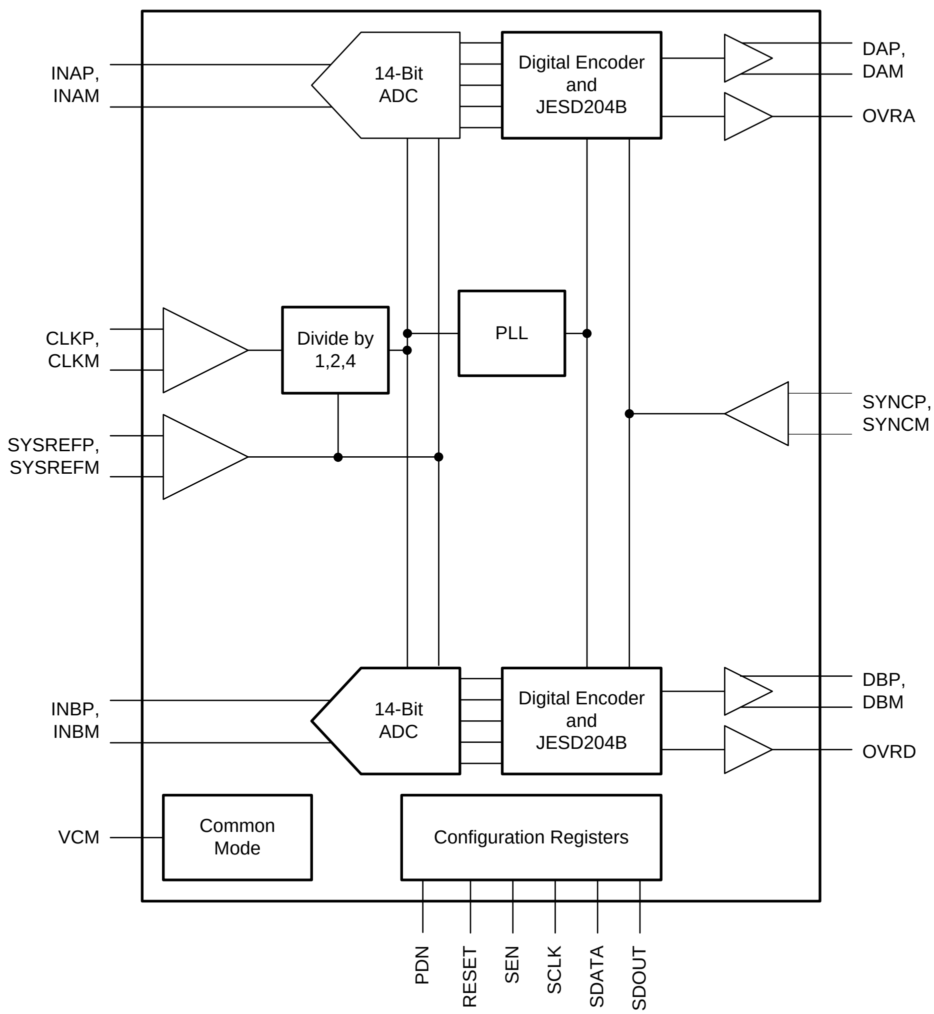
Figure 147. SYNC~ Timing (Subclass 2)

9 Detailed Description

9.1 Overview

The ADC32J4x are a high-linearity, ultra-low power, dual-channel, 14-bit, 50-MSPS to 160-MSPS, analog-to-digital converter (ADC) family. The devices are designed specifically to support demanding, high input frequency signals with large dynamic range requirements. A clock input divider allows more flexibility for system clock architecture design ans the SYSREF input enables complete system synchronization. The ADC32J4x family supports JESD204B interface in order to reduce the number of interface lines, thus allowing for high system integration density. The JESD204B interface is a serial interface, where the data of each ADC are serialized and output over only one differential pair. An internal phase-locked loop (PLL) multiplies the incoming ADC sampling clock by 20 to derive the bit clock, which is used to serialize the 14-bit data from each channel. The ADC32J4x devices support subclass 0, 1, and 2 with interface data rates up to 3.2 Gbps.

9.2 Functional Block Diagram



9.3 Feature Description

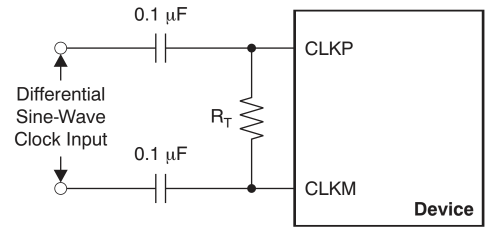
9.3.1 Analog Inputs

The ADC32J4x analog signal inputs are designed to be driven differentially. Each input pin (INP, INM) must swing symmetrically between (VCM + 0.5 V) and (VCM – 0.5 V), resulting in a 2-V_{PP} (default) differential input swing. The input sampling circuit has a 3-dB bandwidth that extends up to 450 MHz (50-Ω source driving a 50-Ω termination between INP and INM).

Feature Description (continued)

9.3.2 Clock Input

The device clock inputs can be driven differentially (sine, LVPECL, or LVDS) or single-ended (LVCMOS), with little or no difference in performance between them. The common-mode voltage of the clock inputs is set to 1.4 V using internal 5-kΩ resistors. The self-bias clock inputs of the ADC32J4x can be driven by the transformer-coupled, sine-wave clock source or by the ac-coupled, LVPECL and LVDS clock sources, as shown in Figure 148, Figure 149, and Figure 150. See Figure 151 for details regarding the internal clock buffer.



NOTE: R_T = termination resistor, if necessary.

Figure 148. Differential Sine-Wave Clock Driving Circuit

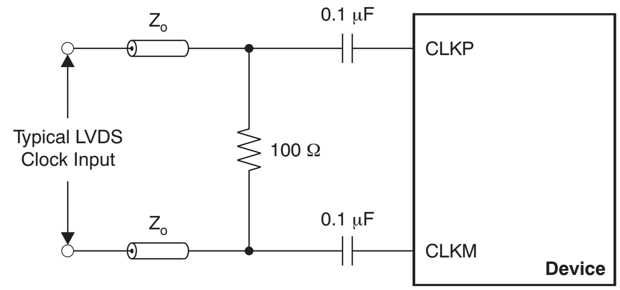


Figure 149. LVDS Clock Driving Circuit

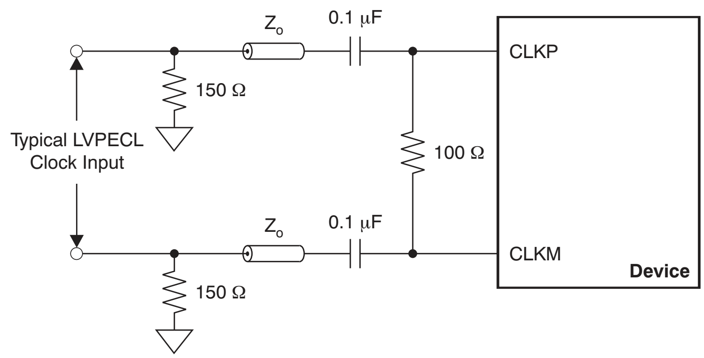
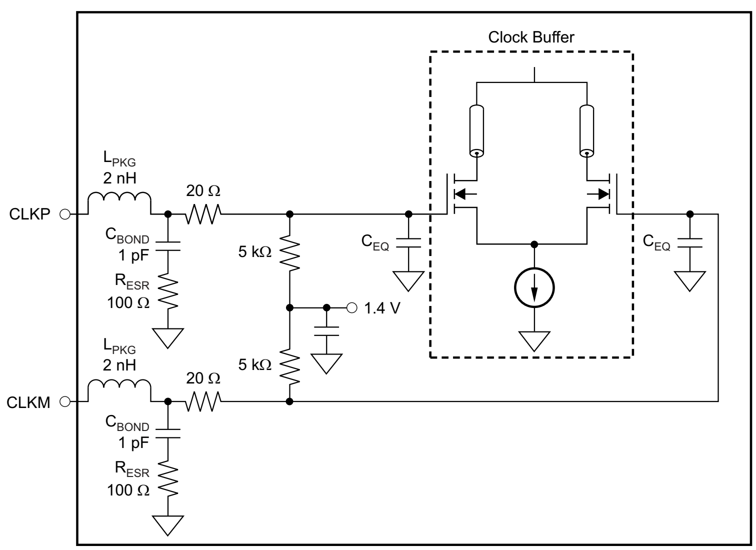


Figure 150. LVPECL Clock Driving Circuit



NOTE: C_{EQ} is 1 pF to 3 pF and is the equivalent input capacitance of the clock buffer.

Figure 151. Internal Clock Buffer

A single-ended CMOS clock can be ac-coupled to the CLKP input, with CLKM connected to ground with a 0.1-µF capacitor, as shown in Figure 152. However, the clock inputs must be driven differentially for best performance, thereby reducing susceptibility to common-mode noise. For high input frequency sampling, TI recommends using a clock source with very low jitter. Band-pass filtering of the clock source can help reduce the effects of jitter. There is no change in performance with a non-50% duty cycle clock input.

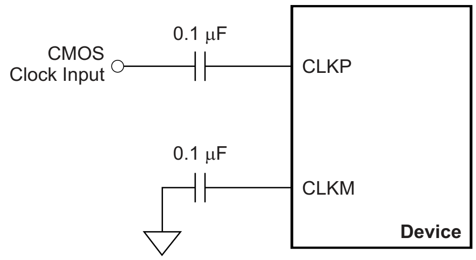


Figure 152. Single-Ended Clock Driving Circuit

9.3.2.1 SNR and Clock Jitter

The signal-to-noise ratio of the ADC is limited by three different factors: quantization noise, thermal noise, and jitter noise, as shown in Equation 1. Quantization noise is typically not noticeable in pipeline converters and is 86 dB for a 14-bit ADC. Thermal noise limits SNR at low input frequencies and the clock jitter sets SNR for higher input frequencies.

$$SNR_{ADC}[dBc] = -20 \cdot \log \sqrt{\left(10^{-\frac{SNR_{Quantizatoin\ Noise}}{20}}\right)^2 + \left(10^{-\frac{SNR_{Thermal\ Noise}}{20}}\right)^2 + \left(10^{-\frac{SNR_{Jitter}}{20}}\right)^2} \quad (1)$$

The SNR limitation resulting from sample clock jitter can be calculated with Equation 2:

$$SNR_{Jitter}[dBc] = -20 \cdot \log(2\pi \cdot f_{in} \cdot T_{Jitter}) \quad (2)$$

The total clock jitter (T_{Jitter}) has two components: the internal aperture jitter (200 fs for the device), is set by the noise of the clock input buffer, and the external clock. T_{Jitter} can be calculated with Equation 3:

$$T_{Jitter} = \sqrt{(T_{Jitter,Ext.Clock\_Input})^2 + (T_{Aperture\_ADC})^2} \quad (3)$$

External clock jitter can be minimized by using high-quality clock sources and jitter cleaners as well as band-pass filters at the clock input, although a faster clock slew rate improves ADC aperture jitter. The devices have a thermal noise of 73.5 dBFS and an internal aperture jitter of 200 fs. The SNR, depending on the amount of external jitter for different input frequencies, is shown in Figure 153.

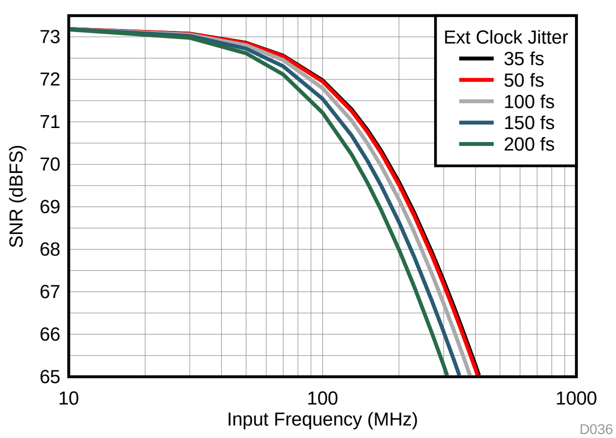


Figure 153. SNR vs Frequency and Jitter

9.3.2.2 Input Clock Divider

The devices are equipped with an internal divider on the clock input. The divider allows operation with a faster input clock, thus simplifying the system clock distribution design. The clock divider can be bypassed (divide-by-1) for operation with a 160-MHz clock; the divide-by-2 option supports a maximum input clock of 320 MHz and the divide-by-4 option supports a maximum input clock frequency of 640 MHz.

9.3.3 Power-Down Control

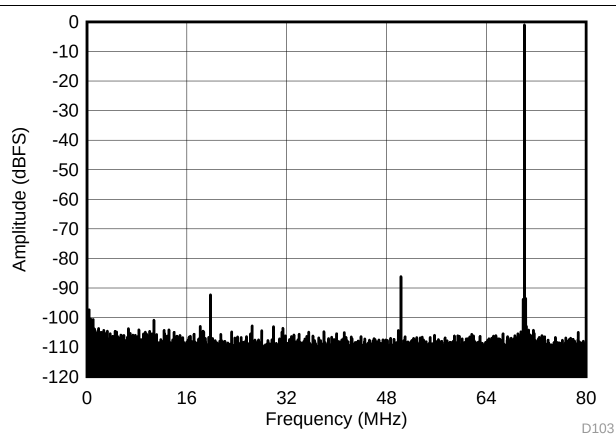
The power-down functions of the ADC32J4x can be controlled either through the parallel control pin (PDN) or through an SPI register setting (see register 15h). The PDN pin can also be configured via SPI to a global power-down or standby functionality, as shown in Table 2.

Table 2. Power-Down Modes

FUNCTION	POWER CONSUMPTION (mW)	WAKE-UP TIME (µs)
Global power-down	5	85
Standby	118	35

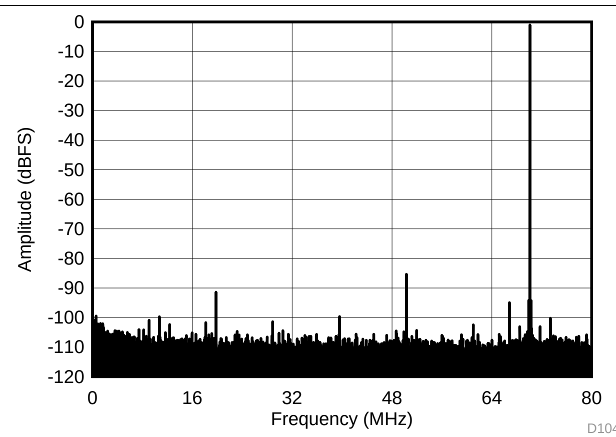
9.3.4 Internal Dither Algorithm

The ADC32J4x uses an internal dither algorithm to achieve high SFDR and a clean spectrum. However, the dither algorithm marginally degrades SNR, creating a trade-off between SNR and SFDR. If desired, the dither algorithm can be turned off by using the DIS DITH CHx registers bits. Figure 154 and Figure 155 show the effect of using dither algorithms.



f_S = 160 MSPS, SNR = 72 dBFS, f_{IN} = 70 MHz, SFDR = 95 dBc

Figure 154. FFT with Dither On



f_S = 160 MSPS, SNR = 72.5 dBFS, f_{IN} = 70 MHz, SFDR = 85 dBc

Figure 155. FFT with Dither Off

9.3.5 JESD204B Interface

The ADC32J4x support device subclass 0, 1, and 2 with a maximum output data rate of 3.2 Gbps for each serial transmitter, as shown in Figure 156. The data of each ADC are serialized by 20X using an internal PLL and then transmitted out on one differential pair each. An external SYSREF (subclass 1) or SYNC~ (subclass 2) signal is used to align all internal clock phases and the local multiframe clock to a specific sampling clock edge. This process allows synchronization of multiple devices in a system and minimizes timing and alignment uncertainty.

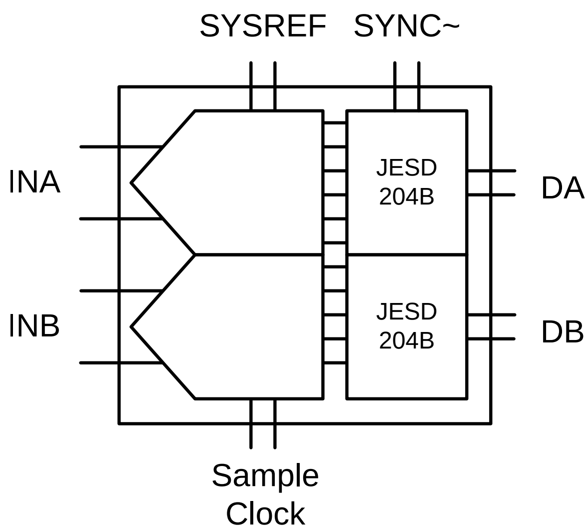


Figure 156. JESD204B Interface

The JESD204B transmitter block consists of the transport layer, the data scrambler, and the link layer, as shown in Figure 157. The transport layer maps the ADC output data into the selected JESD204B frame data format and determines if the ADC output data or test patterns are transmitted. The link layer performs the 8b or 10b data encoding and the synchronization and initial lane alignment using the SYNC~ input signal. Optionally, data from the transport layer can be scrambled.

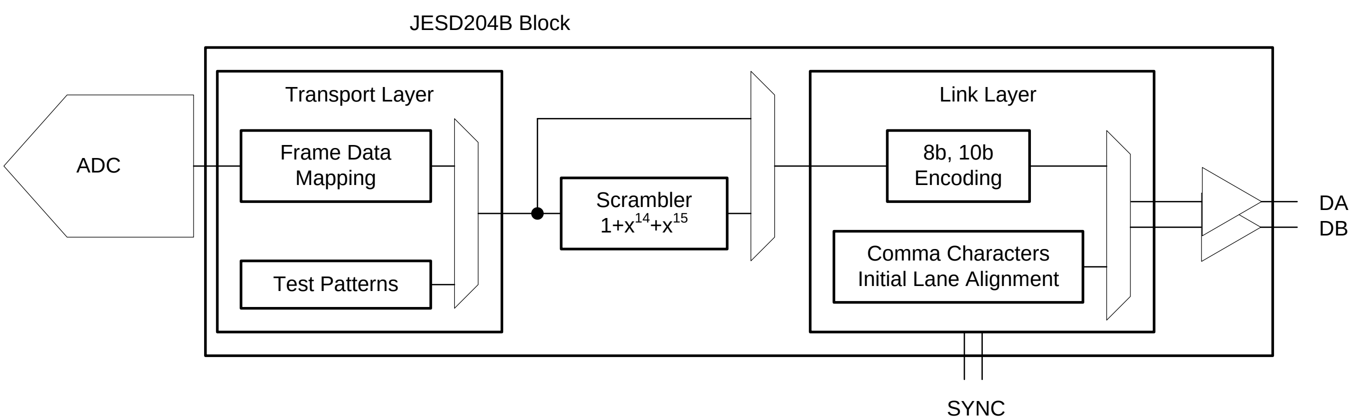


Figure 157. JESD204B Block

9.3.5.1 JESD204B Initial Lane Alignment (ILA)

The initial lane alignment process is started by the receiving device by asserting the SYNC~ signal. When a logic high is detected on the SYNC~ input pins, the ADC32J4x starts transmitting comma (K28.5) characters to establish code group synchronization. When synchronization is complete, the receiving device de-asserts the SYNC~ signal and the ADC32J4x starts the initial lane alignment sequence with the next local multiframe clock boundary. The ADC32J4x transmits four multiframes, each containing K frames (K is SPI programmable). Each multiframe contains the frame start and end symbols; the second multiframe also contains the JESD204 link configuration data.

9.3.5.2 JESD204B Test Patterns

There are three different test patterns available in the transport layer of the JESD204B interface. The ADC32J4x supports a clock output, an encoded, and a PRBS (2^{15} – 1) pattern. These patterns can be enabled via SPI register writes and are located in address 26h (bits 7-6).

9.3.5.3 JESD204B Frame Assembly

The JESD204B standard defines the following parameters:

- L is the number of lanes per link,
- M is the number of converters per device,
- F is the number of octets per frame clock period, and
- S is the number of samples per frame.

Table 3 lists the available JESD204B format and valid range for the ADC32J4x. The ranges are limited by the SERDES line rate and the maximum ADC sample frequency.

Table 3. LMFS Values and Interface Rate

L	M	F	S	MINIMUM ADC SAMPLING RATE (MSPS)	MAXIMUM f_{SERDES} (Mbps)	MAXIMUM ADC SAMPLING RATE (Msps)	MAXIMUM f_{SERDES} (GSPS)	MODE
2	2	2	1	15	300	160	3.2	20X (default)
1	2	4	1	10	400	80	3.2	40X

The detailed frame assembly for quad-channel mode is shown in Figure 158. The frame assembly configuration can be changed from 20X (default) to 40X by setting the registers listed in Table 4.

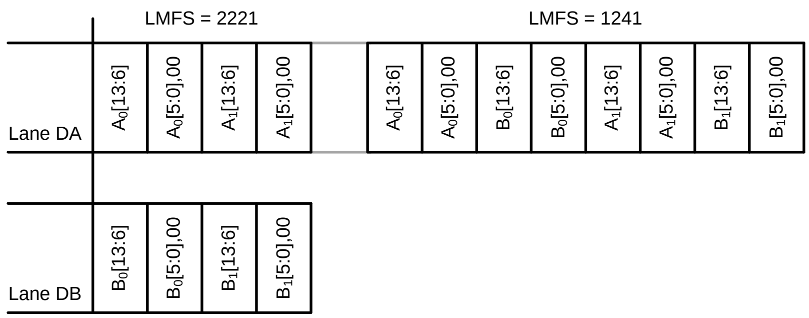


Figure 158. JESD Frame Assembly

Table 4. Configuring 40X Mode

ADDRESS	DATA
2Bh	01h
30h	11h

9.3.5.4 Digital Outputs

The ADC32J4x JESD204B transmitter uses differential CML output drivers. The CML output current is programmable from 5 mA to 20 mA using SPI register settings. The output driver expects to drive a differential 100-Ω load impedance and the termination resistors must be placed as close to the receiver inputs as possible to avoid unwanted reflections and signal distortion. Because the JESD204B employs 8b and 10b encoding, the output data stream is dc-balanced and ac-coupling can be used to avoid the need to match up common-mode voltages between the transmitter and receivers. Connect the termination resistors to the termination voltage, as shown in Figure 159.

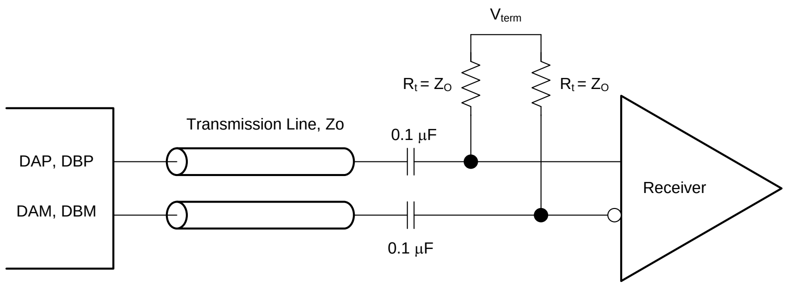


Figure 159. CML Output Connections

Figure 160 shows the data eye measurements of the device JESD204B transmitter against the JESD204B transmitter mask at 3.125 Gbps (156.25 MSPS, 20X mode), respectively.

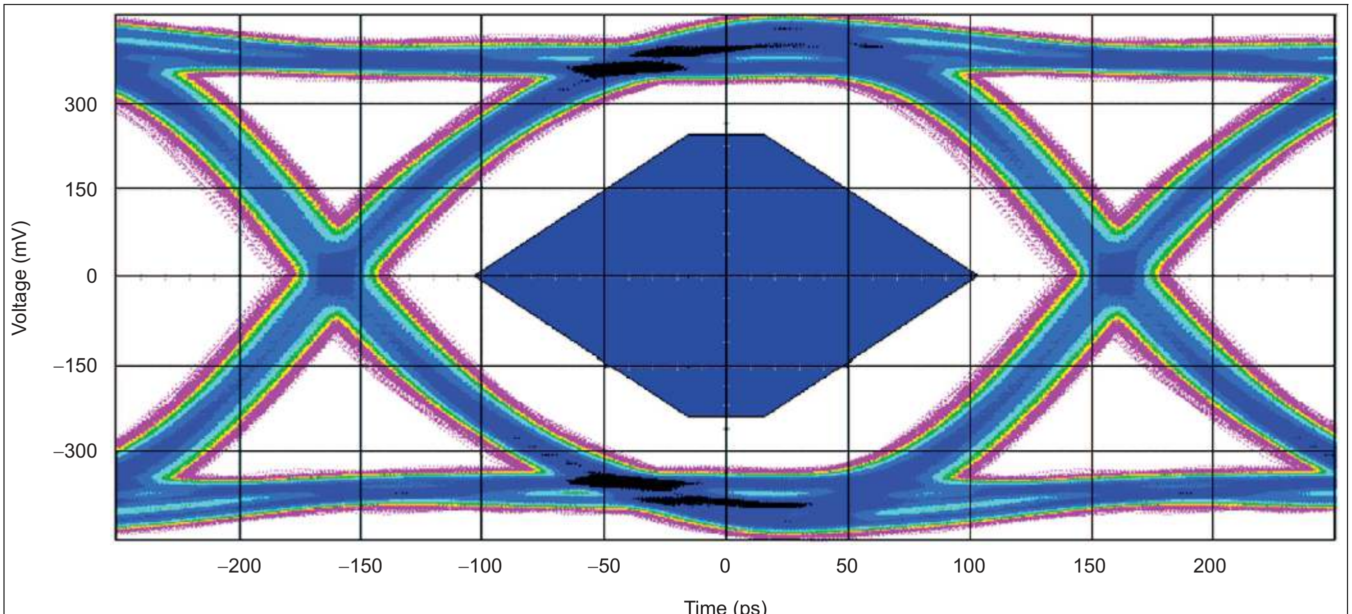


Figure 160. Eye Diagram: 3.125 Gbps

9.4 Device Functional Modes

9.4.1 Digital Gain

The input full-scale amplitude can be selected between 1 V_{PP} to 2 V_{PP} (default is 2 V_{PP}) by choosing the appropriate digital gain setting via an SPI register write. Digital gain provides an option to trade-off SNR for SFDR performance. A larger input full-scale increases SNR performance (2 V_{PP} is recommended for maximum SNR) and a reduced input swing typically results in better SFDR performance. Table 5 lists the available digital gain settings.

Table 5. Digital Gain versus Full-Scale Amplitude

DIGITAL GAIN (dB)	MAX INPUT VOLTAGE (V_{PP})
0	2
0.5	1.89
1	1.78
1.5	1.68
2	1.59
2.5	1.50
3	1.42
3.5	1.34
4	1.26
4.5	1.19
5	1.12
5.5	1.06
6	1.00

9.4.2 Overrange Indication

The ADC32J4x provides two different overrange indications. The normal OVR (default) is triggered if the final 14-bit data output exceeds the maximum code value. The fast OVR is triggered if the input voltage exceeds the programmable overrange threshold and is presented after just nine clock cycles, thus enabling a quicker reaction to an overrange event. By default, the normal overrange indication is output on the OVRA, OVRB pins. The fast OVR indication can be presented on the overrange pins instead by using the SPI register map.

9.5 Programming

The ADC32J4x can be configured using a serial programming interface, as described in this section.

9.5.1 Serial Interface

The device has a set of internal registers that can be accessed by the serial interface formed by the SEN (serial interface enable), SCLK (serial interface clock), SDATA (serial interface data), and SDOUT (serial interface data output) pins. Serially shifting bits into the device is enabled when SEN is low. Serial data SDATA are latched at every SCLK rising edge when SEN is active (low). Serial data are loaded into the register at every 24th SCLK rising edge when SEN is low. When the word length exceeds a multiple of 24 bits, the excess bits are ignored. Data can be loaded in multiples of 24-bit words within a single active SEN pulse. The interface can function with SCLK frequencies from 20 MHz down to very low speeds (of a few hertz) and also with a non-50% SCLK duty cycle.

9.5.1.1 Register Initialization

After power-up, the internal registers must be initialized to their default values through a hardware reset by applying a high pulse on the RESET pin (of durations greater than 10 ns); see Figure 161. If required, the serial interface registers can be cleared during operation either:

1. Through a hardware reset, or
2. By applying a software reset. When using the serial interface, set the RESET bit (D0 in register address 06h) high. This setting initializes the internal registers to the default values and then self-resets the RESET bit low. In this case, the RESET pin is kept low.

9.5.1.1.1 Serial Register Write

The device internal register can be programmed with these steps:

1. Drive the SEN pin low,
2. Set the R/W bit to 0 (bit A15 of the 16-bit address),
3. Set bit A14 in the address field to 1,
4. Initiate a serial interface cycle by specifying the address of the register (A13 to A0) whose content must be written, and
5. Write the 8-bit data that are latched in on the SCLK rising edge.

Programming (continued)

Figure 161 and Table 6 show the timing requirements for the serial register write operation.

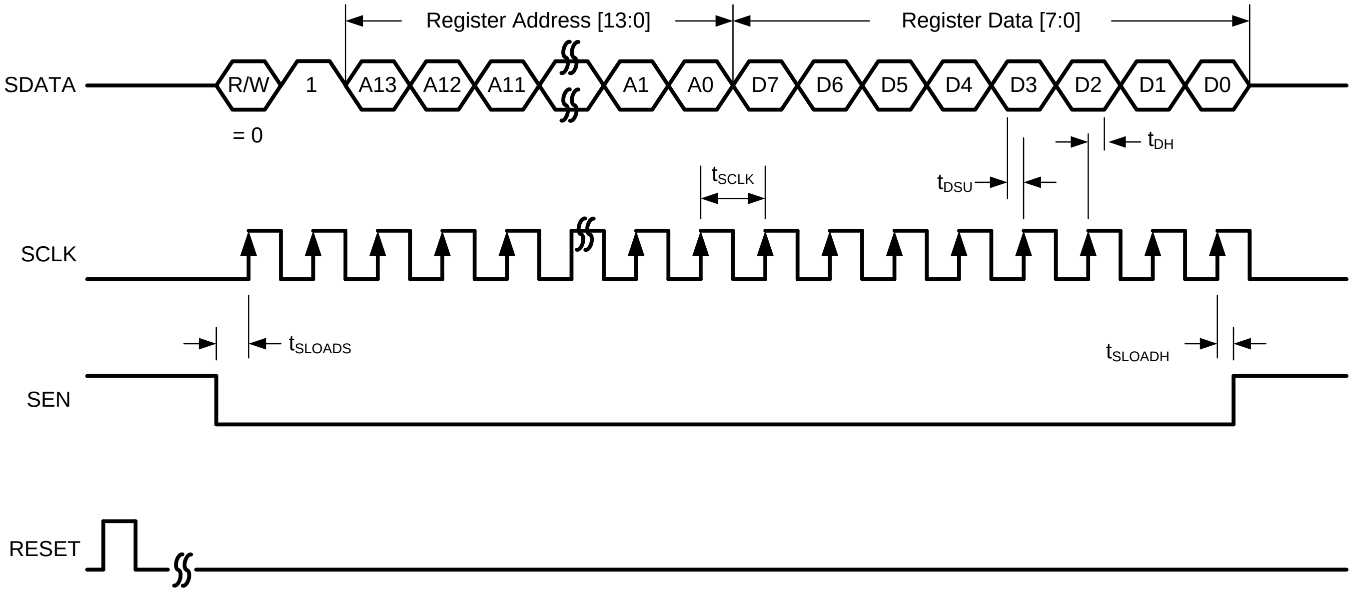


Figure 161. Serial Register Write Timing Diagram

Table 6. Serial Interface Timing(1)

		MIN	TYP	MAX	UNIT
f_{SCLK}	SCLK frequency (equal to 1 / t_{SCLK})	> dc		20	MHz
t_{SLOADS}	SEN to SCLK setup time	25			ns
t_{SLOADH}	SCLK to SEN hold time	25			ns
t_{DSU}	SDIO setup time	25			ns
t_{DH}	SDIO hold time	25			ns

(1) Typical values are at 25°C, full temperature range is from T_{MIN} = –40°C to T_{MAX} = 85°C, and AVDD = DVDD = 1.8 V, unless otherwise noted.

9.5.1.1.2 Serial Register Readout

The device includes a mode where the contents of the internal registers can be read back using the SDOUT pin. This readback mode can be useful as a diagnostic check to verify the serial interface communication between the external controller and the ADC. To read the contents of serial registers, follow this procedure:

1. Drive the SEN pin low.
2. Set the R/W bit (A15) to 1. This setting disables any further writes to the registers.
3. Set bit A14 in the address field to 1.
4. Initiate a serial interface cycle specifying the address of the register (A13 to A0) whose content must be read.
5. The device outputs the contents (D7 to D0) of the selected register on the SDOUT pin.
6. The external controller can latch the contents at the SCLK rising edge.
7. To enable register writes, reset the R/W register bit to 0.

When READOUT is disabled, the SDOUT pin is in a high-impedance mode. If serial readout is not used, the SDOUT pin must float. Figure 162 shows a timing diagram of the serial register read operation. Data appear on the SDOUT pin at the SCLK falling edge with an approximate delay (t_{SD_DELAY}) of 20 ns, as shown in Figure 163.

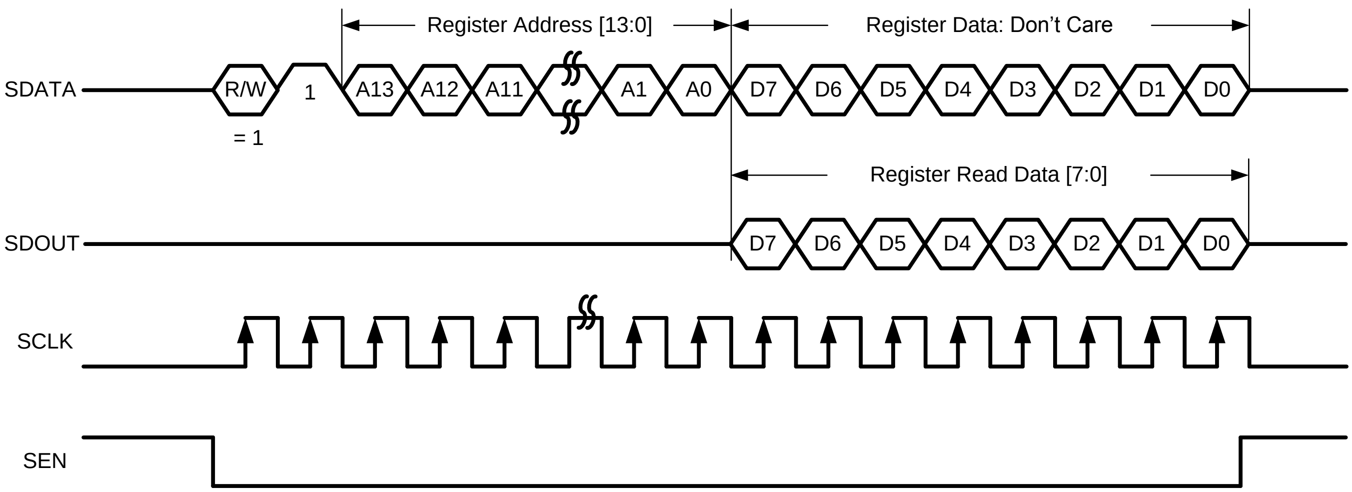


Figure 162. Serial Register Read Timing Diagram

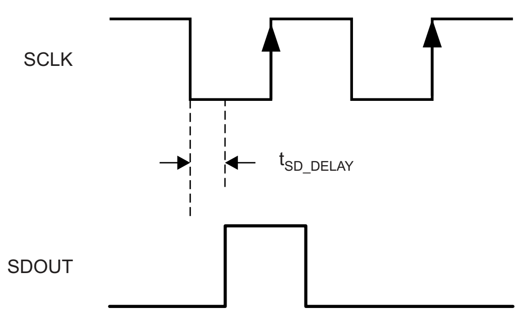


Figure 163. SDOUT Timing Diagram

9.5.2 Register Initialization

After power-up, the internal registers must be initialized to their default values through a hardware reset by applying a high pulse on the RESET pin, as shown in Figure 164 and Table 7.

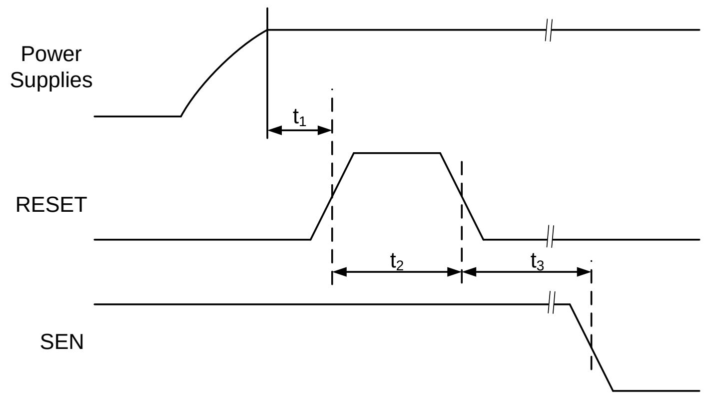


Figure 164. Initialization of Serial Registers after Power-Up

Table 7. Power-Up Timing

		MIN	TYP	MAX	UNIT
t_1	Power-on delay from power-up to an active high RESET pulse	1			ms
t_2	Reset pulse duration: active high RESET pulse duration	10		1000	ns
t_3	Register write delay from RESET disable to SEN active	100			ns

If required, the serial interface registers can be cleared during operation either:

1. Through hardware reset, or
2. By applying a software reset. When using the serial interface, set the RESET bit (D0 in register address 06h) high. This setting initializes the internal registers to the default values and then self-resets the RESET bit low. In this case, the RESET pin is kept low.

9.5.3 Start-Up Sequence

After power-up, the sequence described in Table 8 can be used to set up the ADC32J4x for basic operation.

Table 8. Start-Up Settings

STEP	DESCRIPTION	REGISTER ADDRESS AND DATA
1	Provide all supply voltages. There is no required power-supply sequence for AVDD and DVDD.	—
2	Pulse a hardware reset (low to high to low) on pin 24	—
3	Optionally, configure LMFS of the JESD204B interface to LMFS = 1241 (default is LMFS = 2221)	Address 2Bh, data 01h Address 30h, data 11h
4	Pulse SYNC~ from high to low to transmit data from K28.5 SYNC~ mode	—

9.6 Register Maps

Table 9. Register Map Summary

<table>
<tr><th>REGISTER ADDRESS</th><th colspan="7">REGISTER DATA</th><th></th></tr>
<tr><th>A[13:0] (Hex)</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td>01</td><td>0</td><td>0</td><td colspan="2">DIS DITHER CHA</td><td colspan="2">DIS DITHER CHB</td><td>0</td><td>0</td></tr>
<tr><td>03</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>CHA GAINEN</td><td>0</td></tr>
<tr><td>04</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>CHB GAINEN</td><td>0</td></tr>
<tr><td>06</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>TEST PATTERN EN</td><td>RESET</td></tr>
<tr><td>07</td><td>0</td><td>0</td><td>0</td><td colspan="3">SPECIAL MODE1 CHA</td><td>EN FOVR</td><td>0</td></tr>
<tr><td>08</td><td>0</td><td>0</td><td>0</td><td colspan="3">SPECIAL MODE1 CHB</td><td>0</td><td>0</td></tr>
<tr><td>09</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>ALIGN TEST PATTERN</td><td>DATA FORMAT</td></tr>
<tr><td>0A</td><td>0</td><td>0</td><td>0</td><td>0</td><td colspan="4">CHA TEST PATTERN</td></tr>
<tr><td>0B</td><td colspan="4">CHB TEST PATTERN</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>0C</td><td>0</td><td>0</td><td>0</td><td>0</td><td colspan="4">CHA DIGITAL GAIN</td></tr>
<tr><td>0D</td><td colspan="4">CHB DIGITAL GAIN</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>0E</td><td colspan="8">CUSTOM PATTERN[13:6]</td></tr>
<tr><td>0F</td><td colspan="5">CUSTOM PATTERN[5:0]</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>13</td><td>LOW SPEED MODE</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>15</td><td>0</td><td>CHA PDN</td><td>CHB PDN</td><td>0</td><td>STANDBY</td><td>GLOBAL PDN</td><td>0</td><td>CONFIG PDN PIN</td></tr>
<tr><td>27</td><td colspan="2">CLK DIV</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>2A</td><td colspan="2">SERDES TEST PATTERN</td><td>IDLE SYNC</td><td>TRP LAYER TESTMODE EN</td><td>FLIP ADC DATA</td><td>LANE ALIGN</td><td>FRAME ALIGN</td><td>TXMIT LINKDATA DIS</td></tr>
<tr><td>2B</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>CTRL K</td><td>CTRL F</td></tr>
<tr><td>2F</td><td>SCRAMBLE EN</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>30</td><td colspan="8">OCTETS PER FRAME</td></tr>
<tr><td>31</td><td>0</td><td>0</td><td>0</td><td colspan="5">FRAMES PER MULTIFRAME</td></tr>
<tr><td>34</td><td colspan="3">SUBCLASSV</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>3A</td><td>SYNC REG</td><td>SYNC REQ EN</td><td>0</td><td>0</td><td colspan="4">OUTPUT CURRENT SEL</td></tr>
<tr><td>3B</td><td colspan="3">LINK LAYER TESTMODE SEL[2:0]</td><td>LINK LAYER RPAT</td><td>0</td><td colspan="3">PULSE DET MODES</td></tr>
<tr><td>3C</td><td>FORCE LMFC COUNT</td><td colspan="5">LMFC COUNT INIT</td><td colspan="2">RELEASE ILANE SEQ</td></tr>
<tr><td>422</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>SPECIAL MODE2 CHA</td><td>0</td></tr>
<tr><td>434</td><td>0</td><td>0</td><td>DIS DITH CHA</td><td>0</td><td>DIS DITH CHA</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>522</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>SPECIAL MODE2 CHB</td><td>0</td></tr>
<tr><td>534</td><td>0</td><td>0</td><td>DIS DITH CHB</td><td>0</td><td>DIS DITH CHB</td><td>0</td><td>0</td><td>0</td></tr>
</table>

9.6.1 Summary of Special Mode Registers

Table 10 lists the location, value, and functions of special mode registers in the device.

Table 10. Special Modes Summary

MODE		LOCATION	VALUE AND FUNCTION
Dither mode	DIS DITH CHA	01h (bits 5-4), 434h (bits 5, 3)	Creates a noise floor cleaner and improves SFDR; see the *Internal Dither Algorithm* section. 0000 = Dither disabled 1111 = Dither enabled
	DIS DITH CHB	01h (bits 3-2), 534h (bits 5, 3)	
Special mode 1	SPECIAL MODE 1 CHA	07h (bits 4-2)	Use for improved HD3. 000 = Default after reset 010 = Use for frequency < 120 MHz 111 = Use for frequency > 120 MHz
	SPECIAL MODE 1 CHB	08h (bits 4-2)	
Special mode 2	SPECIAL MODE 2 CHA	422h (bits 1-0)	Helps improve HD2. 00 = Default after reset 11 = Improves HD2
	SPECIAL MODE 2 CHB	522h (bits 1-0)	

9.6.2 Serial Register Descriptions

9.6.2.1 Register 01h (address = 01h)

Figure 165. Register 01h

7	6	5	4	3	2	1	0
0	0	DIS DITHER CHA		DIS DITHER CHB		0	0
W-0h	W-0h	R/W-0h		R/W-0h		W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 11. Register 01h Field Descriptions

Bit	Field	Type	Reset	Description
7-6	0	W	0h	Must write 0.
5-4	DIS DITHER CHA	R/W	0h	These bits enable or disable the on-chip dither. Control these bits with bits 5 and 3 of register 434h. 00 = Dither enabled 11 = Dither disabled. Improves SNR by 0.4 dB for input frequencies up to 170 MHz.
3-2	DIS DITHER CHB	R/W	0h	These bits enable or disable the on-chip dither. Control these bits with bits 5 and 3 of register 534h. 00 = Dither enabled 11 = Dither disabled. Improves SNR by 0.4 dB for input frequencies up to 170 MHz.
1-0	0	W	0h	Must write 0.

9.6.2.2 Register 03h (address = 03h)

Figure 166. Register 03h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	CHA GAINEN	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 12. Register 03h Field Descriptions

Bit	Field	Type	Reset	Description
7-2	0	W	0h	Must write 0.
1	CHA GAINEN	R/W	0h	Digital gain enable bit for channel A. 0 = Digital gain disabled 1 = Digital gain enabled
0	0	W	0h	Must write 0.

9.6.2.3 Register 04h (address = 04h)

Figure 167. Register 04h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	CHB GAINEN	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 13. Register 04h Field Descriptions

Bit	Field	Type	Reset	Description
7-2	0	W	0h	Must write 0.
1	CHB GAINEN	R/W	0h	Digital gain enable bit for channel B. 0 = Digital gain disabled 1 = Digital gain enabled
0	0	W	0h	Must write 0.

9.6.2.4 Register 06h (address = 06h)

Figure 168. Register 06h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	TEST PATTERN EN	RESET
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 14. Register 06h Field Descriptions

Bit	Field	Type	Reset	Description
7-2	0	W	0h	Must write 0.
1	TEST PATTERN EN	R/W	0h	This bit enables the test pattern selection for the digital outputs. 0 = Normal operation 1 = Test pattern output enabled
0	RESET	R/W	0h	Software reset applied. This bit resets all internal registers to the default values and self-clears to 0.

9.6.2.5 Register 07h (address = 07h)

Figure 169. Register 07h

7	6	5	4	3	2	1	0
0	0	0	SPECIAL MODE1 CHA			EN FOVR	0
W-0h	W-0h	W-0h	R/W-0h			R/W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after

Table 15. Register 07h Field Descriptions

Bit	Field	Type	Reset	Description
7-5	0	W	0h	Must write 0.
4-2	SPECIAL MODE1 CHA	R/W	0h	010 = For frequencies < 120 MHz 111 = For frequencies > 120 MHz
1	EN FOVR	R/W	0h	0 = Normal OVR on OVRx pins 1 = Enable fast OVR on OVRx pins
0	0	W	0h	Must write 0.

9.6.2.6 Register 08h (address = 08h)

Figure 170. Register 08h

7	6	5	4	3	2	1	0
0	0	0	SPECIAL MODE1 CHB			0	0
W-0h	W-0h	W-0h	R/W-0h			W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after

Table 16. Register 08h Field Descriptions

Bit	Field	Type	Reset	Description
7-5	0	W	0h	Must write 0.
4-2	SPECIAL MODE1 CHB	R/W	0h	010 = For frequencies < 120 MHz 111 = For frequencies > 120 MHz
1-0	0	W	0h	Must write 0.

9.6.2.7 Register 09h (address = 09h)

Figure 171. Register 09h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	ALIGN TEST PATTERN	DATA FORMAT
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after

Table 17. Register 09h Field Descriptions

Bit	Field	Type	Reset	Description
7-2	0	W	0h	Must write 0.
1	ALIGN TEST PATTERN	R/W	0h	This bit aligns test patterns across the outputs of the four channels. 0 = Test patterns of four channels are free-running 1 = Test patterns of all four channels are aligned
0	DATA FORMAT	R/W	0h	This bit sets the digital output data format. 0 = Twos complement 1 = Offset binary

9.6.2.8 Register 0Ah (address = 0Ah)

Figure 172. Register 0Ah

7	6	5	4	3	2	1	0
0	0	0	0	CHA TEST PATTERN			
W-0h	W-0h	W-0h	W-0h	R/W-0h			

LEGEND: R/W = Read/Write; W = Write only; -n = value after

Table 18. Register 0Ah Field Descriptions

Bit	Field	Type	Reset	Description
7-4	0	W	0h	Must write 0.
3-0	CHA TEST PATTERN	R/W	0h	These bits control the test pattern for channel A after the TEST PATTERN EN bit is set. 0000 = Normal operation 0001 = All 0's 0010 = All 1's 0011 = Toggle pattern: data alternate between 10101010101010 and 01010101010101. 0100 = Digital ramp: data increment by 1 LSB every clock cycle from code 0 to 16383. 0101 = Custom pattern: output data are the same as programmed by the CUSTOM PATTERN register bits. 0110 = Deskew pattern: data are 3AAAh. 1000 = PRBS pattern: data are a sequence of pseudo random numbers. 1001 = 8-point sine-wave: data are a repetitive sequence of the following eight numbers that form a sine-wave: 0, 2399, 8192, 13984, 16383, 13984, 8192, and 2399. Others = Do not use

9.6.2.9 Register 0Bh (address = 0Bh)

Figure 173. Register 0Bh

7	6	5	4	3	2	1	0
CHB TEST PATTERN				0	0	0	0
R/W-0h				W-0h	W-0h	W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after

Table 19. Register 0Bh Field Descriptions

Bit	Field	Type	Reset	Description
7-4	CHB TEST PATTERN	R/W	0h	These bits control the test pattern for channel B after the TEST PATTERN EN bit is set. 0000 = Normal operation 0001 = All 0's 0010 = All 1's 0011 = Toggle pattern: data alternate between 10101010101010 and 01010101010101. 0100 = Digital ramp: data increment by 1 LSB every clock cycle from code 0 to 16383. 0101 = Custom pattern: output data are the same as programmed by the CUSTOM PATTERN register bits. 0110 = Deskew pattern: data are 3AAAh. 1000 = PRBS pattern: data are a sequence of pseudo random numbers. 1001 = 8-point sine-wave: data are a repetitive sequence of the following eight numbers that form a sine-wave: 0, 2399, 8192, 13984, 16383, 13984, 8192, and 2399. Others = Do not use
3-0	0	W	0h	Must write 0.

9.6.2.10 Register 0Ch (address = 0Ch)

Figure 174. Register 0Ch

7	6	5	4	3	2	1	0
0	0	0	0	CHA DIGITAL GAIN			
W-0h	W-0h	W-0h	W-0h	R/W-0h			

LEGEND: R/W = Read/Write; W = Write only; -n = value after

Table 20. Register 0Ch Field Descriptions

Bit	Field	Type	Reset	Description
7-4	0	W	0h	Must write 0.
3-0	CHA DIGITAL GAIN	R/W	0h	These bits set the digital gain for individual channels. Register settings are listed in Table 21.

Table 21. Channel Digital Gain

REGISTER VALUE	DIGITAL GAIN (dB)	MAXIMUM INPUT VOLTAGE (V_{PP})
0000	0	2.0
0001	0.5	1.89
0010	1	1.78
0011	1.5	1.68
0100	2	1.59
0101	2.5	1.50
0110	3	1.42
0111	3.5	1.34
1000	4	1.26
1001	4.5	1.19
1010	5	1.12
1011	5.5	1.06
1100	6	1.00

9.6.2.11 Register 0Dh (address = 0Dh)

Figure 175. Register 0Dh

7	6	5	4	3	2	1	0
CHB DIGITAL GAIN				0	0	0	0
R/W-0h				W-0h	W-0h	W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after

Table 22. Register 0Dh Field Descriptions

Bit	Field	Type	Reset	Description
7-4	CHB DIGITAL GAIN	R/W	0h	These bits set the digital gain for the individual channels. Register settings are listed in Table 21.
3-0	0	W	0h	Must write 0.

9.6.2.12 Register 0Eh (address = 0Eh)

Figure 176. Register 0Eh

7	6	5	4	3	2	1	0
CUSTOM PATTERN[13:6]							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after

Table 23. Register 0Eh Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CUSTOM PATTERN[13:6]	R/W	0h	These bits set the custom pattern[13:6] for all channels.

9.6.2.13 Register 0Fh (address = 0Fh)

Figure 177. Register 0Fh

7	6	5	4	3	2	1	0
CUSTOM PATTERN[5:0]						0	0
R/W-0h						W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after

Table 24. Register 0Fh Field Descriptions

Bit	Field	Type	Reset	Description
7-2	CUSTOM PATTERN[5:0]	R/W	0h	These bits set the custom pattern[5:0] for all channels.
1-0	0	W	0h	Must write 0.

9.6.2.14 Register 13h (address = 13h)

Figure 178. Register 13h

7	6	5	4	3	2	1	0
LOW SPEED MODE	0	0	0	0	0	0	0
R/W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after

Table 25. Register 13h Field Descriptions

Bit	Field	Type	Reset	Description
7	LOW SPEED MODE	R/W	0h	Use this bit for sampling frequencies < 25 MSPS. 0 = Normal operation 1 = Low-speed mode is enabled
6-0	0	W	0h	Must write 0.

9.6.2.15 Register 15h (address = 15h)

Figure 179. Register 15h

7	6	5	4	3	2	1	0
0	CHA PDN	CHB PDN	0	STANDBY	GLOBAL PDN	0	PDN PIN DISABLE
W-0h	R/W-0h	R/W-0h	W-0h	R/W-0h	R/W-0h	W-0h	R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after

Table 26. Register 15h Field Descriptions

Bit	Field	Type	Reset	Description
7	0	W	0h	Must write 0.
6	CHA PDN	R/W	0h	Power-down channel A. 0 = Normal operation 1 = Power-down channel A if the PDN PIN DISABLE register bit is set
5	CHB PDN	R/W	0h	Power-down channel B. 0 = Normal operation 1 = Power-down channel B if the PDN PIN DISABLE register bit is set
4	0	W	0h	Must write 0.
3	STANDBY	R/W	0h	ADCs of both channels enter standby. 0 = Normal operation 1 = Standby
2	GLOBAL PDN	R/W	0h	Global power-down. 0 = Normal operation 1 = Global power-down
1	0	W	0h	Must write 0.
0	PDN PINDISABLE	R/W	0h	This bit disables the power-down control from the pin. 0 = Normal operation 1 = Power-down pin is disabled; use register settings for power-down operations

9.6.2.16 Register 27h (address = 27h)

Figure 180. Register 27h

7	6	5	4	3	2	1	0
CLK DIV		0	0	0	0	0	0
R/W-0h		W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after

Table 27. Register 27h Field Descriptions

Bit	Field	Type	Reset	Description
7-6	CLK DIV	R/W	0h	Internal clock divider for the input sample clock. 00 = Clock divider bypassed 01 = Divide-by-1 10 = Divide-by-2 11 = Divide-by-4
5-0	0	W	0h	Must write 0.

9.6.2.17 Register 2Ah (address = 2Ah)

Figure 181. Register 2Ah

7	6	5	4	3	2	1	0
SERDES TEST PATTERN		IDLE SYNC	TRP LAYER TESTMODE EN	FLIP ADC DATA	LANE ALIGN	FRAME ALIGN	TX LINK CONFIG DATA DIS
R/W-0h		R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after

Table 28. Register 2Ah Field Descriptions

Bit	Field	Type	Reset	Description
7-6	SERDES TEST PATTERN	R/W	0h	00 = Normal operation 01 = Outputs clock pattern: output is 10101010 10 = Encoded pattern: output is 1111111100000000 11 = PRBS sequence: output is $2^{15} – 1$
5	IDLE SYNC	R/W	0h	This bit sets the output pattern when SYNC~ is high. 0 = Sync code is K28.5 (BCBCh) 1 = Sync code is BC50h
4	TRP LAYER TESTMODE EN	R/W	0h	This bit generates the long transport layer test pattern mode according to section 5.1.6.3 of the JESD204B specification. 0 = Test mode disabled 1 = Test mode enabled
3	FLIP ADC DATA	R/W	0h	0 = Normal operation 1 = Output data order is reversed: MSB – LSB
2	LANE ALIGN	R/W	0h	This bit inserts a lane alignment character (K28.3) for the receiver to align to the lane boundary per section 5.3.3.5 of the JESD204B specification. 0 = Normal operation 1 = Inserts lane alignment characters
1	FRAME ALIGN	R/W	0h	This bit inserts a frame alignment character (K28.7) for the receiver to align to the lane boundary per section 5.3.3.4 of the JESD204B specification. 0 = Normal operation 1 = Inserts frame alignment characters
0	TX LINK CONFIG DATA DIS	R/W	0h	This bit disables sending the initial link alignment (ILA) sequence when SYNC~ is de-asserted. 0 = Normal operation 1 = ILA disabled

9.6.2.18 Register 2Bh (address = 2Bh)

Figure 182. Register 2Bh

7	6	5	4	3	2	1	0
0	0	0	0	0	0	CTRL K	CTRL F
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after

Table 29. Register 2Bh Field Descriptions

Bit	Field	Type	Reset	Description
7-2	0	W	0h	Must write 0.
1	CTRL K	R/W	0h	Enable bit for the number of frames per multiframe. 0 = Default is 9 (20X mode) frames per multiframe 1 = Frames per multiframe can be set in register 31h
0	CTRL F	R/W	0h	Enable bit for the number of octets per frame. 0 = 20X mode using one lane per ADC (default is F = 2) 1 = Octets per frame can be specified in register 30h

9.6.2.19 Register 2Fh (address = 2Fh)

Figure 183. Register 2Fh

7	6	5	4	3	2	1	0
SCRAMBLE EN	0	0	0	0	0	0	0
R/W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after

Table 30. Register 2Fh Field Descriptions

Bit	Field	Type	Reset	Description
7	SCRAMBLE EN	R/W	0h	Scramble enable bit in the JESD204B interface. 0 = Scrambling disabled 1 = Scrambling enabled
6-0	0	W	0h	Must write 0.

9.6.2.20 Register 30h (address = 30h)

Figure 184. Register 30h

7	6	5	4	3	2	1	0
OCTETS PER FRAME							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after

Table 31. Register 30h Field Descriptions

Bit	Field	Type	Reset	Description
7-0	OCTETS PER FRAME	R/W	0h	These bits set the number of octets per frame (F). 01 = 20X serialization: two octets per frame 11 = 40X serialization: four octets per frame

9.6.2.21 Register 31h (address = 31h)

Figure 185. Register 31h

7	6	5	4	3	2	1	0
0	0	0	FRAMES PER MULTI FRAME				
W-0h	W-0h	W-0h	R/W-0h				

LEGEND: R/W = Read/Write; W = Write only; -n = value after

Table 32. Register 31h Field Descriptions

Bit	Field	Type	Reset	Description
7-5	0	W	0h	Must write 0.
4-0	FRAMES PER MULTI FRAME	R/W	0h	These bits set the number of frames per multiframe. After reset, the default settings for frames per multiframe are: 20X mode: K = 8 For each mode, K must not be set to a lower value.

9.6.2.22 Register 34h (address = 34h)

Figure 186. Register 34h

7	6	5	4	3	2	1	0
SUBCLASSV			0	0	0	0	0
R/W-0h			W-0h	W-0h	W-0h	W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after

Table 33. Register 34h Field Descriptions

Bit	Field	Type	Reset	Description
7-5	SUBCLASSV	R/W	0h	JESD204B subclass setting. 000 = Subclass 0 backward compatibility with JESD204A 001 = Subclass 1 deterministic latency using the SYSREF signal 010 = Subclass 2 deterministic latency using SYNC~ detection
4-0	0	W	0h	Must write 0.

9.6.2.23 Register 3Ah (address = 3Ah)

Figure 187. Register 3Ah

7	6	5	4	3	2	1	0
SYNC REQ	SYNC REQ EN	0	0	OUTPUT CURRENT SEL			
R/W-0h	R/W-0h	W-0h	W-0h	R/W-0h			

LEGEND: R/W = Read/Write; W = Write only; -n = value after

Table 34. Register 3Ah Field Descriptions

Bit	Field	Type	Reset	Description
7	SYNC REQ	R/W	0h	This bit generates a synchronization request only when the SYNC REQ EN register bit is set. 0 = Normal operation 1 = Generates sync request
6	SYNC REQ EN	R/W	0h	0 = Sync request is made with the SYNCP~, SYNCM~ pins 1 = Sync request is made with the SYNC REQ register bit
5-4	0	W	0h	Must write 0.
3-0	OUTPUT CURRENT SEL	R/W	0h	JESD output buffer current selection. 0000 = 16 mA 0001 = 15 mA 0010 = 14 mA 0011 = 13 mA 0100 = 20 mA 0101 = 19 mA 0110 = 18 mA 0111 = 17 mA 1000 = 8 mA 1001 = 7 mA 1010 = 6 mA 1011 = 5 mA 1100 = 12 mA 1101 = 11 mA 1110 = 10 mA 1111 = 9 mA

9.6.2.24 Register 3Bh (address = 3Bh)

Figure 188. Register 3Bh

7	6	5	4	3	2	1	0
LINK LAYER TESTMODE			LINK LAYER RPAT	0	PULSE DET MODES		
R/W-0h			R/W-0h	W-0h	R/W-0h		

LEGEND: R/W = Read/Write; W = Write only; -n = value after

Table 35. Register 3Bh Field Descriptions

Bit	Field	Type	Reset	Description
7-5	LINK LAYER TESTMODE	R/W	0h	These bits generate a pattern according to section 5.3.3.8.2 of the JESD204B specification. 000 = Normal ADC data 001 = D21.5 (high-frequency jitter pattern) 010 = K28.5 (mixed-frequency jitter pattern) 011 = Repeat initial lane alignment (generates a K28.5 character and continuously repeats lane alignment sequences) 100 = 12 octet RPAT jitter pattern
4	LINK LAYER RPAT	R/W	0h	This bit changes the running disparity in the modified RPAT pattern test mode (only when link layer test mode = 100). 0 = Normal operation 1 = Changes disparity
3	0	W	0h	Must write 0.
2-0	PULSE DET MODES	R/W	0h	These bits select different detection modes for SYSREF (subclass 1) and SYNC~ (subclass2). Register settings are listed in Table 36.

Table 36. PULSE DET MODES Register Settings

D2	D1	D0	FUNCTIONALITY
0	Don’t care	0	Allow all pulses to reset input clock dividers
1	Don’t care	0	Do not allow reset of analog clock dividers
Don’t care	0 to 1 transition	1	Allow one pulse immediately after the 0 to 1 transition to reset the divider

9.6.2.25 Register 3Ch (address = 3Ch)

Figure 189. Register 3Ch

7	6	5	4	3	2	1	0
FORCE LMFC COUNT	LMFC COUNT INIT					RELEASE ILAN SEQ	
R/W-0h	R/W-0h					R/W-0h	

LEGEND: R/W = Read/Write; -n = value after

Table 37. Register 3Ch Field Descriptions

Bit	Field	Type	Reset	Description
7	FORCE LMFC COUNT	R/W	0h	0 = Normal operation 1 = Enables using a different starting value for the LMFC counter
6-2	LMFC COUNT INIT	R/W	0h	If SYSREF is transmitted to the digital block, the LMFC count resets to 0 and K28.5 stops transmitting when the LMFC count reaches 31. The initial value that the LMFC count resets to can be set using LMFC COUNT INIT. In this manner, the Rx can be synchronized early because the Rx receives the LANE ALIGNMENT SEQUENCE early. The FORCE LMFC COUNT register bit must be enabled.
1-0	RELEASE ILAN SEQ	R/W	0h	These bits delay the lane alignment sequence generation by 0, 1, 2, or 3 multiframes after the code group synchronization. 00 = 0 01 = 1 10 = 2 11 = 3

9.6.2.26 Register 422h (address = 422h)

Figure 190. Register 422h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	SPECIAL MODE2 CHA	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-1h	W-0h

LEGEND: W = Write only; -n = value after

Table 38. Register 422h Field Descriptions

Bit	Field	Type	Reset	Description
7-2	0	W	0h	Must write 0.
1	SPECIAL MODE2 CHA	W	1h	Always write 1 for improved HD2 performance.
0	0	W	0h	Must write 0.

9.6.2.27 Register 434h (address = 434h)

Figure 191. Register 434h

7	6	5	4	3	2	1	0
0	0	DIS DITH CHA	0	DIS DITH CHA	0	0	0
W-0h	W-0h	R/W-0h	W-0h	R/W-0h	W-0h	W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after

Table 39. Register 434h Field Descriptions

Bit	Field	Type	Reset	Description
7-6	0	W	0h	Must write 0.
5	DIS DITH CHA	R/W	0h	Set this bit along with bits 5 and 4 of register 01h. 00 = Default 11 = Dither is disabled for channel A. In this mode, SNR typically improves by 0.5 dB at 70 MHz.
4	0	W	0h	Must write 0.
3	DIS DITH CHA	R/W	0h	Set this bit along with bits 5 and 4 of register 01h. 00 = Default 11 = Dither is disabled for channel A. In this mode, SNR typically improves by 0.5 dB at 70 MHz.
2-0	0	W	0h	Must write 0.

9.6.2.28 Register 522h (address = 522h)

Figure 192. Register 522h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	SPECIAL MODE2 CHB	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-1h	W-0h

LEGEND: W = Write only; -n = value after

Table 40. Register 522h Field Descriptions

Bit	Field	Type	Reset	Description
7-2	0	W	0h	Must write 0.
1	SPECIAL MODE2 CHB	W	1h	Always write 1 for better HD2 performance.
0	0	W	0h	Must write 0.

9.6.2.29 Register 534h (address = 534h)

Figure 193. Register 534

7	6	5	4	3	2	1	0
0	0	DIS DITH CHB	0	DIS DITH CHB	0	0	0
W-0h	W-0h	R/W-0h	W-0h	R/W-0h	W-0h	W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after

Table 41. Register 534 Field Descriptions

Bit	Field	Type	Reset	Description
7-6	0	W	0h	Must write 0.
5	DIS DITH CHB	R/W	0h	Set this bit along with bits 3 and 2 of register 01h. 00 = Default 11 = Dither is disabled for channel B. In this mode, SNR typically improves by 0.5 dB at 70 MHz.
4	0	W	0h	Must write 0.
3	DIS DITH CHB	R/W	0h	Set this bit along with bits 3 and 2 of register 01h. 00 = Default 11 = Dither is disabled for channel B. In this mode, SNR typically improves by 0.5 dB at 70 MHz.
2-0	0	W	0h	Must write 0.

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

Typical applications involving transformer-coupled circuits are discussed in this section. Transformers (such as ADT1-1WT or WBC1-1) can be used up to 250 MHz to achieve good phase and amplitude balances at ADC inputs. When designing the dc driving circuits, the ADC input impedance must be considered. Figure 194 and Figure 195 show the impedance ($Z_{in} = R_{in} \mid\mid C_{in}$) across the ADC input pins.

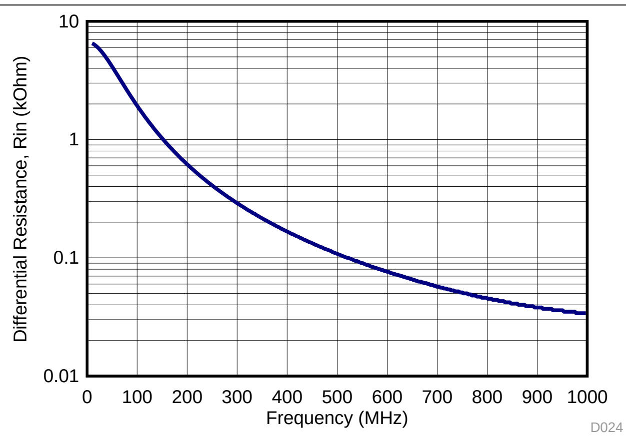


Figure 194. Differential Input Resistance, R_{in}

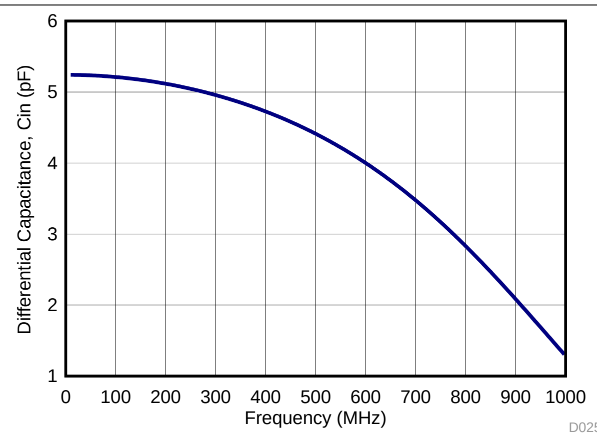


Figure 195. Differential Input Capacitance, C_{in}

10.2 Typical Applications

10.2.1 Driving Circuit Design: Low Input Frequencies

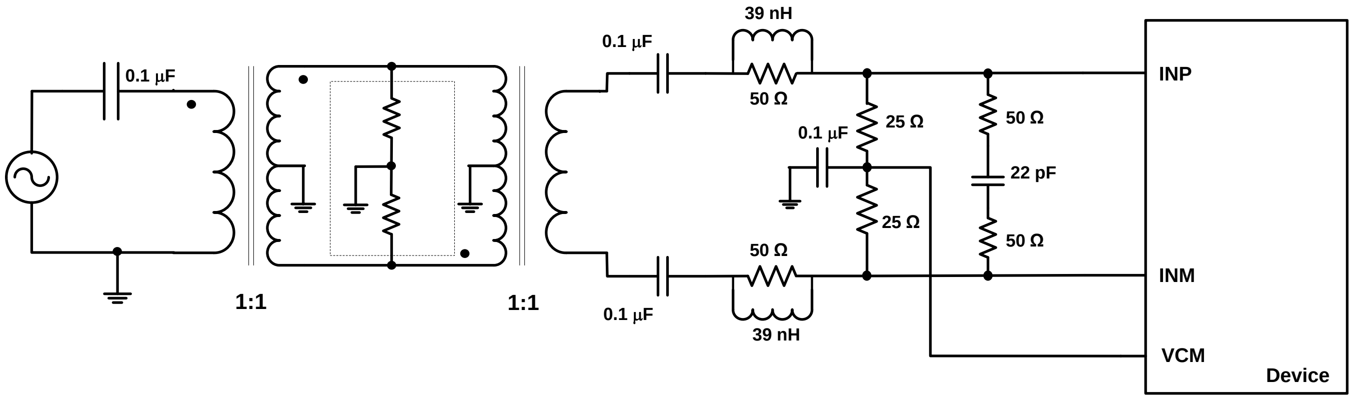


Figure 196. Driving Circuit for Low Input Frequencies

10.2.1.1 Design Requirements

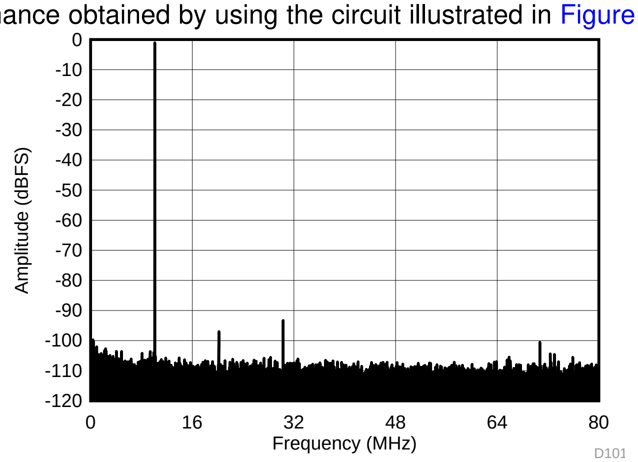
For optimum performance, the analog inputs must be driven differentially. An optional 5-Ω to 15-Ω resistor in series with each input pin can be kept to damp out ringing caused by package parasitics. The drive circuit may have to be designed to minimize the affect of kick-back noise generated by sampling switches opening and closing inside the ADC, as well as ensuring low insertion loss over the desired frequency range and matched impedance to the source.

10.2.1.2 Detailed Design Procedure

A typical application using two back-to-back coupled transformers is illustrated in Figure 196. The circuit is optimized for low input frequencies. An external R-C-R filter using 50-Ω resistors and a 22-pF capacitor is used. With the series inductor (39 nH), this combination helps absorb the sampling glitches.

10.2.1.3 Application Curves

Figure 197 shows the performance obtained by using the circuit illustrated in Figure 196.



f_S = 160 MSPS, SNR = 72.4 dBFS, f_{IN} = 10 MHz,
SFDR = 92.3 dBc

Figure 197. FFT for 10-MHz Input Signal (Dither On)

Typical Applications (continued)

10.2.2 Driving Circuit Design: Input Frequencies Between 100 MHz to 230 MHz

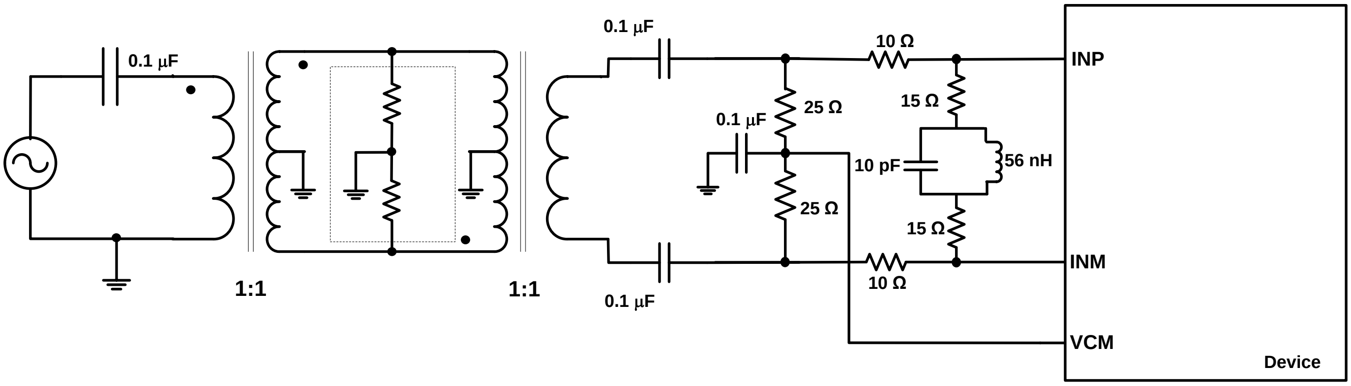


Figure 198. Driving Circuit for Mid-Range Input Frequencies (100 MHz < f_{IN} < 230 MHz)

10.2.2.1 Design Requirements

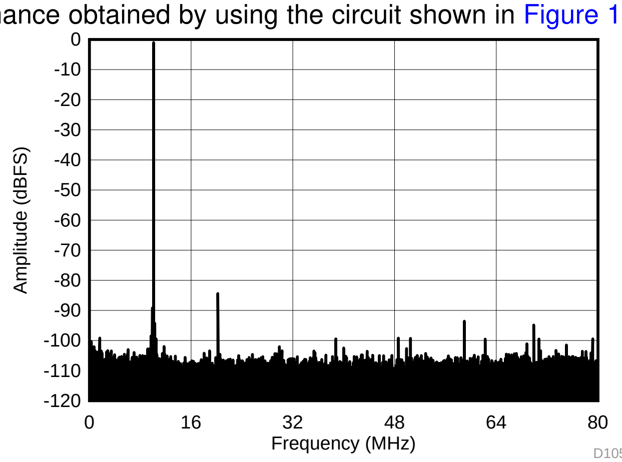
See the *Design Requirements* section for further details.

10.2.2.2 Detailed Design Procedure

When input frequencies are between 100 MHz to 230 MHz, an R-LC-R circuit can be used to optimize performance, as shown in Figure 198.

10.2.2.3 Application Curve

Figure 199 shows the performance obtained by using the circuit shown in Figure 198.



f_S = 160 MSPS, SNR = 70.6 dBFS, f_{IN} = 170 MHz,
SFDR = 94.4 dBc

Figure 199. FFT for 170-MHz Input Signal (Dither On)

Typical Applications (continued)

10.2.3 Driving Circuit Design: Input Frequencies Greater than 230 MHz

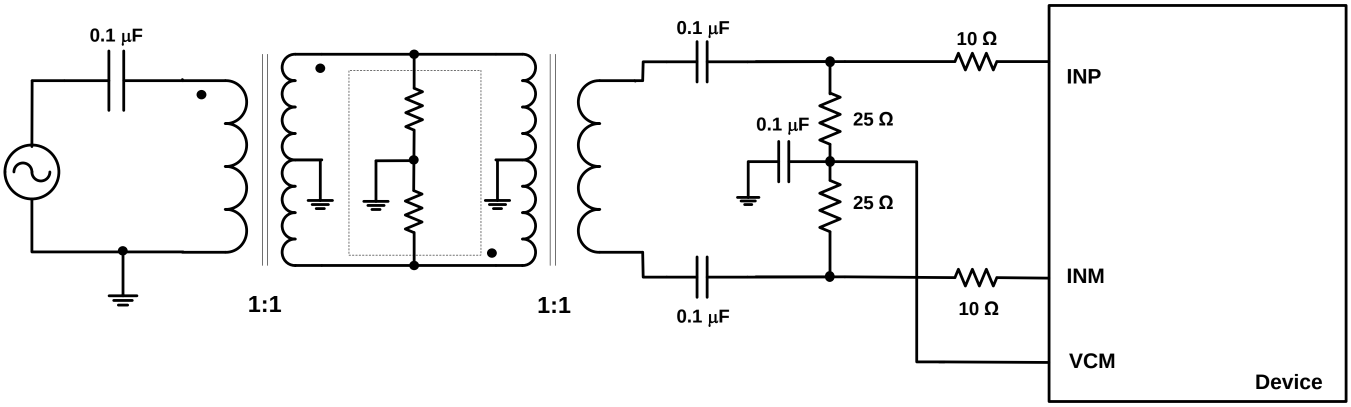


Figure 200. Driving Circuit for High Input Frequencies (f_{IN} > 230 MHz)

10.2.3.1 Design Requirements

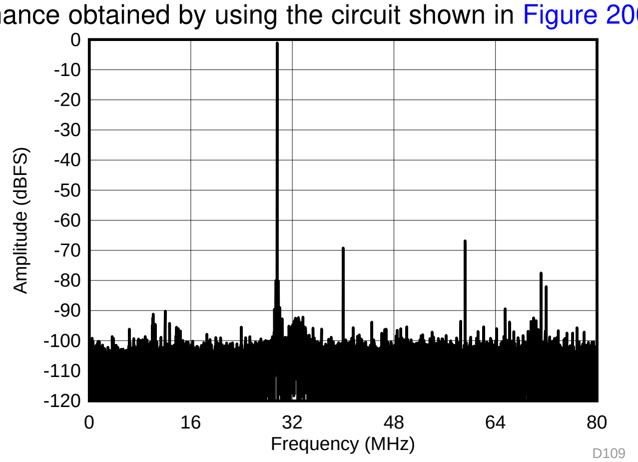
See the *Design Requirements* section for further details.

10.2.3.2 Detailed Design Procedure

For high input frequencies (> 230 MHz), using the R-C-R or R-LC-R circuit does not show significant improvement in performance. However, a series resistance of 10 Ω can be used, as shown in Figure 200.

10.2.3.3 Application Curve

Figure 201 shows the performance obtained by using the circuit shown in Figure 200.



f_S = 160 MSPS, SNR = 63.2 dBFS, f_{IN} = 450 MHz,
SFDR = 65.7 dBc

Figure 201. FFT for 450-MHz Input Signal (Dither On)

11 Power-Supply Recommendations

The device requires a 1.8-V nominal supply for AVDD and DVDD. There are no specific sequence power-supply requirements during device power-up. AVDD and DVDD can power up in any order.

12 Layout

12.1 Layout Guidelines

The ADC32J4x EVM layout can be used as a reference layout to obtain the best performance. A layout diagram of the EVM top layer is provided in Figure 202. Some important points to remember when laying out the board are:

1. Analog inputs are located on opposite sides of the device pin out to ensure minimum crosstalk on the package level. To minimize crosstalk onboard, the analog inputs must exit the pin out in opposite directions as much as possible, as shown in the reference layout of Figure 202.
2. In the device pin out, the sampling clock is located on a side perpendicular to the analog inputs in order to minimize coupling between them. This configuration is also maintained on the reference layout of Figure 202 as much as possible.
3. Keep digital outputs away from the analog inputs. When these digital outputs exit the pin out, the digital output traces must not be kept parallel to the analog input traces because this configuration may result in coupling from digital outputs to analog inputs and degrade performance. All digital output traces to the receiver [such as a field-programmable gate array (FPGA) or an application-specific integrated circuit (ASIC)] must be matched in length to avoid skew among outputs.
4. At each power-supply pin (AVDD and DVDD), a 0.1-µF decoupling capacitor must be kept close to the device. A separate decoupling capacitor group consisting of a parallel combination of 10-µF, 1-µF, and 0.1-µF capacitors can be kept close to the supply source.

12.2 Layout Example

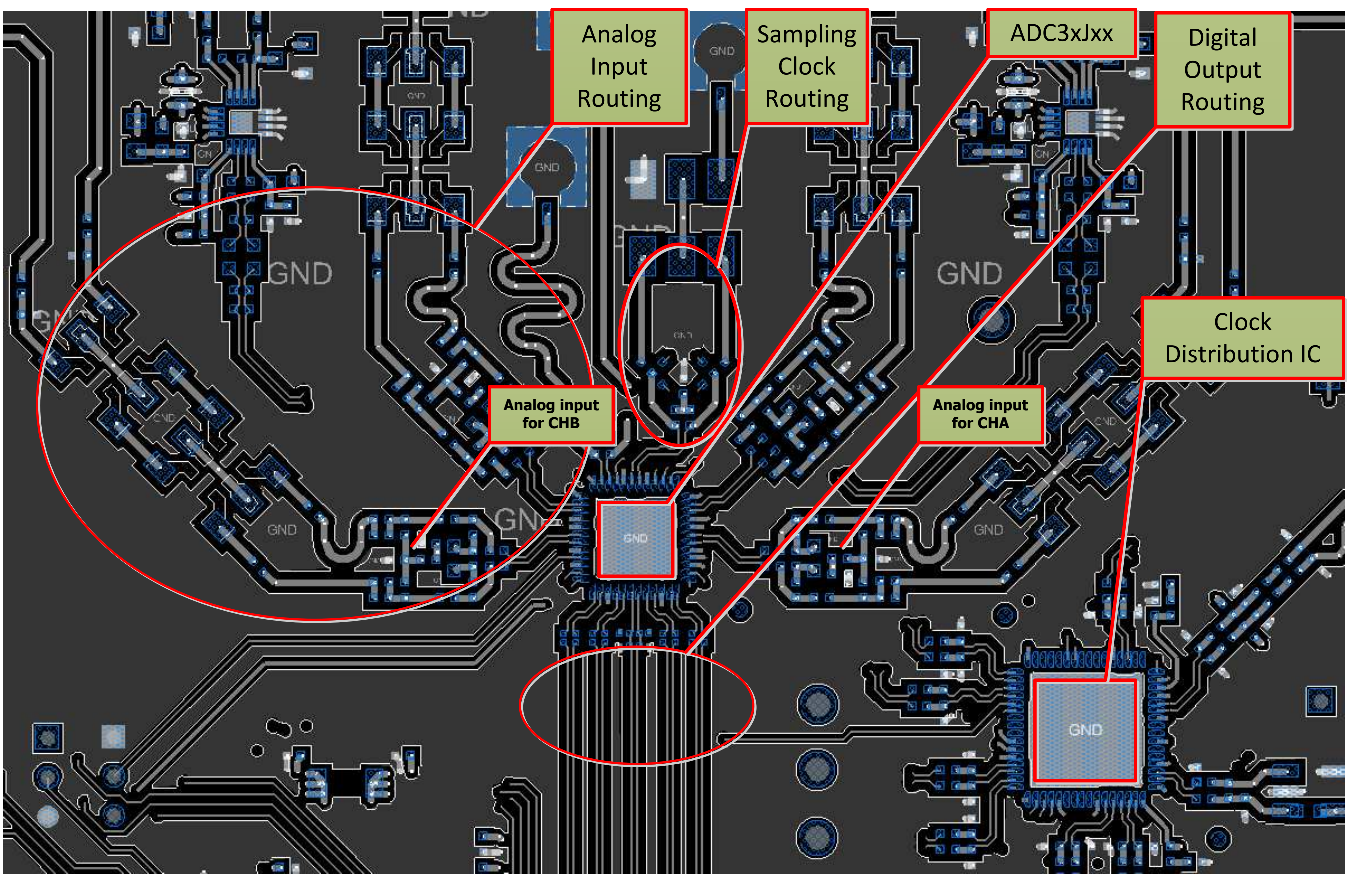


Figure 202. Typical Layout of the ADC32J4x Board

13 Device and Documentation Support

13.1 Related Links

Table 42 lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 42. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
ADC32J45	Click here	Click here	Click here	Click here	Click here
ADC32J44	Click here	Click here	Click here	Click here	Click here
ADC32J43	Click here	Click here	Click here	Click here	Click here
ADC32J42	Click here	Click here	Click here	Click here	Click here

13.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.3 Trademarks

E2E is a trademark of Texas Instruments.
PowerPAD is a trademark of Texas Instruments, Inc.
All other trademarks are the property of their respective owners.

13.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADC32J42IRGZR	ACTIVE	VQFN	RGZ	48	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ32J42	Samples
ADC32J42IRGZT	ACTIVE	VQFN	RGZ	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ32J42	Samples
ADC32J43IRGZR	ACTIVE	VQFN	RGZ	48	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ32J43	Samples
ADC32J43IRGZT	ACTIVE	VQFN	RGZ	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ32J43	Samples
ADC32J44IRGZR	ACTIVE	VQFN	RGZ	48	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ32J44	Samples
ADC32J44IRGZT	ACTIVE	VQFN	RGZ	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ32J44	Samples
ADC32J45IRGZR	ACTIVE	VQFN	RGZ	48	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ32J45	Samples
ADC32J45IRGZT	ACTIVE	VQFN	RGZ	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ32J45	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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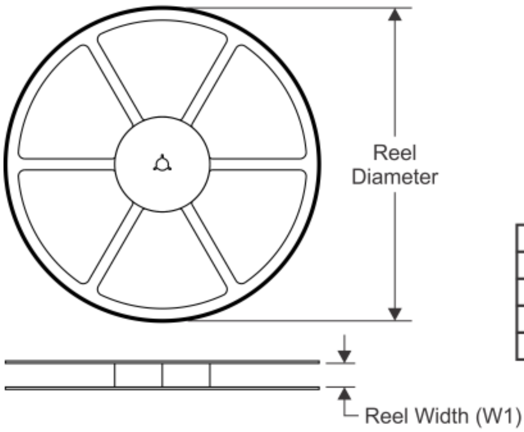
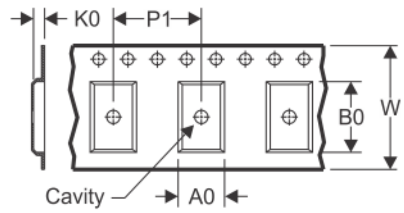
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

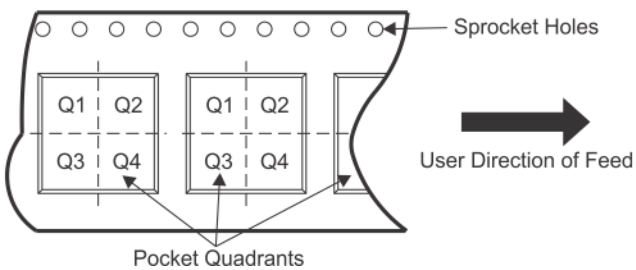


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

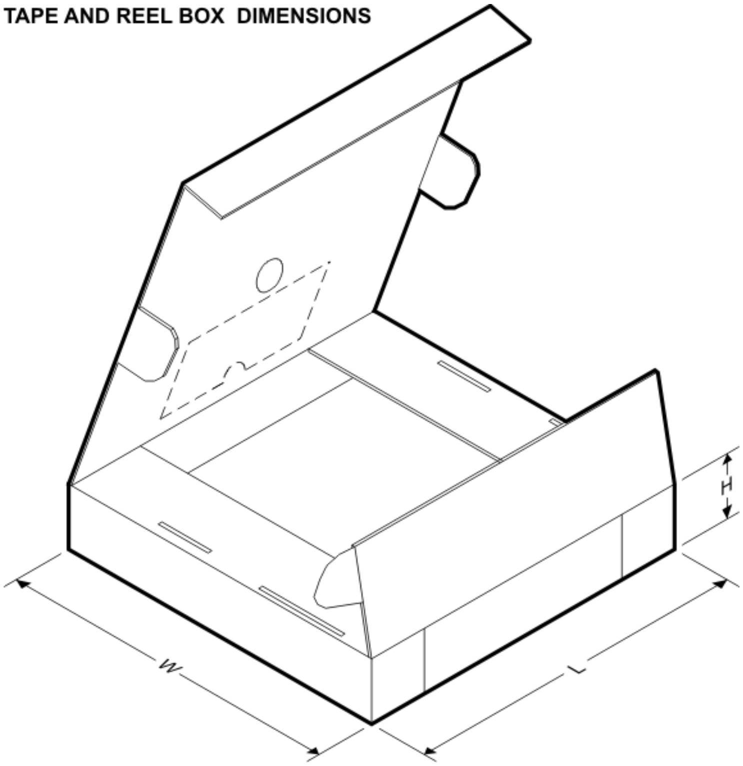
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADC32J42IRGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2
ADC32J42IRGZT	VQFN	RGZ	48	250	180.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2
ADC32J43IRGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2
ADC32J43IRGZT	VQFN	RGZ	48	250	180.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2
ADC32J44IRGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2
ADC32J44IRGZT	VQFN	RGZ	48	250	180.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2
ADC32J45IRGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2
ADC32J45IRGZT	VQFN	RGZ	48	250	180.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2

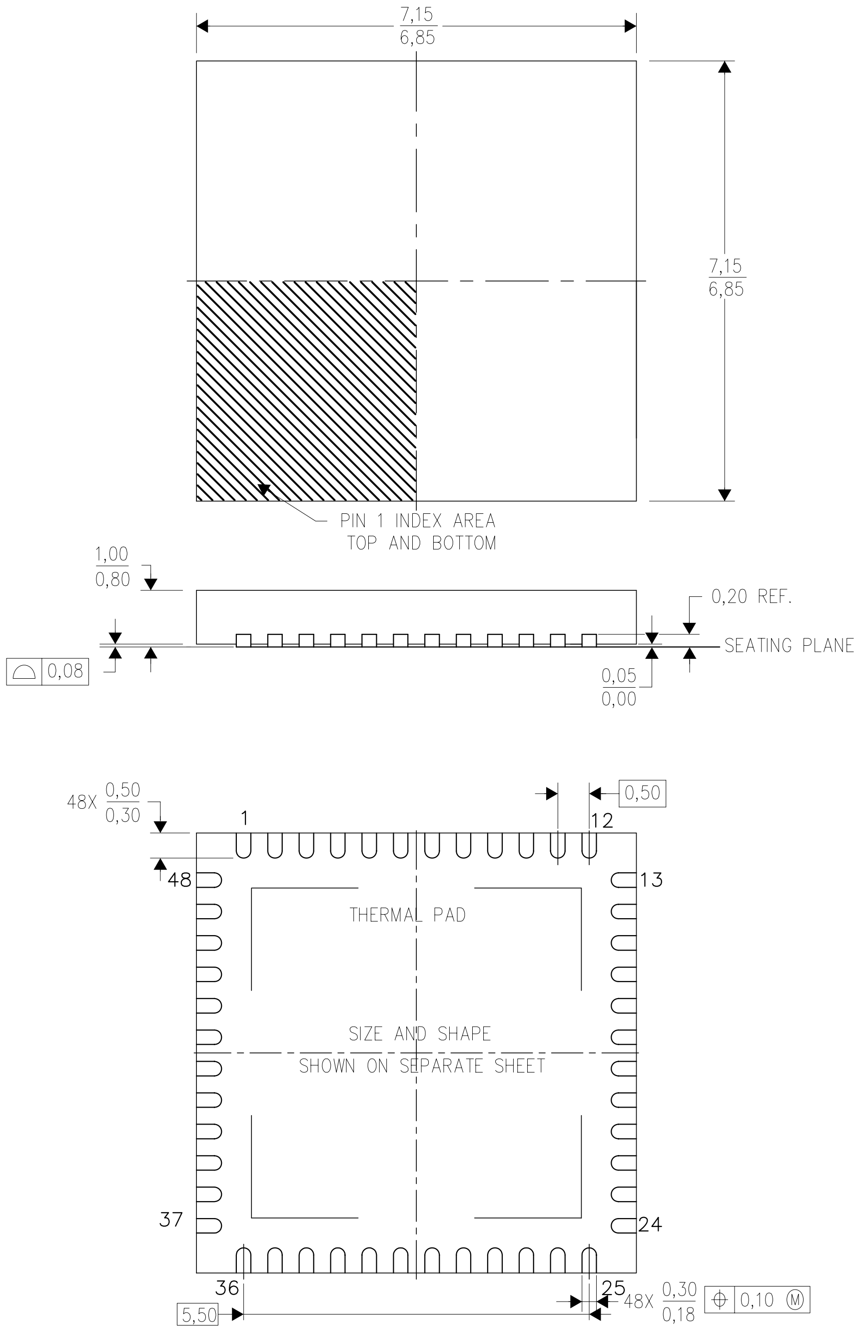
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADC32J42IRGZR	VQFN	RGZ	48	2500	336.6	336.6	28.6
ADC32J42IRGZT	VQFN	RGZ	48	250	213.0	191.0	55.0
ADC32J43IRGZR	VQFN	RGZ	48	2500	336.6	336.6	28.6
ADC32J43IRGZT	VQFN	RGZ	48	250	213.0	191.0	55.0
ADC32J44IRGZR	VQFN	RGZ	48	2500	336.6	336.6	28.6
ADC32J44IRGZT	VQFN	RGZ	48	250	213.0	191.0	55.0
ADC32J45IRGZR	VQFN	RGZ	48	2500	336.6	336.6	28.6
ADC32J45IRGZT	VQFN	RGZ	48	250	213.0	191.0	55.0

RGZ (S-PVQFN-N48) PLASTIC QUAD FLATPACK NO-LEAD



NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
- B. This drawing is subject to change without notice.
- C. Quad Flatpack, No-leads (QFN) package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- F. Falls within JEDEC MO-220.

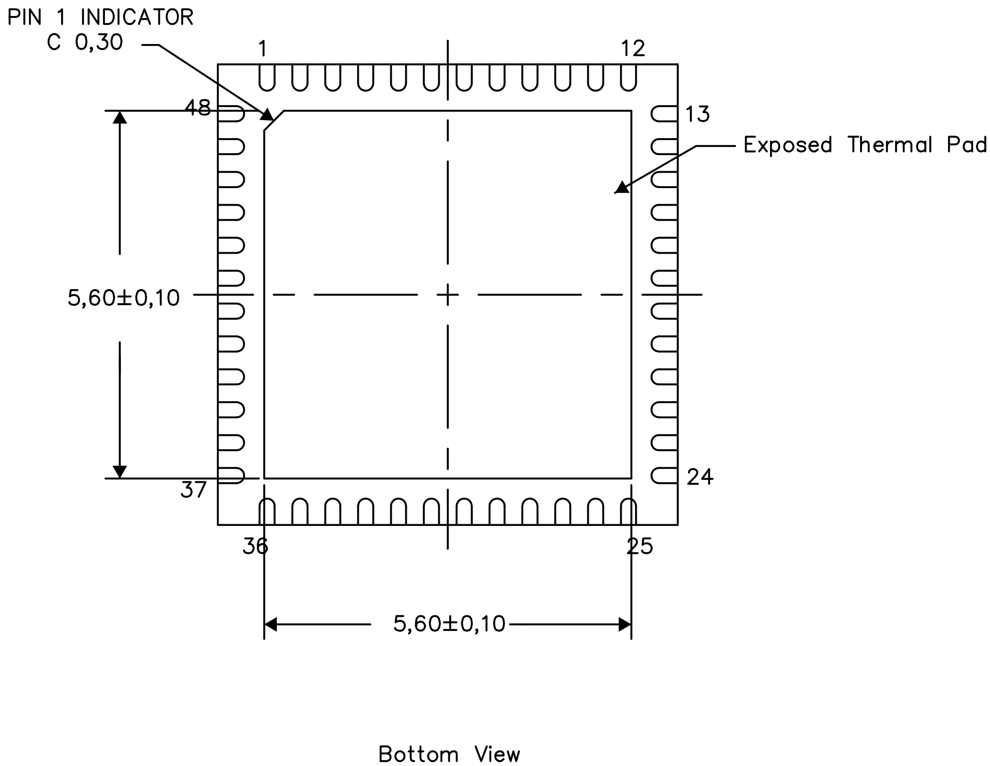
RGZ (S-PVQFN-N48) PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

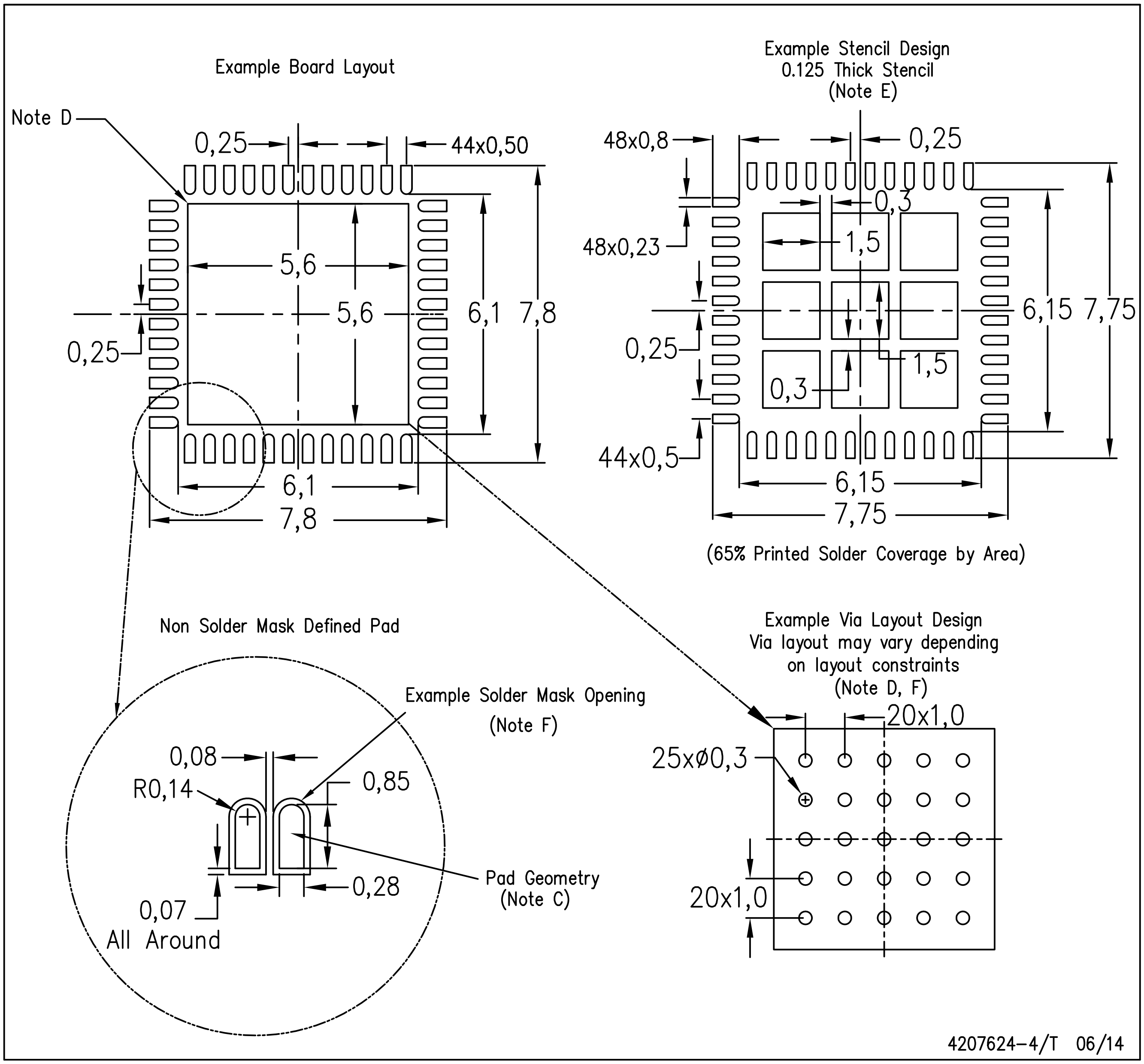


Exposed Thermal Pad Dimensions

4206354-5/Z 03/15

NOTE: All linear dimensions are in millimeters

RGZ (S–PVQFN–N48) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.