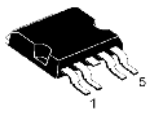
VN920D-B5
VN920DSO

High-side driver

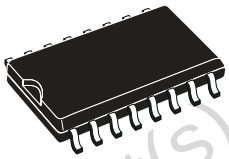
Features

Type	$R_{DS(on)}$	I_{OUT}	V_{CC}
VN920D-B5 VN920DSO	18 mΩ	30 A	36 V

- CMOS-compatible input
- On-state open load detection
- Off-state open load detection
- Shorted load protection
- Under-voltage and over-voltage shutdown
- Protection against loss of ground
- Very low standby current
- Reverse battery protected (see *Application schematic*)



P²PAK



SO-16L

Description

The VN920D-B5 and VN920DSO are monolithic devices designed in STMicroelectronics VIPower M0-3 technology. The VN920D-B5 and VN920DSO are intended for driving any type of load with one side connected to ground. The active V_{CC} pin voltage clamp protects the devices against low energy spikes (see ISO7637 transient compatibility table).

Active current limitation combined with thermal shutdown and automatic restart protects the devices against overload. The devices detect the open load condition in both the on and off-state. In the off-state the devices detect if the output is shorted to V_{CC}. The devices automatically turn-off in the case where the ground pin becomes disconnected.

Table 1. Device summary

Package	Order codes	
	Tube	Tape and reel
P²PAK	VN920D-B5	VN920D-B513TR
SO-16L	VN920DSO	VN920DSO13TR

Contents

List of tables

List of figures

1 Block diagram and pin description

Figure 1. Block diagram

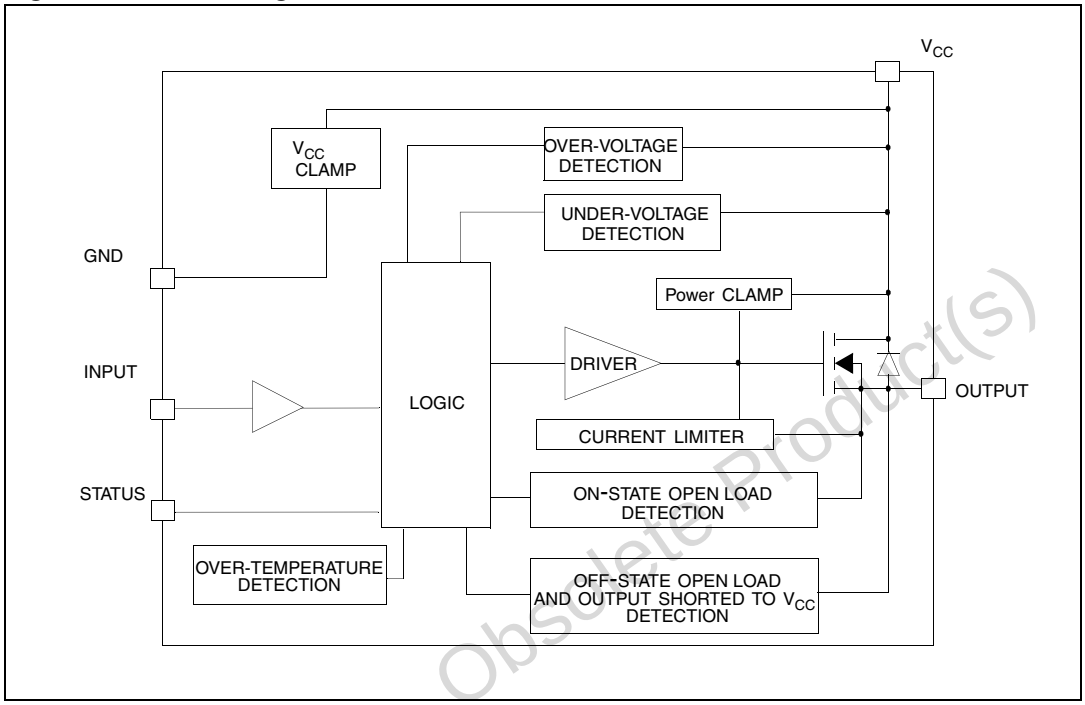


Figure 2. Configuration diagram (top view)

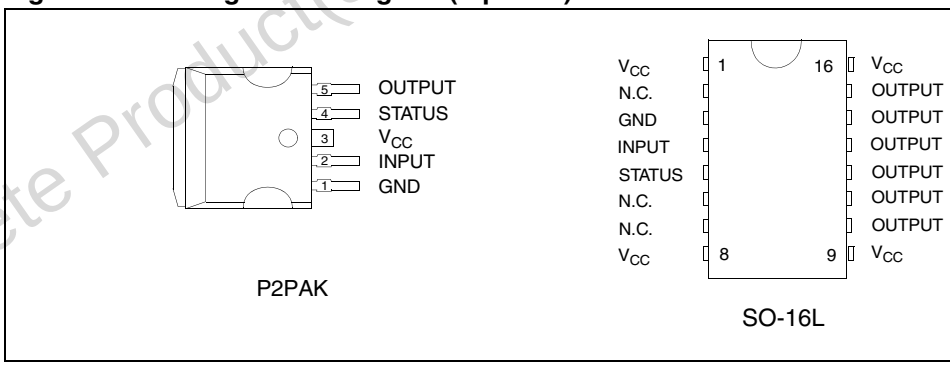
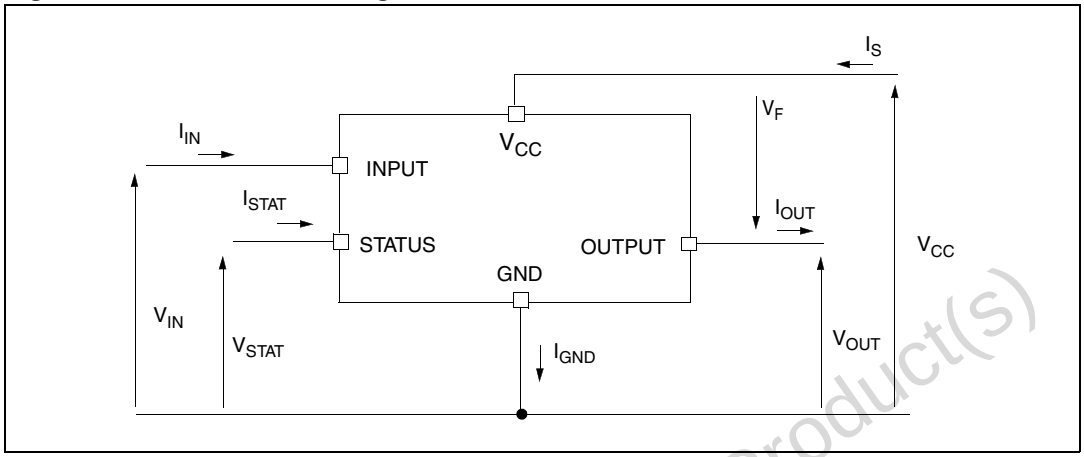


Table 2. Suggested connections for unused and not connected pins

Connection / pin	Status	N.C.	Output	Input
Floating	X	X	X	X
To ground		X		Through 10KΩ resistor

2 Electrical specifications

Figure 3. Current and voltage conventions



2.1 Absolute maximum ratings

Stressing the device above the rating listed in the “Absolute maximum ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to Absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics sure program and other relevant quality document.

Table 3. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		SO-16L	P^2PAK	
V_{CC}	DC supply voltage	41		V
- V_{CC}	Reverse DC supply voltage	- 0.3		V
- I_{gnd}	DC reverse ground pin current	- 200		mA
I_{OUT}	DC output current	Internally limited		A
- I_{OUT}	Reverse DC output current	- 25		A
I_{IN}	DC input current	+/- 10		mA
I_{STAT}	DC Status current	+/- 10		mA
V_{ESD}	Electrostatic discharge (human body model: R = 1.5KΩ, C = 100pF) - INPUT - STATUS - OUTPUT - V_{CC}	 4000 4000 5000 5000		 V V V V

Table 3. Absolute maximum ratings (continued)

Symbol	Parameter	Value		Unit
		SO-16L	P^2PAK	
E_{MAX}	Maximum switching energy (L = 0.25mH; R_L= 0Ω; V_{bat} = 13.5V; T_{jstart} = 150ºC; I_L = 45A)	352	364	mJ
P_{tot}	Power dissipation T_C = 25°C	8.3	96.1	W
T_j	Junction operating temperature	Internally limited		°C
T_c	Case operating temperature	- 40 to 150		°C
T_{stg}	Storage temperature	- 55 to 150		°C

2.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Max. value		Unit
		SO-16L	P^2PAK	
$R_{thj\text{-}case}$	Thermalresistance junction-case	-	1.3	°C/W
$R_{thj\text{-}lead}$	Thermalresistance junction-lead	15	-	°C/W
$R_{thj\text{-}amb}$	Thermalresistance junction-ambient	65 (1)	51.3(2)	°C/W

1. When mounted on FR4 printed circuit board with 0.5cm^2 of Cu (at least 35µm thick) connected to all V_{CC} pins.
2. When mounted on a standard single-sided FR-4 board with 0.5cm2 of Cu (at least 35µm thick).

2.3 Electrical characteristics

Values specified in this section are for 8V < V_{CC} < 36V; -40°C < T_j < 150°C, unless otherwise stated.

Table 5. Power

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CC}	Operating supply voltage		5.5	13	36	V
V_{USD}	Under-voltage shutdown		3	4	5.5	V
$V_{USDhyst}$	Under-voltage shutdown hysteresis			0.5		V
V_{OV}	Over-voltage shutdown		36			V
R_{ON}	On-state resistance	I_{OUT} = 10A; T_j = 25°C; I_{OUT} = 10A; I_{OUT} = 3A; V_{CC} = 6V			18 36 50	mΩ mΩ mΩ
I_S	Supply current	Off-state; V_{CC} = 13V; V_{IN} = V_{OUT} = 0V Off-state; V_{CC} = 13V; V_{IN} = V_{OUT} = 0V; T_j = 25°C On-state; V_{CC} = 13V; V_{IN} = 5V; I_{OUT} = 0A		10 10	25 20 3.5	µA µA mA
$I_{L(off1)}$	Off-state output current	V_{IN} = V_{OUT} = 0V	0		50	µA
$I_{L(off2)}$	Off-state output current	V_{IN} = 0V; V_{OUT} = 3.5V	-75		0	µA
$I_{L(off3)}$	Off-state output current	V_{IN} = V_{OUT} = 0V; V_{CC} = 13V; T_j = 125°C			5	µA
$I_{L(off4)}$	Off-state output current	V_{IN} = V_{OUT} = 0V; V_{CC} = 13V; T_j = 25°C			3	µA

Table 6. Switching (V_{CC}=13V)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	R_L = 1.3Ω		50		µs
$t_{d(off)}$	Turn-off delay time	R_L = 1.3Ω		50		µs
$dV_{OUT}/dt_{(on)}$	Turn-on voltage slope	R_L = 1.3Ω	See *Figure 20.*			V/µs
$dV_{OUT}/dt_{(off)}$	Turn-off voltage slope	R_L = 1.3Ω	See *Figure 21.*			V/µs

Table 7. Input pin

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input low-level				1.25	V
I_{IL}	Low-level input current	V_{IN} = 1.25V	1			µA
V_{IH}	Input high-level		3.25			V
I_{IH}	High-level input current	V_{IN} = 3.25V			10	µA
V_{hyst}	Input hysteresis voltage		0.5			V
V_{ICL}	Input clamp voltage	I_{IN} = 1mA I_{IN} = -1mA	6	6.8 - 0.7	8	V V

Table 8. V_{CC} output diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_F	Forward on voltage	- I_{OUT} = 5.5A; T_j = 150°C			0.7	V

Table 9. Status pin

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{STAT}	Status low output voltage	I_{STAT} = 1.6mA			0.5	V
I_{LSTAT}	Status leakage current	Normal operation; V_{STAT} = 5V			10	µA
C_{STAT}	Status pin input capacitance	Normal operation; V_{STAT} = 5V			100	pF
V_{SCL}	Status clamp voltage	I_{STAT} = 1mA I_{STAT} = - 1mA	6	6.8 - 0.7	8	V V

Table 10. Protections(1)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
T_{TSD}	Shutdown temperature		150	175	200	°C
T_R	Reset temperature		135			°C
T_{hyst}	Thermal hysteresis		7	15		°C
t_{SDL}	Status delay in overload condition	$T_j > T_{jsh}$			20	ms
I_{lim}	Current limitation	5.5V < V_{CC} < 36V	30	45	75 75	A A
V_{demag}	Turn-off output clamp voltage	I_{OUT} = 2 A; V_{IN} = 0V; L = 6mH	V_{CC} - 41	V_{CC} - 48	V_{CC} - 55	V

1. To ensure long term reliability under heavy overload or short circuit conditions, protection and related diagnostic signals must be used together with a proper software strategy. If the device operates under abnormal conditions this software must limit the duration and number of activation cycles.

Table 11. Open load detection

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{OL}	Open load on-state detection threshold	V_{IN} = 5V	300	500	700	mA
$t_{DOL(on)}$	Open load on-state detection delay	I_{OUT} = 0A			250	µs
V_{OL}	Open load off-state voltage detection threshold	V_{IN} = 0V	1.5	2.5	3.5	V
$t_{DOL(off)}$	Open load detection delay at turn-off				1000	µs

Figure 4. Status timings

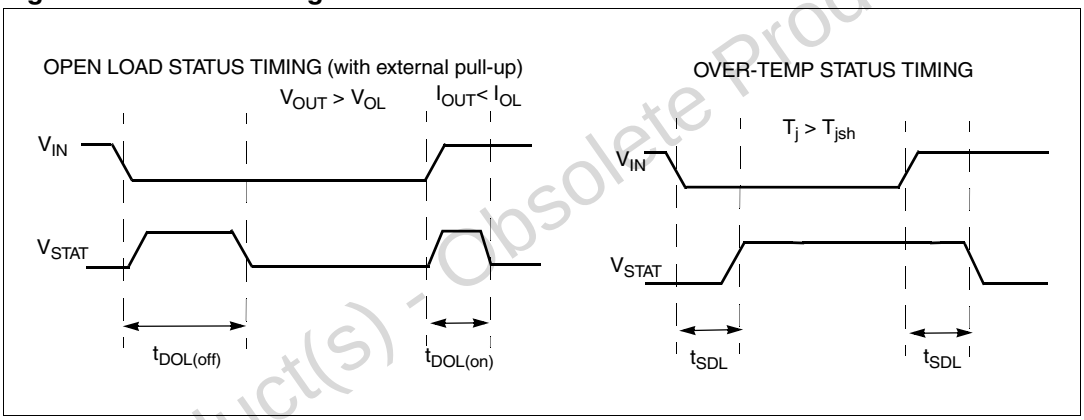


Figure 5. Switching time waveforms

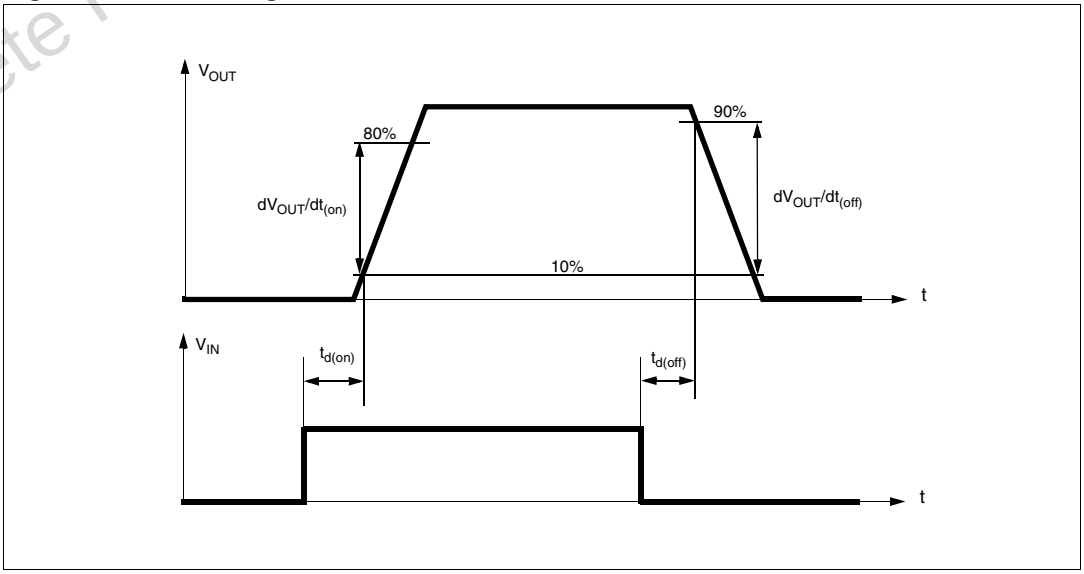


Table 12. Truth table

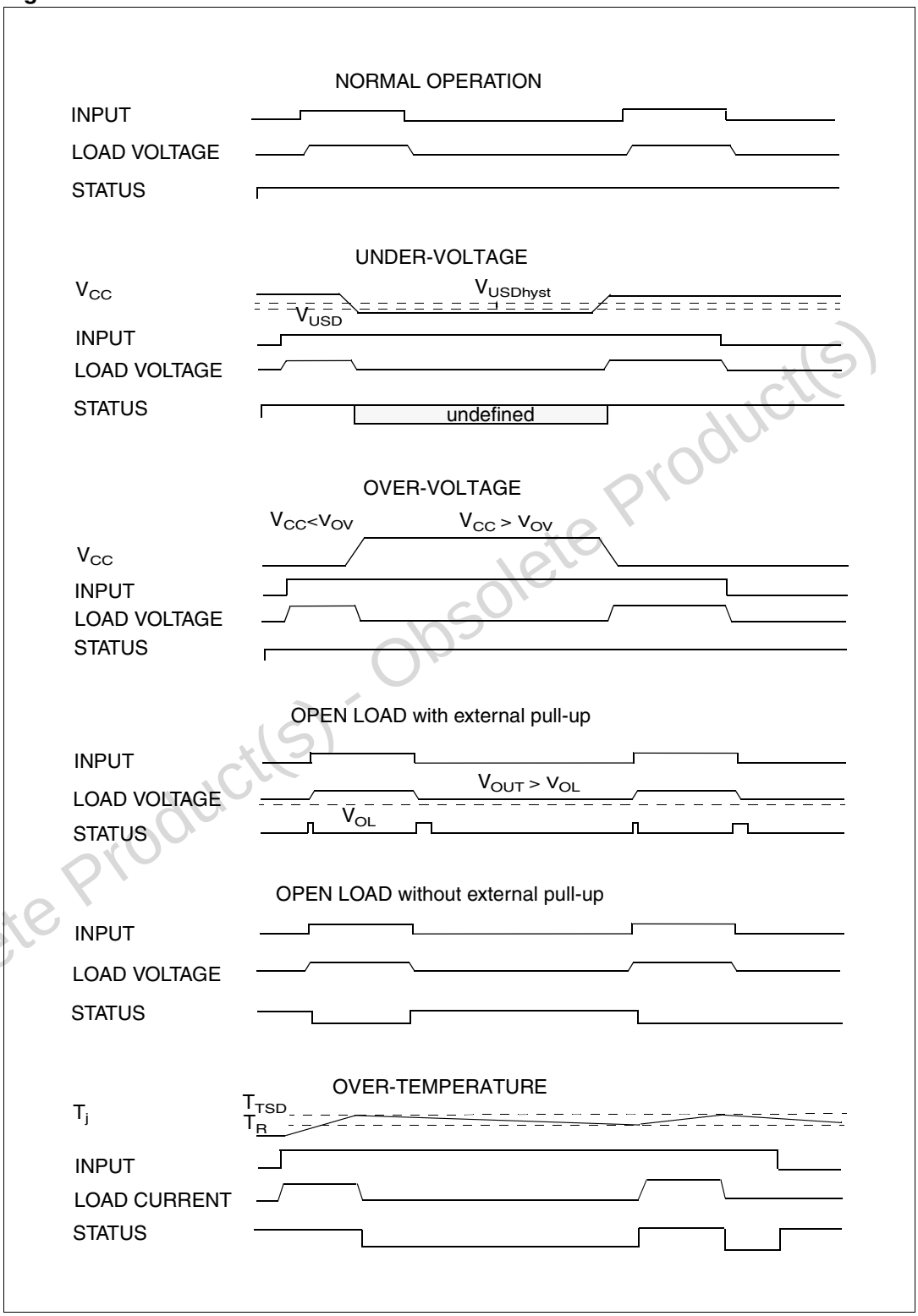
Conditions	Input	Output	Status
Normal operation	L H	L H	H H
Current limitation	L H H	L X X	H ($T_j < T_{TSD}$) H ($T_j > T_{TSD}$) L
Over-temperature	L H	L L	H L
Under-voltage	L H	L L	X X
Over-voltage	L H	L L	H H
Output voltage > V_{OL}	L H	H H	L H
Output current < I_{OL}	L H	L H	H L

Table 13. Electrical transient requirements

ISO T/R 7637/1 Test pulse	Test level				
	I	II	III	IV	Delays and impedance
1	- 25V(1)	- 50V(1)	- 75V(1)	- 100V(1)	2ms, 10Ω
2	+ 25V(1)	+ 50V(1)	+ 75V(1)	+ 100V(1)	0.2ms, 10Ω
3a	- 25V(1)	- 50V(1)	- 100V(1)	- 150V(1)	0.1µs, 50Ω
3b	+ 25V(1)	+ 50V(1)	+ 75V(1)	+ 100V(1)	0.1µs, 50Ω
4	- 4V(1)	- 5V(1)	- 6V(1)	- 7V(1)	100ms, 0.01Ω
5	+ 26.5V(1)	+ 46.5V(2)	+ 66.5V(2)	+ 86.5V(2)	400ms, 2Ω

1. All functions of the device are performed as designed after exposure to disturbance.
2. One or more functions of the device is not performed as designed after exposure and cannot be returned to proper operation without replacing the device.

Figure 6. Waveforms



2.4 Electrical characteristics curves

Figure 7. Off-state output current

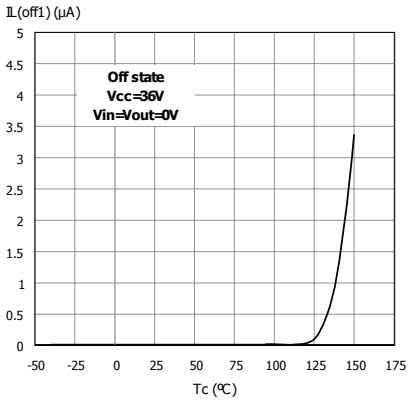


Figure 8. High-level input current

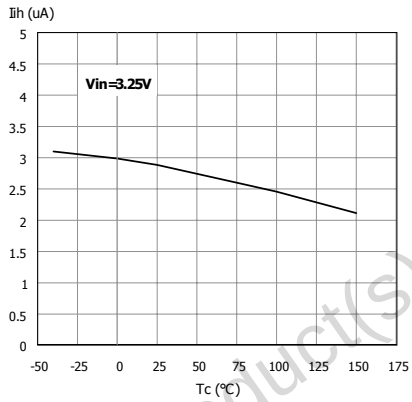


Figure 9. Input clamp voltage

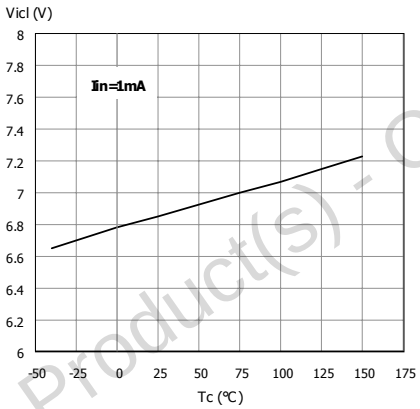


Figure 10. Status leakage current

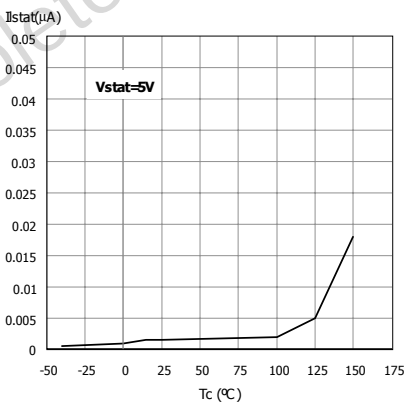


Figure 11. Status low output voltage

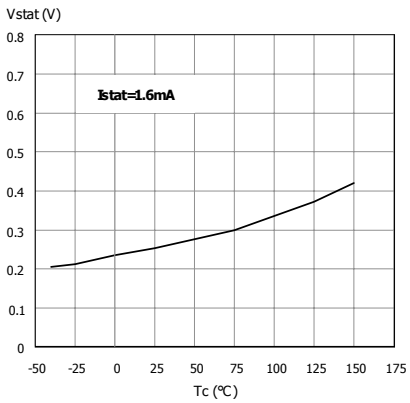


Figure 12. Status clamp voltage

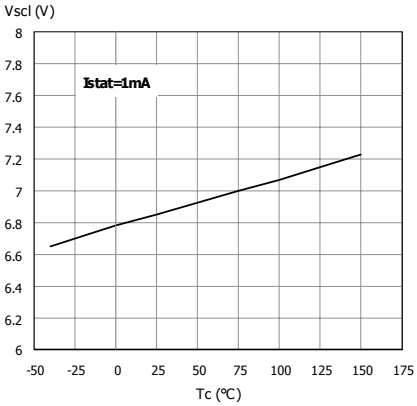


Figure 13. On-state resistance Vs T_{case}

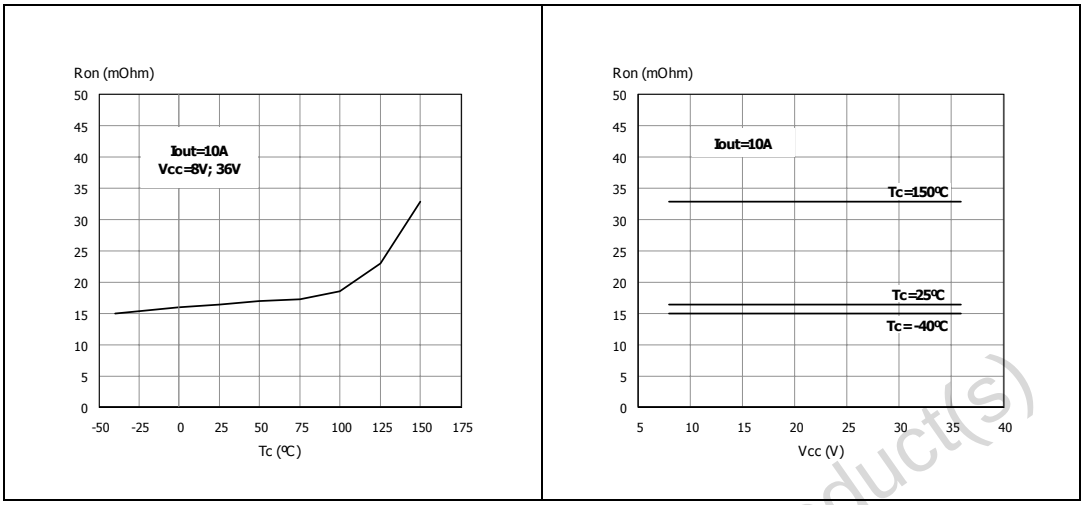


Figure 14. On-state resistance Vs V_{CC}

Figure 15. Over-voltage shutdown

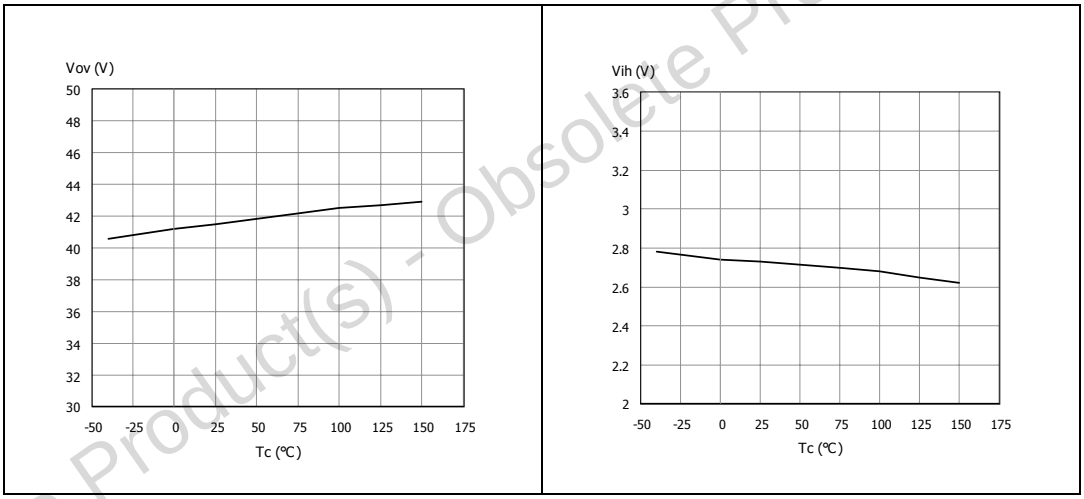


Figure 16. Input high-level

Figure 17. Input low-level

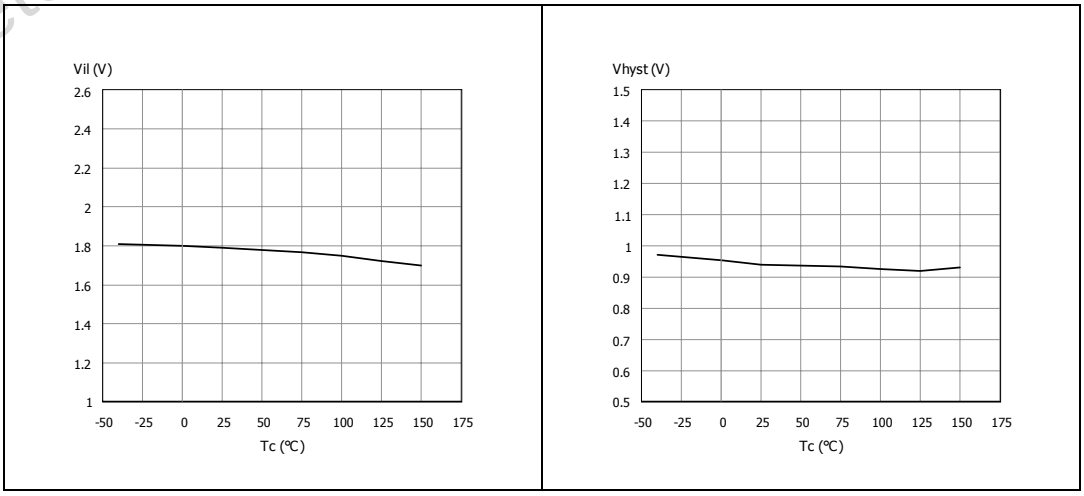


Figure 18. Input hysteresis voltage

Figure 19. I_{lim} Vs T_{case}

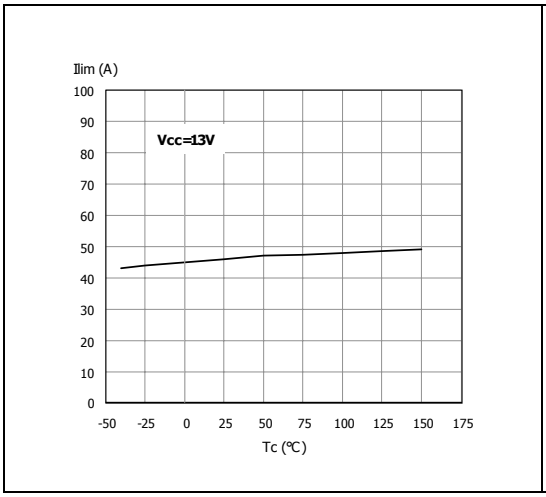


Figure 20. Turn-on voltage slope

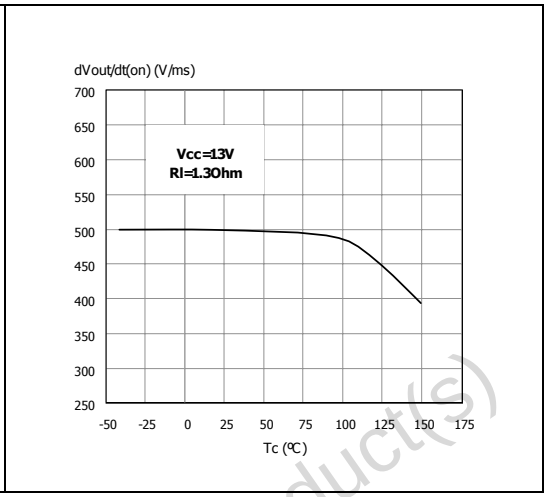
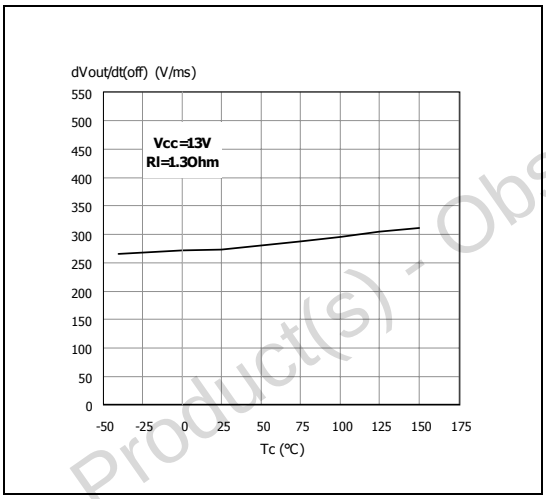
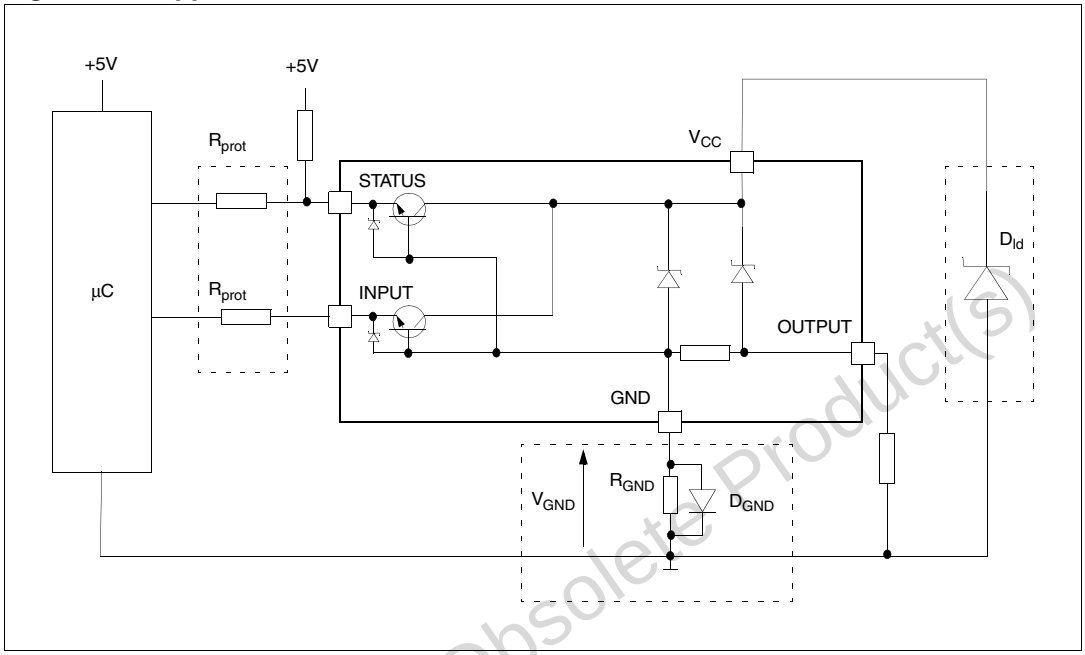


Figure 21. Turn-off voltage slope



3 Application information

Figure 22. Application schematic



3.1 GND protection network against reverse battery

3.1.1 Solution 1: resistor in the ground line (R_{GND} only)

This can be used with any type of load.

The following is an indication on how to dimension the R_{GND} resistor.

1. $R_{GND} \leq 600mV / (I_{S(on)max})$.
2. $R_{GND} \geq (- V_{CC}) / (- I_{GND})$

where $- I_{GND}$ is the DC reverse ground pin current and can be found in the absolute maximum rating section of the device datasheet.

Power Dissipation in R_{GND} (when $V_{CC} < 0$: during reverse battery situations) is:

$P_D = (- V_{CC})^2 / R_{GND}$

This resistor can be shared amongst several different HSDs. Please note that the value of this resistor should be calculated with formula (1) where $I_{S(on)max}$ becomes the sum of the maximum on-state currents of the different devices.

Please note that if the microprocessor ground is not shared by the device ground then the R_{GND} will produce a shift ($I_{S(on)max} * R_{GND}$) in the input thresholds and the status output values. This shift will vary depending on how many devices are ON in the case of several high-side drivers sharing the same R_{GND}.

If the calculated power dissipation leads to a large resistor or several devices have to share the same resistor then ST suggests to utilize Solution 2 (see below).

3.1.2 Solution 2: diode (D_{GND}) in the ground line

A resistor (R_{GND} = 1kΩ) should be inserted in parallel to D_{GND} if the device drives an inductive load.

This small signal diode can be safely shared amongst several different HSDs. Also in this case, the presence of the ground network will produce a shift (≈ 600mV) in the input threshold and in the status output values if the microprocessor ground is not common to the device ground. This shift will not vary if more than one HSD shares the same diode/resistor network.

Series resistor in INPUT and STATUS lines are also required to prevent that, during battery voltage transient, the current exceeds the absolute maximum rating.

Safest configuration for unused INPUT and STATUS pin is to leave them unconnected.

3.2 Load dump protection

D_{ld} is necessary (Voltage Transient Suppressor) if the load dump peak voltage exceeds the V_{CC} max DC rating. The same applies if the device is subject to transients on the V_{CC} line that are greater than the ones shown in the ISO 7637-2: 2004(E) table.

3.3 MCU I/Os protection

If a ground protection network is used and negative transient are present on the V_{CC} line, the control pins will be pulled negative. ST suggests to insert a resistor (R_{prot}) in line to prevent the µC I/Os pins to latch-up.

The value of these resistors is a compromise between the leakage current of µC and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of µC I/Os.

$-V_{CCpeak}/I_{latchup} \leq R_{prot} \leq (V_{OH\mu C}-V_{IH}-V_{GND}) / I_{IHmax}$

Calculation example:

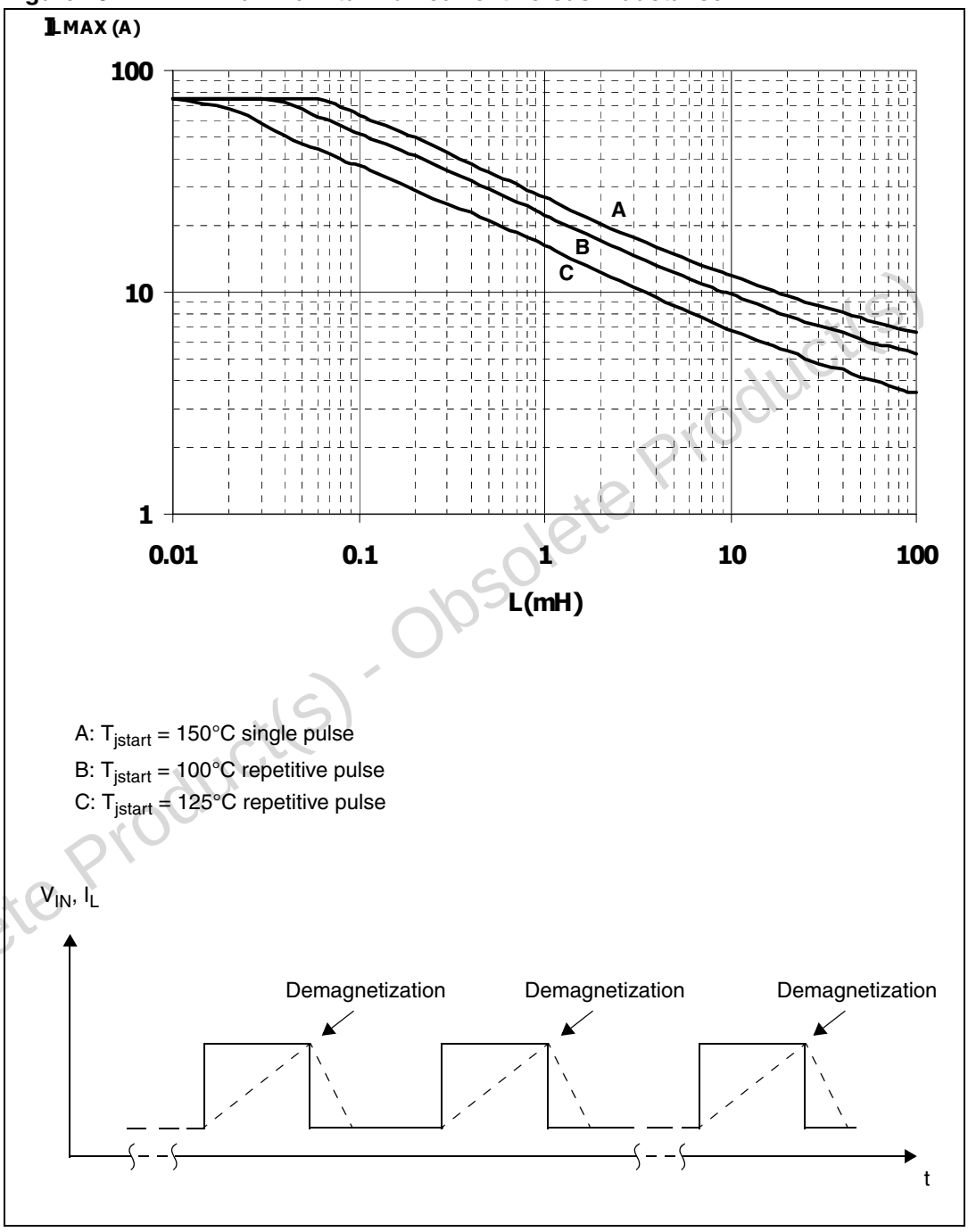
For V_{CCpeak}= - 100V and $I_{latchup} \geq$ 20mA; $V_{OH\mu C} \geq$ 4.5V

5kΩ $\leq R_{prot} \leq$ 65kΩ

Recommended values: R_{prot} =10kΩ.

3.4 P²PAK maximum demagnetization energy (V_{CC} = 13.5V)

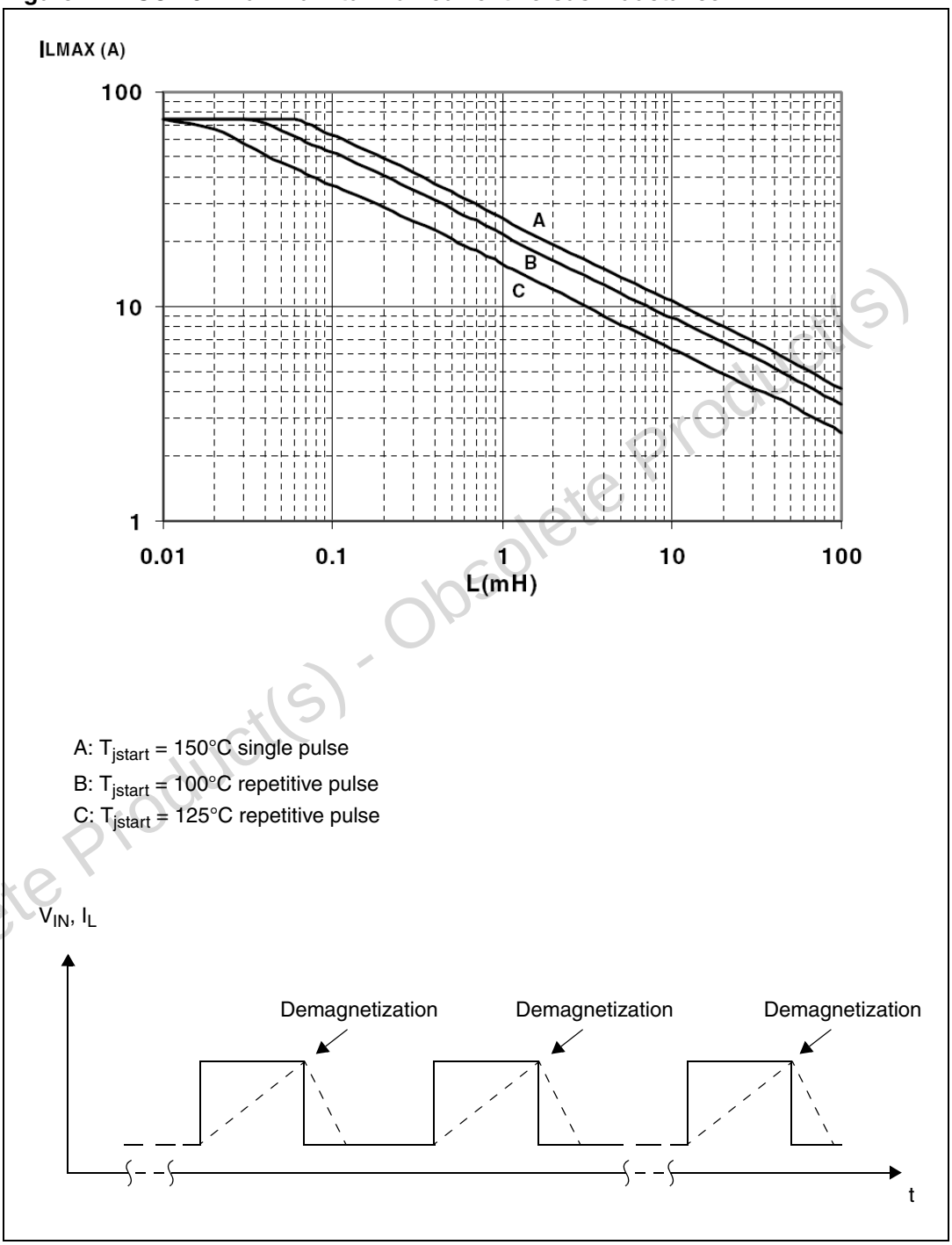
Figure 23. P²PAK maximum turn-off current versus inductance



Note: Values are generated with R_L =0 Ω In case of repetitive pulses, T_{jstart} (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves A and B.

3.5 SO-16L maximum demagnetization energy (V_{CC} = 13.5V)

Figure 24. SO-16L maximum turn-off current versus inductance

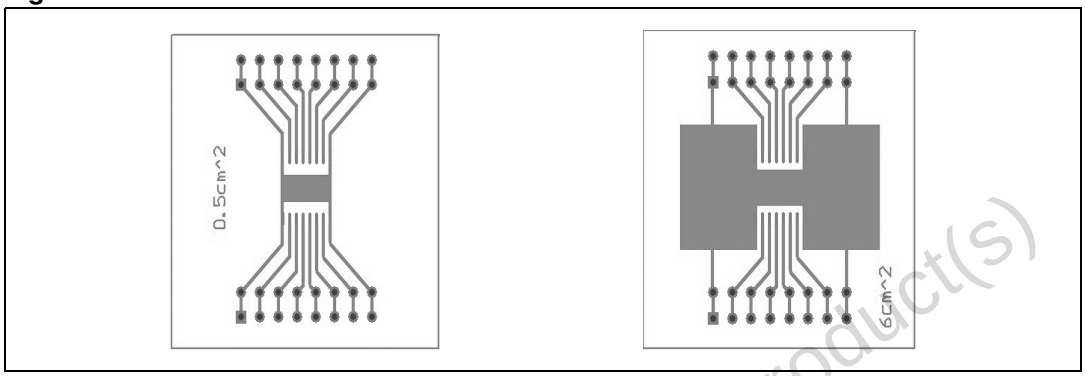


Note: Values are generated with R_L =0 Ω In case of repetitive pulses, T_{jstart} (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves A and B.

4 Package and PCB thermal data

4.1 SO-16L thermal data

Figure 25. SO-16L PC board



Note: Layout condition of R_{th} and Z_{th} measurements (PCB FR4 area = 41mm x 48mm, PCB thickness = 2mm, Cu thickness = 35µm, Copper areas: 0.5cm^2, 6cm^2).

Figure 26. SO-16L $R_{thj\text{-}amb}$ Vs PCB copper area in open box free air condition

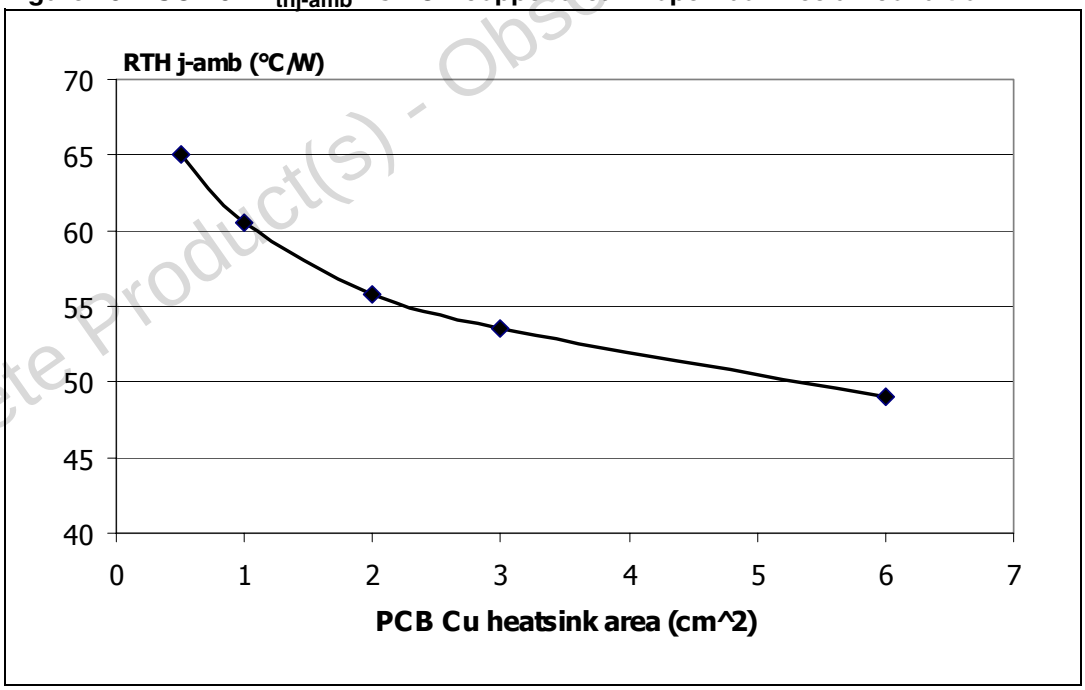
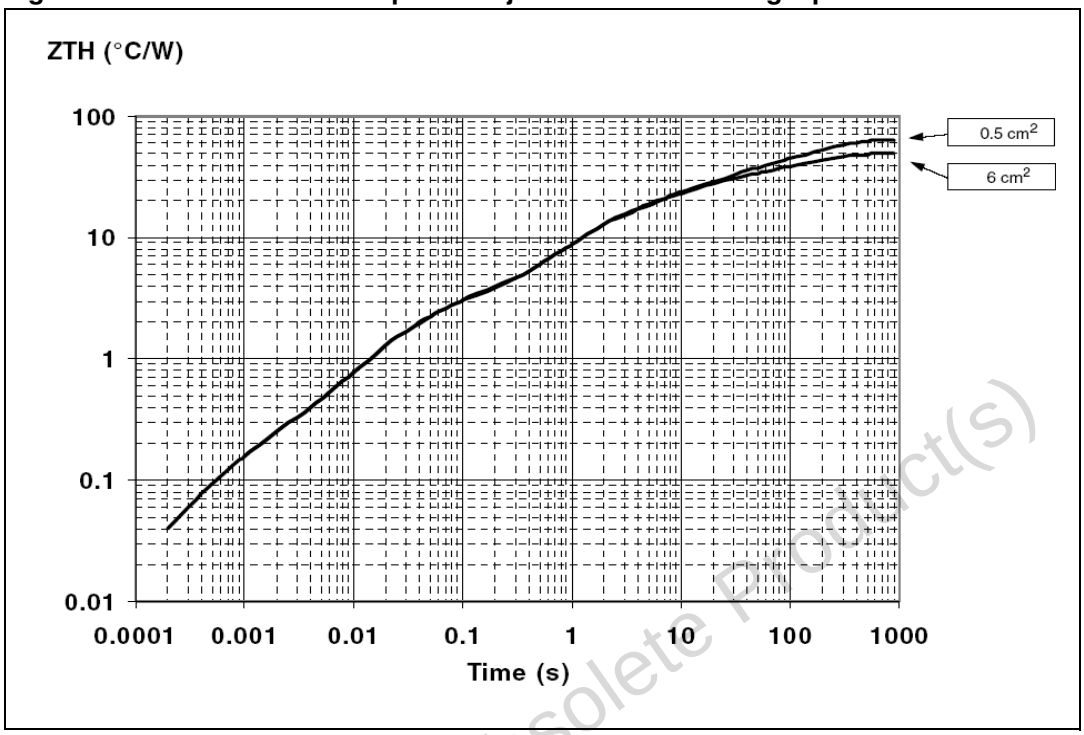


Figure 27. SO-16L thermal impedance junction ambient single pulse



Equation 1: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1-\delta)$$

where $\delta = t_p / T$

Figure 28. Thermal fitting model of a single channel HSD in SO-16L

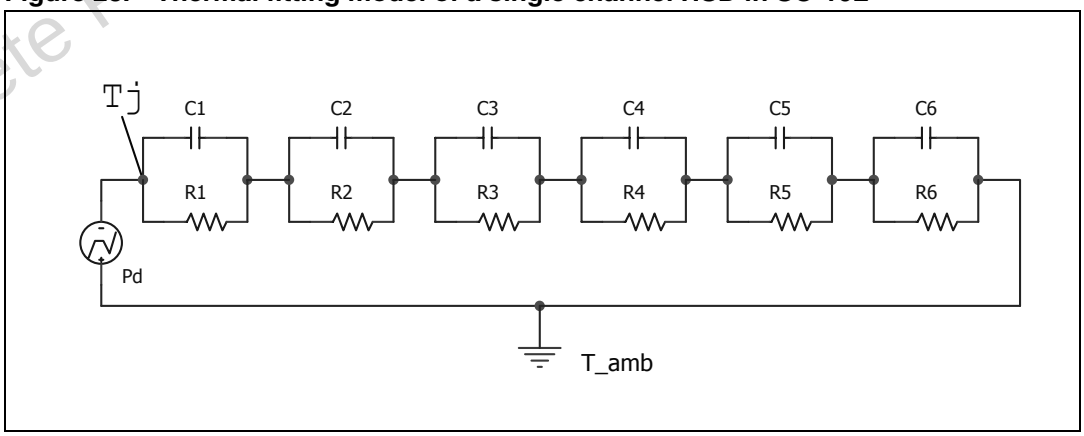
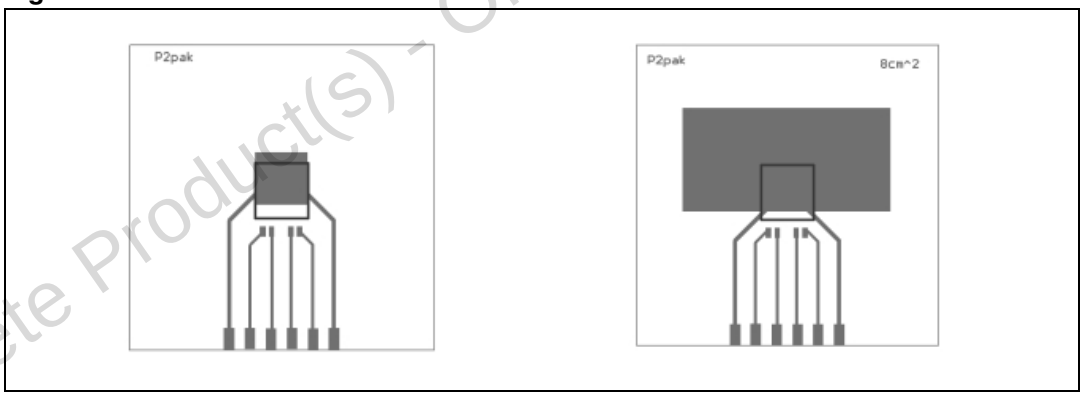


Table 14. SO-16L thermal parameters

Area / island (cm^2)	Footprint	6
R1 (°C/W)	0.02	
R2 (°C/W)	0.1	
R3 (°C/W)	2.2	
R4 (°C/W)	12	
R5 (°C/W)	15	
R6 (°C/W)	35	20
C1 (W.s/°C)	0.0015	
C2 (W.s/°C)	7E-03	
C3 (W.s/°C)	1.5E-02	
C4 (W.s/°C)	0.14	
C5 (W.s/°C)	1	
C6 (W.s/°C)	5	8

4.2 P^2PAK thermal data

Figure 29. P^2PAK PC board



Note: Layout condition of R_{th} and Z_{th} measurements (PCB FR4 area = 60mm x 60mm, PCB thickness = 2 mm, Cu thickness = 35µm , Copper areas: 0.97cm^2, 8cm^2).

Figure 30. P^2PAK $R_{thj-amb}$ Vs. PCB copper area in open box free air condition

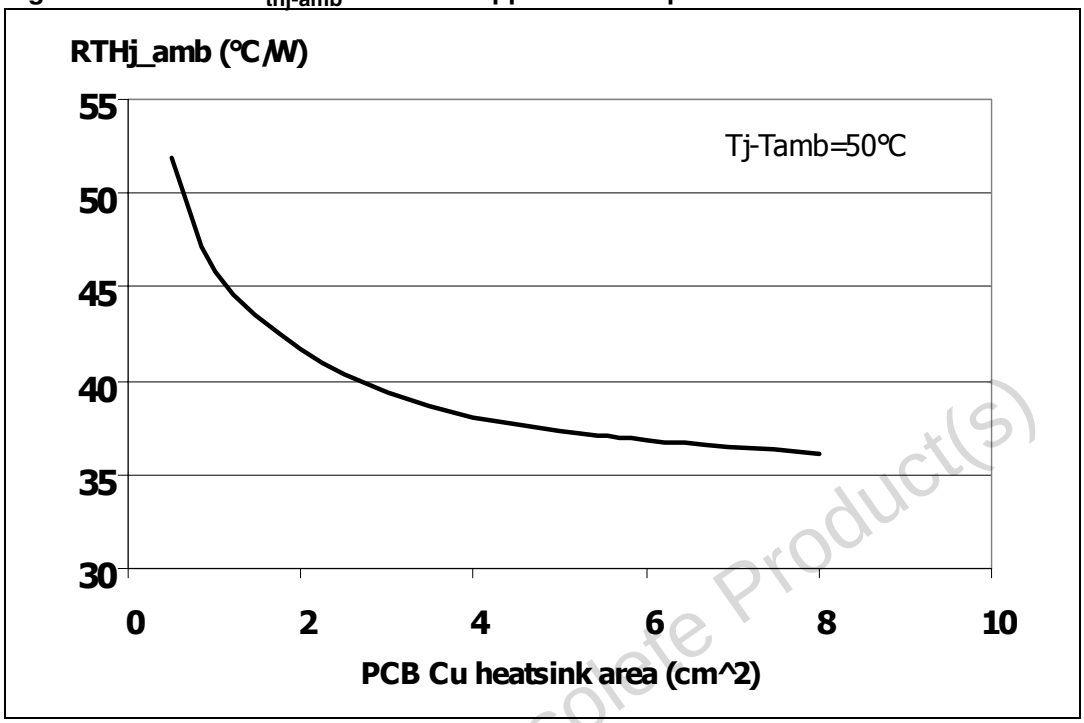
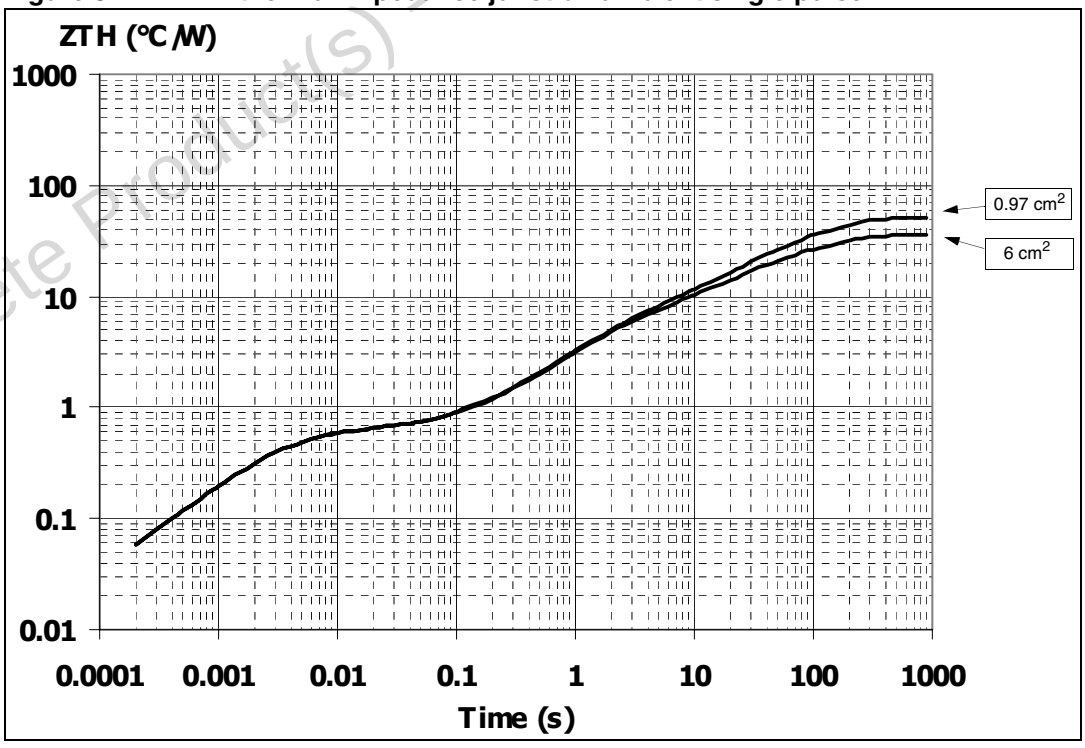


Figure 31. P^2PAK thermal impedance junction ambient single pulse



Equation 2: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_P/T$

Figure 32. Thermal fitting model of a single channel HSD in P²PAK

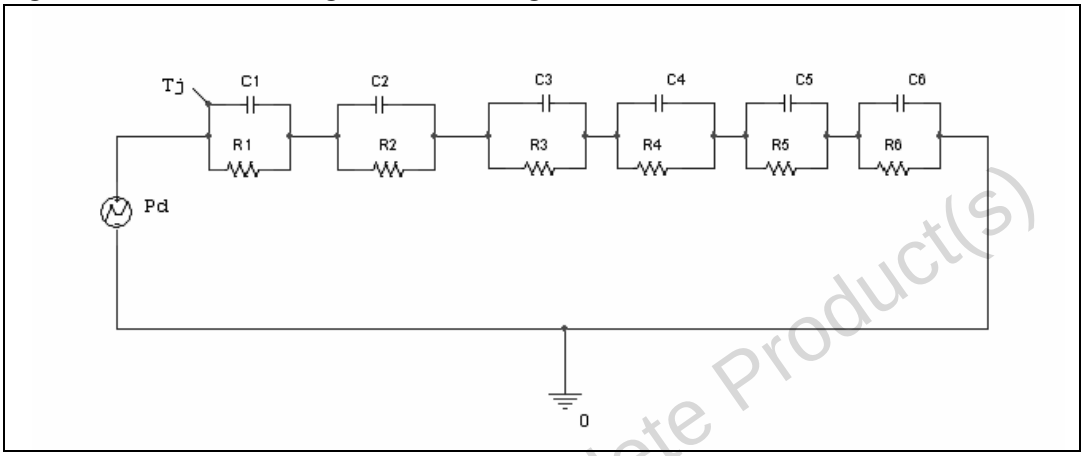


Table 15. P²PAK thermal parameters

Area/island (cm²)	0.97	6
R1 (°C/W)	0.02	
R2 (°C/W)	0.1	
R3 (°C/W)	0.22	
R4 (°C/W)	4	
R5 (°C/W)	9	
R6 (°C/W)	37	22
C1 (W·s/°C)	0.0015	
C2 (W·s/°C)	0.007	
C3 (W·s/°C)	0.015	
C4 (W·s/°C)	0.4	
C5 (W·s/°C)	2	
C6 (W·s/°C)	3	5

5 Package and packing information

5.1 ECOPACK® packages

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

Figure 33. SO-16L package dimensions

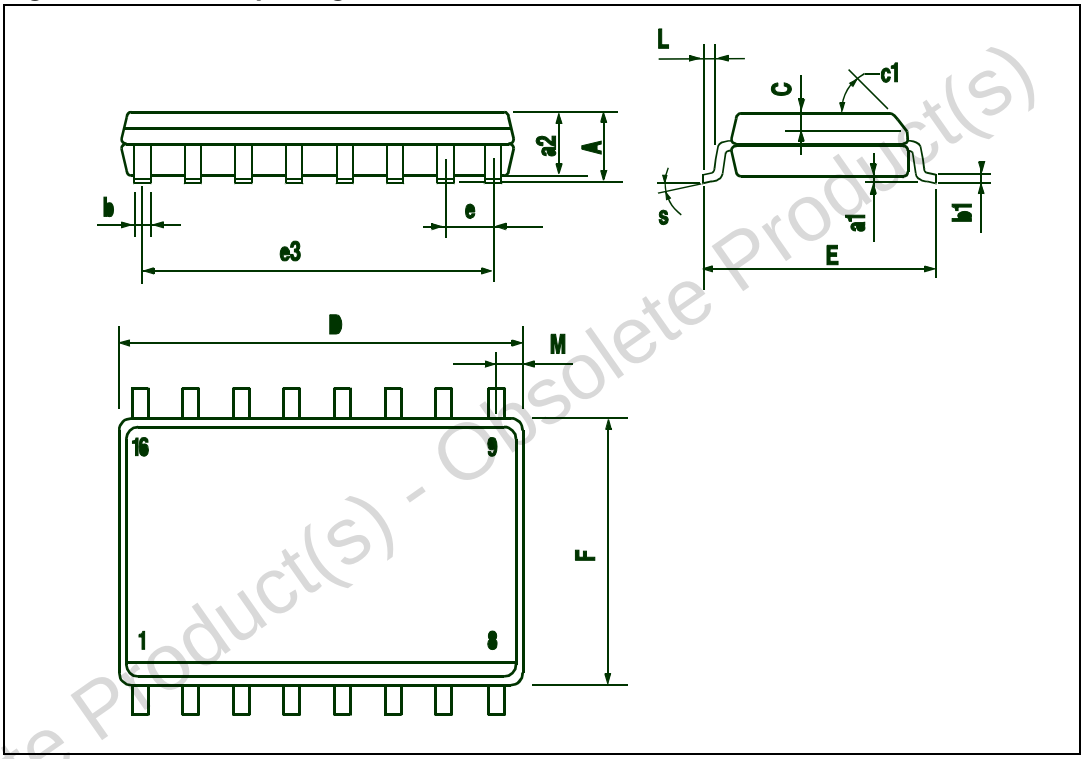


Table 16. SO-16L mechanical data

DIM.	mm.		
	Min.	Typ.	Max.
A			2.65
a1	0.1		0.2
a2			2.45
b	0.35		0.49
b1	0.23		0.32
C		0.5	
c1	45° (typ.)		

Table 16. SO-16L mechanical data (continued)

DIM.	mm.		
	Min.	Typ.	Max.
D	10.1		10.5
E	10.0		10.65
e		1.27	
e3		8.89	
F	7.4		7.6
L	0.5		1.27
M			0.75
S	8° (max.)		

5.2 P²PAK mechanical data

Figure 34. P²PAK package dimensions

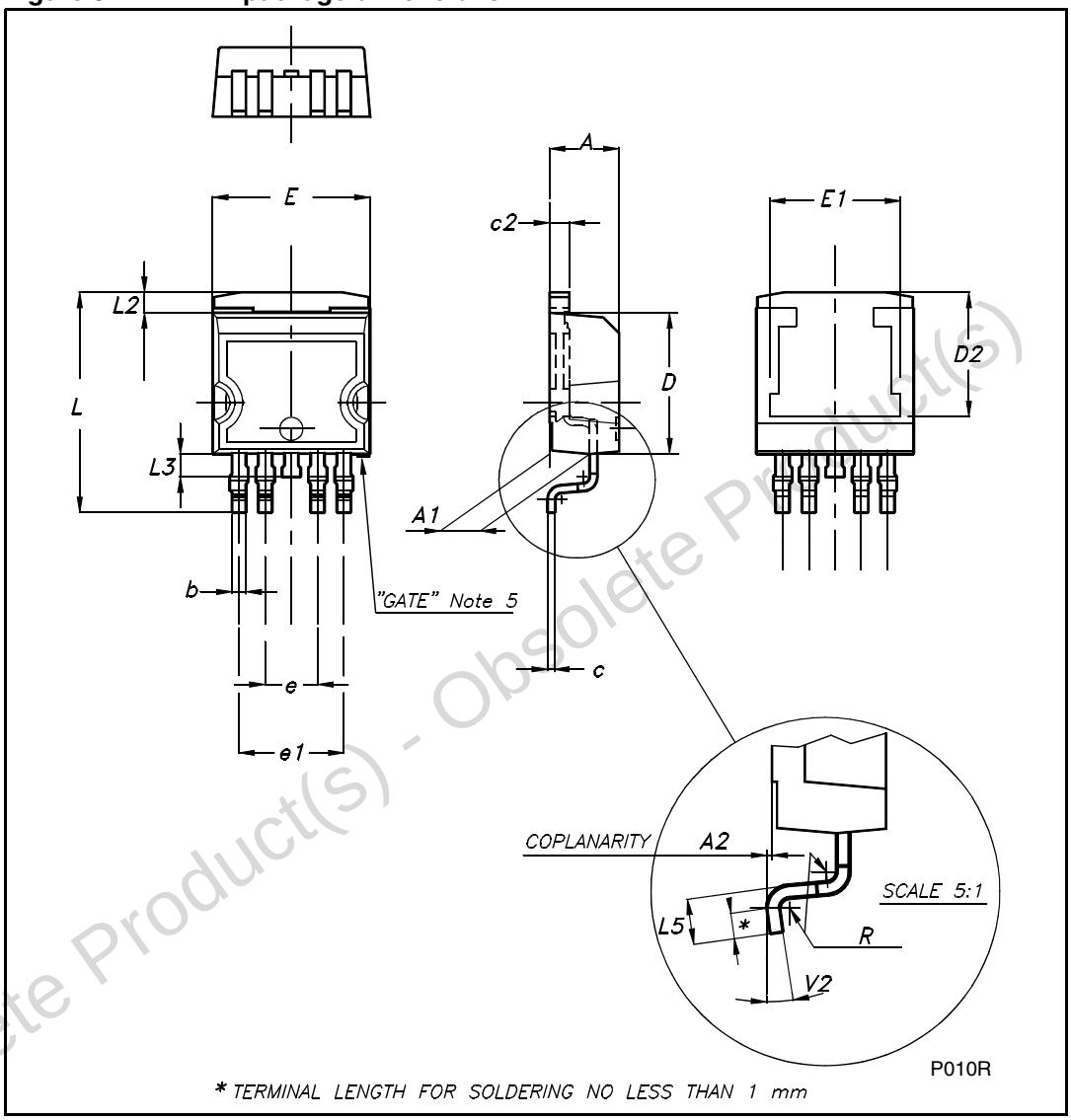
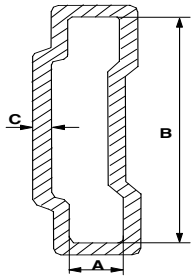


Table 17. P^2PAK mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.30		4.80
A1	2.40		2.80
A2	0.03		0.23
b	0.80		1.05
c	0.45		0.60
c2	1.17		1.37
D	8.95		9.35
D2		8.00	
E	10.00		10.40
E1		8.50	
e	3.20		3.60
e1	6.60		7.00
L	13.70		14.50
L2	1.25		1.40
L3	0.90		1.70
L5	1.55		2.40
R		0.40	
V2	0º		8º
Package weight	1.40 Gr (typ)		

5.3 SO-16L packing information

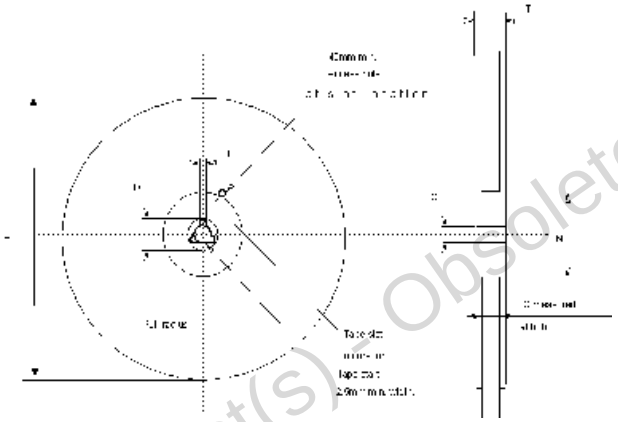
Figure 35. SO-16L tube shipment (no suffix)



Base Q.ty	50
Bulk Q.ty	1000
Tube length (± 0.5)	532
A	3.5
B	13.8
C (± 0.1)	0.6

All dimensions are in mm.

Figure 36. SO-16L tape and reel shipment (suffix "TR")



Reel dimensions

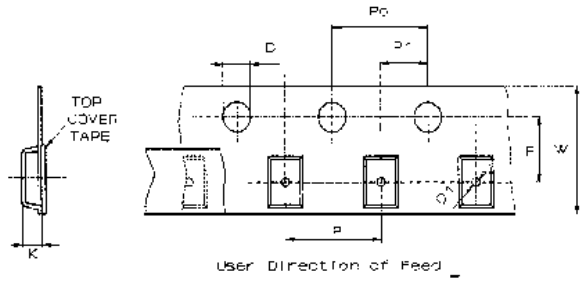
Base Q.ty	1000
Bulk Q.ty	1000
A (max)	330
B (min)	1.5
C (± 0.2)	13
F	20.2
G (+ 2 / -0)	16.4
N (min)	60
T (max)	22.4

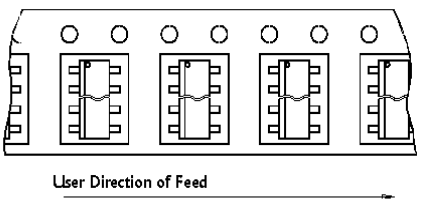
Tape dimensions

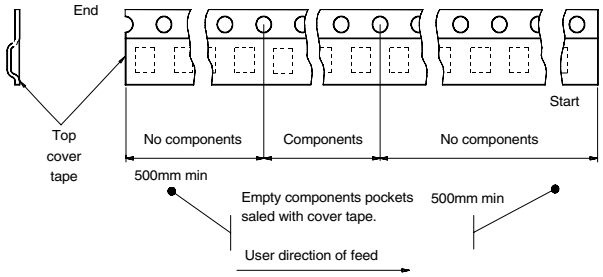
According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb. 1986

Tape width	**W**	16
Tape Hole Spacing	**P0 (± 0.1)**	4
Component Spacing	**P**	12
Hole Diameter	**D (± 0.1/-0)**	1.5
Hole Diameter	**D1 (min)**	1.5
Hole Position	**F (± 0.05)**	7.5
Compartment Depth	**K (max)**	6.5
Hole Spacing	**P1 (± 0.1)**	2

All dimensions are in mm.

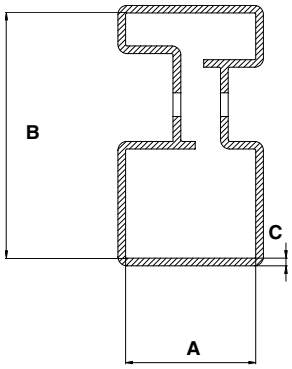






5.4 P²PAK packing information

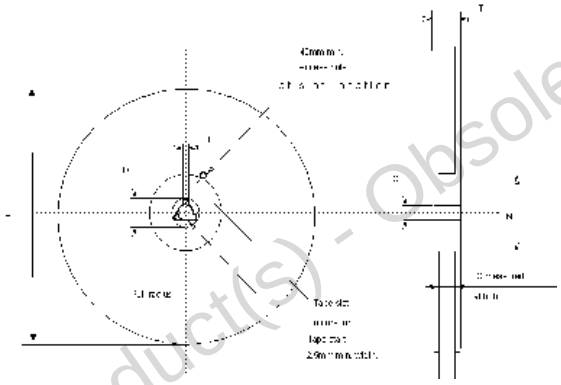
Figure 37. P²PAK tube shipment (no suffix)



Base Q.ty	50
Bulk Q.ty	1000
Tube length (± 0.5)	532
A	18
B	33.1
C (± 0.1)	1

All dimensions are in mm.

Figure 38. P²PAK tape and reel (suffix "13TR")



REEL DIMENSIONS

All dimensions are in mm.

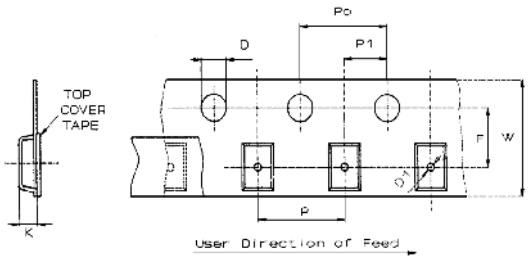
Base Q.ty	1000
Bulk Q.ty	1000
A (max)	330
B (min)	1.5
C (± 0.2)	13
F	20.2
G (+ 2 / -0)	24.4
N (min)	60
T (max)	30.4

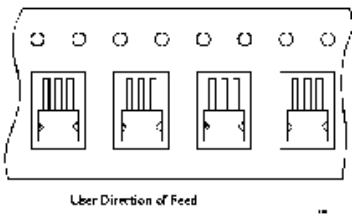
TAPE DIMENSIONS

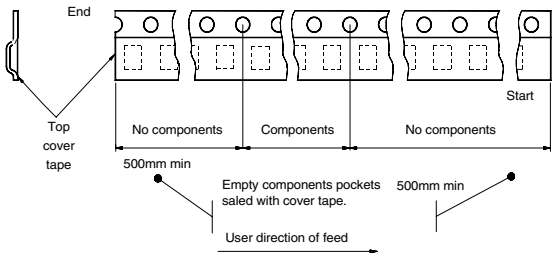
According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb 1986

Tape width	**W**	24
Tape Hole Spacing	**P0 (± 0.1)**	4
Component Spacing	**P**	12
Hole Diameter	**D (± 0.1/-0)**	1.5
Hole Diameter	**D1 (min)**	1.5
Hole Position	**F (± 0.05)**	11.5
Compartment Depth	**K (max)**	6.5
Hole Spacing	**P1 (± 0.1)**	2

All dimensions are in mm.







6 Revision history

Table 18. Document revision history

Date	Revision	Changes
09-Sep-2004	1	Initial release.
03-May-2006	2	Suggested connections for unused and n.c.pins correction (page 2).
19-Dec-2008	3	Document reformatted and restructured. Added content, list of figures and tables. Added *ECOPACK® packages* information. Updated *Figure 38.: P^2PAK tape and reel (suffix "13TR")*: changed component spacing (P) in tape dimensions table from 16 mm to 12 mm.
24-Sep-2013	4	Updated Disclaimer.

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