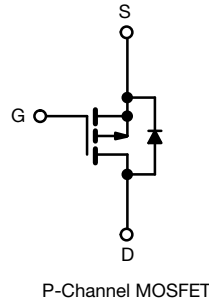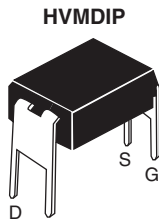# Power MOSFET

HVMDIP

P-Channel MOSFET

FEATURES
- Dynamic dV/dt rating
- Repetitive avalanche rated
- For automatic insertion
- End stackable
- P-channel
- Fast switching
- Ease of paralleling
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

RoHS
COMPLIANT

DESCRIPTION

The power MOSFETs technology is the key to Vishay advanced line of power MOSFET transistors. The efficient geometry and unique processing of the power MOSFETs design archieve very low on-state resistance combined with high transconductance and extreme device ruggedness.

The 4 pin DIP package is a low cost machine-insertable case style which can be stacked in multiple combinations on standard 0.1" pin centers. The dual drain serves as a thermal link to the mounting surface for power dissipation levels up to 1 W.

PRODUCT SUMMARY

V_{DS} (V)	-200	
$R_{DS(on)}$ (Ω)	V_{GS} = -10 V	3.0
Q_g (Max.) (nC)	8.9	
Q_{gs} (nC)	2.1	
Q_{gd} (nC)	3.9	
Configuration	Single	

ORDERING INFORMATION

Package	HVMDIP
Lead (Pb)-free	IRFD9210PbF

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)

PARAMETER			SYMBOL	LIMIT	UNIT
Drain-source voltage			V_{DS}	-200	V
Gate-source voltage			V_{GS}	± 20	
Continuous drain current	V_{GS} at -10 V	T_A = 25 °C	I_D	-0.40	A
		T_A = 100 °C		-0.25	
Pulsed drain current [a]			I_{DM}	-3.2	
Linear derating factor				0.0083	W/°C
Single pulse avalanche energy [b]			E_{AS}	210	mJ
Repetitive avalanche current [a]			I_{AR}	-0.40	A
Repetitive avalanche energy [a]			E_{AR}	0.10	mJ
Maximum power dissipation		T_A = 25 °C	P_D	1.0	W
Peak diode recovery dv/dt [c]			dV/dt	-5.0	V/ns
Operating junction and storage temperature range			T_J, T_{stg}	-55 to + 150	°C
Soldering rRecommendations (peak temperature) [d]		For 10 s		300[d]	

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)

b. V_{DD} = -50 V, starting T_J = 25 °C, L = 123 mH, R_g = 25 Ω, I_{AS} = -1.6 A (see fig. 12)

c. I_{SD} ≤ -2.3 A, dI/dt ≤ 70 A/µs, V_{DD} ≤ V_{DS}, T_J ≤ 150 °C

d. 1.6 mm from case

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	120	°C/W

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = -250 µA		-200	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to 25 °C, I_D = -1 mA		-	-0.23	-	V/°C
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -250 µA		-2.0	-	-4.0	V
Gate-Source Leakage	I_{GSS}	V_{GS} = ± 20 V		-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -200 V, V_{GS} = 0 V		-	-	-100	µA
		V_{DS} = -160 V, V_{GS} = 0 V, T_J = 125 °C		-	-	-500	
Drain-Source On-State Resistance	$R_{DS(on)}$	V_{GS} = -10 V	I_D = -0.24 A[b]	-	-	3.0	Ω
Forward Transconductance	g_{fs}	V_{DS} = -50 V, I_D = -0.24 A		0.27	-	-	S
Dynamic							
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = -25 V, f = 1.0 MHz, see fig. 5		-	170	-	pF
Output Capacitance	C_{oss}			-	54	-	
Reverse Transfer Capacitance	C_{rss}			-	16	-	
Total Gate Charge	Q_g	V_{GS} = -10 V	I_D = -1.3 A, V_{DS} = -160 V see fig. 6 and 13[b]	-	-	8.9	nC
Gate-Source Charge	Q_{gs}			-	-	2.1	
Gate-Drain Charge	Q_{gd}			-	-	3.9	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = -100 V, I_D = -2.3 A R_g = 24 Ω, R_D = 41 Ω, see fig. 10[b]		-	8.0	-	ns
Rise Time	t_r			-	12	-	
Turn-Off Delay Time	$t_{d(off)}$			-	11	-	
Fall Time	t_f			-	13	-	
Internal Drain Inductance	L_D	Between lead, 6 mm (0.25") from package and center of die contact		-	4.0	-	nH
Internal Source Inductance	L_S			-	6.0	-	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode		-	-	-0.40	A
Pulsed Diode Forward Current[a]	I_{SM}			-	-	-3.2	
Body Diode Voltage	V_{SD}	T_J = 25 °C, I_S = -0.40 A, V_{GS} = 0 V[b]		-	-	-5.8	V
Body Diode Reverse Recovery Time	t_{rr}	T_J = 25 °C, I_F = -2.3 A, dI/dt = 100 A/µs[b]		-	110	220	ns
Body Diode Reverse Recovery Charge	Q_{rr}			-	0.56	1.1	µC

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)

b. Pulse width ≤ 300 µs; duty cycle ≤ 2 %

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)
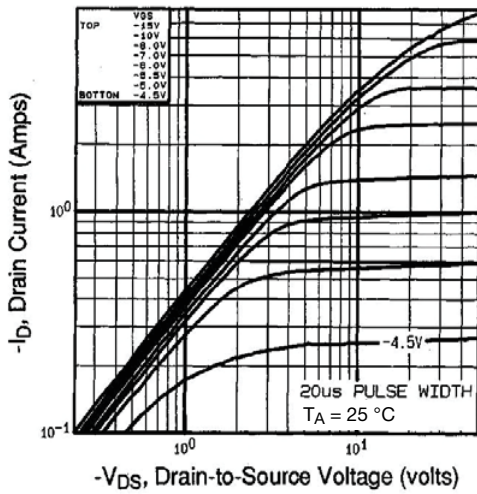

Fig. 1 - Typical Output Characteristics, T_A = 25 °C
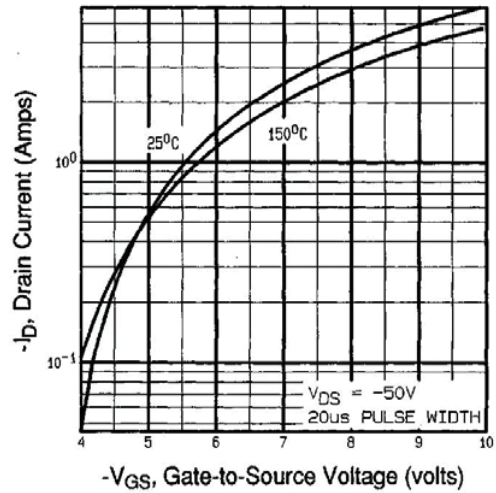

Fig. 3 - Typical Transfer Characteristics
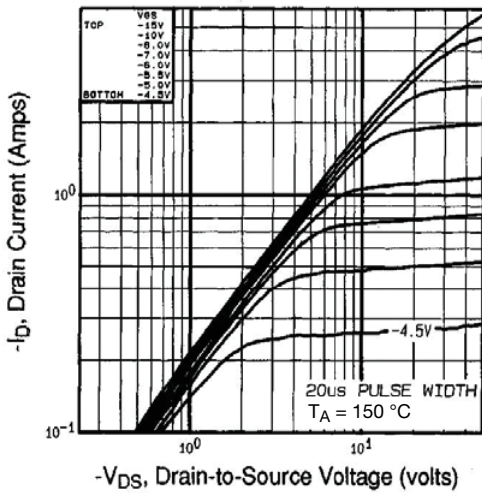

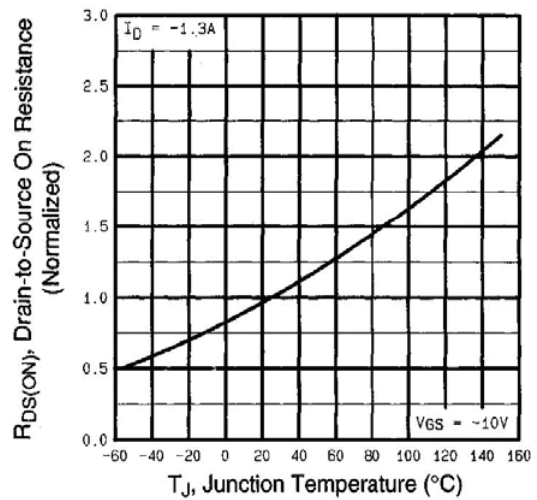Fig. 2 - Typical Output Characteristics, T_A = 150 °C

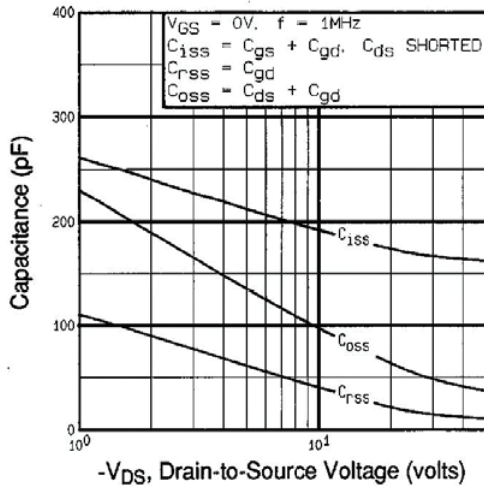Fig. 4 - Normalized On-Resistance vs. Temperature

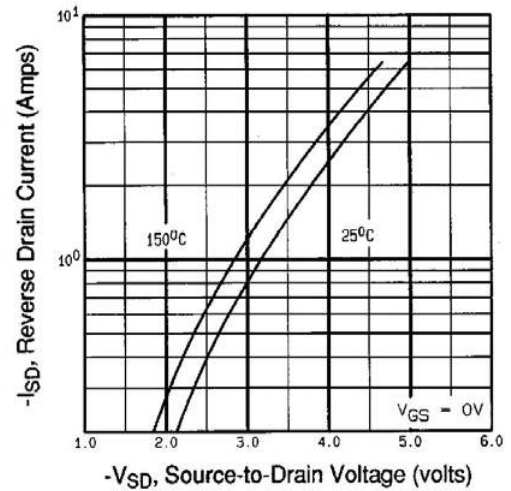Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

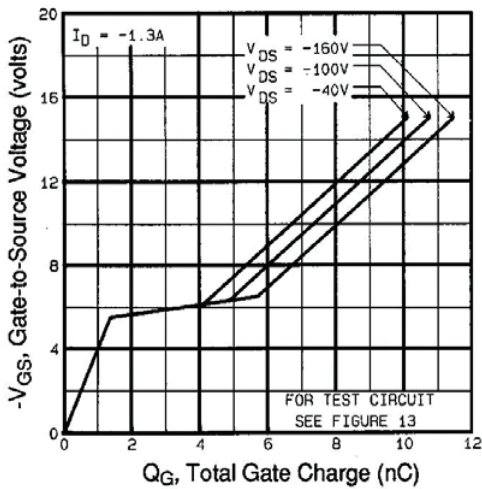Fig. 7 - Typical Source-Drain Diode Forward Voltage
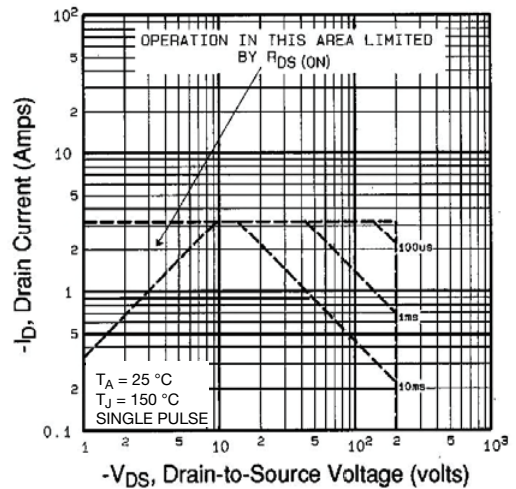

Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

Fig. 8 - Maximum Safe Operating Area

4

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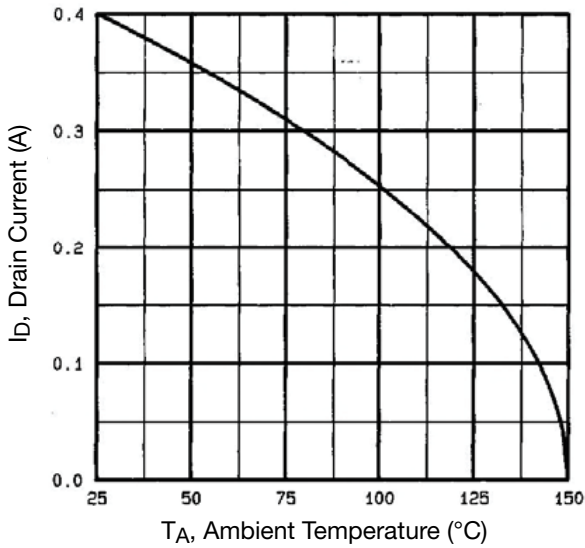For technical questions, contact: hvmos.techsupport@vishay.com

Fig. 9 - Maximum Drain Current vs. Ambient Temperature
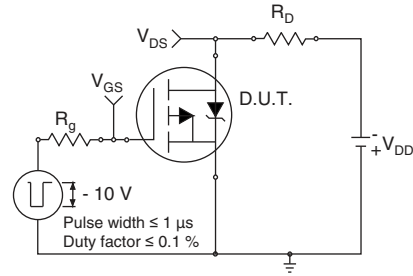
Fig. 10a - Switching Time Test Circuit

Fig. 10b - Switching Time Waveforms

NOTES:
1. DUTY FACTOR, $D = t_1/t_2$
2. PEAK $T_j = P_{DM} \times Z_{thjc} + T_C$
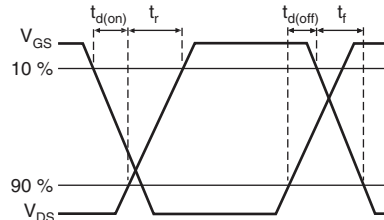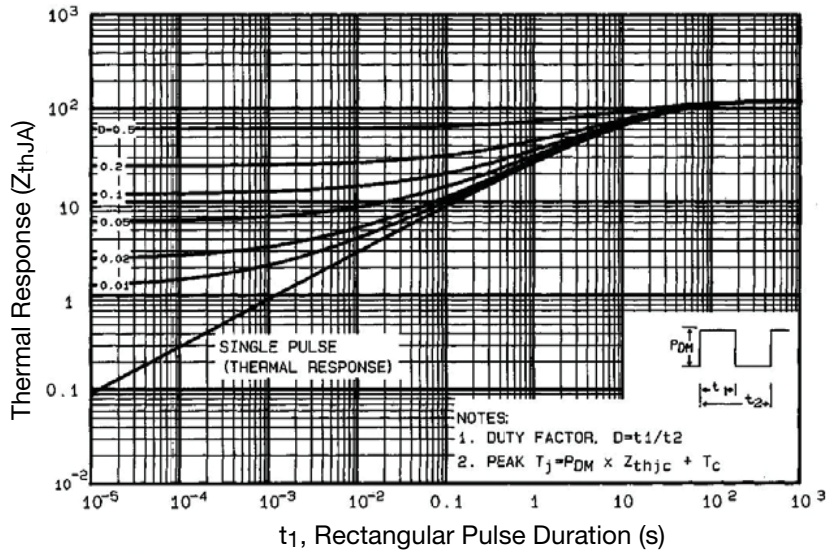
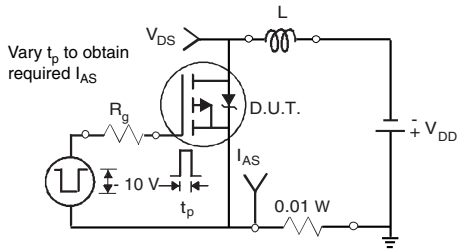Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

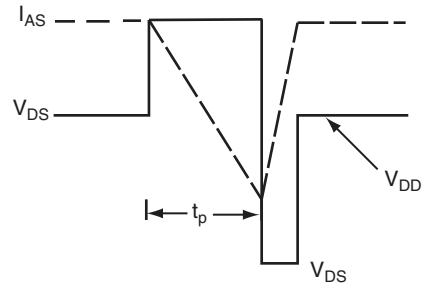Fig. 12a - Unclamped Inductive Test Circuit
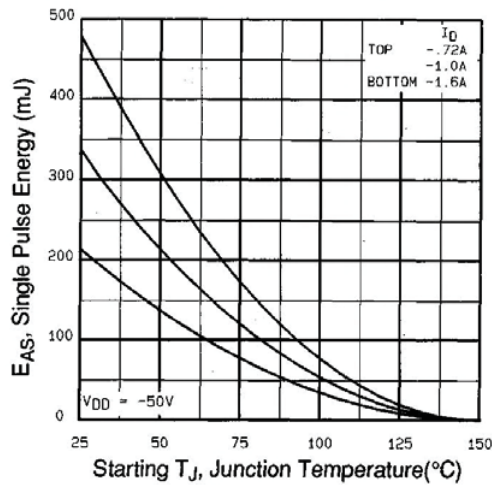

Fig. 12b - Unclamped Inductive Waveforms

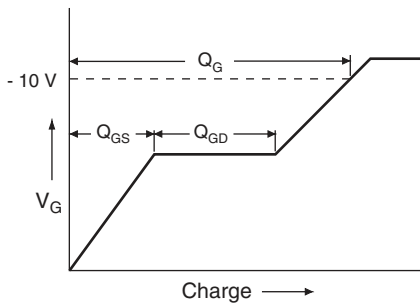Fig. 12c - Maximum Avalanche Energy vs. Drain Current
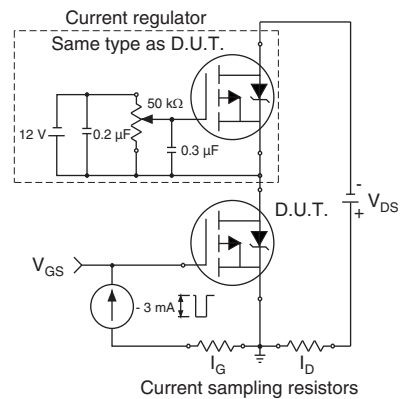

Fig. 13a - Basic Gate Charge Waveform

Fig. 13b - Gate Charge Test Circuit

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Peak Diode Recovery dV/dt Test Circuit

D.U.T.

③

Circuit layout considerations
• Low stray inductance
• Ground plane
• Low leakage inductance
  current transformer

②

④

①

R_g

• dV/dt controlled by R_g
• I_{SD} controlled by duty factor "D"
• D.U.T. - device under test

V_{DD}
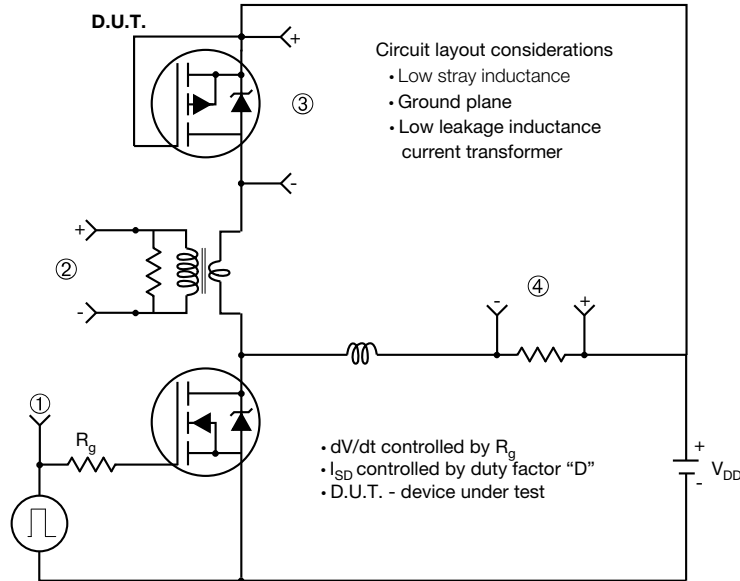
Note
• Compliment N-Channel of D.U.T. for driver
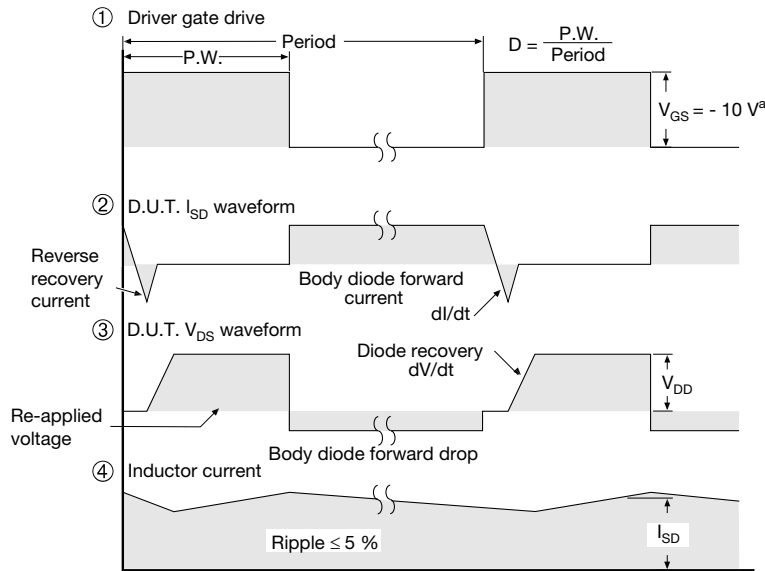
① Driver gate drive

P.W.

Period

$D = \dfrac{\text{P.W.}}{\text{Period}}$

$V_{GS} = -10\ V^a$

② D.U.T. I_{SD} waveform

Reverse recovery current

Body diode forward current

dI/dt

③ D.U.T. V_{DS} waveform

Diode recovery dV/dt

V_{DD}

Re-applied voltage

Body diode forward drop

④ Inductor current

Ripple ≤ 5 %

I_{SD}

Note
a. $V_{GS} = -5\ V$ for logic level and $-3\ V$ drive devices

Fig. 14 - For P-Channel

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HVM DIP (High voltage)
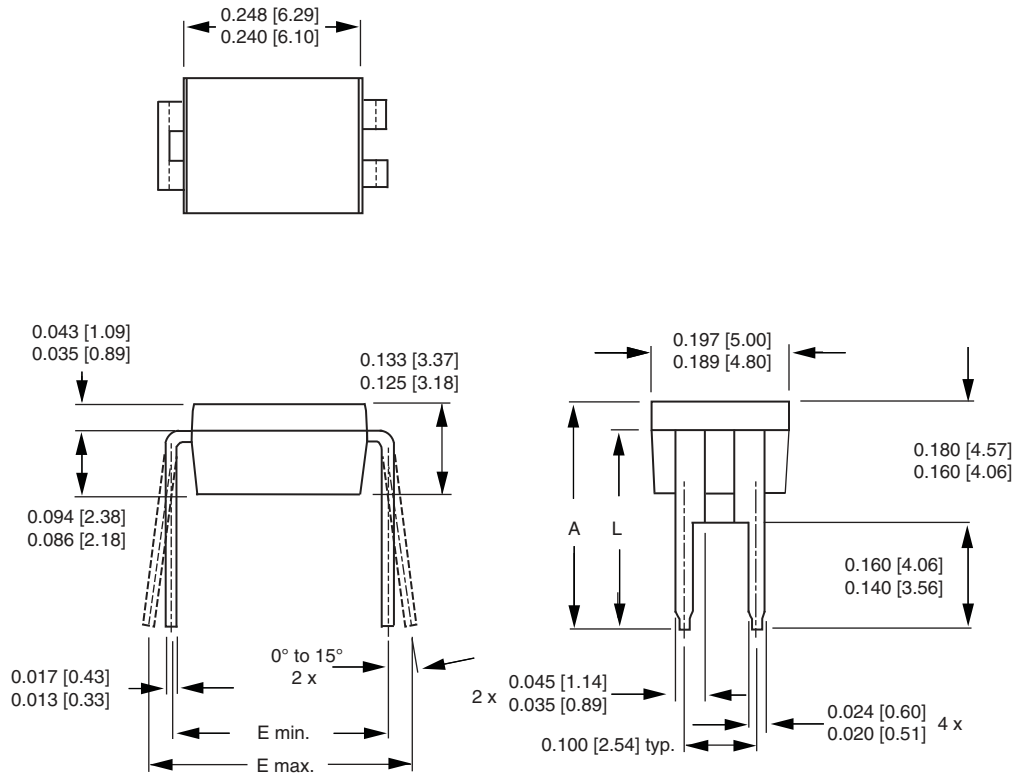
	INCHES		MILLIMETERS	
DIM.	**MIN.**	**MAX.**	**MIN.**	**MAX.**
A	0.310	0.330	7.87	8.38
E	0.300	0.425	7.62	10.79
L	0.270	0.290	6.86	7.36
ECN: X10-0386-Rev. B, 06-Sep-10 DWG: 5974				

Note

1. Package length does not include mold flash, protrusions or gate burrs. Package width does not include interlead flash or protrusions.

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