

NEW PRODUCT

Product Summary

$V_{(BR)DSS}$	$R_{DS(on) \text{ max}}$	I_D $T_C = +25^\circ\text{C}$
-60V	55m Ω @ $V_{GS} = -10\text{V}$	-11.3A
	70m Ω @ $V_{GS} = -4.5\text{V}$	-9.1A

Description

This new generation MOSFET is designed to minimize the on-state resistance ($R_{DS(on)}$) and yet maintain superior switching performance, making it ideal for high efficiency power management applications.

Applications

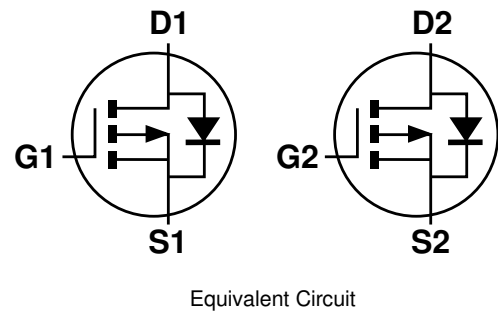
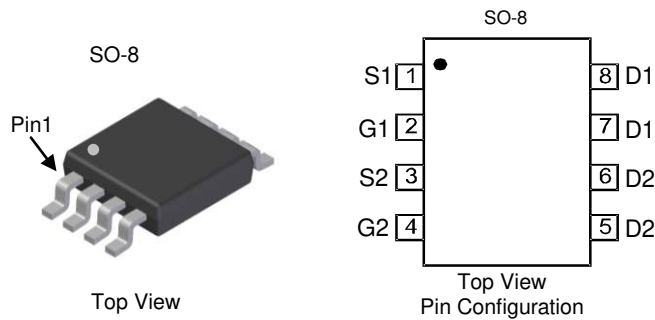
- DC-DC Converters
- Power Management Functions
- Backlighting

Features

- Low On-Resistance
- Low Input Capacitance
- Fast Switching Speed
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**

Mechanical Data

- Case: SO-8
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections: See Diagram
- Terminals: Finish – Matte Tin Annealed over Copper Leadframe Solderable per MIL-STD-202, Method 208^{e3}
- Weight: 0.076 grams (Approximate)

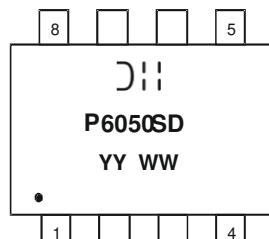


Ordering Information (Note 4)

Part Number	Case	Packaging
DMP6050SSD-13	SO-8	2500 / Tape & Reel

- Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
 2. See http://www.diodes.com/quality/lead_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
 4. For packaging details, go to our website at <http://www.diodes.com/products/packages.html>.

Marking Information



Dii = Manufacturer's Marking
 P6050SD = Product Type Marking Code
 YYWW = Date Code Marking
 YY or YY = Year (ex: 14 = 2014)
 WW = Week (01 - 53)

Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit
Drain-Source Voltage	V _{DSS}	-60	V
Gate-Source Voltage	V _{GSS}	±20	V
Continuous Drain Current (Note 6) V _{GS} = -10V	I _D	T _C = +25°C	-11.3
		T _C = +70°C	-9.1
	I _D	T _A = +25°C	-4.8
		T _A = +70°C	-3.9
Pulsed Drain Current (10µs pulse, duty cycle = 1%)	I _{DM}	-32	A
Maximum Continuous Body Diode Forward Current (Note 6)	I _S	-2.8	A
Avalanche Current (Note 7) L = 0.1mH	I _{AS}	-24.8	A
Avalanche Energy (Note 7) L = 0.1mH	E _{AS}	30.8	mJ

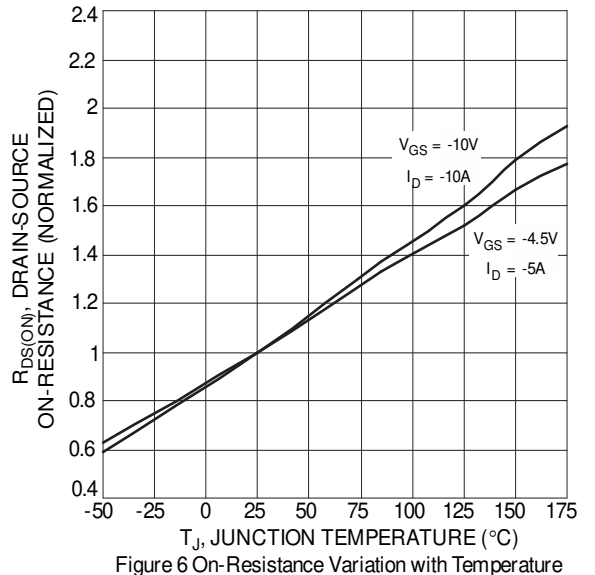
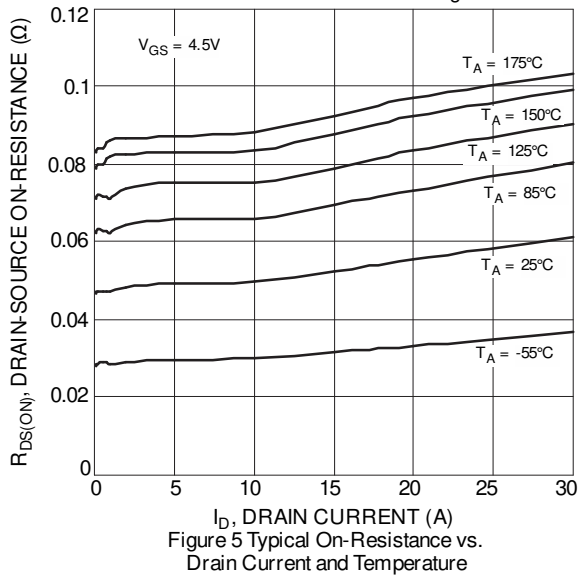
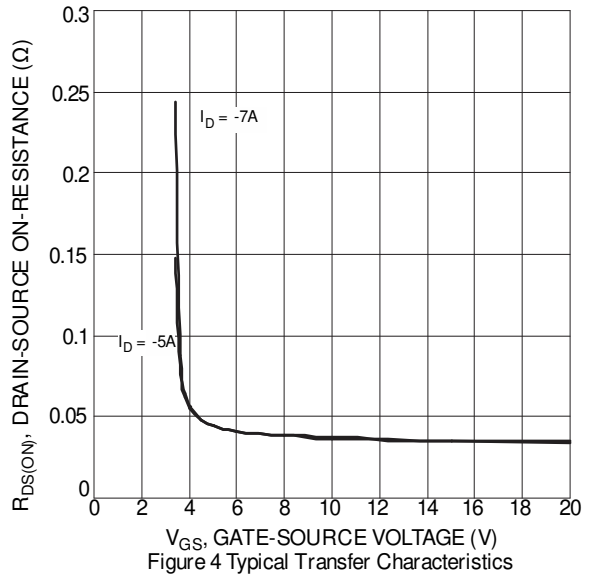
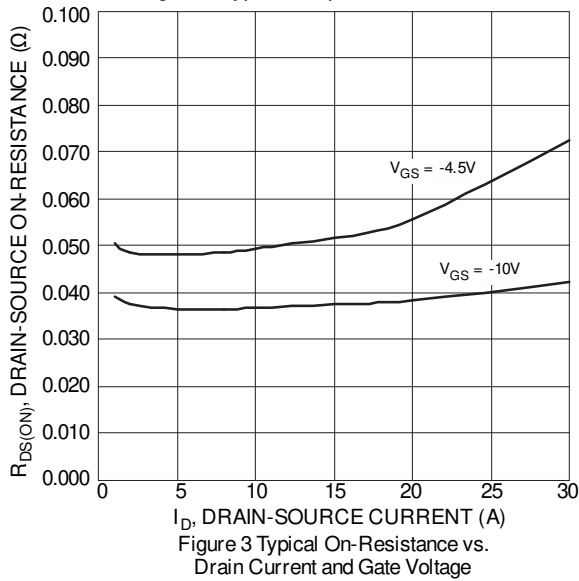
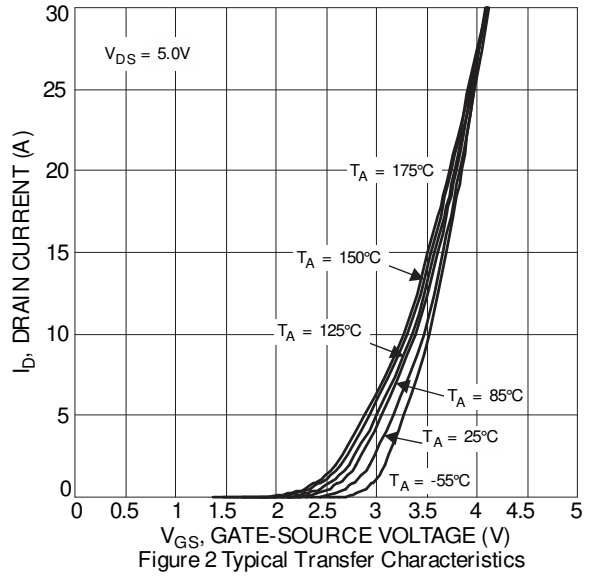
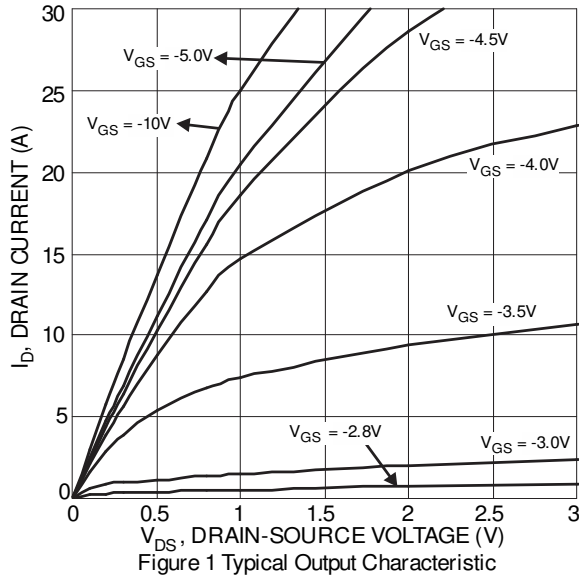
Thermal Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Units
Total Power Dissipation (Note 5)	P _D	T _A = +25°C	1.2
		T _A = +70°C	0.9
Thermal Resistance, Junction to Ambient (Note 5)	R _{θJA}	Steady state	104
		t < 10s	45
Total Power Dissipation (Note 6)	P _D	T _A = +25°C	1.7
		T _A = +70°C	1.1
Thermal Resistance, Junction to Ambient (Note 6)	R _{θJA}	Steady state	72
		t < 10s	37
Thermal Resistance, Junction to Case (Note 6)	R _{θJC}	13	
Operating and Storage Temperature Range	T _J , T _{STG}	-55 to +150	°C

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 8)						
Drain-Source Breakdown Voltage	BV _{DSS}	-60	—	—	V	V _{GS} = 0V, I _D = -250µA
Zero Gate Voltage Drain Current T _J = +25°C	I _{DSS}	—	—	-1	µA	V _{DS} = -60V, V _{GS} = 0V
Gate-Source Leakage	I _{GSS}	—	—	±100	nA	V _{GS} = ±20V, V _{DS} = 0V
ON CHARACTERISTICS (Note 8)						
Gate Threshold Voltage	V _{GS(th)}	-1.0	—	-3.0	V	V _{DS} = V _{GS} , I _D = -250µA
Static Drain-Source On-Resistance	R _{DS(on)}	-	36	55	mΩ	V _{GS} = -10V, I _D = -5A
		-	47	70		V _{GS} = -4.5V, I _D = -4A
Diode Forward Voltage	V _{SD}	-	-0.7	-1.2	V	V _{GS} = 0V, I _S = -1A
DYNAMIC CHARACTERISTICS (Note 9)						
Input Capacitance	C _{iss}	-	1293	-	pF	V _{DS} = -30V, V _{GS} = 0V, f = 1.0MHz
Output Capacitance	C _{oss}	-	86.3	-	pF	
Reverse Transfer Capacitance	C _{rss}	-	64.7	-	pF	
Gate Resistance	R _g	-	12	-	Ω	V _{DS} = 0V, V _{GS} = 0V, f = 1MHz
Total Gate Charge (V _{GS} = -4.5V)	Q _g	-	11.9	-	nC	V _{DS} = -30V, I _D = -5A
Total Gate Charge (V _{GS} = -10V)	Q _g	-	24	-	nC	
Gate-Source Charge	Q _{gs}	-	3.6	-	nC	
Gate-Drain Charge	Q _{gd}	-	5.7	-	nC	
Turn-On Delay Time	t _{D(on)}	-	4.3	-	ns	
Turn-On Rise Time	t _r	-	6.3	-	ns	V _{GS} = -10V, V _{DS} = -30V, R _G = 3Ω, I _D = -5A
Turn-Off Delay Time	t _{D(off)}	-	46.7	-	ns	
Turn-Off Fall Time	t _f	-	25.3	-	ns	
Body Diode Reverse Recovery Time	t _{rr}	—	13.6	—	ns	I _F = -5A, di/dt = 100A/µs
Body Diode Reverse Recovery Charge	Q _{rr}	—	7.4	—	nC	I _F = -5A, di/dt = 100A/µs

- Notes:
- Device mounted on FR-4 PC board, with minimum recommended pad layout, single sided.
 - Device mounted on FR-4 substrate PC board, 2oz copper, with thermal bias to bottom layer 1inch square copper plate.
 - I_{AS} and E_{AS} rating are based on low frequency and duty cycles to keep T_J = +25°C.
 - Short duration pulse test used to minimize self-heating effect.
 - Guaranteed by design. Not subject to product testing.



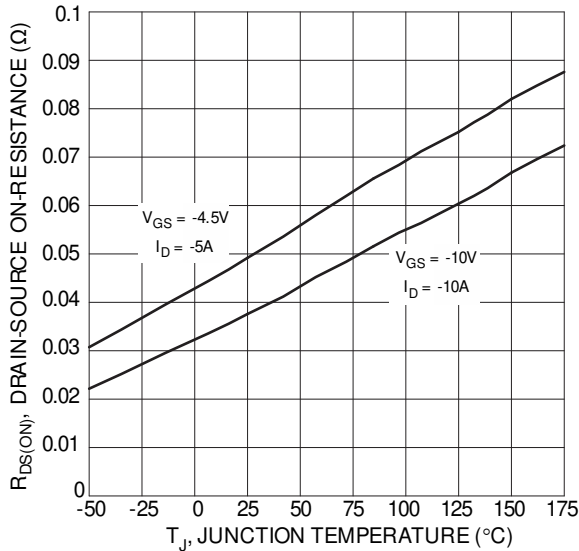


Figure 7 On-Resistance Variation with Temperature

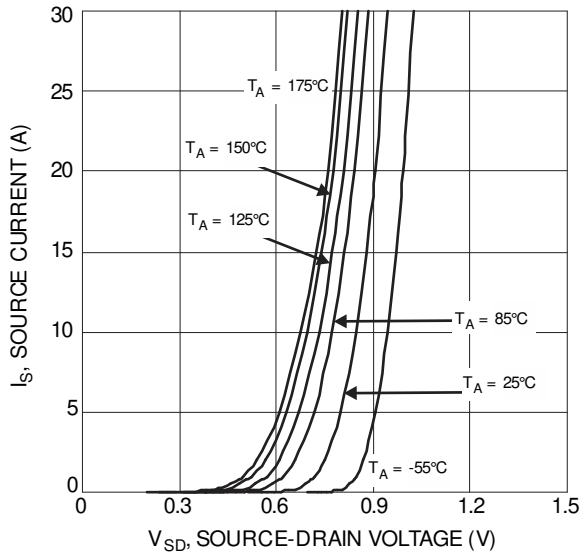


Figure 9 Diode Forward Voltage vs. Current

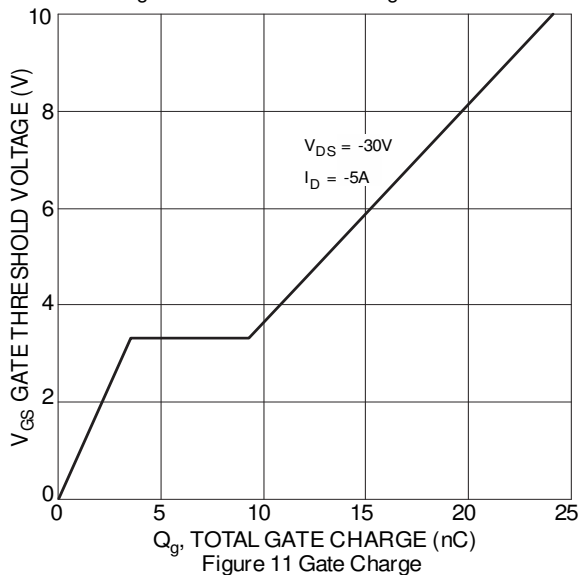


Figure 11 Gate Charge

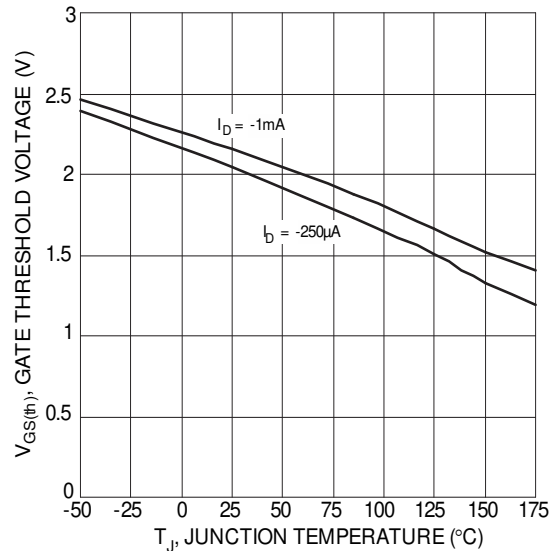


Figure 8 Gate Threshold Variation vs. Ambient Temperature

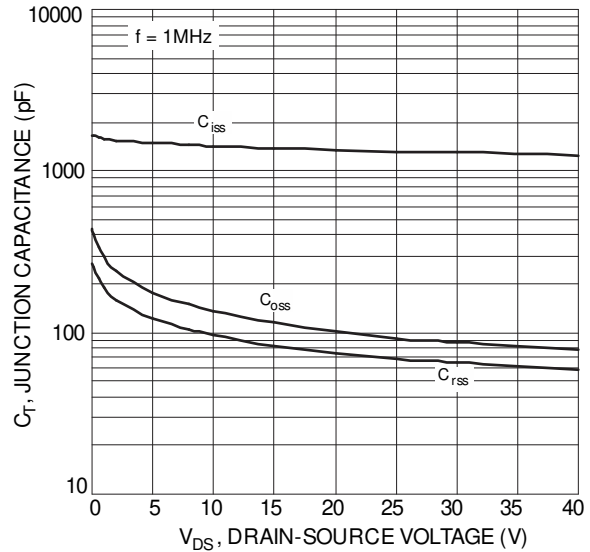


Figure 10 Typical Junction Capacitance

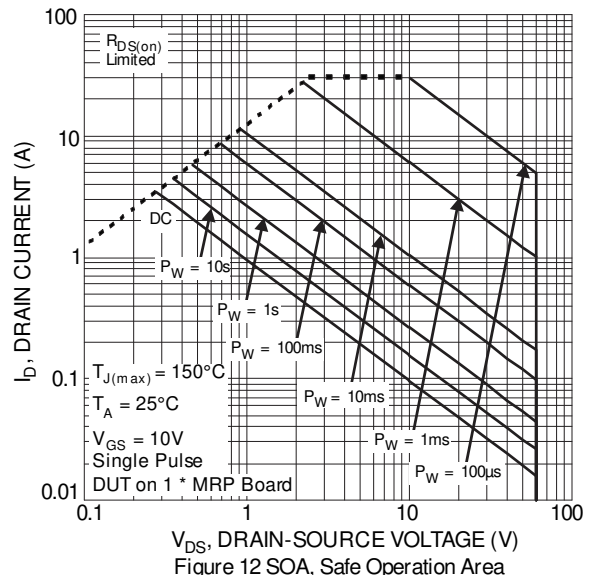
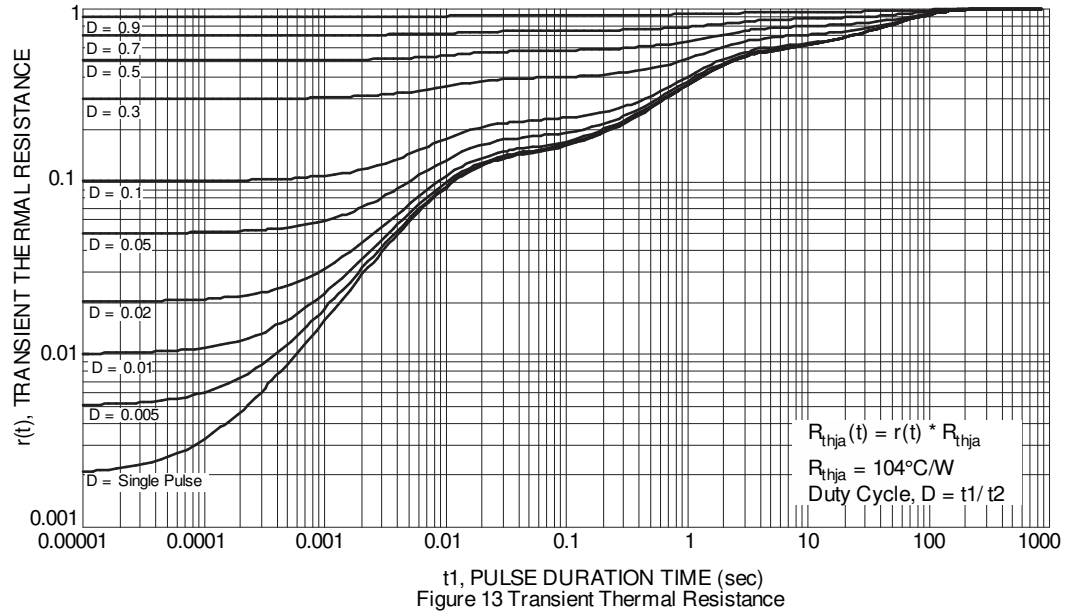
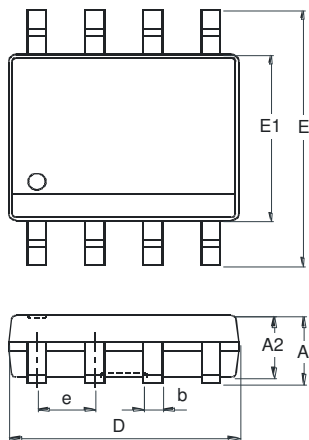


Figure 12 SOA, Safe Operation Area



Package Outline Dimensions

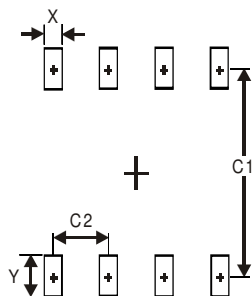
Please see AP02002 at <http://www.diodes.com/datasheets/ap02002.pdf> for the latest version.



SO-8		
Dim	Min	Max
A	-	1.75
A1	0.10	0.20
A2	1.30	1.50
A3	0.15	0.25
b	0.3	0.5
D	4.85	4.95
E	5.90	6.10
E1	3.85	3.95
e	1.27 Typ	
h	-	0.35
L	0.62	0.82
θ	0°	8°
All Dimensions in mm		

Suggested Pad Layout

Please see AP02001 at <http://www.diodes.com/datasheets/ap02001.pdf> for the latest version.



Dimensions	Value (in mm)
X	0.60
Y	1.55
C1	5.4
C2	1.27

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