STL20NM20N

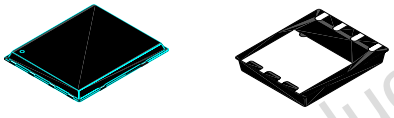
N-CHANNEL 200V - 0.088Ω - 20A PowerFLAT™ ULTRA LOW GATE CHARGE MDmesh™ II MOSFET

Table 1: General Features

TYPE	V_{DSS}	$R_{DS(on)}$	I_D
STL20NM20N	200 V	< 0.105 Ω	20 A

- WORLDWIDE LOWEST GATE CHARGE
- TYPICAL $R_{DS}(on)$ = 0.088Ω
- IMPROVED DIE-TO-FOOTPRINT RATIO
- VERY LOW PROFILE PACKAGE (1mm MAX)
- VERY LOW THERMAL RESISTANCE
- LOW GATE RESISTANCE
- LOW INPUT CAPACITANCE
- HIGH dv/dt and AVALANCHE CAPABILITIES

Figure 1: Package

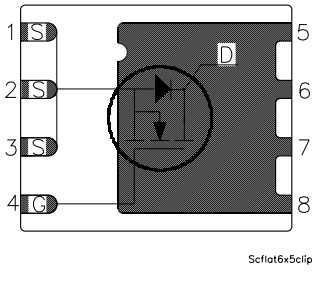


PowerFlat (6x5)
(Chip Scale Package)

DESCRIPTION

This 200V MOSFET with a new advanced layout brings all unique advantages of MDmesh technology to lower voltages. The device exhibits worldwide lowest gate charge for any given on-resistance.Its use is therefore ideal as primary switch in isolated DC-DC converters for Telecom and Computer applications.Used in combination with secondary-side low-voltage STripFET™ products, it contributes to reducing losses and boosting efficiency.The new PowerFLAT™ package allows a significant reduction in board space without compromising performance.

Figure 2: Internal Schematic Diagram



APPLICATIONS

The MDmesh™ family is very suitable for increasing power density allowing system miniaturization and higher efficiencies

Table 2: Order Codes

SALES TYPE	MARKING	PACKAGE	PACKAGING
STL20NM20N	L20NM20N	PowerFLAT™(6x5)	TAPE & REEL

Table 3: Absolute Maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source Voltage (V_{GS} = 0)	200	V
V_{DGR}	Drain-gate Voltage (R_{GS} = 20 kΩ)	200	V
V_{GS}	Gate- source Voltage	± 30	V
I_D (1)	Drain Current (continuous) at T_C = 25°C (Steady State) Drain Current (continuous) at T_C = 100°C	20 12.3	A A
I_{DM} (3)	Drain Current (pulsed)	80	A
P_{TOT} (2)	Total Dissipation at T_C = 25°C (Steady State)	2.5	W
P_{TOT} (1)	Total Dissipation at T_C = 25°C (Steady State)	80	W
	Derating Factor (2)	0.02	W/°C
dv/dt (4)	Peak Diode Recovery voltage slope	10	V/ns

Table 4: Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
Rthj-c	Thermal Resistance Junction-case		1.56	°C/W
Rthj-pcb (2)	Thermal Resistance Junction-pcb	35	50	°C/W
T_j T_{stg}	Max. Operating Junction Temperature Storage Temperature	-55 to 150		°C

Table 5: Avalanche Characteristics

Symbol	Parameter	Max. Value	Unit
I_{AS}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T_j max)	20	A
E_{AS}	Single Pulse Avalanche Energy (starting T_j = 25 °C, I_D = I_{AR}, V_{DD} = 35 V)	380	mJ

ELECTRICAL CHARACTERISTICS (T_{CASE} =25°C UNLESS OTHERWISE SPECIFIED)

Table 6: On/Off

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	I_D = 1 mA, V_{GS} = 0	200			V
I_{DSS}	Zero Gate Voltage Drain Current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating, T_C = 125 °C			1 10	µA µA
I_{GSS}	Gate-body Leakage Current (V_{DS} = 0)	V_{GS} = ± 30 V			±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	3	4	5	V
$R_{Ds(on)}$	Static Drain-source On Resistance	V_{GS} = 10V, I_D = 10 A		0.088	0.105	Ω

ELECTRICAL CHARACTERISTICS (CONTINUED)

Table 7: Dynamic

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g_{fs} (5)	Forward Transconductance	V_{DS} = 15 V, I_D = 10 A		8		S
C_{iss} C_{oss} C_{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0		800 330 130		pF pF pF
$C_{oss\ eq.}$ (*)	Equivalent Output Capacitance	V_{GS} = 0V, V_{DS} = 0V to 160 V		225		pF
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on Delay Time Rise Time Turn-off Delay Time Fall Time	V_{DD} = 100 V, I_D = 10 A R_G = 4.7Ω V_{GS} = 10 V (see Figure 16)		40 15 40 11		ns ns ns ns
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	V_{DD} = 160 V, I_D = 20 A, V_{GS} = 10 V (see Figure 19)		32 6 25	50	nC nC nC

(*) $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 8: Source Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain Current				20	A
I_{SDM} (3)	Source-drain Current (pulsed)				80	A
V_{SD} (5)	Forward On Voltage	I_{SD} = 20 A, V_{GS} = 0			1.3	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	I_{SD} = 20 A, di/dt = 100 A/µs, V_{DD} = 100 V, T_j = 25°C (see Figure 17)		160 960 128		ns nC A
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	I_{SD} = 20 A, di/dt = 100 A/µs, V_{DD} = 100 V, T_j = 150°C (see Figure 17)		225 1642 15		ns nC A

Note: 1. The value is rated according to $R_{thj\text{-}c}$.
2. When Mounted on FR-4 Board of 1inch^2, 2 oz Cu
3. Pulse width limited by safe operating area
4. I_{SD} ≤ 20A, di/dt ≤ 400A/µs, V_{DD} ≤ $V_{(BR)DSS}$
5. Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %

Figure 3: Safe Operating Area

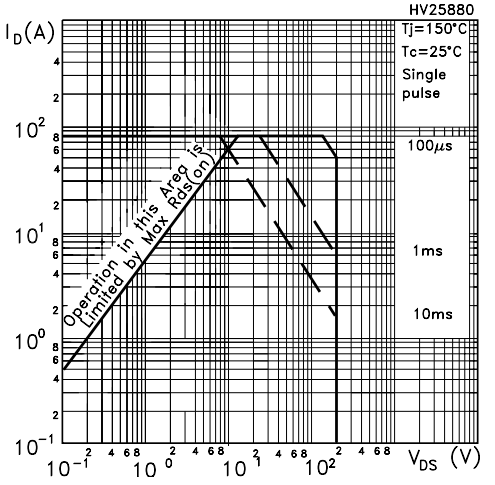


Figure 4: Output Characteristics

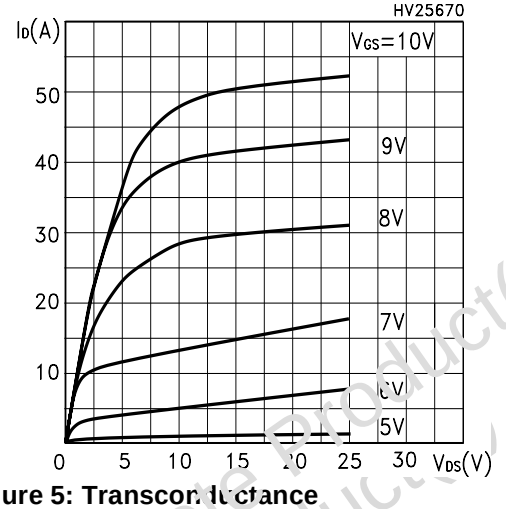


Figure 5: Transconductance

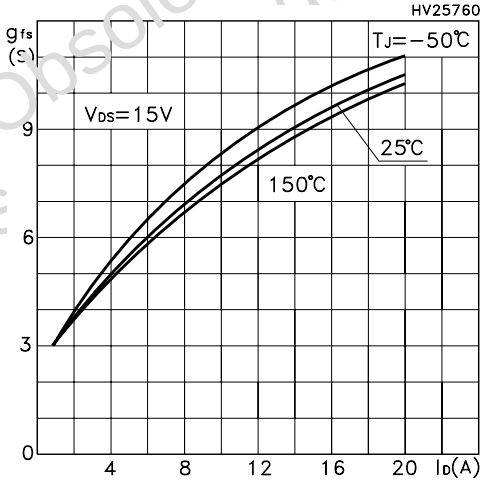


Figure 6: Thermal Impedance

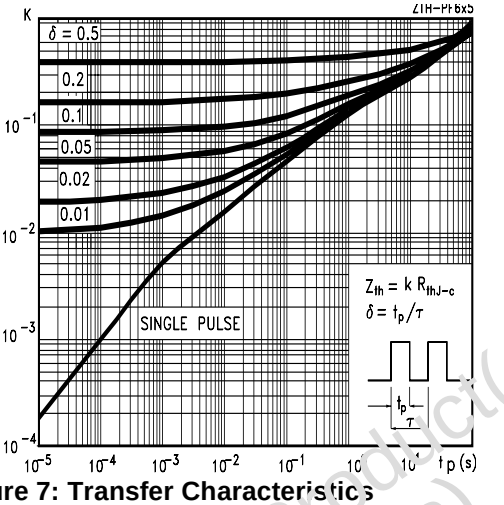


Figure 7: Transfer Characteristics

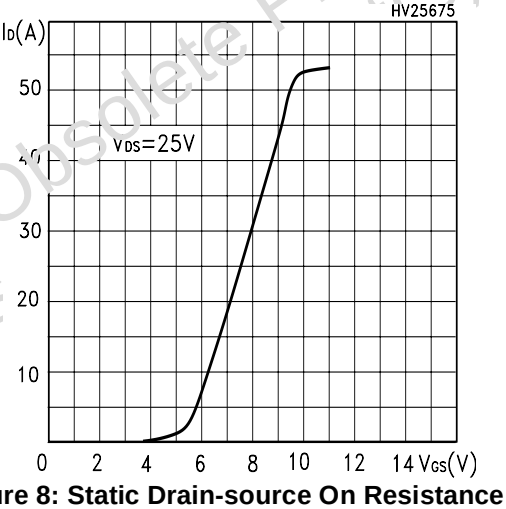


Figure 8: Static Drain-source On Resistance

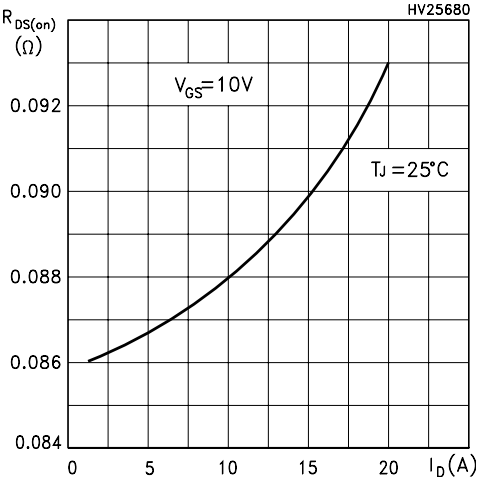


Figure 9: Gate Charge vs Gate-source Voltage

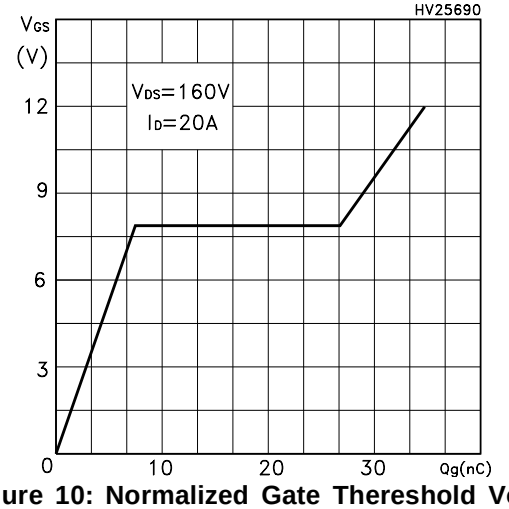


Figure 10: Normalized Gate Thereshold Voltage vs Temperature

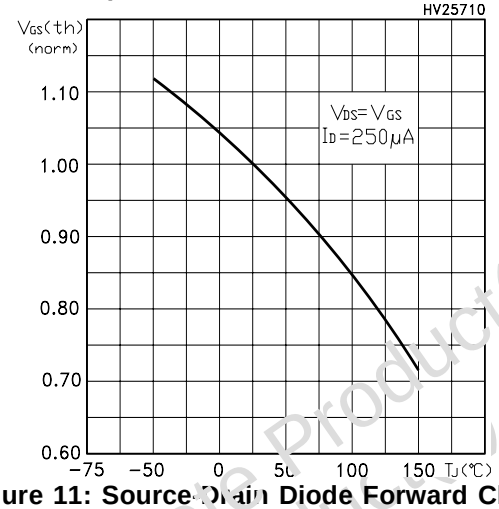


Figure 11: Source-Drain Diode Forward Characteristics

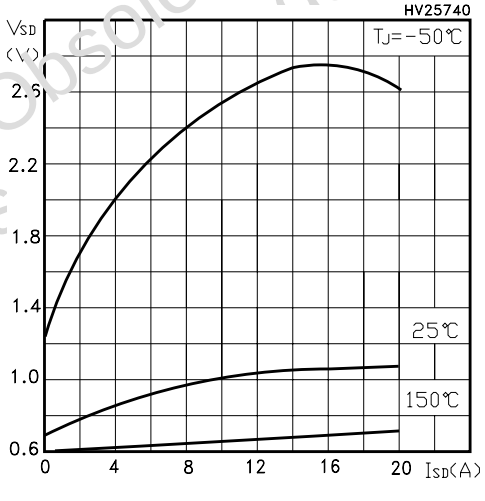


Figure 12: Capacitance Variations

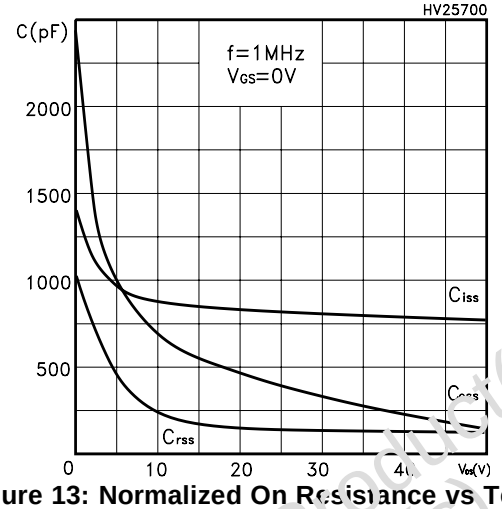


Figure 13: Normalized On Resistance vs Temperature

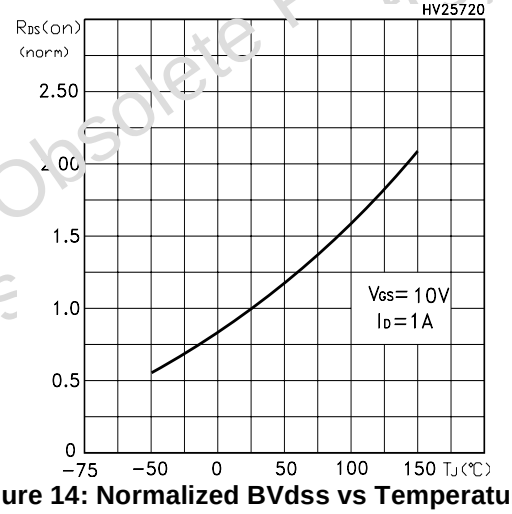


Figure 14: Normalized BVdss vs Temperature

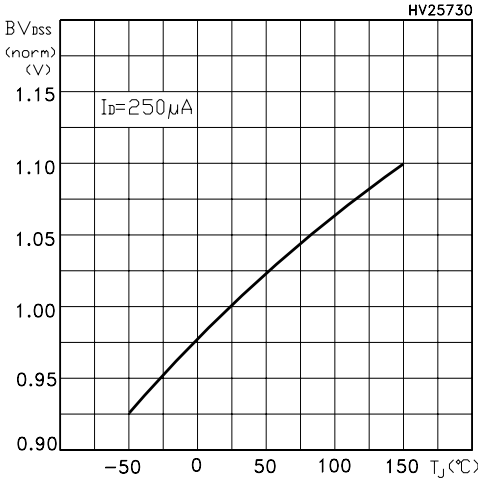


Figure 15: Unclamped Inductive Load Test Circuit

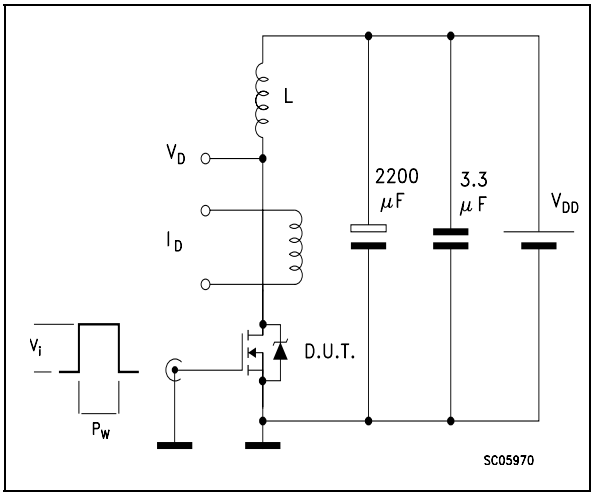


Figure 16: Switching Times Test Circuit For Resistive Load

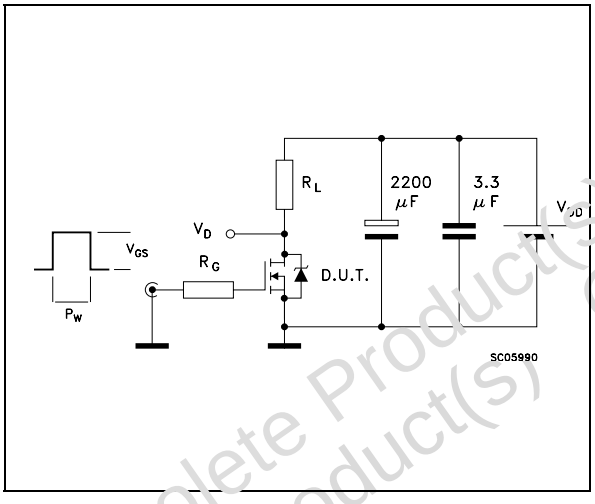


Figure 17: Test Circuit For Inductive Load Switching and Diode Recovery Times

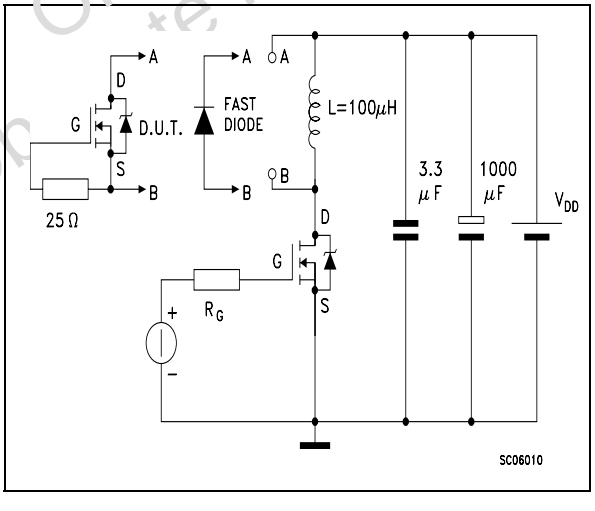


Figure 18: Unclamped Inductive Wafeform

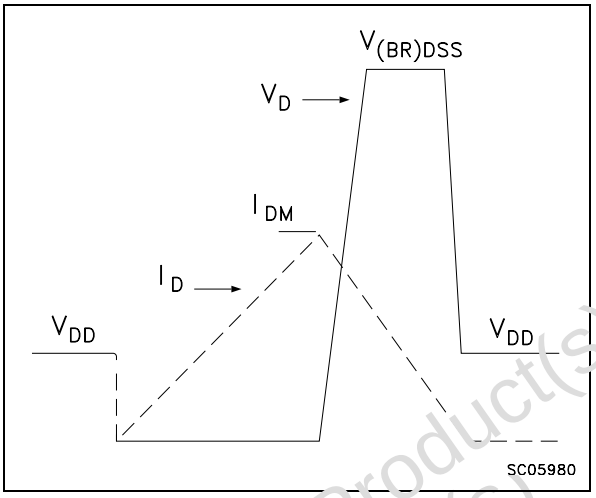
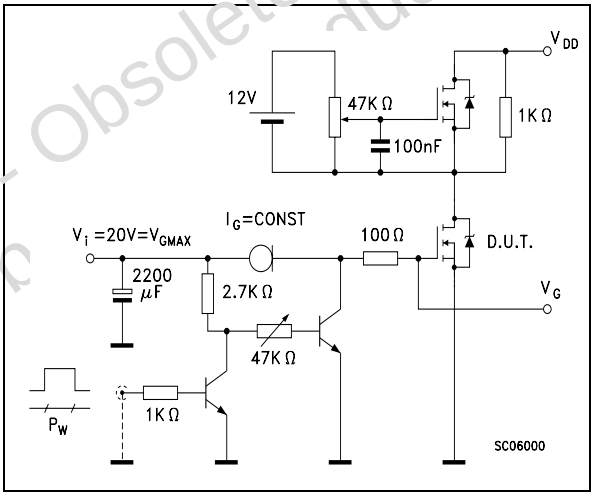


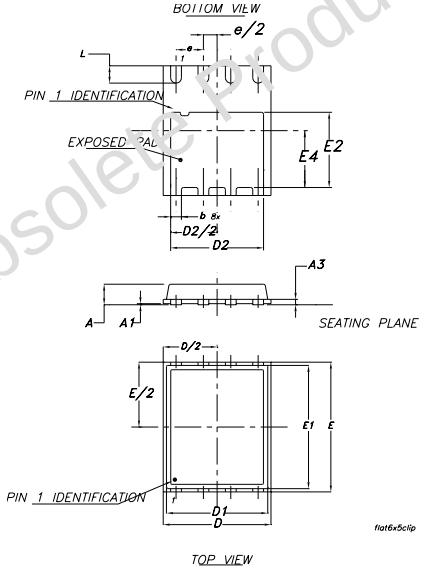
Figure 19: Gate Charge Test Circuit

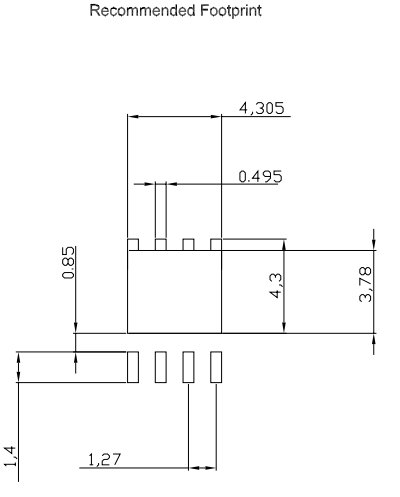


In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

PowerFLAT™ (6x5) MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	0.80	0.83	0.93	0.031	0.032	0.036
A1		0.02	0.05		0.0007	0.0019
A3		0.20			0.007	
b	0.35	0.40	0.47	0.013	0.015	0.018
D		5.00			0.196	
D1		4.75			0.187	
D2	4.15	4.20	4.25	0.163	0.165	0.167
E		6.00			0.236	
E1		5.75			0.226	
E2	3.43	3.48	3.53	0.135	0.137	0.139
E4	2.58	2.63	2.68		0.103	0.105
e		1.27			0.050	
L	0.70	0.80	0.90	0.027	0.031	0.035





Note: all dimentions are in mm.

Table 9: Revision History

Date	Revision	Description of Changes
16-Feb-2005	2	New stylesheet Some Values changed on table 6 and 8
09-Jun-2005	3	Inserted curves
20-Jun-2005	4	Updated mechanical data
04-Nov-2005	5	Modified value on table 8, inserted ecopack indication
09-Jan-2006	6	New footprint