DRV3211-Q1 3-Phase Brushless Motor Driver

Not Recommended for New Designs

1 Features

- 3-Phase Pre-drivers for N-channel MOS Field Effect Transistors (MOSFETs)
- Pulse Width Modulation (PWM) Frequency up to 20 kHz
- Fault Diagnostics
- Charge Pump
- Phase Comparators
- Phase Monitoring Sample and Hold Op-Amps
- Central Processing Unit (CPU) Reset Generator
- Serial Port I/F (SPI)
- Motor Current Sense
- 80-pin HTQFP
- 5-V Regulator

2 Applications

Automotive

3 Description

The DRV3211-Q1 device is a field effect transistor (FET) pre-driver designed for 3-phase motor control and its application such as an oil pump or a water pump. It is equipped with three high-side pre-FET drivers and three low-side drivers which are controlled by an external microcontroller (MCU). The power for the high side is supplied by a charge pump and no bootstrap cap is needed. For commutation, this integrated circuit (IC) sends a conditional motor drive signal and output to the MCU. Diagnostics provide undervoltage, overvoltage, overcurrent, overtemperature and power bridge faults. The motor current can be measured using an integrated current sense amplifier and comparator in a battery common-mode range, which allows the motor current to be used in a high-side current sense application. Gain is attained by external resistors. If the MCU does not have enough bandwidth, the phase monitoring sample and hold amplifiers can hold phase information until the MCU is ready to process it. The pre-driver and other internal settings can be configured through the SPI interface.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DRV3211-Q1	HTQFP (80)	12.00 mm × 12.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (October 2012) to Revision A **Page**

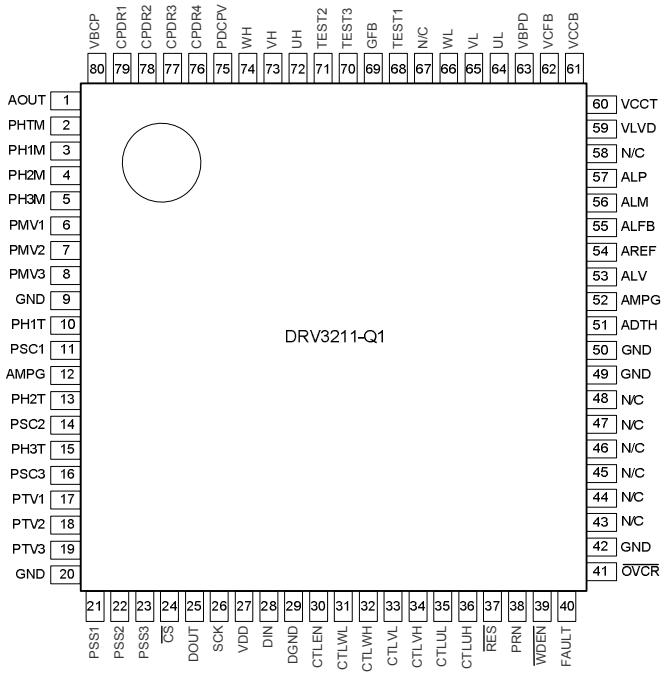
- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section 1
- Changed max rating for PHTM, PH1M, PH2M, and PH3M from -2 –40 V to -1–40 V. 3
- Deleted Table 1 Pin Equivalent Circuits. 5
- Changed V_{chv1_12} to V_{chv1_1}, V_{chv1_20} to V_{chv1_2}, V_{chv2_12} to V_{chv2_1}, V_{chv2_20} to V_{chv2_2}, V_{chv3_12} to V_{chv3_1}, V_{chv3_20} to V_{chv3_2}. 6
- Added min and typ values to V_{chvmax} parameter. 6
- Changed min, typ and max values for V_{chv1_0} through V_{chv3_2}; changed typ R_{on} value from 10 to 8. 6
- Added 3 new parameters to VCC and VDD Electrical Characteristics table. Changed min, typ, and max values VLRVCC, CVCC, TVCC1, TVCC2, VDDOV, TVDD. Added table note. 6
- Removed R_{ONH_H} row, removed cross-references from R_{ONH_HP} and R_{ONH_HN}, added conditions to R_{ONH_HP} and R_{ONH_HN}, changed typ and max values for R_{ONH_HN}. 7
- Removed "side" from V_{OH_L} and V_{OL_L} description, changed high side and low side to pull up and pull down respectively for R_{ONH_L} and R_{ONL_L}. Changed values for R_{ONL_L} from 10 typ to 7 typ and from 20 max to 14 max in pre-driver electrical characteristics table. 7
- Changed Turn-off time from T_{off_h} to T_{off_l} 7
- Changed min value for V_{inm} from -2 to -1. 7
- Changed typ and max values for V_{ofs_SH} and SH Error Voltage. 7
- Added C1 = 4.7 pF to T_{set_TR1}, T_{set_TR2}, T_{set_TF1}, and T_{set_TF2} conditions in motor current sense electrical characteristics 8
- Changed max current limit from 500 to 550. 9
- Added typ and max values to VB monitor electrical characteristics table. 9
- Changed max I_{VB} from 40 to 35 mA. 10
- Changed charge pump description. 17
- Changed pre-driver description and updated block diagram. 18
- Updated phase comparator description. 20
- Changed motor current sense description and motor current sense block diagram. 21
- Updated Sample and Hold Mode Block Diagram. 22
- Changed V_{CC} Block Diagram. 24
- Changed VB Monitor description. 25
- Changed thermal shutdown description. 25
- Changed location of EN in Figure 34. 26

Revision History (continued)

- Changed MCU RESET column to $\overline{\text{RES}}$ column; changed values..... 27

5 Pin Configuration and Functions

PFP Package
80-Pins HTQFP
Top View



Pin Functions

PIN			MAX RATING	FUNCTION
NO.	NAME	TYPE		
1	AOUT	O	–0.3–6 V	Test mode output
2	PHTM	I	–1–40 V	Phase comparator reference input
3	PH1M	I	–1–40 V	Phase comparator input
4	PH2M	I	–1–40 V	Phase comparator input
5	PH3M	I	–1–40 V	Phase comparator input
6	PMV1	O	–0.3–6 V	Phase comparator output
7	PMV2	O	–0.3–6 V	Phase comparator output
8	PMV3	O	–0.3–6 V	Phase comparator output
9, 20, 42, 49, 50	GND	I	–0.3–0.3 V	GND
10	PH1T	I	–2–40 V	Phase amplifier input
11	PSC1	O	–0.3–6 V	Sample and hold filter output
12	AMPG	I	–0.3–0.3 V	Quiet GND
13	PH2T	I	–2–40 V	Phase amplifier input
14	PSC2	O	–0.3–6 V	Sample and hold filter output
15	PH3T	I	–2–40 V	Phase amplifier input
16	PSC3	O	–0.3–6 V	Sample and hold filter output
17	PTV1	O	–0.3–6 V	Phase amplifier output
18	PTV2	O	–0.3–6 V	Phase amplifier output
19	PTV3	O	–0.3–6 V	Phase amplifier output
21	PSS1	I	–0.3–6 V	Sample and hold control signal input
22	PSS2	I	–0.3–6 V	Sample and hold control signal input

Pin Functions (continued)

PIN			MAX RATING	FUNCTION
NO.	NAME	TYPE		
23	PSS3	I	–0.3–6 V	Sample and hold control signal input
24	$\overline{CS}$	I	–0.3–6 V	SPI chip select
25	DOUT	O	–0.3–6 V	SPI data output
26	SCK	I	–0.3–6 V	SPI clock
27	VDD	O	–0.3–3.6 V	Digital supply output
28	DIN	I	–0.3–6 V	SPI data input
29	DGND	I	–0.3–0.3 V	Digital GND
30	CTLEN	I	–0.3–6 V	Pre-driver parallel enable input
31	CTLWL	I	–0.3–6 V	Pre-driver parallel input
32	CTLWH	I	–0.3–6 V	Pre-driver parallel input
33	CTLVL	I	–0.3–6 V	Pre-driver parallel input
34	CTLVH	I	–0.3–6 V	Pre-driver parallel input
35	CTLUL	I	–0.3–6 V	Pre-driver parallel input
36	CTLUH	I	–0.3–6 V	Pre-driver parallel input
37	$\overline{RES}$	O	–0.3–6 V	Reset output
38	PRN	I	–0.3–6 V	Pulse input
39	$\overline{WDEN}$	I	–0.3–6 V	Reset generator enable input
40	FAULT	O	–0.3–6 V	Diagnosis output
41	$\overline{OVCR}$	I	–0.3–6 V	Over current reset input
43-48, 58, 67	N/C	—	—	Not connected
51	ADTH	I	–0.3–6 V	Motor overcurrent threshold input
52	AMPG	I	–0.3–0.3 V	Quiet GND
53	ALV	O	–0.3–6 V	Motor current sense amp output
54	AREF	O	–0.3–40 V	Motor current sense reference output
55	ALFB	O	–0.3–40 V	Motor current sense amp feedback
56	ALM	I	–0.3–40 V	Motor current sense amp negative input
57	ALP	I	–0.3–40 V	Motor current sense amp positive input
59	VLVD	I	–0.3–6 V	V_{CC} undervoltage threshold input
60	VCCT	I	–0.3–6 V	V_{CC} supply input
61	VCCB	O	–0.3–40 V	V_{CC} regulator base drive for PNP external transistor
62	VCFB	I	–0.3–40 V	V_{CC} regulator current sense input
63	VBPD	I	–0.3–40 V	VB input
64	UL	O	-0.3–20 V	Pre-driver output
65	VL	O	-0.3–20 V	Pre-driver output
66	WL	O	-0.3–20 V	Pre-driver output
68	TEST1	I	–0.3–6 V	Test input
69	GFB	I	–0.3–0.3 V	Power GND
70	TEST3	I	-0.3–20 V	Test input
71	TEST2	I	–0.3–6 V	Test input
72	UH	O	–0.3–40 V	Pre-driver output
73	VH	O	–0.3–40 V	Pre-driver output
74	WH	O	–0.3–40 V	Pre-driver output
75	PDCPV	O	–0.3–40 V	Charge pump output
76	CPDR4	O	–0.3–40 V	Charge pump output
77	CPDR3	O	–0.3–40 V	Charge pump output
78	CPDR2	O	–0.3–40 V	Charge pump output

Pin Functions (continued)

PIN			MAX RATING	FUNCTION
NO.	NAME	TYPE		
79	CPDR1	O	–0.3–40 V	Charge pump output
80	VBCP	I	–0.3–4 0V	VB input

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
T_A	Operating temperature range	-40	125	degree
T_J	Junction temperature	-40	150	degree
T_s	Storage temperature	–55	150	degree

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge(1)	Human-body model (HBM)	±2000	V
		Charged-device model (CDM)	±500	

(1) ESD testing is performed according to the ACE-Q100 standard.

6.3 Thermal Information

THERMAL METRIC(1)		DRV3211-Q1 PFP (HTQFP) 80 PINS	UNIT
θ_{JA}	Junction-to-ambient thermal resistance	23.0	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	7.5	°C/W
θ_{JB}	Junction-to-board thermal resistance	7.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	7.4	°C/W
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	0.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.4 Electrical Characteristics

VB = 12 V, T_A = –40°C to 125°C (unless otherwise specified)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
WATCHDOG						
VSTN	Function start V_{CC} voltage $\overline{RES}$	Refer to Figure 1	–	0.8	1.3	V
t_{ON}	Power-on time $\overline{RES}$		32	40	48	ms
t_{OFF}	Clock off reset time $\overline{RES}$		64	80	96	ms
t_{RL}	Reset pulse low time $\overline{RES}$		16	20	24	ms
t_{RH}	Reset pulse high time $\overline{RES}$		64	80	96	ms
t_{RES}	Reset delay time $\overline{RES}$		30	71.5	90	µs
P_{wth}	Pulse width PRN		200	–	–	ns
SPI						
F_{op}	Operating frequency	Refer to Figure 2	DC	–	4	MHz
T_{lead}	Enable lead time		100	–	–	ns
T_{wait}	Wait time between two successive communications		5	–	–	µs
T_{lag}	Enable lag time		100	–	–	ns
T_{pw}	SCLK pulse width		100	–	–	ns
T_{su}	Data setup time		80	–	–	ns
T_h	Data hold time		80	–	–	ns
T_{dis}	Disable time		–	–	80	ns
T_{del}	Data delay time (SCK to DOUT)	C_L = 50 pF, Refer to Figure 2	–	–	80	ns
CHARGE PUMP(1)						
V_{chv1_0}	Output voltage	VB = 5.3 V, I_{load} = 0 mA, C1 = C2 = 47 nF, CCP = 2.2 µF	VB + 7	VB + 8	VB + 9	V
V_{chv1_1}		VB = 5.3 V, I_{load} = 5 mA, C1 = C2 = 47 nF, CCP = 2.2 µF	VB + 6	VB + 7	VB + 8	V
V_{chv1_2}		VB = 5.3 V, I_{load} = 8 mA, C1 = C2 = 47 nF, CCP = 2.2 µF	VB + 5	VB + 6	VB + 7	V
V_{chv2_0}		VB = 12 V, I_{load} = 0 mA, C1 = C2 = 47 nF, CCP = 2.2 µF	VB + 13	VB + 14	VB + 15	V
V_{chv2_1}		VB = 12 V, I_{load} = 11 mA, C1 = C2 = 47 nF, CCP = 2.2 µF	VB + 13	VB + 14	VB + 15	V
V_{chv2_2}		VB = 12 V, I_{load} = 18 mA, C1 = C2 = 47 nF, CCP = 2.2 µF	VB + 12.5	VB + 13.5	VB + 15	V
V_{chv3_0}		VB = 18 V, I_{load} = 0 mA, C1 = C2 = 47 nF, CCP = 2.2 µF	VB + 13	VB + 14	VB + 15	V
V_{chv3_1}		VB = 18 V, I_{load} = 13 mA, C1 = C2 = 47 nF, CCP = 2.2 µF	VB + 13	VB + 14	VB + 15	V
V_{chv3_2}		VB = 18 V, I_{load} = 22 mA, C1 = C2 = 47 nF, CCP = 2.2 µF	VB + 13	VB + 14	VB + 15	V
V_{chvmax}	Maximum voltage		35	37.5	40	V
V_{chvUV}	Undervoltage detection threshold		VB + 4	VB + 4.5	VB + 5	V
T_{chv}(1)	Rise time	VB = 5.3 V, C1 = C2 = 47 nF, CCP = 2.2 µF, V_{chvUV} released		1	2	ms
R_{on}	On resistance S1~S4			8		Ω
HIGH SIDE PRE-DRIVER						
V_{OH_H}	Output voltage high	I_{sink} = 10 mA, U(V/W)H – GFB	V_{chv} – 2.7	V_{chv} – 1.35		V
V_{OL_H}	Output voltage low	I_{source} = 10 mA, U(V/W)H – GFB		60	120	mV
R_{ONH_HP}	ON resistance pull up (Pch)	U(V/W)H = PDCPV - 1 V		135	270	Ω

(1) Specified by design

Electrical Characteristics (continued)

VB = 12 V, T_A = –40°C to 125°C (unless otherwise specified)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{ONH_HN}	ON resistance pull up (Nch)	U(V/W)H = PDCPV - 2.5 V		8	16	Ω
R_{ONL_H}	ON resistance pull down			6	12	Ω
T_{on_h} (1)	Turn-on time	VB = 5.3 ~ 18 V, C_L = 11 nF, R_L = 0 Ω from 20% to 80%	100	300	500	ns
T_{off_h} (1)	Turn-off time	VB = 5.3 ~ 18 V, C_L = 11 nF, R_L = 0 Ω from 80% to 20%	100	300	500	ns
$T_{h\text{-}ondly}$ (1)	Output delay time	VB = 5.3 ~ 18 V, C_L = 11 nF, R_L = 0 Ω to 20%, see Figure 13	100	200	400	ns
$T_{h\text{-}offdly}$ (1)	Output delay time	VB = 5.3 ~ 18 V, C_L = 11 nF, R_L = 0 Ω to 80%, see Figure 13	100	200	400	ns
LOW SIDE PRE-DRIVER						
V_{OH_L}	Output voltage high	I_{sink} = 10 mA, U(V/W)L – GFB	VB – 0.14	VB-0.07		V
V_{OL_L}	Output voltage low	I_{source} = 10 mA, U(V/W)L – GFB		70	140	mV
R_{ONH_L}	ON resistance pull up			7	14	Ω
R_{ONL_L}	ON resistance pull down			7	14	Ω
T_{on_l} (1)	Turn-on time	VB = 5.3 ~ 18 V, C_L = 22 nF, R_L = 0 Ω from 20% to 80%	100	300	800	ns
T_{off_l} (1)	Turn-off time	VB = 5.3 ~ 18 V, C_L = 22 nF, R_L = 0 Ω from 80% to 20%	100	300	800	ns
$T_{l\text{-}ondly}$ (1)	Output delay time	VB = 5.3 ~ 18 V, C_L = 22 nF, R_L = 0 Ω to 20%, see Figure 13	100	200	400	ns
$T_{l\text{-}offdly}$ (1)	Output delay time	VB = 5.3 ~ 18 V, C_L = 22 nF, R_L = 0 Ω to 80%, see Figure 13	100	200	400	ns
V_{CLAMP}	VGS protection voltage		16	18	20	V
T_{diff1} (1)	Differential time 1	VB = 5.3 ~ 18 V ($T_{h\text{-}on}$)–($T_{l\text{-}off}$), see Figure 13	–300		300	ns
T_{diff2} (1)	Differential time 2	VB = 5.3 ~ 18 V ($T_{l\text{-}on}$)–($T_{h\text{-}off}$), see Figure 13	–300		300	ns
PHASE COMPARATOR						
V_{iofs}	Input offset voltage		–15	–	15	mV
V_{inp}	Input voltage range (PHTM)	VB = 5.3 ~18 V	1.325	–	4.5	V
V_{inm}	Input voltage range (PHxM)		–1	–	VB	V
V_{ihys}	Input hysteresis voltage		100	200	400	mV
V_{OH}	Output high voltage	I_{sink} = 2.5 mA	0.9 × V_{CC}	–	–	V
V_{OL}	Output low voltage	I_{source} = 2.5 mA	–	–	0.1 × V_{CC}	V
T_{res_tr} (1)	Response time (rising)	C_L = 100 pF	–	0.2	0.5	µs
T_{res_tf} (1)	Response time (falling)	C_L = 100 pF	–	0.4	1	µs
MOTOR CURRENT SENSE (2) (3)						
V_{Ofs}	Input offset voltage		–5		5	mV
V_{O_0}	Output voltage (ALV)	VB = 5.3 ~ 18 V, I_{motor} = 0 A		1		V
V_{Line}	Linearity (ALV)	VB = 5.3 ~ 18 V, R_{shunt} = 1 mΩ, R11 = R12 = 1 kΩ, R21 = R22 = 30 kΩ	–2%	30	2%	mV/A

(2) Motor current is converted to voltage in test
(3) No variation of the external components

Electrical Characteristics (continued)

VB = 12 V, T_A = –40°C to 125°C (unless otherwise specified)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{Gain}	Gain		10		30	
T_{set_TR1}	Settling time (Rise) ALV ±1%	VB = 5.3 ~ 18 V, R_{shunt} = 1 mΩ, C1 = 4.7 pF, C_L = 100 pF, R11 = R12 = 1 kΩ, R21 = R22 = 30 kΩ, I_{motor} = 0 → 30 A, (ALV : 1→1.9 V)	–	1	2.5	µs
T_{set_TR2}	Settling time (Rise) ALV ±1%	VB = 5.3 ~ 18 V, R_{shunt} = 1 mΩ, C1 = 4.7 pF, C_L = 100 pF, R11 = R12 = 1 kΩ, R21 = R22 = 30 kΩ, I_{motor} = 0 → 100 A, (ALV : 1 → 4 V)	–	1	2.5	µs
T_{set_TF1}	Settling time (Fall) ALV ±1%	VB = 5.3 ~ 18 V, R_{shunt} = 1 mΩ, C1 = 4.7 pF, C_L = 100 pF, R11 = R12 = 1 kΩ, R21 = R22 = 30 kΩ, I_{motor} = 30 → 0 A, (ALV : 1.9 → 1 V)	–	1	2.5	µs
T_{set_TF2}	Settling time (Fall) ALV ±1%	VB = 5.3 ~ 18 V, R_{shunt} = 1 mΩ, C1 = 4.7 pF, C_L = 100 pF, R11 = R12 = 1 kΩ, R21 = R22 = 30 kΩ, I_{motor} = 100 → 0 A, (ALV : 4 → 1 V)	–	1	2.5	µs
OVAD	Overcurrent threshold	150-A detection, R_{shunt} = 1 mΩ, R11 = R12 = 1 kΩ, R21 = R22 = 30 kΩ, R3 = 8.2 kΩ, R4 = 10 kΩ	–10%	150	10%	A
TDEL_OVAD[1]	Propagation delay (Rise or fall)		–	–	1.5	µs
PHASE AMPLIFIER						
V_{ofs_SH}	Output offset voltage, sample and hold mode	VB = 5.3–18 V, Gain = 1	–50	–	50	mV
V_{ofs_TH}	Output offset voltage, through mode	VB = 5.3–18 V, Gain = 1	–50	–	50	mV
V_{in_cm}	Common mode input range	VB = 5.3–18 V, Gain = 1–4	1.5		VB – 1.5	V
V_{out_max}	Maximum output voltage	VB = 5.3–18 V, Gain = 1–4	4.5	–	–	V
V_{out_min}	Minimum output voltage	VB = 5.3–18 V, Gain = 1–4	–	–	0.5	V
V_{gain}[4]	Gain		–	1 2 3 4	–	
V_{out_SH0}	Output voltage, sample and hold mode	VB = 5.3–18 V, Gain = 1–4, PHxT = VB / 2	–	2.5	–	V
V_{out_TH0}	Output voltage, through mode	VB = 5.3–18 V, Gain = 1–4 PHxT = VB / 2	–	2.5	–	V
V_{out_SH1}	Output voltage, sample and hold mode	VB = 12 V, Gain = 1, PHxT = 1.5 V	–	1.375	–	V
V_{out_TH1}	Output voltage, through mode	VB = 12 V, Gain = 1, PHxT = 1.5 V	–	1.375	–	V
V_{out_SH2}	Output voltage, sample and hold mode	VB = 12 V, Gain = 1, PHxT = 10.5 V	–	3.625	–	V
V_{out_TH2}	Output voltage, through mode	VB = 12 V, Gain = 1, PHxT = 10.5 V	–	3.625	–	V

(4) V_{gain} is an SPI setting

Electrical Characteristics (continued)

VB = 12 V, T_A = –40°C to 125°C (unless otherwise specified)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STL_SHTR	Settling time (rise), sample and hold mode PTVx ±1%	VB = 12 V, Gain = 1, PSC = 470 pF, PTVx = 100 pF, PHxT = 1.5 V ≥ 10.5 V, (PTVx = 1.375 V → 3.625 V), see Figure 7		1.5	3	µs
STL_THTR	Settling time (rise), through mode PTVx ±1%	VB = 12 V, Gain = 1, PTVx = 100 pF, PHxT = 1.5 V ≥ 10.5 V, (PTVx = 1.375 V → 3.625 V), see Figure 8		1.5	3	µs
STL_SHTF	Settling time (fall), sample and hold mode PTVx ±1%	VB = 12 V, Gain = 1, PSC = 470 pF, PTVx = 100 pF, PHxT = 10.5 V ≥ 1.5 V, (PTVx = 3.625 V → 1.375 V), see Figure 7		1.5	3	µs
STL_THTF	Settling time (fall), through mode PTVx ±1%	VB = 12 V, Gain = 1, PTVx = 100 pF, PHxT = 10.5 V ≥ 1.5V, (PTVx = 3.625 V → 1.375 V), see Figure 8		1.5	3	µs
SH Error Voltage	Falling voltage	VB = 5.3–18 V, PSC = 470 pF, TH = 1 mS, see Figure 6		5	75	mV
V_{CC}						
V_{CC}	Output voltage	VB = 5.3–18 V, I_{load} = 5–150 mA	4.9	5	5.1	V
IBVCC	Base current		1.5			mA
hfePNP	DC current gain of external VCC		100			
VLRVCC	Load regulation	VB = 5.3–18 V, I_{load} = 5–150 mA	–50	–	50	mV
CVCC	Load capacitance		22		100	µF
RVCC	ESR of external capacitance				300	mΩ
VCCUV	Undervoltage detection threshold	R1 = 7.5 kΩ, R2 = 10 kΩ, VCCUV > 4 V	3.97	4.07	4.17	V
VCCUVHYS	Undervoltage detection threshold hysteresis			100		mV
VCCOV	Overvoltage detection threshold		6	6.5	7	V
ICLVCC	Current limit	R_{sns} = 0.51 Ω	300	400	550	mA
TVCC1	Rise time	V_{CC} > UVVCC, CVCC = 22 µF		0.3	0.5	ms
TVCC2	Rise time	V_{CC} > UVVCC, CVCC = 100 µF		1	1.5	ms
V_{DD}						
V_{DD}	Output voltage	VB = 5.3–18 V, I_{load} = 0–2 mA	3	3.3	3.6	V
CVDD	Load capacitance			1		µF
VDDUV	Undervoltage detection threshold		2.2	2.3	2.4	V
VDDOV	Overvoltage detection threshold		4.1	4.3	4.5	V
T_{vdd} (1)	Rise time	V_{DD} > VDDUV, CVDD = 1 µF		75	150	µs
VB MONITOR						
V_{stop}	Pre-driver stop VB voltage		26.5	27.5	28.5	V
THERMAL SHUT DOWN						
TSD (1)	Thermal shut down threshold		155	175	195	°C
OSCILLATOR						
OSC	OSC frequency		9	10	11	MHz
INPUT BUFFER 1						
V_{IH}	Input threshold logic high		0.7 × V_{CC}			V

Electrical Characteristics (continued)

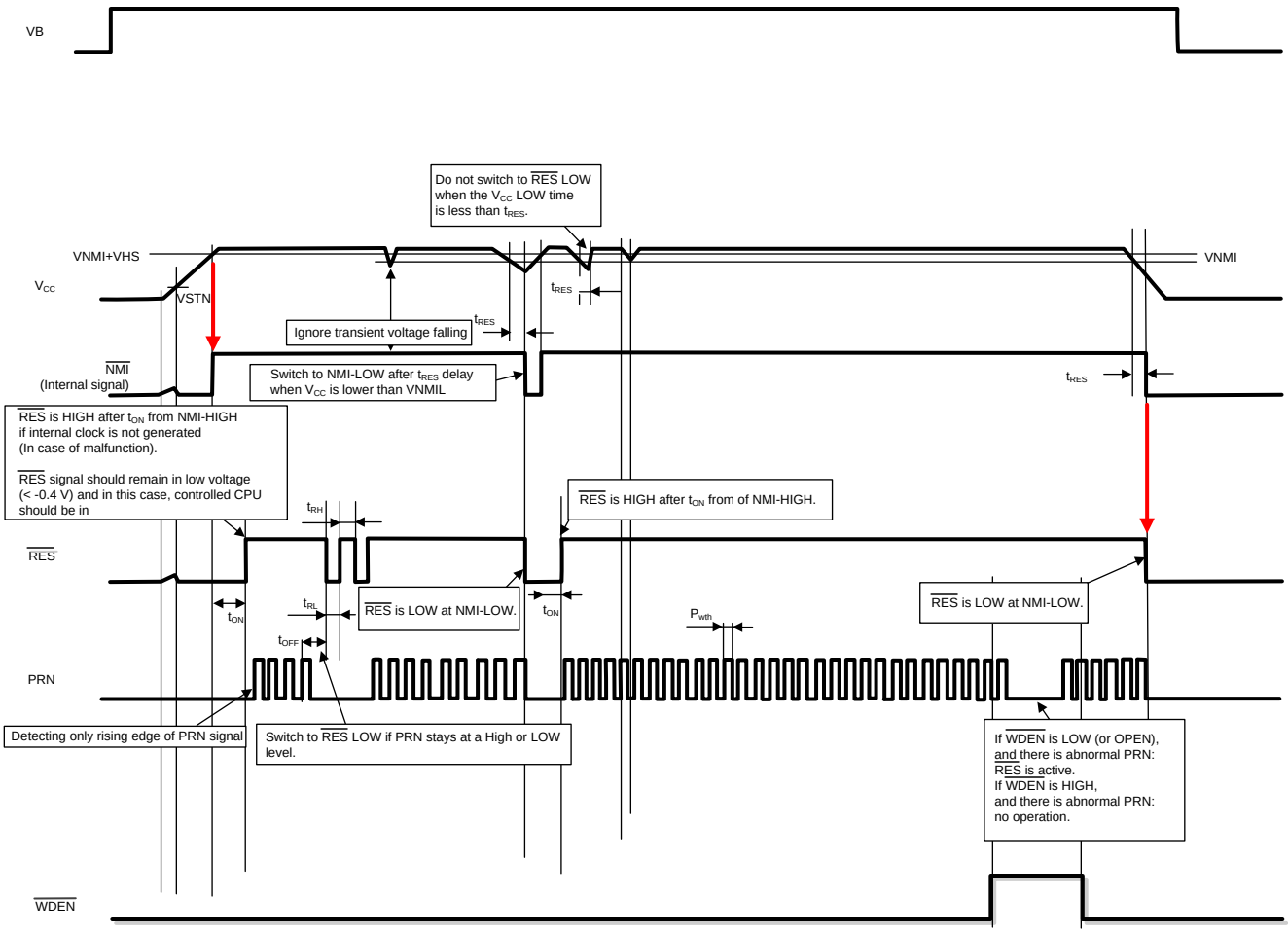
VB = 12 V, T_A = –40°C to 125°C (unless otherwise specified)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IL}	Input threshold logic low				0.3 × V_{CC}	V
R_u	Input pullup resistance		50	100	150	kΩ
R_d	Input pulldown resistance		50	100	150	kΩ
OUTPUT BUFFER 1 AND 2						
V_{OH}	Output level logic high	I_{sink} = 2.5 mA	0.9 × V_{CC}			V
V_{OL}	Output level logic low	I_{source} = 2.5 mA			0.1 × V_{CC}	V
OUTPUT BUFFER 3						
R_RES	Pullup resistor		1.5	3	4.5	kΩ
V_{OL}	Output level logic low	I_{source} = 2 mA			0.1 × V_{CC}	V

6.5 Supply Voltage and Current

VB = 12 V, T_A = –40°C to 125°C (unless otherwise specified)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY INPUT						
VB	VB Supply voltage		5.3	12	18	V
I_{VB}	VB Operating current	VB = 5.3 ~18 V, No PWM		20	35	mA



NOTE: $\overline{WDEN}$ = High, V_{CC} undervoltage condition sets $\overline{RES}$ = Low

Figure 1. Watchdog Timing Chart

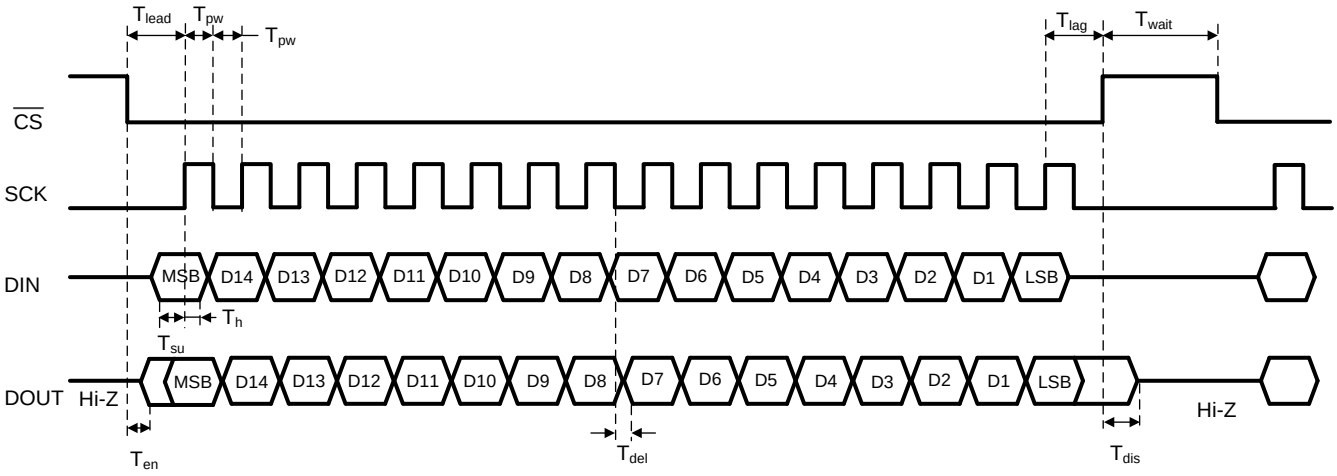


Figure 2. SPI AC Timing Definition

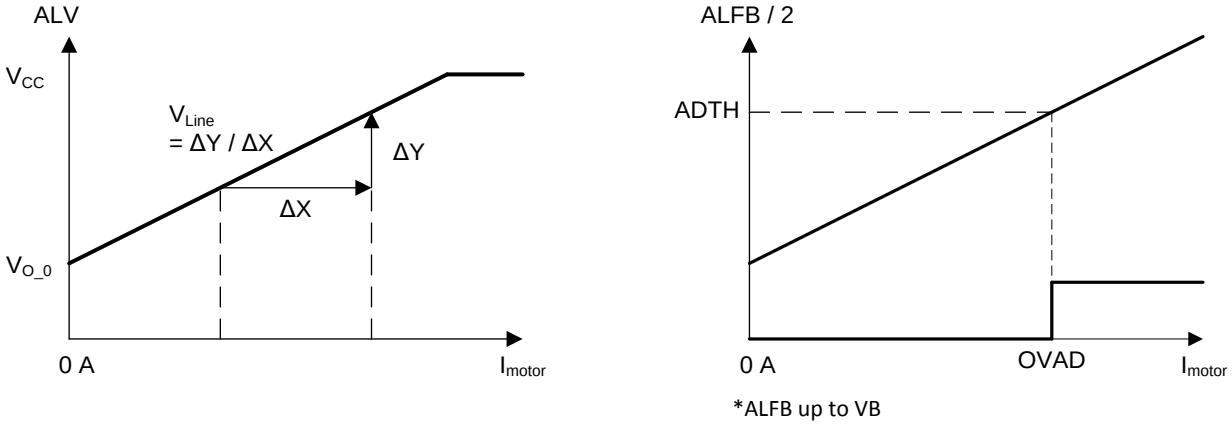


Figure 3. Motor Current Sense and Overcurrent

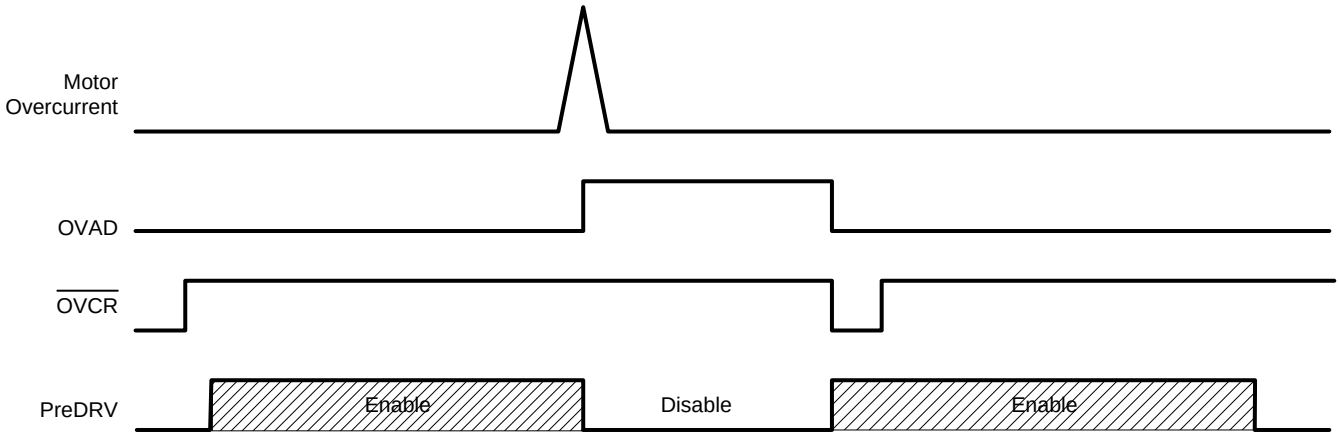


Figure 4. Motor Overcurrent Event

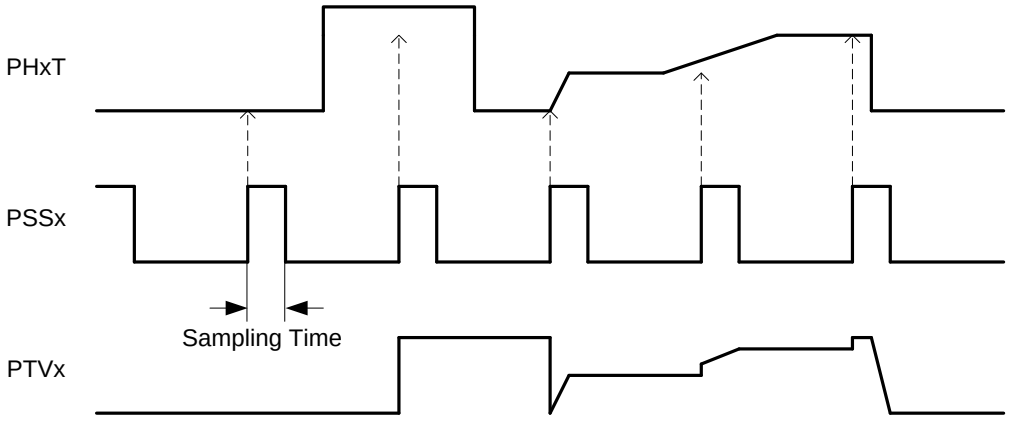


Figure 5. Sampling Timing Chart

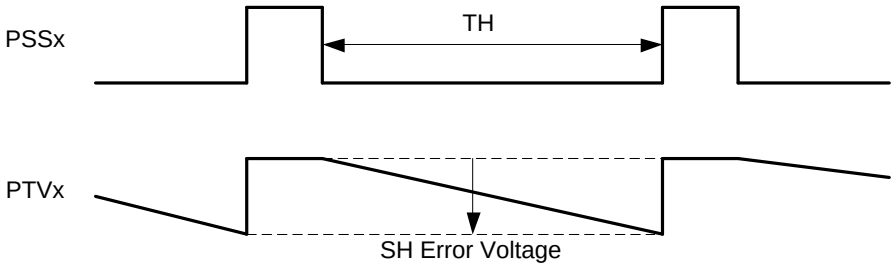


Figure 6. Holding Timing Chart

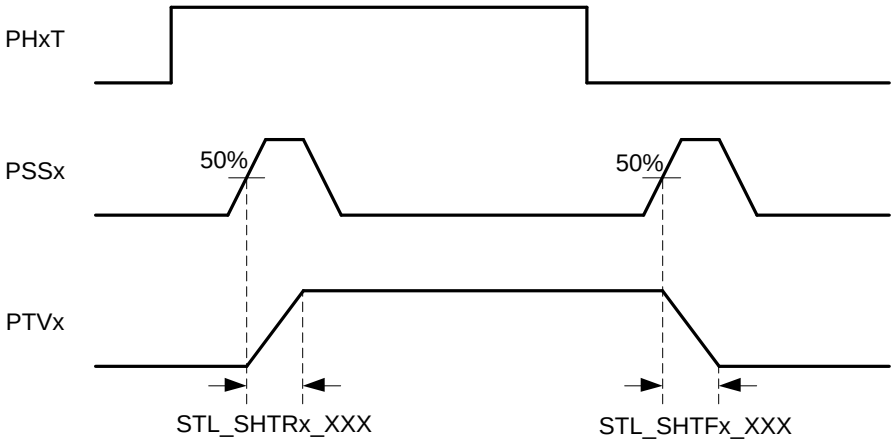


Figure 7. Settling Time Timing Chart (Sample and Hold Mode)

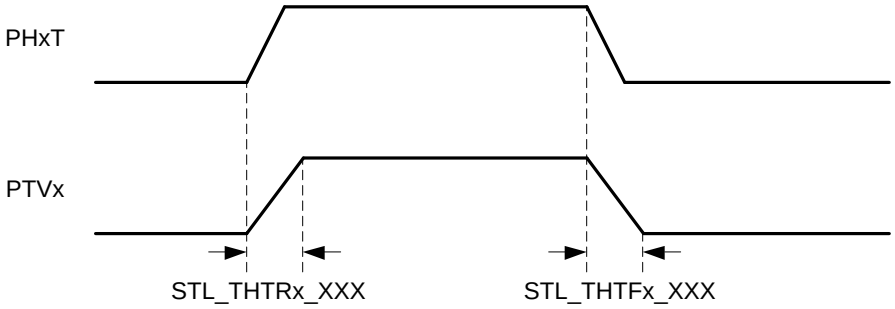
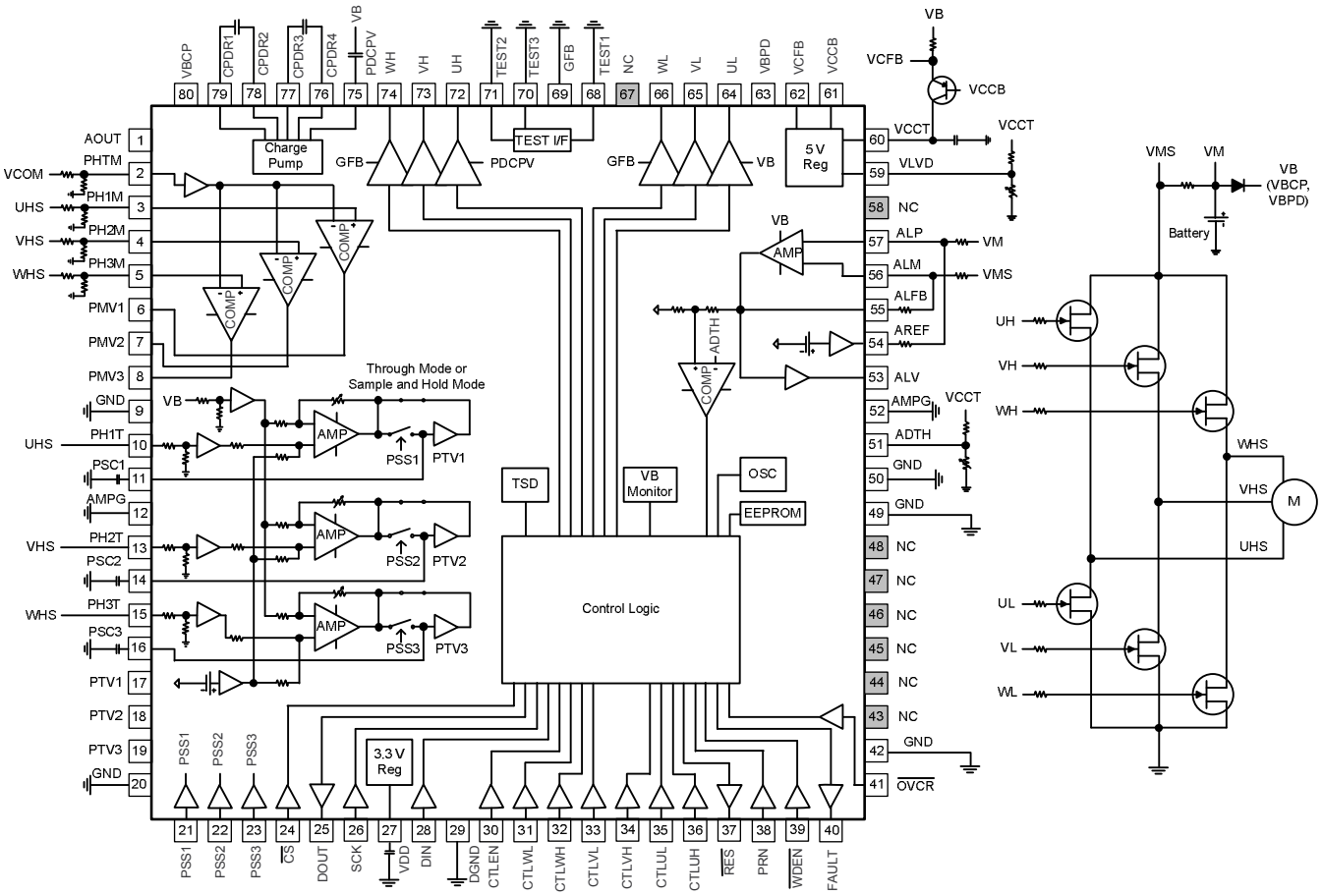


Figure 8. Settling Time Timing Chart (Through Mode)

7 Detailed Description

7.1 Functional Block Diagram



7.2 Feature Description

7.2.1 Watchdog

The watchdog monitors the PRN signal and V_{CC} supply level and generates a reset to the MCU through the $\overline{RES}$ pin if the status of the PRN is not normal or the V_{CC} is lower than the specified threshold level. The watchdog can be disabled if $\overline{WDEN}$ is set high.

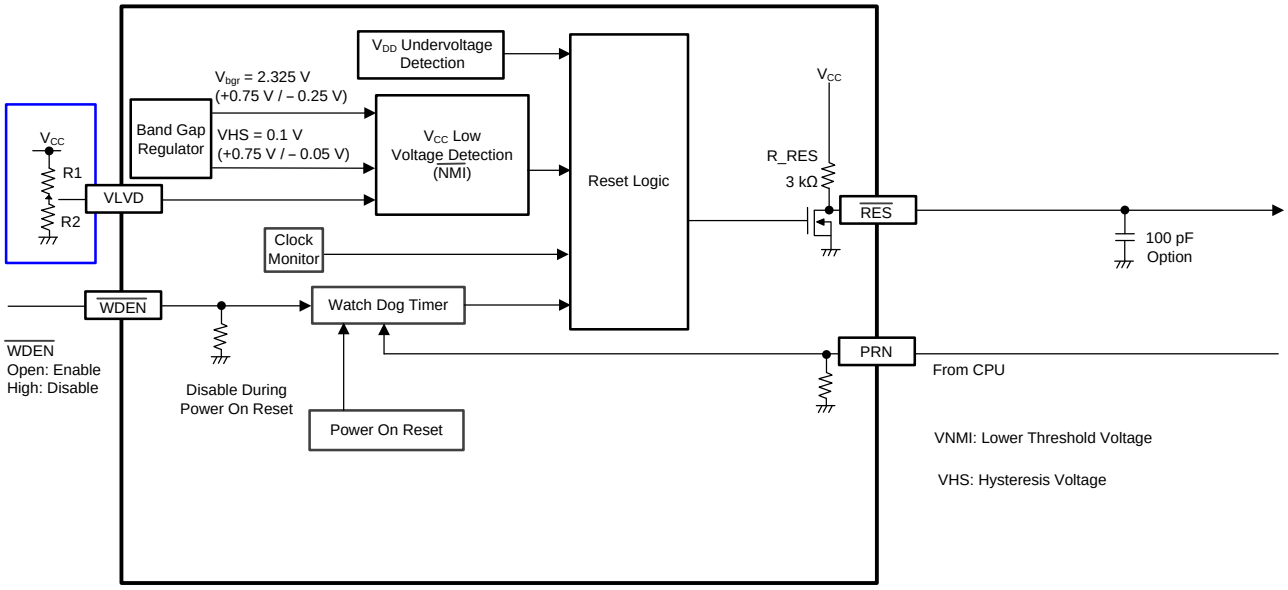


Figure 9. Watchdog Block Diagram

Feature Description (continued)

7.2.2 Serial Port I/F

The SPI is used to receive an input byte from CPU and to transmit an output byte to CPU. Four signals are utilized according to the timing chart of Figure 10.

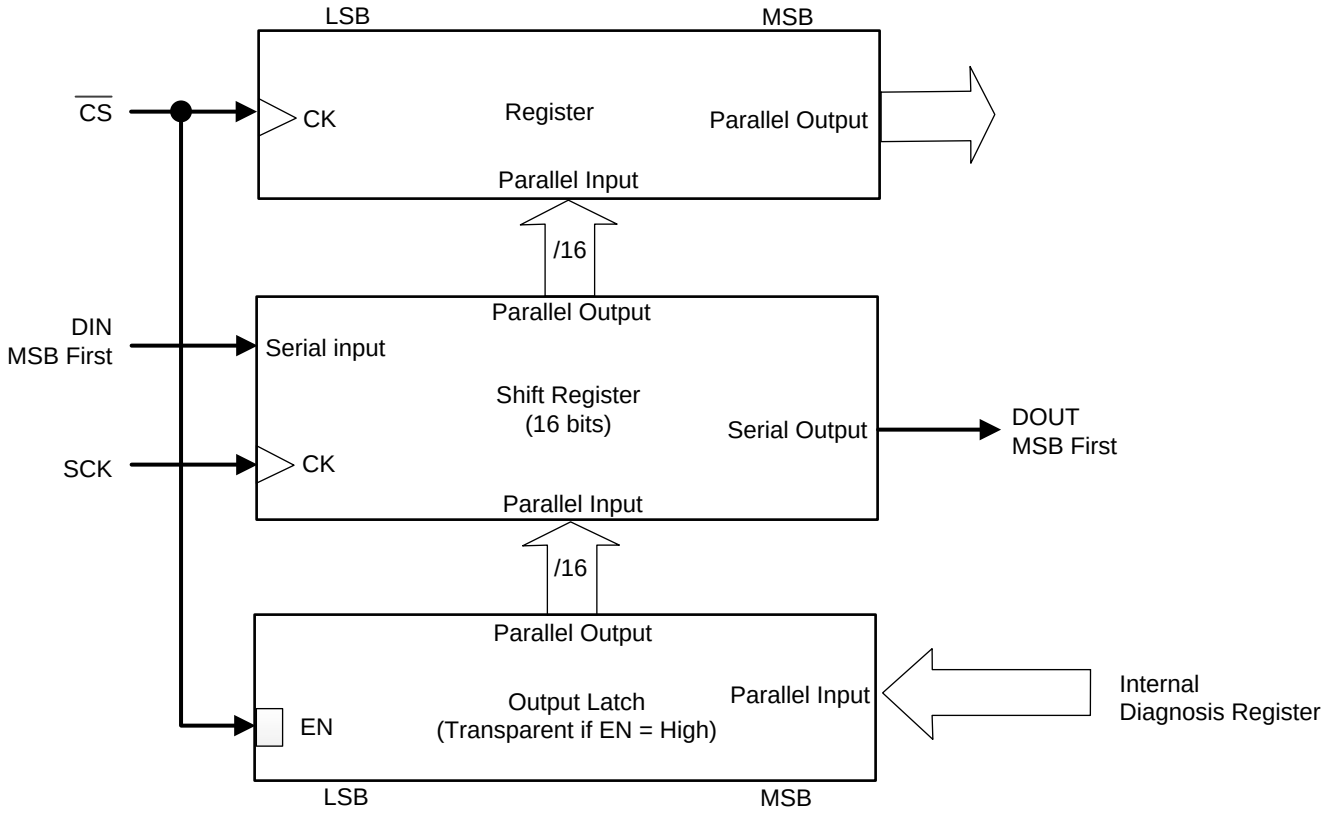


Figure 10. Block Diagram of SPI

- **$\overline{CS}$ – Chip Select**
  - This input signal is utilized to select this IC by CPU.
  - This input signal is normally high and the communication is possible only when it is forced low.
  - When this input signal falls, the communication between this IC and the CPU starts.
  - Transmitted data is latched and the DOUT pin comes out of high impedance.
  - When this input signal rises, the communication stops.
  - The DOUT pin goes into high impedance. Then, the internal input register updates with the received bits (only if the clock pulse numbers are right and the key bit of the DIN signals is correct).
  - The next falling edge starts another communication.
  - There is a minimum waiting time between two communications (T_{wait}).
  - The pin has an internal pullup.
- **SCK – Synchronization Serial Clock**
  - This input signal is utilized to synchronize the communication by CPU.
  - It is normally high and the correct clock pulse number is 16.
  - At each falling edge, the CPU writes a new bit on the DIN input and this IC writes a new bit on the DOUT pin. At each rising edge, this IC reads the new bit on the DIN pin and the CPU reads the new bit on the DOUT pin.
  - The maximum clock frequency is 4 MHz.
  - The pin has an internal pullup.

Feature Description (continued)

- **DIN – Serial Input Data**
  - This input signal is used to receive 16-bit data.
  - The bits are received in order from the MSB (first) to the LSB (last).
  - The pin has an internal pullup.
- **DOUT – Serial Output Data**
  - This output signal is used to transmit 16-bit data.
  - It is a 3-state output and it is in high impedance mode when $\overline{CS}$ is high.
  - The serial data bits are transmitted in order from the MSB (first) to the LSB (last).

7.2.3 Charge Pump

The charge pump block generates the supply for high-side and low-side pre-drivers to maintain the gate voltage on the external FETs. External storage cap (CCP) and bucket caps (C1, C2) are used to support pre-driver slope and switching frequency requirements. R1 and R2 can reduce switching current if required. The charge pump has a voltage supervisor for over and undervoltage, and a selectable stop condition for pre-drivers.

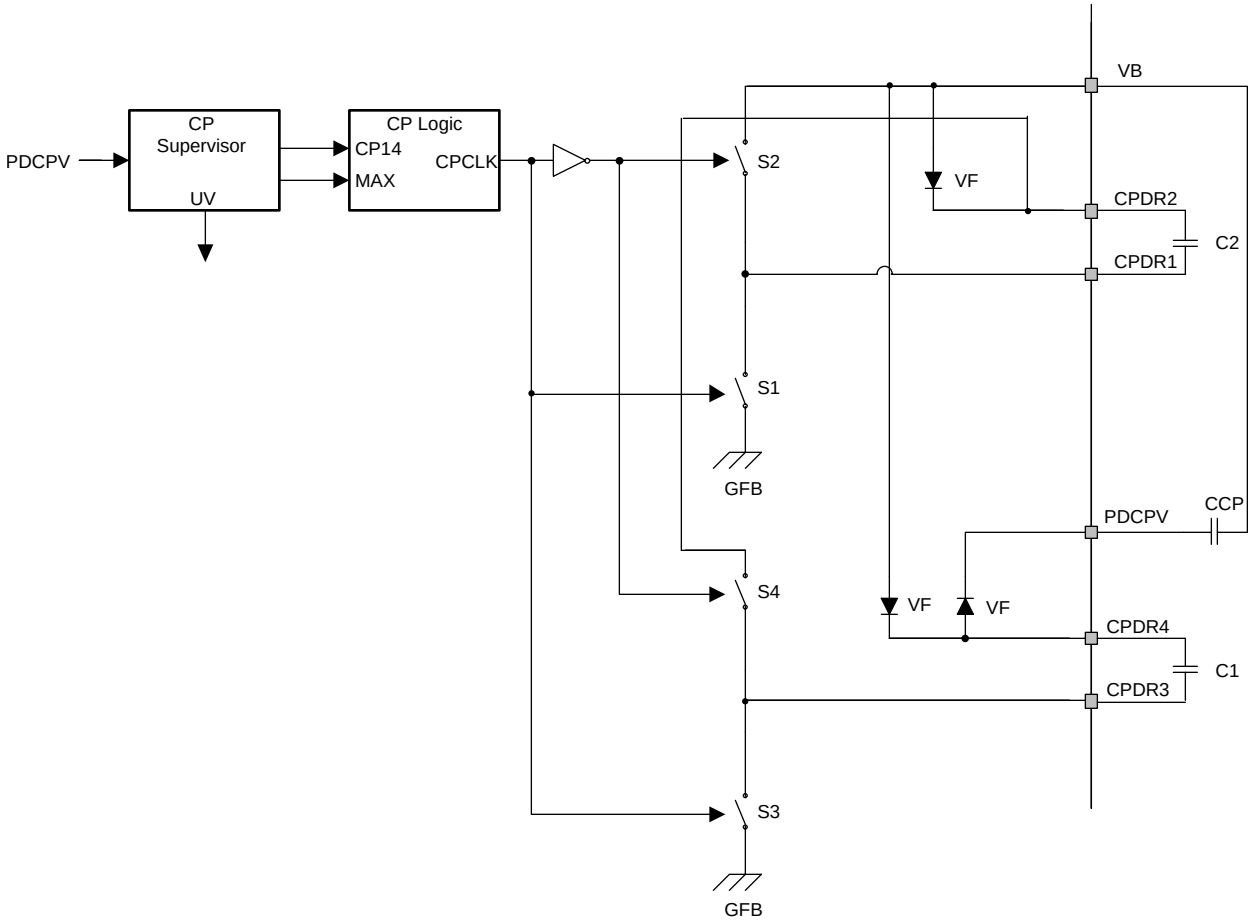


Figure 11. Charge Pump Block Diagram

Feature Description (continued)

7.2.4 Pre-Driver

The pre-driver block provides three high-side pre-drivers and three low-side pre-drivers to drive external N-channel MOSFETs. The turn on side of the high-side pre-drivers supply the large N-channel transistor current to quickly charge and PMOS support output voltage up to PDCPV. The turn off side supplies the large N-channel transistor current to quickly discharge, while the low-side pre-drivers supply the large N-channel transistor current for charge and discharge. The output voltage of the low-side pre-driver is controlled by VB and it has VGS protection to make less than 18 V. The pre-driver has a stop condition in some fault conditions ($16 Error Detection).

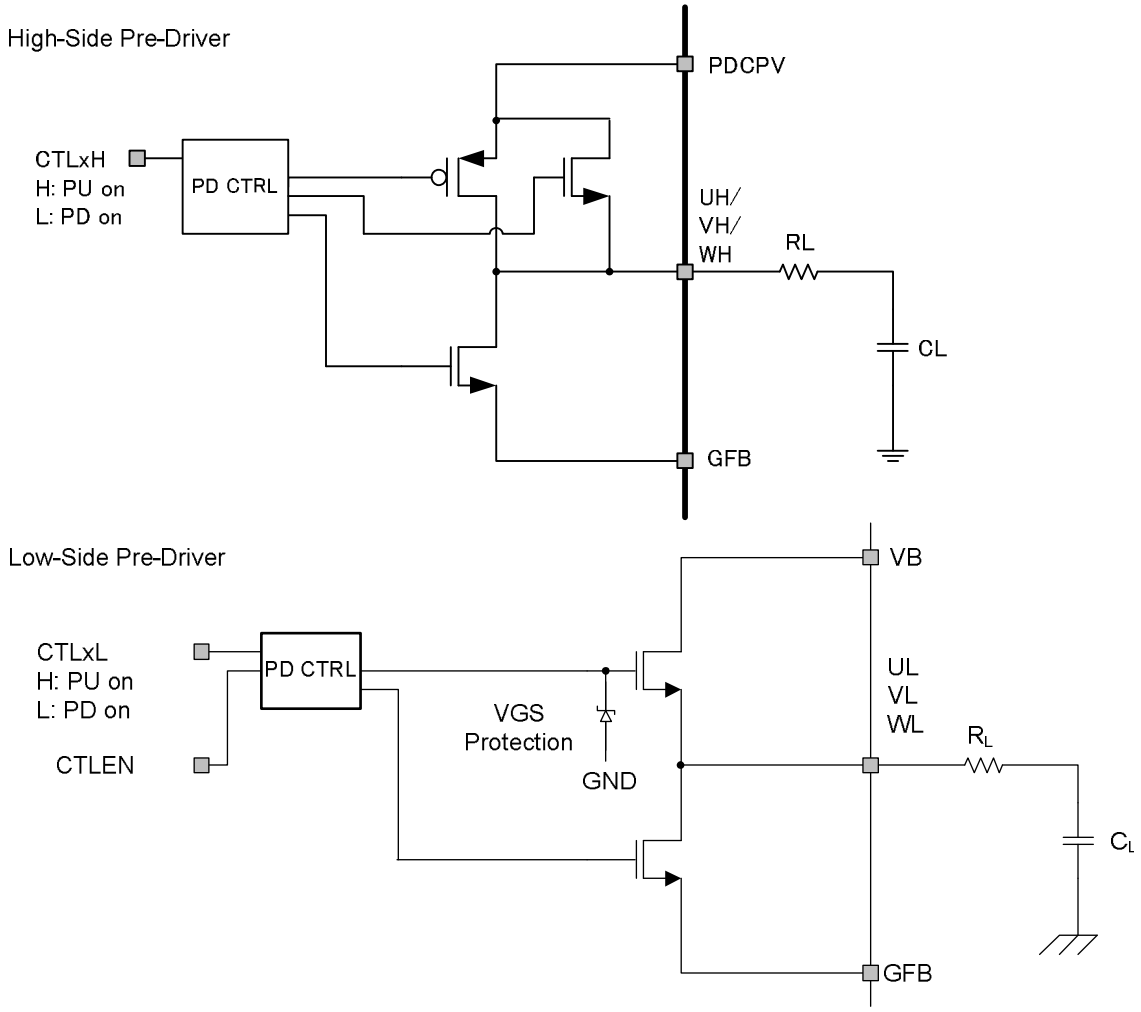


Figure 12. Pre-Driver Block Diagram

Feature Description (continued)

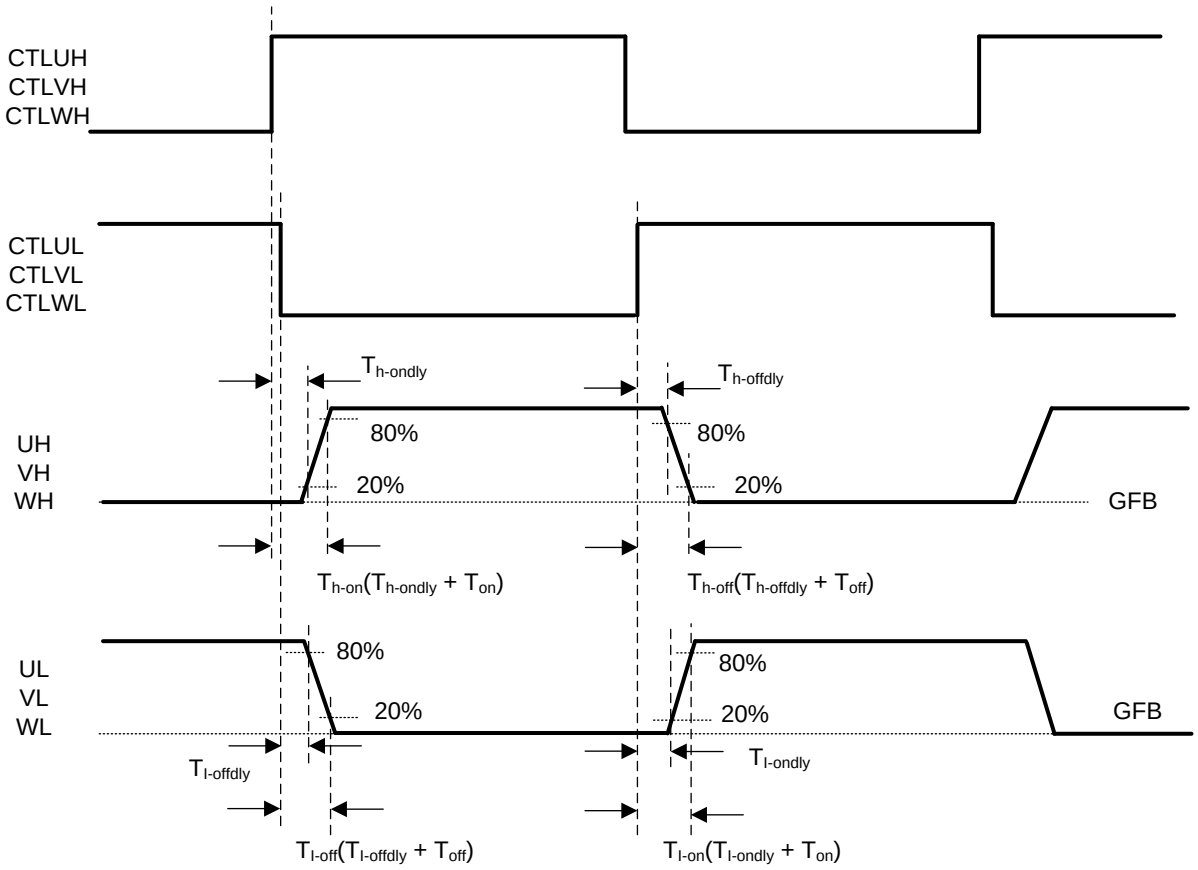


Figure 13. Delay Time from Input to Output

Feature Description (continued)

7.2.5 Phase Comparator

A 3-channel comparator module monitors the external FET by detecting voltage across the drain-source for high-side and low-side FETs. PHTM is the threshold level of comparators usable for sensorless communication. Figure 14 shows an example of the threshold level. There is no detection when CTLEN = Low.

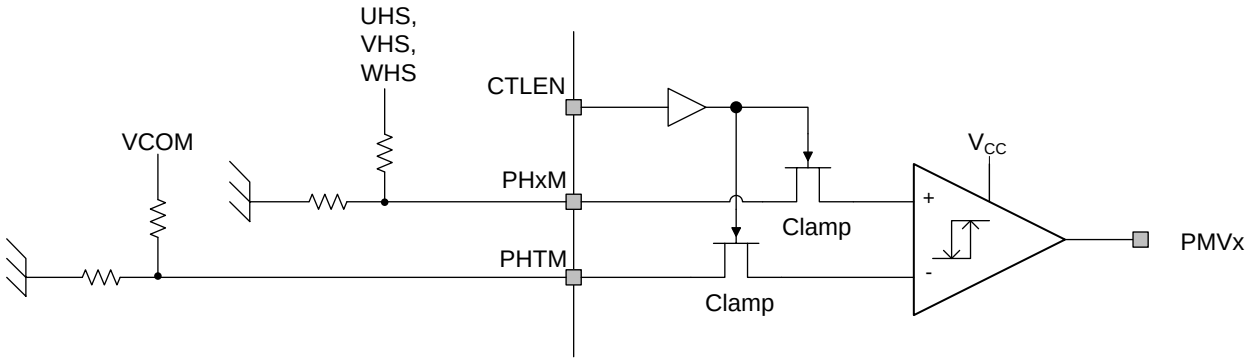


Figure 14. Phase Comparator Block Diagram

Feature Description (continued)

7.2.6 Motor Current Sense

The operational amplifier is operating with an external resistor network for higher flexibility to adjust the current measurement to application requirements. The first stage amplifier is operating with the external resistor and the output voltage up to VB at ALFB. The gain of the amplifier is adjustable by external resistors from x10 to x30. The second stage amplifier is a buffer to MCU at ALV. Current sense has a comparator for motor overcurrent (OVAD). ADTH is the overcurrent threshold level and sets the value by the external resistor as well. Figure 3 shows the curve of the detection level. ALFB is divided by 2, compare this value with ADTH. In the recommended application, zero-point adjustment is required as a large error offset in the initial condition.

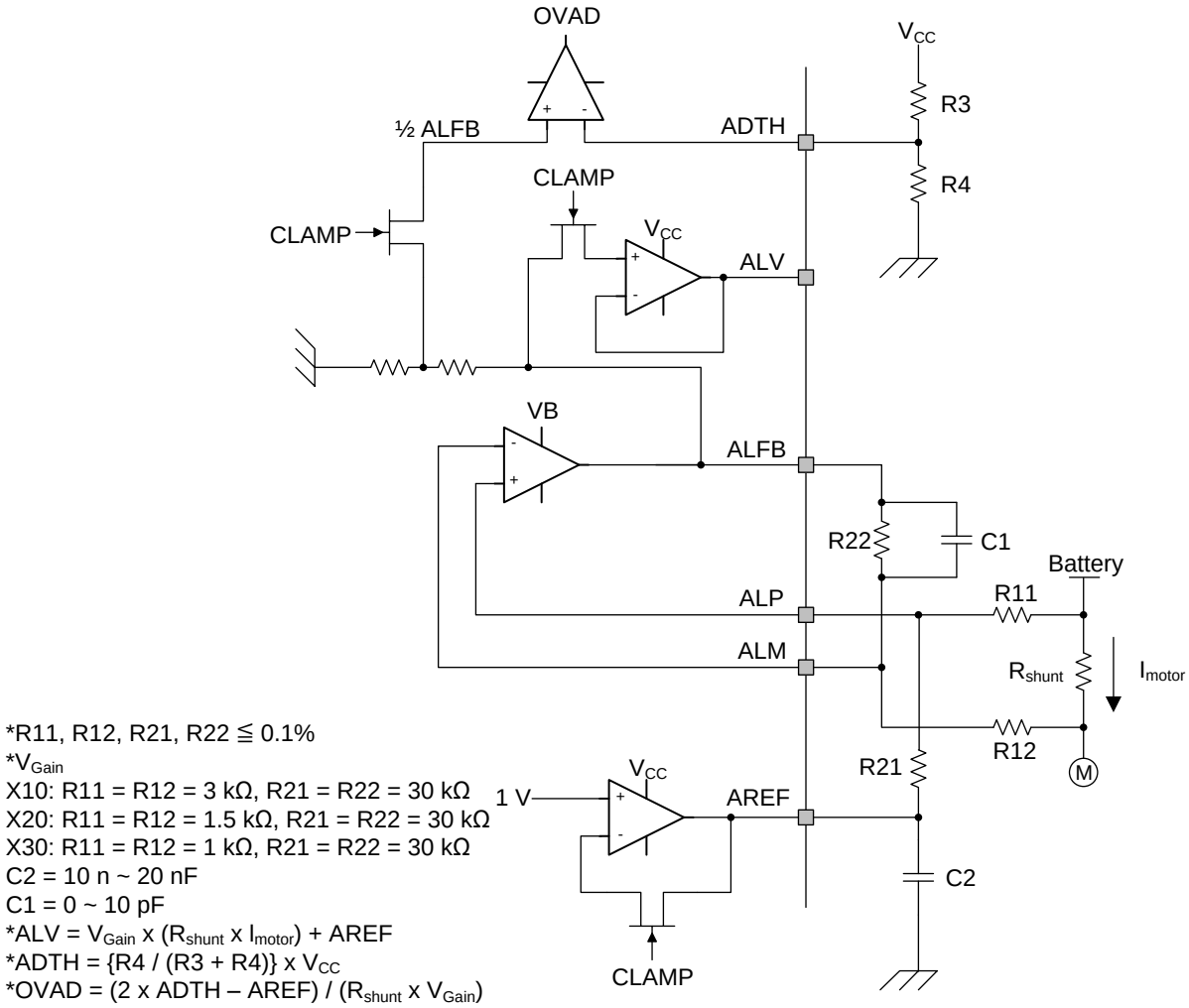


Figure 15. Motor Current Sense Block Diagram

Feature Description (continued)

7.2.7 Phase Amplifier (Sample and Hold Mode and Through Mode)

The 3-channel amplifier module monitors the drain-source for high-side and low-side FETs. Two modes (selected by the SPI) are provided: sample and hold mode, and through mode. Sample and hold is controlled by PSSx at the external pins and PSCx connects the charging capacitor. Through mode is real-time detection and the amplifier has x1–x4 gain control.

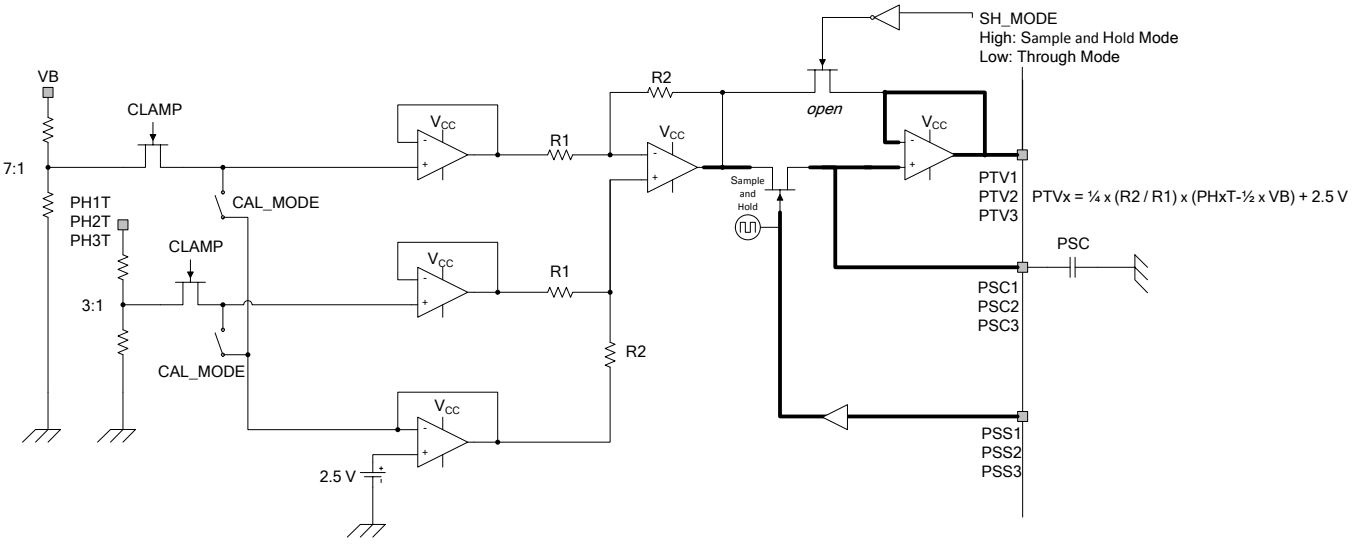


Figure 16. Sample and Hold Mode Block Diagram

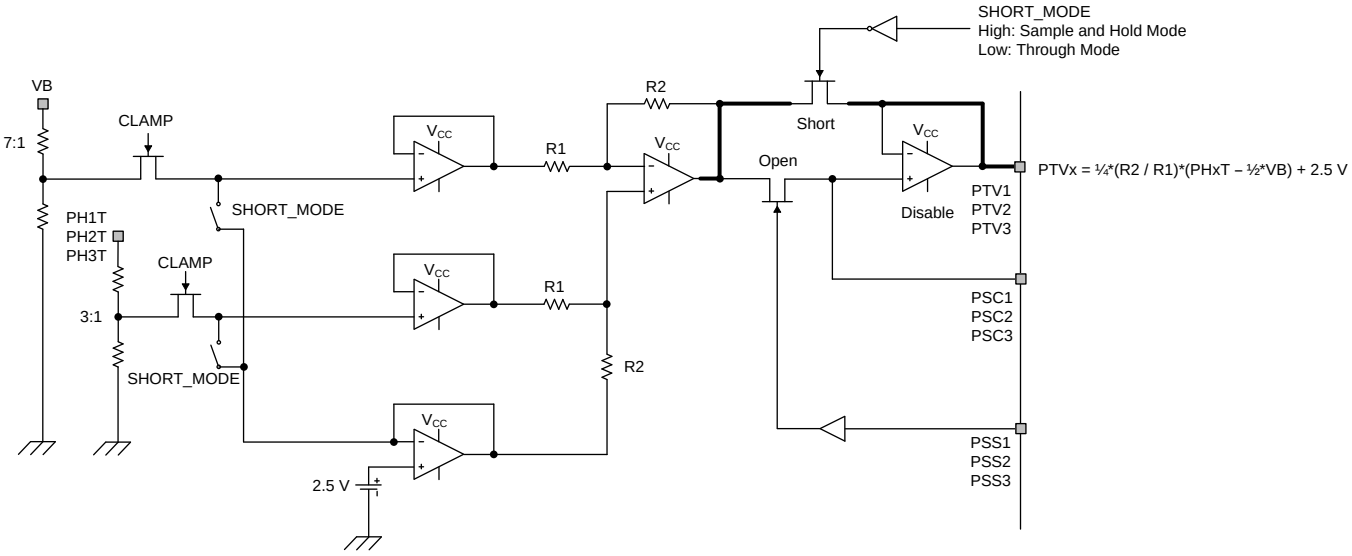


Figure 17. Through Mode Block Diagram

Feature Description (continued)

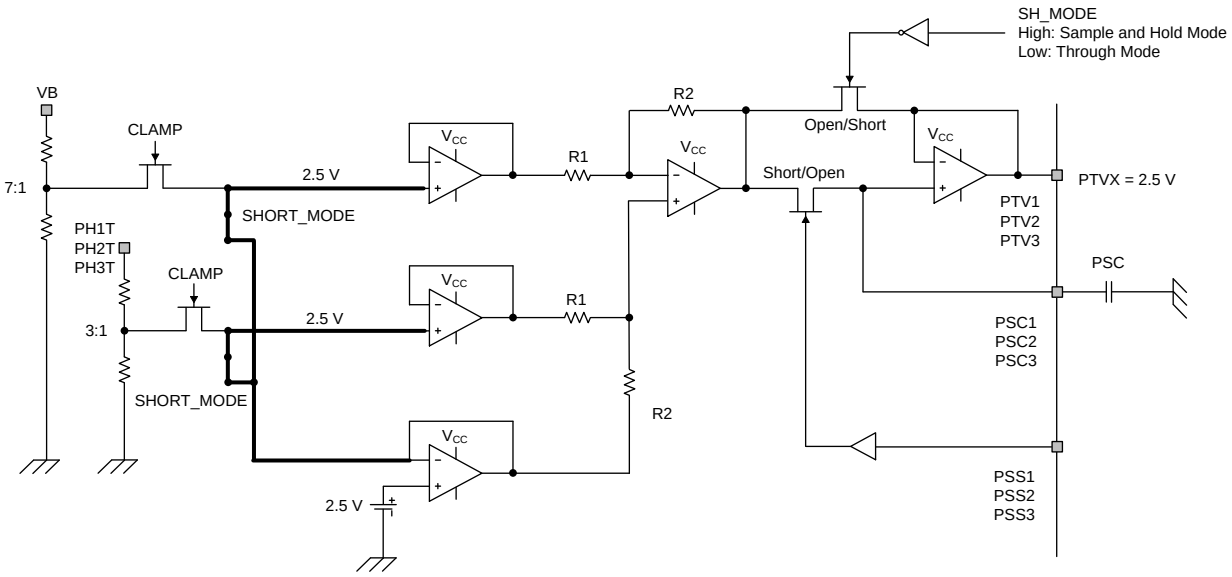


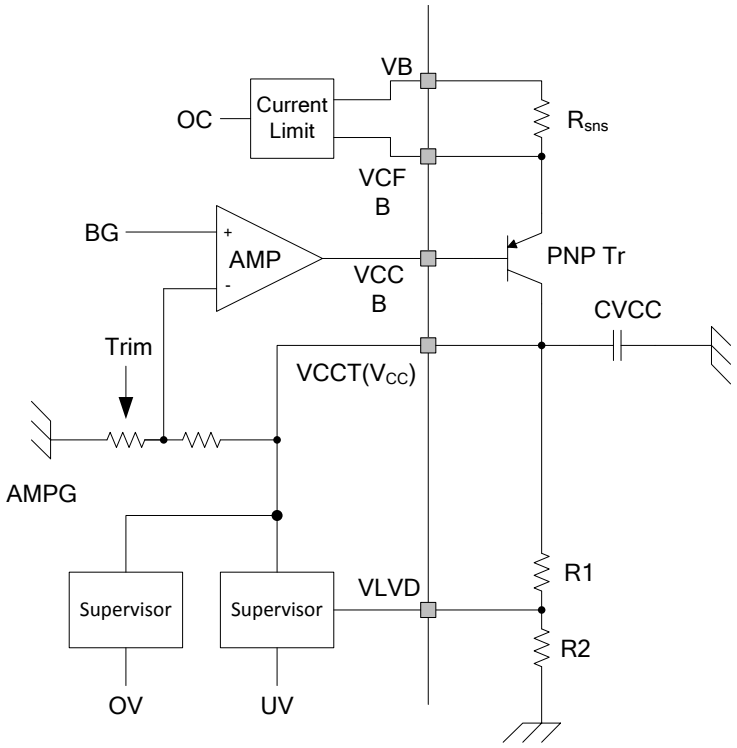
Figure 18. Short Mode (Optional) Block Diagram

Feature Description (continued)

7.2.8 Regulators

The regulator block offers a 5-V LDO and a 3.3-V LDO. The V_{CC} LDO regulates VB down to 5 V with an external PNP controlled by the regulator block. The 5-V LDO is supplied to the MCU and other components. The 5-V LDO is protected against a short to GND fault, and the external resistors R1 and R2 set the undervoltage. The V_{DD} regulator regulates VB down to 3.3-V with an internal FET and a controller.

The regulators detect the overvoltage and undervoltage events of both supplies.



* R_{sns} = 0.2 V / ICLVCC
* VCCUV = 2.325 x {(R1+R2) / R2}

Figure 19. V_{CC} Block Diagram

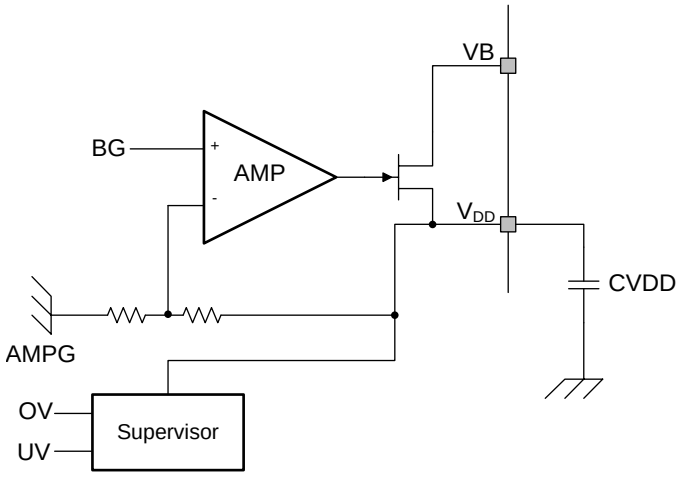


Figure 20. V_{DD} Block Diagram

Feature Description (continued)

7.2.9 VB Monitor

The block monitors VB overvoltage.

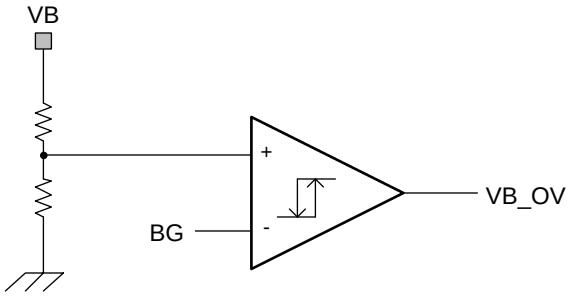


Figure 21. VB Monitor Block Diagram

7.2.10 Thermal Shutdown

The device has temperature sensors that produce a pre-driver stop condition if the chip temperature exceeds 175°.

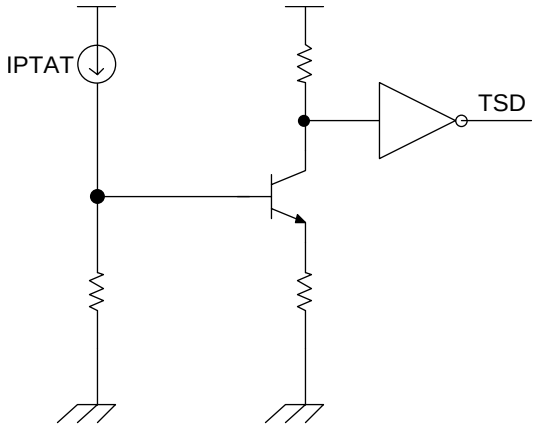


Figure 22. Thermal Shutdown Block Diagram

Feature Description (continued)

7.2.11 Oscillator

Oscillator block generates two 10-MHZ clock signals. OSC1 is the main clock used for internal logic synchronization and timing control. OSC2 is the secondary clock which is used to monitor the status of OSC1.

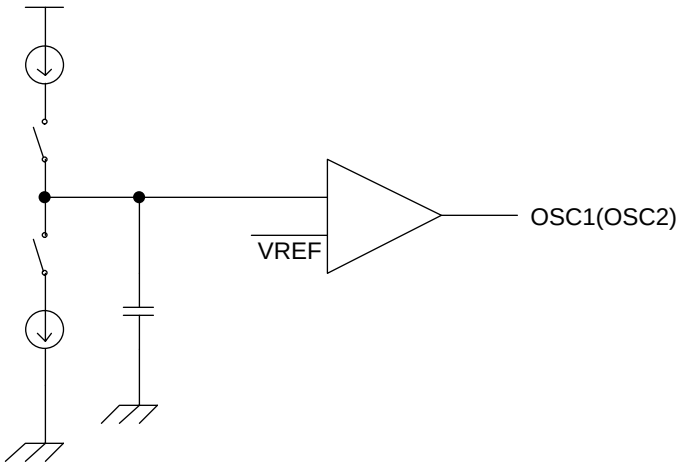


Figure 23. Oscillator Block Diagram

7.2.12 I/O

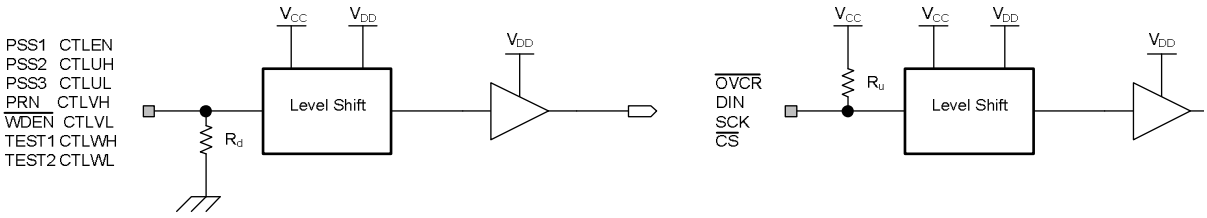


Figure 24. Input Buffer 1 Block Diagram

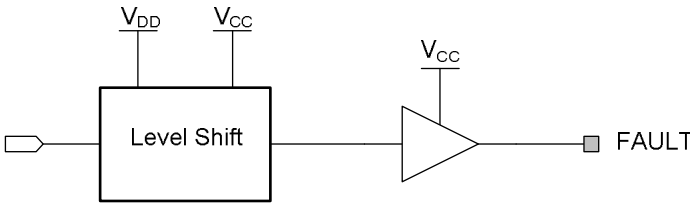


Figure 25. Output Buffer 1 Block Diagram

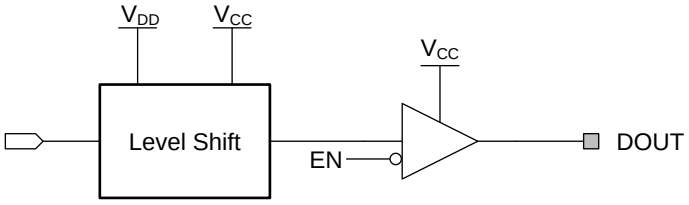


Figure 26. Output Buffer 2 Block Diagram

Feature Description (continued)

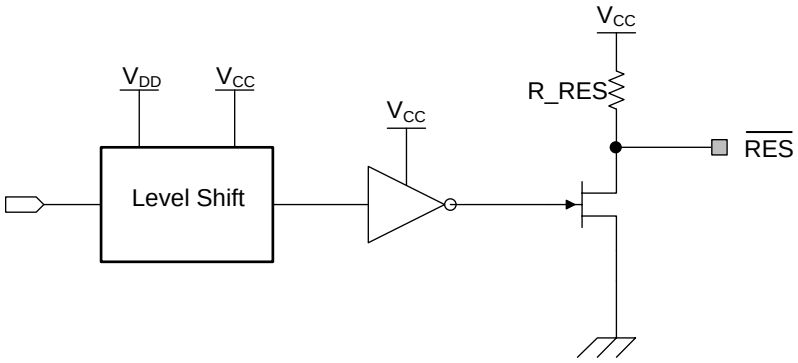


Figure 27. Output Buffer 3 Block Diagram

7.2.13 Error Detection

Table 1. Error Detection

ITEMS	SPI	PRE-DRIVER	FAULT SIGNAL	$\overline{RES}$
VB – Overvoltage	–	STOP	L	H
CP – Overvoltage	–	STOP	L	H
CP – Undervoltage	Error Bit (CPLV)	–	L	H
V_{CC} – Overvoltage	Error Bit (VCO)	–	L	H
V_{CC} – Undervoltage	–	STOP	L	L
V_{CC} – Overcurrent	Error Bit (V_{CC})	–	H	H
Motor – Overcurrent	Error Bit (OVAD)	STOP	H	H
V_{DD} – Overvoltage	Error Bit (VDO)	–	L	H
V_{DD} – Undervoltage	–	STOP	L	L
Thermal Shut Down	Error Bit (TD)	STOP	H	H
Watchdog	–	–	L	L
EEPROM Data Check	Error Bit (EEP)	–	L	H
Clock Monitor	–	–	L	L
SPI	Error Bit (SPI)	–	L	H

7.3 Device Functional Modes

Table 2. Motor Overcurrent Truth Table

$\overline{RES}$	$\overline{OVCR}$	MOTOR OVERCURRENT	OVAD	PRE-DRIVER ENABLE OR DISABLE
0	–	–	0 (Clear)	Disable (1)
1	0	–	0 (Clear) (2) (3)	Enable
	1	0	Keep	Enable
		1	1 (Set)	Disable

(1) The CTLEN goes to Hi-Z because the external CPU will not drive it when $\overline{RES}$ = 0, then all the pre-drivers are turned off because CTLEN is internally pulled down.
(2) The OVAD is not set, even if a motor overcurrent error is generated during $\overline{OVCR}$ = 0.
(3) The OVAD is cleared if $\overline{OVCR}$ = 0 even when the motor overcurrent error is generated.

7.4 Register Maps

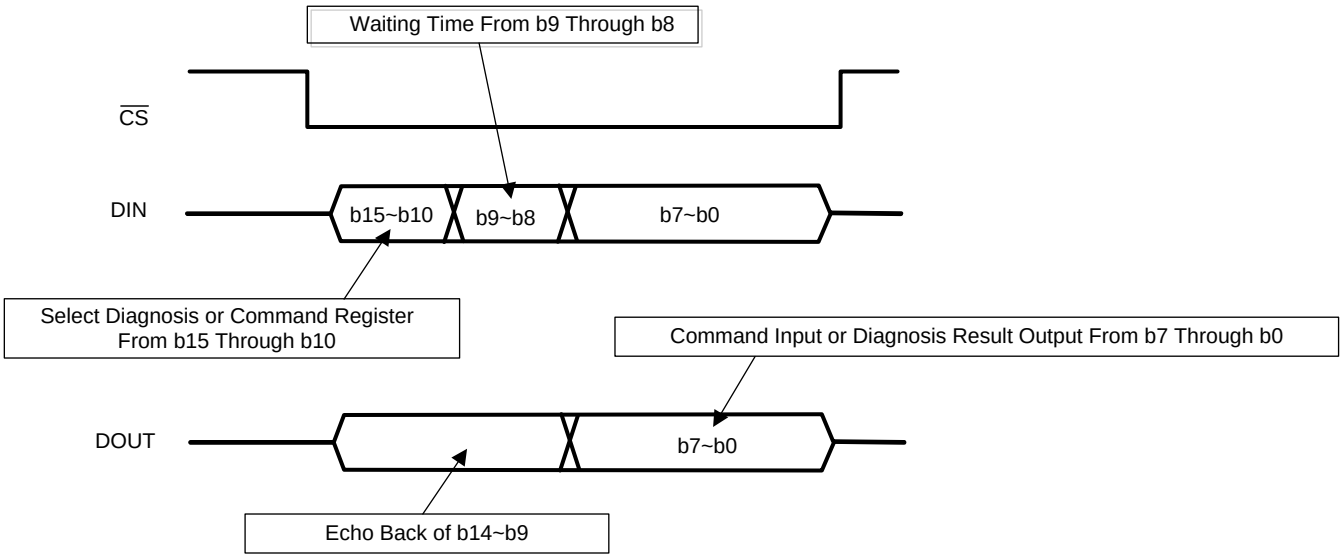


Figure 28. SPI Bit Sequence

Table 3. SPI Bit Map (DIN)

ITEM	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
COMMAND1	0	0	0	0	0	1	–	–	SHM	SRT	–	–	–	–	–	–
COMMAND2	0	0	0	0	1	0	–	–	AG1	AG0	–	–	–	–	–	–
COMMAND3	0	0	0	0	1	1	–	–	–	–	–	–	–	–	–	–
DIAG_READ1	0	0	1	0	0	0	–	–	–	–	–	–	–	–	–	–
DIAG_READ2	0	1	0	0	0	0	–	–	–	–	–	–	–	–	–	–
DIAG_READ3	0	1	1	0	0	0	–	–	–	–	–	–	–	–	–	–

In Table 3, the B15–B10 are the control bits, so the each command depends on them (listed below).

1. **B15-B10 = 0 0 0 0 0 1**

   These are the commands:

   1) Phase AMP Sampling Hold Mode (B7 bit)
      0: OFF (through) (INITIAL VALUE)
      1: ON (use sample hold mode)
   2) Phase AMP Short Mode [Short_Mode] (B6 bit)
      0: OFF (no calibration) (INITIAL VALUE)
      1: ON (use calibration mode)

2. **B15-B10 = 0 0 0 0 1 0**

   These are the commands:

   1) Phase AMP Gain (B7 bit and B6 bit)
      B7:0 B6:0; Gain x1 (INITIAL VALUE)
      B7:0 B6:1; Gain x2
      B7:1 B6:0; Gain x3
      B7:1 B6:1; Gain x4

3. **B15-B10 = 0 0 0 0 1 1**

   Not used

4. **B15-B10 = 0 0 1 0 0 0**

   This command is to read the diagnosis of the current regulator, SPI communication, overvoltage detection, and input diagnosis.

5. **B15-B10 = 0 1 0 0 0 0**

This command is to read the diagnosis of SPI communication.

6. **B15-B10 = 0 1 1 0 0 0**

   Not used

7. **B15-B10 = Other command**

   This command sets the SPI-NG (DOUT, B7) bit.

Table 4. SPI Bit Map (DOUT)

ITEM	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
ON/OFF COMMAND ECHO BACK	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
	0	0	0	0	0	1	0	0	–	–	–	–	–	–	–	–
	0	0	0	0	0	1	1	0	–	–	–	–	–	–	–	–
DIAG_READ1	0	0	0	1	0	0	0	0	VCC	Rsvd	CCD	VCO	VDO	CPLV	TD	EEP
DIAG_READ2	0	0	1	0	0	0	0	0	SPI	–	–	–	–	–	–	–
DIAG_READ3	0	0	1	1	0	0	0	0	–	–	–	–	–	–	–	–

1. **B14-B9 = 0 0 1 0 0 0**

   This flag is cleared after the register is read by the CPU.

   1) V_{CC} Current Detection (B7)
   0: NORMAL
   1: Fail (Short to GND or open)

   2) Overcurrent Detection (B6)
   0: NORMAL
   1: Fail (Overcurrent)

   4) V_{CC} Overvoltage Detection (B4)
   0: NORMAL
   1: Fail (V_{CC} overvoltage)

   5) V_{DD} Overvoltage Detection (B3)
   0: NORMAL
   1: Fail (V_{DD} overvoltage)

   6) CPV Low Voltage Detection (B2)
   0: NORMAL
   1: Fail (CPV low voltage)

   7) Thermal Detection (B1)
   0: NORMAL
   1: Fail (Overtemperature)

   8) EEPROM* Data Consistency Check (B0)
   0: NORMAL
   1: Fail (EEPROM DATA CRC error)

   *ASIC calibration EEPROM

NOTE

Just after power-on of the IC, some of the bits listed above may be set depending on the apply sequence of VB. It is recommended to issue a DIAG_READ1 to clear these bits prior to all S/W sequences.

2. **B14-B9 = 0 1 0 0 0 0**

   This flag is cleared after the register is read by the CPU.

   1) SPI-NG (B7)
   0: NORMAL
   1: Fail (SPI read and write command is wrong)

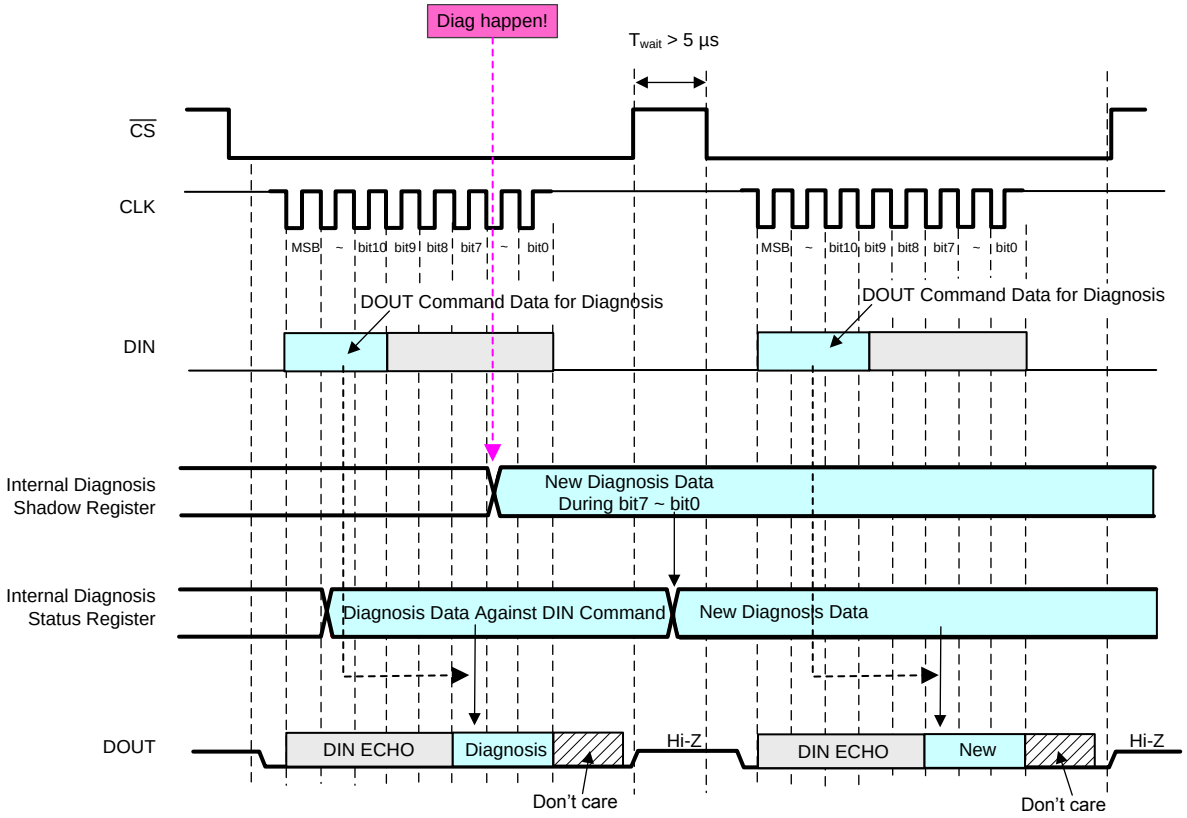


Figure 29. DIAG_READ

7.4.1 Internal Diagnosis Register (Status Register and Shadow Register)

If the diagnosis happens during the SPI communication, the function follows this protocol:

The diagnosis information is stored in the shadow register when the diagnosis happens.
After the output of the previous information a new diagnosis is sent from the shadow to the status register, and both registers are output through the DOUT pin.
In this case, a FAULT signal continues to be output until a new diagnosis is read by the CPU.

All diagnosis bits read by the DIAG_READ1 command happen before the $\overline{CS}$ falling edge. So, all the diagnosis events that happen right after the $\overline{CS}$ falling edge are not read by the current DIAG_READ1 command, instead they are read by the next DIAG_READ1 command.

8 Device and Documentation Support

8.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

8.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

8.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

8.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DRV3211QPFPQ1	NRND	HTQFP	PFP	80	96	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	DRV3211	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

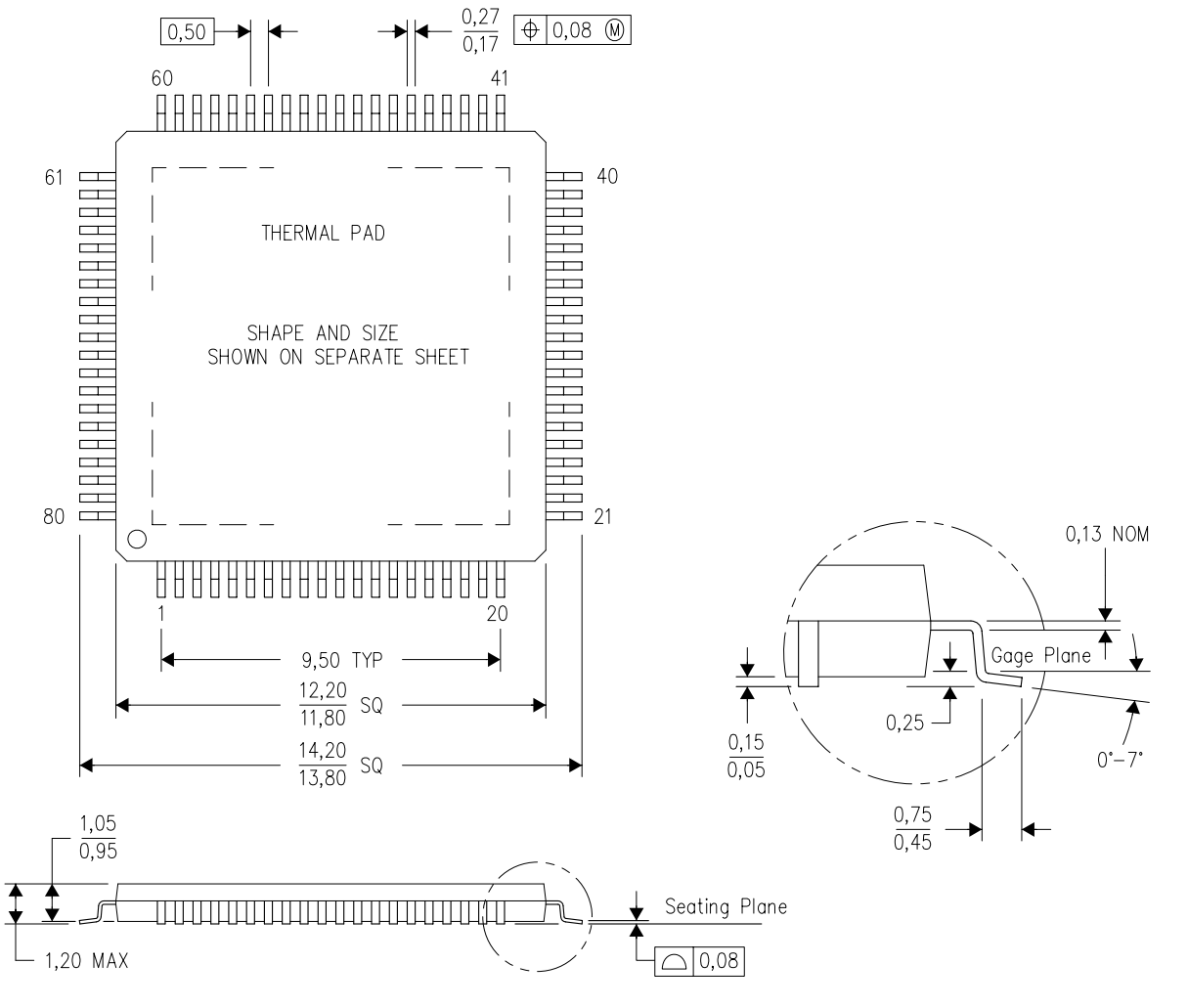
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

PFP (S–PQFP–G80) PowerPAD™ PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MS–026

PowerPAD is a trademark of Texas Instruments.

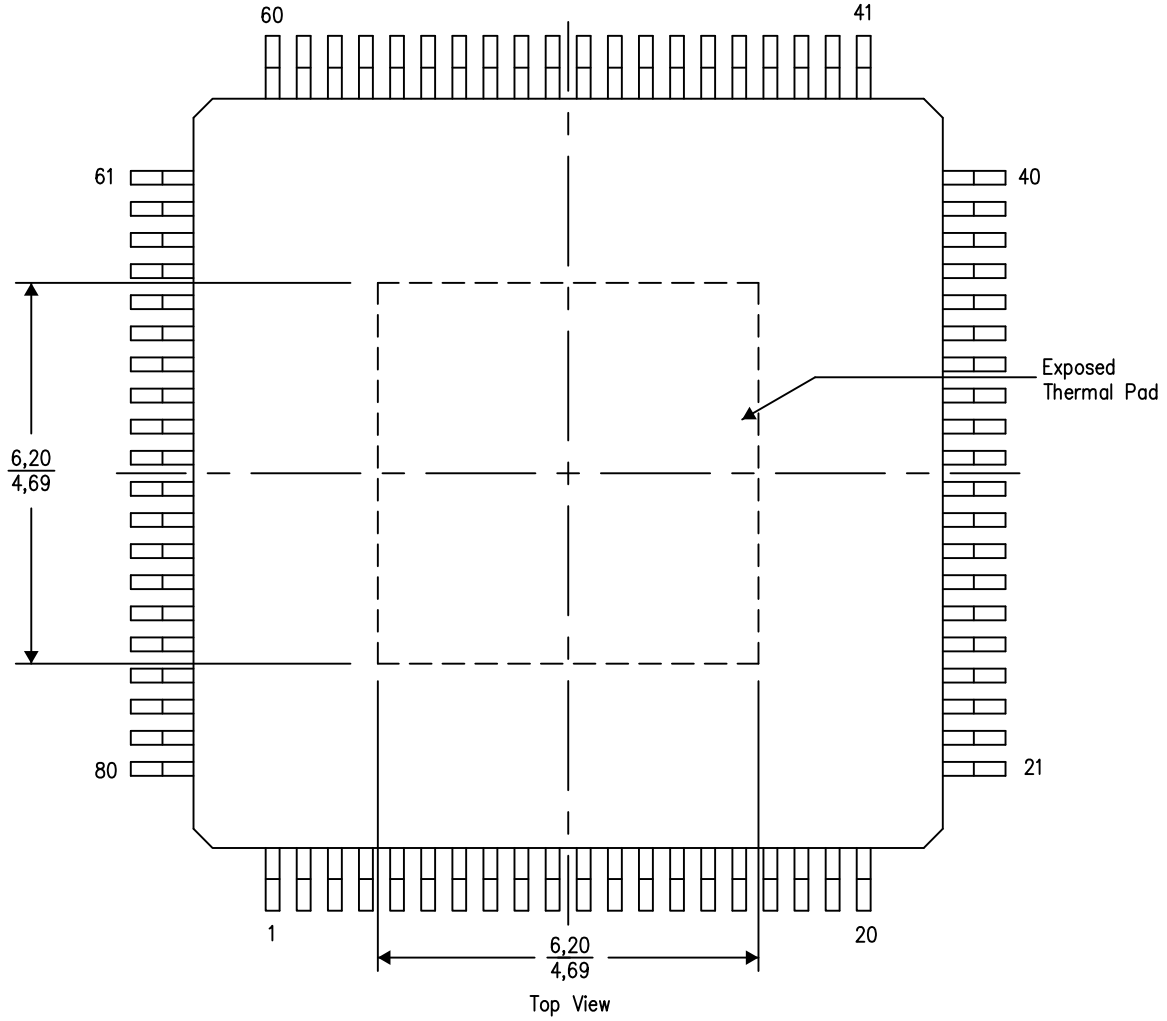
PFP (S–PQFP–G80) PowerPAD™ PLASTIC QUAD FLATPACK

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



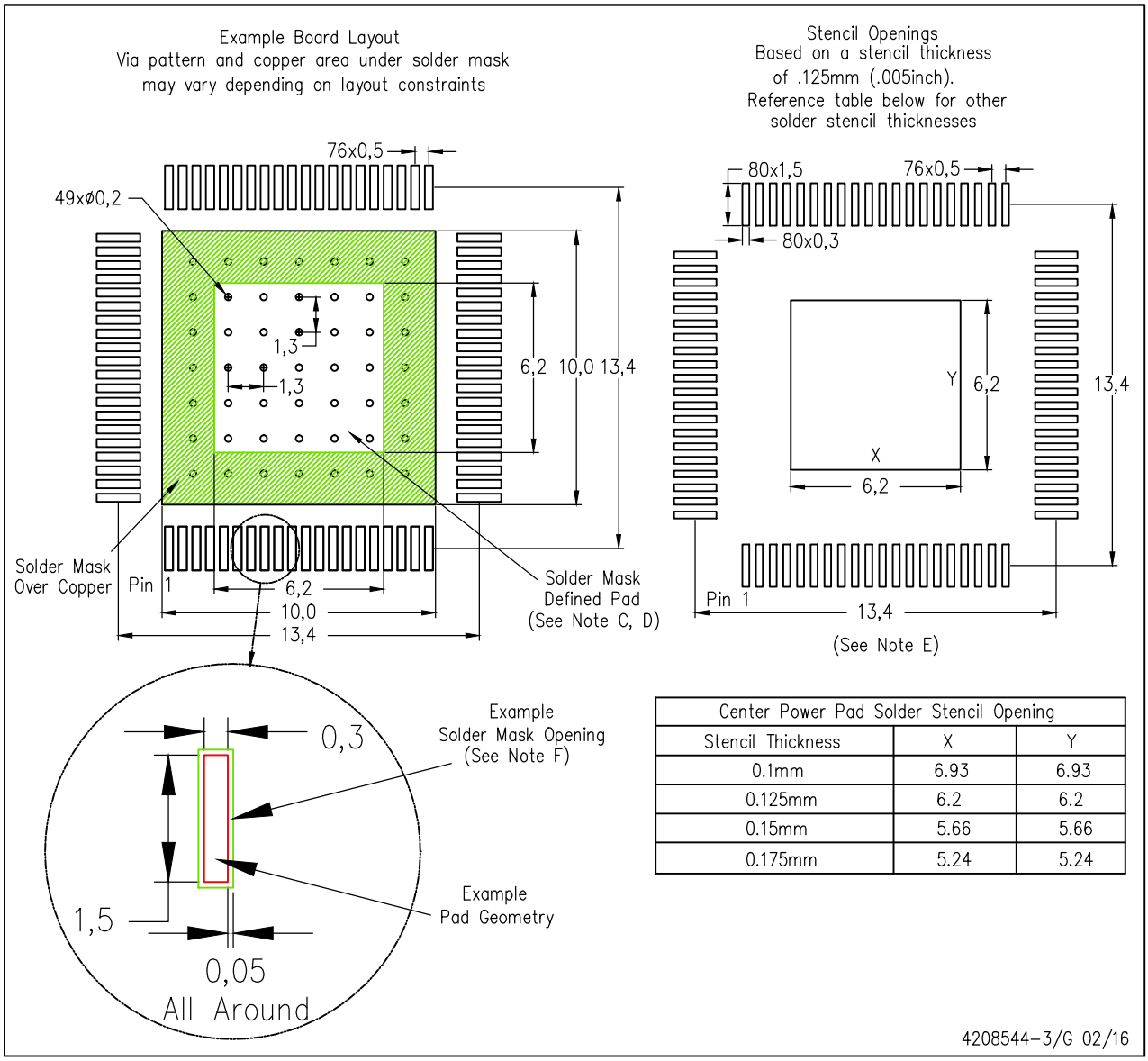
Exposed Thermal Pad Dimensions

4206327–3/P 05/14

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

PFP (S–PQFP–G80) PowerPAD™ PLASTIC QUAD FLATPACK



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	6.93	6.93
0.125mm	6.2	6.2
0.15mm	5.66	5.66
0.175mm	5.24	5.24

PowerPAD is a trademark of Texas Instruments.

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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