TPS65165EVM-233

The TPS65165EVM-233 takes a 2.5-V to 6-V input rail and provides the three bias-supply voltages and three integrated opamps that are required for TV and monitor TFT-LCD panels. The TPS65165EVM-233 has one boost converter with an integrated low-side FET, one negative charge-pump controller requiring external Schottky diodes, and one fully-integrated positive charge pump. External passive components to support the boost converter include inductors and capacitors, and external components for the charge pumps include capacitors.

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1 Introduction

This chapter contains background information for the TPS65165EVM-233 evaluation module.

1.1 Specification

Table 1 provides a summary of the TPS65165EVM-233 performance specifications. All specifications are given for an ambient temperature of 25°C.

Table 1. Performance Specification Summary

Specification	Voltage Range (V)			Current Range (mA)		
	Min	Typ	Max	Min	Typ	Max
VIN	4.5	5	5.5	5000		
Vs	14.7	15	15.3			1000
VGL	–5.15	–5	–4.85			50
VGH	23.0	23.8(1)	24.5			50

(1) Assumes that SUP = V_S.

1.2 Modifications

The primary goal of this EVM is to facilitate user evaluation of the TPS65165 in a power-supply application for a typical large TFT display. To facilitate user customization of the EVM, the board was designed with devices having 603 or larger footprints. A production-optimized implementation would likely occupy less total board space.

1.2.1 Customizing the Power Supply

The user can change each rail's regulated output voltage by changing the appropriate feedback resistors per the device data sheet (SLVS723). The user is responsible for not exceeding each output's maximum voltage specifications. In addition, alternate capacitors, inductors and/or diodes can be used. When using alternate capacitors, ensure that at least the minimum recommended capacitance per the data sheet is used, and that the capacitor voltage rating is appropriate for the application. The switching converters are designed to be used with ceramic output capacitors. Using non-ceramic output capacitors with significantly large equivalent series resistances (ESR) can result in larger output ripple or unstable operation of the inductive switching converters. Each charge pump's flying and output capacitors must be ceramic capacitors. When selecting an alternate inductor, use the datasheet design equations to ensure that an appropriate inductance value is selected, and that the inductor current rating is appropriate for the desired output current. Using an inductor with larger dc resistance will result in lower efficiency. When using alternate diodes, ensure that the diode is rated for both the expected peak current and expected power per the datasheet design equations.

The user can change the soft-start time of Vs (boost converter), VGL (negative charge pump), VGH (positive charge pump) by changing the value of C15 on the ADLY pin and C14 on the GDLY pin, respectively. When the EN pin goes high, Vs and VGL start up after a delay time set by C15 on the ADLY pin. C14 on the GDLY pin sets the startup delay time until VGH goes active with CTRL=high.

1.2.2 Input to Output Isolation

The non-synchronous boost converter has a path from input to output, i.e VIN to Vs, through external switching diode D1. Therefore, even though EN is low, the Vs terminal has a voltage equal to VIN-V_f where V_f is the diode forward voltage.

2 Setup and Test Results

This chapter explains the input, output and jumper connections of the TPS65165EVM-233. It also describes how to set up test equipment for evaluating the EVM, and provides test results.

2.1 Connections and Jumpers

The DEFAULT jumper settings are required for the EVM to operate within the specifications of Table 1.

Table 2. Default Jumper Settings

Jumper	Default Setting
JP1 – EN	GND
JP2 – HVS	GND
JP3 – CTRL	VIN
JP4 – DRN	GND
JP5 – POS3	GND
JP6 – POS2	GND
JP7 – NEG2	OUT2
JP8 – NEG1	OUT1
JP9 – POS1	GND

J1-GND:	Ground return connection for negative charge pump (VGL)
J2-VGL:	Output voltage of negative charge pump (VGL)
J3-GND:	The input power supply ground must be connected to J3 for 5-A capability
J4-VIN:	The input power supply positive connection must be connected to J4 for 5-A capability
J5-VIN:	Test point for measuring input voltage—not intend for power supply connection.
J6-Vs:	Output connection for the main boost converter (Vs)
J7-GND:	Ground return connection for the main boost converter (Vs)
J8-VGH:	Output connection for the internal high voltage switch (VGH)
J9-GND:	Ground return connection for the internal high voltage switch (VGH)
J10-GND:	Test point for measuring input ground voltage—not intend for power supply connection
J11-OUT3:	Output voltage of opamp 3. Half the voltage of Vs is generated in this EVM.
J12-POUT:	Output voltage of the positive charge pump—internally connected to the high voltage switch Q4
J13-GND:	Ground return of POUT
JP1-EN:	When EN pin is connected to VIN, the IC is enabled. When EN is connected to GND, the IC is disabled. The EN pin must be connected to either VIN or GND, and not left floating.
JP2-HVS:	When the HVS pin is connected to VIN, high-voltage stress test is enabled (Vs goes high, and VGH goes to a fixed 30 V). When the HVS pin is connected to GND, the high-voltage stress test is disabled.
JP3-CTRL:	When the CTRL pin is connected to VIN, internal MOSFET Q4 between POUT and VGH is on, and Q5 between VGH and DRN is off. When the CTRL pin is connected GND, it is the opposite; Q4 is off and Q5 is on. The user can do Gate-voltage shaping by applying a pulsed waveform to the CTRL pin.
JP4-DRN:	Connect the discharge resistor for Gate-voltage shaping to this pin. If not used, connect to GND.
JP5-POS3 and GND:	Non-inverting input of opamp 3 and GND. Half the voltage of Vs is applied at POS3 in this EVM. If opamp 3 is not used, connect POS3 to GND.
JP6-POS2 and GND:	Non-inverting input of opamp 2 and GND. If opamp 2 is not used, connect POS2 to GND.
JP7-NEG2 and OUT2:	Inverting input and the output voltage of opamp 2. If opamp 2 is not used, connect OUT2 to NEG2.
JP8-NEG1 and OUT1:	Inverting input and the output voltage of opamp 1. If opamp 1 is not used, connect OUT1 to NEG1.
JP9-POS1 and GND:	Non-inverting input of the opamp 1 and GND. If opamp 1 is not used, connect POS1 to GND.

2.2 Recommended Test Setup

Connect a power supply rated at 5 A or more to provide 5 V ±5% to J4 and J3. Do not exceed 6 V on J4. Operation at an input voltage down to 2.5 V is possible, but maximum output-current levels decrease. In order to avoid voltage drop through the input power supply line, connect heavy gauge, twisted-pair wire to J4 and J3. The output voltages can be monitored by voltmeters and/or an oscilloscope with standard high impedance voltage probes.

Before enabling this IC by connecting the EN pin to VIN pin at JP1, the user must ensure jumpers JP2 – JP9 are in their default positions. When the EN pin is connected to the VIN pin at JP1, the boost converter (Vs) and negative charge pump (VGL) start up with the delay ADLY. The positive charge pump (VGH) starts up with the delay GDLY from EN-high if CTRL = high.

The output voltages reach their respective regulation voltages per Table 1 after the appropriate soft-start times and relative delays. Resistive or electronic loads can be attached to output J6 for Vs, and only resistive loads can be attached to outputs J2 for VGL and J8 for VGH. Exceeding an output load specified in Table 1 results in the output voltage falling out of regulation.

2.3 Test Results

Test results using the TPS65160EVM-233 are shown in Figure 1.

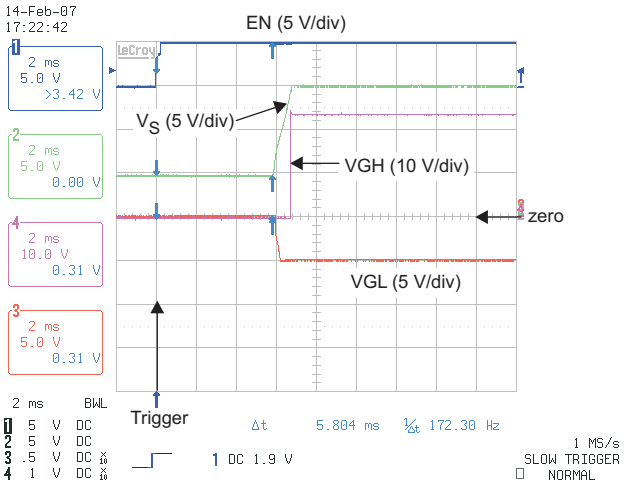

Figure 1. Startup Waveform

3 Board Layout

This chapter provides board layout recommendations as well as pictures of the EVM board layers.

3.1 Board Layout Recommendations

For complete information regarding PC-board layout, please refer to the TPS65165 Data Sheet, literature number SLVS723. An excerpt from that document follows:

1. Place the power components outlined in bold first on the PCB.
2. Rout the traces outlined in bold with wide PCB traces
3. Place a 1-µF bypass capacitor directly from the Vin pin to GND since this is the supply pin for internal circuits.
4. Place a 1-µF bypass capacitor directly from the SUP pin to GND since this is the supply pin for internal circuits.
5. Use a short and wide trace to connect the SUP pin to the output of the boost converter Vs.
6. Place the 220-nF reference capacitor directly from REF to AGND close to the IC pins.
7. The feedback resistor for the negative charge pump between FBN and REF needs to be >40kΩ.
8. Use short traces for the charge pump drive pin (DRVN) of VGL because the traces carry switching waveforms.
9. Place the flying capacitors as close as possible to the C1P, C1N and C2P, C2N pin.
10. Solder the Power Pad of the QFN package to GND and use thermal vias to lower the thermal resistance

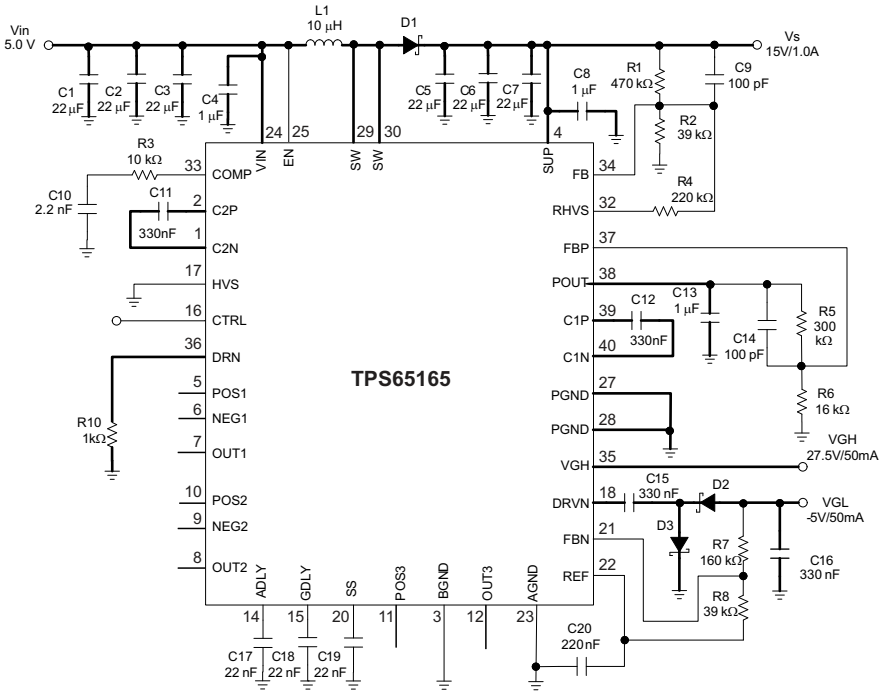

Figure 2. Layout Recommendation

3.2 Board Layers

The following pages show the top assembly, top and bottom layers of the TPS65165EVM-233.

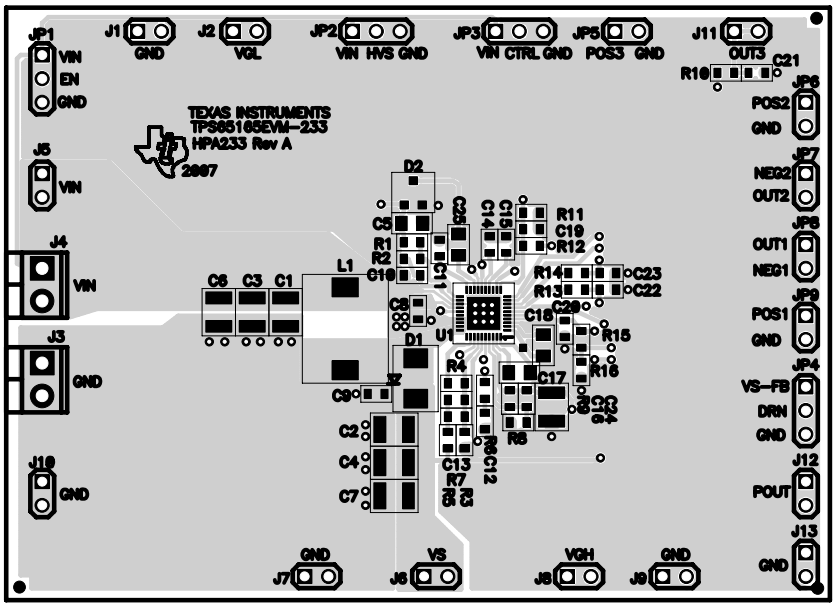

Figure 3. Top Assembly

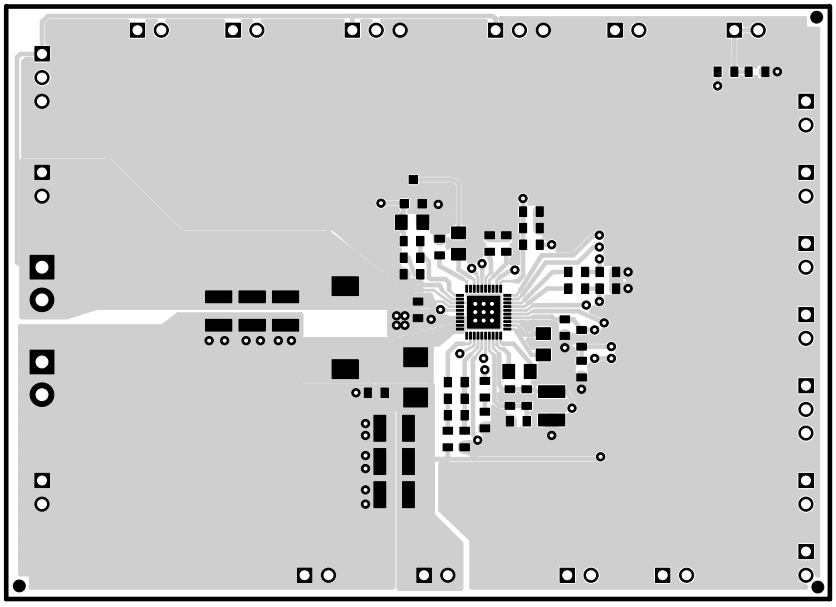

Figure 4. Top Layer

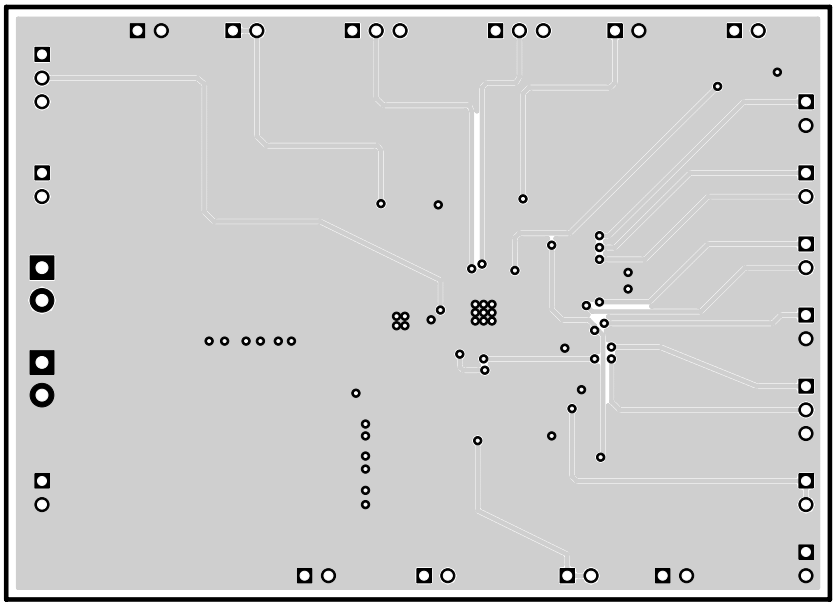

Figure 5. Bottom Layer

4 Schematic and Bill of Materials

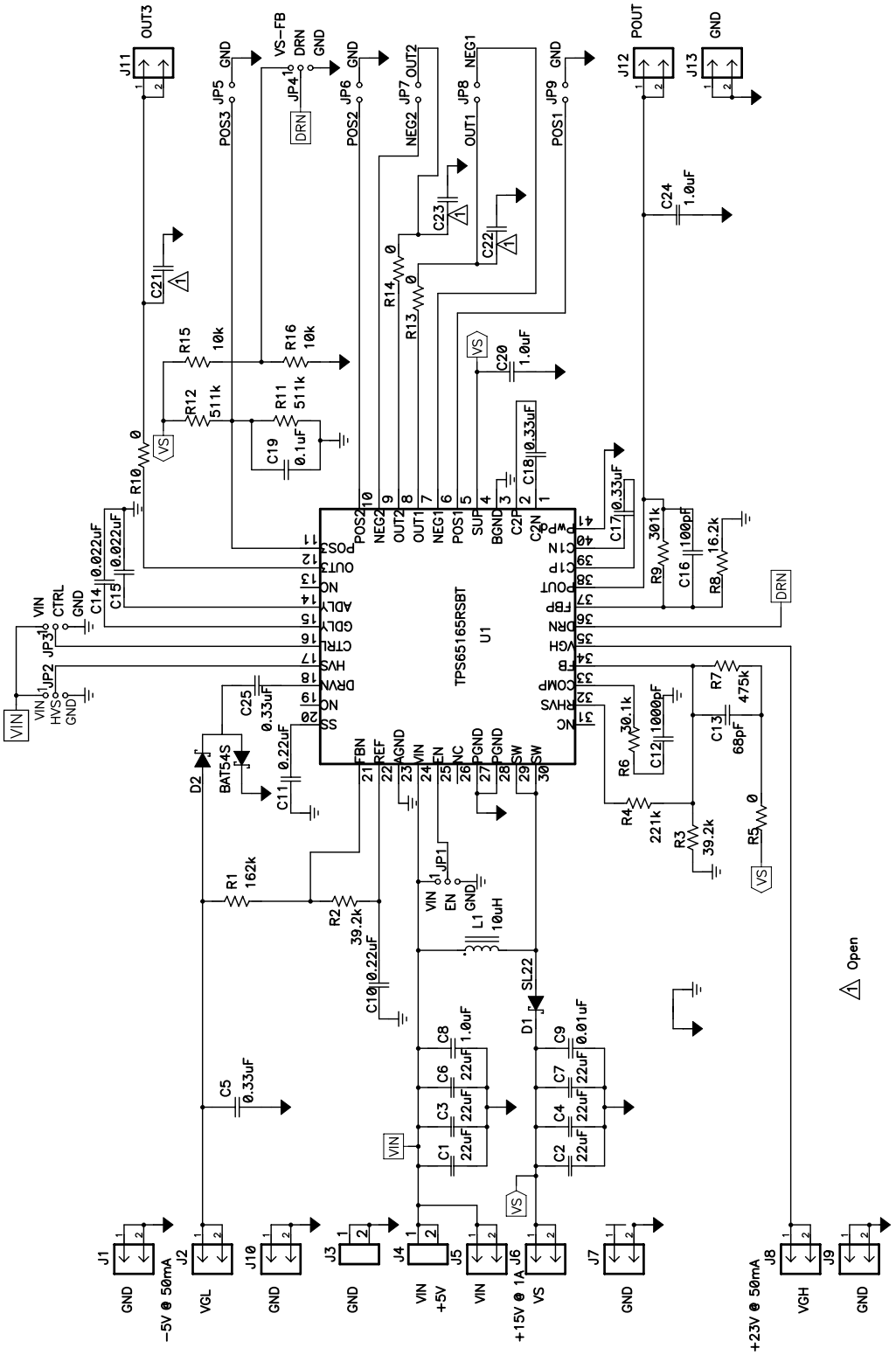

Table 3. Bill of Materials

Count	RefDes	Value	Description	Size	Part Number	MFR
6	C1–C4, C6, C7	22 µF	Capacitor, Ceramic, 25V, X5R, 20%	1210	ECJ-4YB1E226M	Pansonic
2	C10, C11	0.22 µF	Capacitor, Ceramic, 25V, X5R, 10%	0603	06033D224KAT2A	AVX
1	C12	1000 pF	Capacitor, Ceramic, 50V, C0G, 5%	0603	C1608C0G1H102J	TDK
1	C13	68 pF	Capacitor, Ceramic, 50V, C0G, 5%	0603	C1608C0G1H680J	TDK
2	C14, C15	0.022 µF	Capacitor, Ceramic, 50V, X7R, 10%	0603	C1608X7R1H223K	TDK
1	C16	100 pF	Capacitor, Ceramic, 50V, C0G, 5%	0603	C1608C0G1H101J	TDK
1	C19	0.1 µF	Capacitor, Ceramic, 50V, X7R, 10%	0603	C16088X7R1H104K	TDK
2	C20, C8	1.0 µF	Capacitor, Ceramic, 25V, X5R, 10%	0603	GRM188R61E105KA12D	Murata
0	C21–C23	Open	Capacitor, Ceramic	0603		
1	C24	1.0 µF	Capacitor, Ceramic, 50V, X7R, 10%	1210	C3225X7R1H105K	TDK
4	C5, C17, C18, C25	0.33 µF	Capacitor, Ceramic, 50V, X7R, 10%	0805	GRM219R71H333KA01D	Murata
1	C9	0.01 µF	Capacitor, Ceramic, 50V, X7R, 10%	0603	C1608X7R1H103K	TDK
1	D1		Diode, Schottky Rectiifier, 2A, 20 V	DO-214AA	SL22	Vishay
1	D2		Diode, Dual Schottky, 200mA, 30V	SOT23	BAT54S	Zetex
11	J1, J2, J5–J13		Header, 2 pin, 100mil spacing, (36-pin strip)	0.100 × 2	PTC36SAAN	Sullins
2	J3, J4		Terminal Block, 2 pin, 6A, 3.5 mm	0.27 × 0.25	ED1514	OST
4	JP1–JP4		Header, 3 pin, 100mil spacing, (36-pin strip)	0.100 × 3	PTC36SAAN	Sullins
5	JP5–JP9		Header, 2 pin, 100mil spacing, (36-pin strip)	0.100 × 2	PTC36SAAN	Sullins
1	L1	10 µH	Inductor, SMT, 4.3A, 44 mΩ	0.327 × 0.327	CDRH8D43HPNP-100NC	Sumida
1	R1	162 kΩ	Resistor, Chip, 1/16W, 1%	0603	Std	Std
2	R11, R12	511 kΩ	Resistor, Chip, 1/16W, 1%	0603	Std	Std
2	R15, R16	10 kΩ	Resistor, Chip, 1/16W, 1%	0603	Std	Std
2	R2, R3	39.2 kΩ	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R4	221 kΩ	Resistor, Chip, 1/16W, 1%	0603	Std	Std
4	R5, R10, R13, R14	0 Ω	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R6	30.1 kΩ	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R7	475 kΩ	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R8	16.2 kΩ	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R9	301 kΩ	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	U1		IC, Compact LCD bias with high-speed Amplifier for TV and Monitor TFT-LCD panels	QFN-40	TPS65165RSBT	TI
1	–		PCB, 3.45 in × 2.5 in × 0.062 in		HPA233	Any
9	–		Shunt, 100mil, black	0.100	929950-00	3M

EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of 4.5 V to 5.5 V and the output voltage range of 14.7 V to 15.3 V (Vs).

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 85°C. The EVM is designed to operate properly with certain components above 85°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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