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ON Semiconductor®

# FXLA104

## Low-Voltage Dual-Supply 4-Bit Voltage Translator with Configurable Voltage Supplies and Signal Levels, 3-State Outputs, and Auto Direction Sensing

FXLA104 — Low-Voltage Dual-Supply 4-Bit Voltage Translator

### Features

- Bi-Directional Interface between Two Levels: from 1.1V to 3.6V
- Fully Configurable: Inputs and Outputs Track  $V_{CC}$
- Non-Preferential Power-Up; Either  $V_{CC}$  May Be Powered Up First
- Outputs Switch to 3-State if Either  $V_{CC}$  is at GND
- Power-Off Protection
- Bus-Hold on Data Inputs Eliminates the Need for Pull-Up Resistors; Do Not Use Pull-Up Resistors on A or B Ports
- Control Input (/OE) Referenced to  $V_{CCA}$  Voltage
- Available in 16-Terminal UMLP (1.8mm x 2.6mm) and 12-Terminal, Quad UMLP, 1.8 x 1.8mm Packages
- Direction Control Not Necessary
- 100Mbps Throughput when Translating Between 1.8V and 2.5V
- ESD Protection Exceeds:
  - 8kV HBM (per JEDEC22-A114 & Mil Std 883e 3015.7)
  - 2kV CDM (per ESD STM 5.3)

### Description

The FXLA104 is a configurable dual-voltage supply translator for both uni-directional and bi-directional voltage translation between two logic levels. The device allows translation between voltages as high as 3.6V to as low as 1.1V. The A port tracks the  $V_{CCA}$  level and the B port tracks the  $V_{CCB}$  level. This allows for bi-directional voltage translation over a variety of voltage levels: 1.2V, 1.5V, 1.8V, 2.5V, and 3.3V.

The device remains in three-state as long as either  $V_{CC}=0V$ , allowing either  $V_{CC}$  to be powered up first. Internal power-down control circuits place the device in 3-state if either  $V_{CC}$  is removed.

The /OE input, when HIGH, disables both the A and B ports by placing them in a 3-state condition. The /OE input is supplied by  $V_{CCA}$ .

The FXLA104 supports bi-directional translation without the need for a direction control pin. The two ports of the device have auto-direction sense capability. Either port may sense an input signal and transfer it as an output signal to the other port.

### Applications

- Cell Phone, PDA, Digital Camera, Portable GPS

### Ordering Information

Part Number	Operating Temperature Range	Top Mark	Package	Packing Method
FXLA104UMX	-40 to 85°C	XJ	16-Terminal UMLP 1.8 x 2.6mm Package	5K Units Tape and Reel
FXLA104UM12X		XJ	12-Terminal, Quad UMLP, 1.8 x 1.8mm Package	

## Pin Configuration

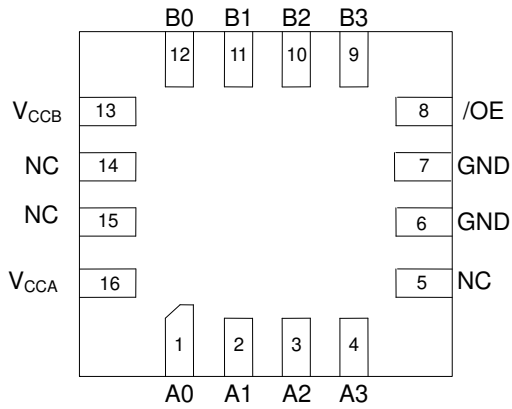


Figure 1. 16-Pin UMLP (Top Through View)

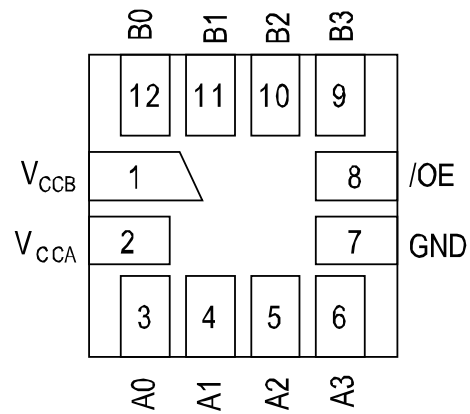


Figure 2. 12-Pin UMLP (Top Through View)

## Pin Definitions

16 Pin #	12 Pin #	Name	Description
1	3	A0	A-Side Inputs or 3-State Outputs
2	4	A1	A-Side Inputs or 3-State Outputs
3	5	A2	A-Side Inputs or 3-State Outputs
4	6	A3	A-Side Inputs or 3-State Outputs
5		NC	No Connect
6,7	7	GND	Ground
8	8	/OE	Output Enable Input
9	9	B3	B-Side Inputs or 3-State Outputs
10	10	B2	B-Side Inputs or 3-State Outputs
11	11	B1	B-Side Inputs or 3-State Outputs
12	12	B0	B-Side Inputs or 3-State Outputs
13	1	V <sub>CCB</sub>	B-Side Power Supply
14,15		NC	No Connect
16	2	V <sub>CCA</sub>	A-Side Power Supply

### Functional Diagram

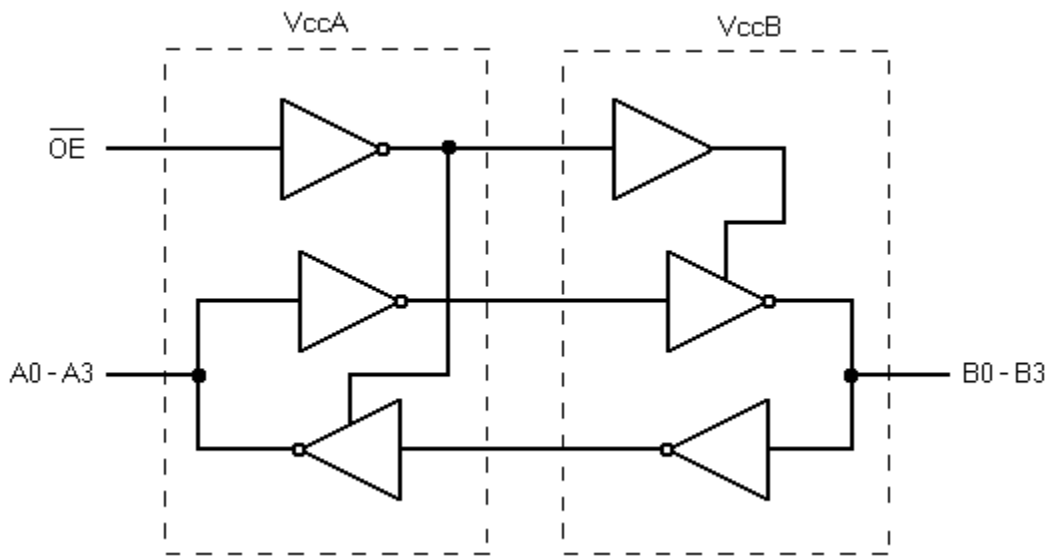


Figure 3. Functional Diagram

### Function Table

Control	Outputs
$\overline{OE}$	
LOW Logic Level	Normal Operation
HIGH Logic Level	3-State

## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Conditions	Min.	Max.	Unit
$V_{CC}$	Supply Voltage	$V_{CCA}$	-0.5	4.6	V
		$V_{CCB}$	-0.5	4.6	
$V_I$	DC Input Voltage	I/O Ports A and B	-0.5	4.6	V
		Control Input (/OE)	-0.5	4.6	
$V_O$	Output Voltage <sup>(2)</sup>	Output 3-State	-0.5	4.6	V
		Output Active ( $A_n$ )	-0.5	$V_{CCA} + 0.5$	
		Output Active ( $B_n$ )	-0.5	$V_{CCB} + 0.5$	
$I_{IK}$	DC Input Diode Current	$V_{IN} < 0V$		-50	mA
$I_{OK}$	DC Output Diode Current	$V_O < 0V$		-50	mA
		$V_O > V_{CC}$		+50	
$I_{OH}/I_{OL}$	DC Output Source/Sink Current		-50	+50	mA
$I_{CC}$	DC $V_{CC}$ or Ground Current (per Supply Pin)			$\pm 100$	mA
$T_{STG}$	Storage Temperature Range		-65	+150	$^{\circ}C$
$P_D$	Power Dissipation			17	mW
ESD	Electrostatic Discharge Capability	Human Body Model (per JESD22-A114 & Mil Std 883e 3015.7)		8	kV
		Charged Device Model (per ESD STM 5.3)		2	

### Notes:

- $I_O$  absolute maximum ratings must be observed.
- All unused inputs and input/outputs must be held at  $V_{CCI}$  or GND.

Symbol	Parameter	Conditions	Min.	Max.	Unit
$V_{CC}$	Power Supply	Operating $V_{CCA}$ or $V_{CCB}$	1.1	3.6	V
$V_{IN}$	Input Voltage	Ports A and B	0	3.6	V
		Control Input (/OE)	0	$V_{CCA}$	V
$T_A$	Operating Temperature, Free Air		-40	+85	$^{\circ}C$
dt/dV	Minimum Input Edge Rate	$V_{CCA/B} = 1.1$ to $3.6V$		10	ns/V
$\theta_{JA}$	Thermal Resistance: Junction-to-Ambient	UMLP-16		315	$^{\circ}C/W$
		UMLP-12		300	
$\theta_{JC}$	Thermal Resistance: Junction-to-Case	UMLP-16		155	$^{\circ}C/W$
		UMLP-12		165	

## Power-Up/Power-Down Sequence

FXL translators offer an advantage in that either  $V_{CC}$  may be powered up first. This benefit derives from the chip design. When either  $V_{CC}$  is at 0V, outputs are in a high-impedance state. The control input ( $/OE$ ) is designed to track the  $V_{CCA}$  supply. A pull-up resistor tying  $/OE$  to  $V_{CCA}$  should be used to ensure that bus contention, excessive currents, or oscillations do not occur during power-up or power-down. The size of the pull-up resistor is based upon the current-sinking capability of the device driving the  $/OE$  pin.

The recommended power-up sequence is:

1. Apply power to the first  $V_{CC}$ .
2. Apply power to the second  $V_{CC}$ .
3. Drive the  $/OE$  input LOW to enable the device.

The recommended power-down sequence is:

1. Drive  $/OE$  input HIGH to disable the device.
2. Remove power from either  $V_{CC}$ .
3. Remove power from other  $V_{CC}$ .

## Pull-Up/Pull-Down Resistors

Do not use pull-up or pull-down resistors. This device has bus-hold circuits: pull-up or pull-down resistors are not recommended because they interfere with the output state. The current through these resistors may exceed the hold drive,  $I_{I(HOLD)}$  and/or  $I_{I(OD)}$  bus-hold currents, resulting in data transition and/or auto-direction sensing failures. The bus-hold feature eliminates the need for extra resistors.

## DC Electrical Characteristics

T<sub>A</sub> = -40 to 85°C

Symbol	Parameter	Conditions	V <sub>CCA</sub> (V)	V <sub>CCB</sub> (V)	Min.	Typ.	Max.	Units
V <sub>IHA</sub>	High-Level Input Voltage	Data Inputs A <sub>n</sub> Control Pin /OE	2.70 to 3.60	1.10 to 3.60	2.00			V
			2.30 to 2.70		1.60			
			1.65 to 2.30		.65xV <sub>CCA</sub>			
			1.40 to 1.65		.65xV <sub>CCA</sub>			
			1.10 to 1.40		.90xV <sub>CCA</sub>			
V <sub>IHB</sub>	Data Inputs B <sub>n</sub>	1.10 to 3.60	2.70 to 3.60	2.00			V	
			2.30 to 2.70	1.60				
			1.65 to 2.30	.65xV <sub>CCB</sub>				
			1.40 to 1.65	.65xV <sub>CCB</sub>				
			1.10 to 1.40	.90xV <sub>CCB</sub>				
V <sub>ILA</sub>	Low-Level Input Voltage	Data Inputs A <sub>n</sub> Control Pin /OE	2.70 to 3.60	1.10 to 3.60			.80	V
			2.30 to 2.70				.70	
			1.65 to 2.30				.35xV <sub>CCA</sub>	
			1.40 to 1.65				.35xV <sub>CCA</sub>	
			1.10 to 1.40				.10xV <sub>CCA</sub>	
V <sub>ILB</sub>	Data Inputs B <sub>n</sub>	1.10 to 3.60	2.70 to 3.60				.80	V
			2.30 to 2.70			.70		
			1.65 to 2.30			.35xV <sub>CCB</sub>		
			1.40 to 1.65			.35xV <sub>CCB</sub>		
			1.10 to 1.40			.10xV <sub>CCB</sub>		
V <sub>OHA</sub>	High-Level Output Voltage <sup>(3)</sup>	I <sub>OH</sub> = -4μA	1.10 to 3.60	1.10 to 3.60	V <sub>CCA</sub> - .4			V
V <sub>OHB</sub>		I <sub>OH</sub> = -4μA	1.10 to 3.60	1.10 to 3.60	V <sub>CCB</sub> - .4			
V <sub>OLA</sub>	Low-Level Output Voltage <sup>(3)</sup>	I <sub>OL</sub> = 4μA	1.10 to 3.60	1.10 to 3.60			.4	V
V <sub>OLB</sub>		I <sub>OL</sub> = 4μA	1.10 to 3.60	1.10 to 3.60			.4	
I <sub>I(HOLD)</sub>	Bus-Hold Input Minimum Drive Current	V <sub>IN</sub> = 0.8V	3.00	3.00	75.0			μA
		V <sub>IN</sub> = 2.0V	3.00	3.00	-75.0			
		V <sub>IN</sub> = 0.7V	2.30	2.30	45.0			
		V <sub>IN</sub> = 1.6V	2.30	2.30	-45.0			
		V <sub>IN</sub> = 0.57V	1.65	1.65	25.0			
		V <sub>IN</sub> = 1.07V	1.65	1.65	-25.0			
		V <sub>IN</sub> = 0.49V	1.40	1.40	11.0			
		V <sub>IN</sub> = 0.91V	1.40	1.40	-11.0			
		V <sub>IN</sub> = 0.11V	1.10	1.10		4.0		
		V <sub>IN</sub> = 0.99V	1.10	1.10		-4.0		

**Note:**

3. This is the output voltage for static conditions. Dynamic drive specifications are given in the Dynamic Output Electrical Characteristics table.

*Continued on following page...*

**DC Electrical Characteristics** (Continued)T<sub>A</sub> = -40 to 85°C.

Symbol	Parameter	Conditions	V <sub>CCA</sub> (V)	V <sub>CCB</sub> (V)	Min.	Max.	Units
I <sub>I(ODH)</sub>	Bus-Hold Input Overdrive High Current <sup>(4)</sup>	Data Inputs A <sub>n</sub> , B <sub>n</sub>	3.60	3.60	450.0		μA
			2.70	2.70	300.0		
			1.95	1.95	200.0		
			1.60	1.60	120.0		
			1.40	1.40	80.0		
I <sub>I(ODL)</sub>	Bus-Hold Input Overdrive Low Current <sup>(5)</sup>	Data Inputs A <sub>n</sub> , B <sub>n</sub>	3.60	3.60	-450.0		μA
			2.70	2.70	-300.0		
			1.95	1.95	-200.0		
			1.60	1.60	-120.0		
			1.40	1.40	-80.0		
I <sub>I</sub>	Input Leakage Current	Control Inputs /OE, V <sub>I</sub> =V <sub>CCA</sub> or GND	1.10 to 3.60	3.60		±1.0	μA
I <sub>OFF</sub>	Power-Off Leakage Current	A <sub>n</sub> V <sub>O</sub> =0V to 3.6V	0	3.60		±2.0	μA
		B <sub>n</sub> V <sub>O</sub> =0V to 3.6V	3.60	0		±2.0	
I <sub>OZ</sub>	3-State Output Leakage	A <sub>n</sub> , B <sub>n</sub> V <sub>O</sub> =0V or 3.6V, /OE=V <sub>IH</sub>	3.60	3.60		±5.0	μA
		A <sub>n</sub> V <sub>O</sub> =0V or 3.6V, /OE=GND	3.60	0		±5.0	
		B <sub>n</sub> V <sub>O</sub> =0V or 3.6V, /OE=GND	0	3.60		±5.0	
I <sub>CCA/B</sub>	Quiescent Supply Current <sup>(6,7)</sup>	V <sub>I</sub> =V <sub>CCI</sub> or GND; I <sub>O</sub> =0, /OE=GND	1.10 to 3.60	1.10 to 3.60		10.0	μA
I <sub>CCZ</sub>		V <sub>I</sub> =V <sub>CCI</sub> or GND; I <sub>O</sub> =0, /OE=V <sub>IH</sub>	1.10 to 3.60	1.10 to 3.60		10.0	μA
I <sub>CCA</sub>	Quiescent Supply Current	V <sub>I</sub> =V <sub>CCB</sub> or GND; I <sub>O</sub> =0 B-to-A Direction, /OE=GND	0	1.10 to 3.60		-10.0	μA
		V <sub>I</sub> =V <sub>CCA</sub> or GND; I <sub>O</sub> =0 A-to-B Direction	1.10 to 3.60	0		10.0	
I <sub>CCB</sub>		V <sub>I</sub> =V <sub>CCA</sub> or GND; I <sub>O</sub> =0, A-to-B Direction, /OE=GND	1.10 to 3.60	0		-10.0	μA
		V <sub>I</sub> =V <sub>CCB</sub> or GND; I <sub>O</sub> =0 B-to-A Direction	0	1.10 to 3.60		10.0	

**Notes:**

- An external drive must source at least the specified current to switch LOW-to-HIGH.
- An external drive must source at least the specified current to switch HIGH-to-LOW.
- V<sub>CCI</sub> is the V<sub>CC</sub> associated with the input side.
- Reflects current per supply, V<sub>CCA</sub> or V<sub>CCB</sub>.



## Dynamic Output Electrical Characteristic

### A Port (A<sub>n</sub>)

Output Load: C<sub>L</sub>=15pF, R<sub>L</sub> ≥ MΩ (C<sub>I/O</sub>=4pF), T<sub>A</sub>=-40 to 85°C

Symbol	Parameter	V <sub>CCA</sub> =3.0V to 3.6V		V <sub>CCA</sub> =2.3V to 2.7V		V <sub>CCA</sub> =1.65V to 1.95V		V <sub>CCA</sub> =1.4V to 1.6V		V <sub>CCA</sub> =1.1V to 1.3V	Units
		Typ.	Max.	Typ.	Max.	Typ.	Max.	Typ.	Max.	Typ.	
t <sub>rise</sub>	Output Rise Time A Port <sup>(9)</sup>		3.0		3.5		4.0		5.0	7.5	ns
t <sub>fall</sub>	Output Fall Time A Port <sup>(10)</sup>		3.0		3.5		4.0		5.0	7.5	ns
I <sub>OHD</sub>	Dynamic Output Current High <sup>(9)</sup>	-11.4		-7.5		-4.7		-3.2		-1.7	mA
I <sub>OLD</sub>	Dynamic Output Current Low <sup>(10)</sup>	+11.4		+7.5		+4.7		+3.2		+1.7	mA

### B Port (B<sub>n</sub>)

Output Load: C<sub>L</sub>=15pF, R<sub>L</sub> ≥ MΩ (C<sub>I/O</sub>=5pF), T<sub>A</sub>=-40 to 85°C

Symbol	Parameter	V <sub>CCB</sub> =3.0V to 3.6V		V <sub>CCB</sub> =2.3V to 2.7V		V <sub>CCB</sub> =1.65V to 1.95V		V <sub>CCB</sub> =1.4V to 1.6V		V <sub>CCB</sub> =1.1V to 1.3V	Units
		Typ.	Max.	Typ.	Max.	Typ.	Max.	Typ.	Max.	Typ.	
t <sub>rise</sub>	Output Rise Time B Port <sup>(9)</sup>		3.0		3.5		4.0		5.0	7.5	ns
t <sub>fall</sub>	Output Fall Time B Port <sup>(10)</sup>		3.0		3.5		4.0		5.0	7.5	ns
I <sub>OHD</sub>	Dynamic Output Current High <sup>(9)</sup>	-12.0		-7.9		-5.0		-3.4		-1.8	mA
I <sub>OLD</sub>	Dynamic Output Current Low <sup>(10)</sup>	+12.0		+7.9		+5.0		+3.4		+1.8	mA

#### Notes:

8. Dynamic output characteristics are guaranteed, but not tested.
9. See Figure 8.
10. See Figure 9.

## AC Characteristics

$V_{CCA} = 3.0V$  to  $3.6V$ ,  $T_A = -40$  to  $85^\circ C$

Symbol	Parameter	$V_{CCB}=3.0V$ to $3.6V$		$V_{CCB}=2.3V$ to $2.7V$		$V_{CCB}=1.65V$ to $1.95V$		$V_{CCB}=1.4V$ to $1.6V$		$V_{CCB}=1.1V$ to $1.3V$	Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Typ.	
$t_{PLH}, t_{PHL}$	A to B	0.2	4.0	0.3	4.2	0.5	5.4	0.6	6.8	6.9	ns
	B to A	0.2	4.0	0.2	4.1	0.3	5.0	0.5	6.0	4.5	ns
$t_{PZL}, t_{PZH}$	/OE to A, /OE to B		1.7		1.7		1.7		1.7	1.7	$\mu s$
$t_{SKEW}$	A Port, B Port <sup>(11)</sup>		0.5		0.5		0.5		1.0	1.0	ns

$V_{CCA} = 2.3V$  to  $2.7V$ ,  $T_A = -40$  to  $85^\circ C$

Symbol	Parameter	$V_{CCB}=3.0V$ to $3.6V$		$V_{CCB}=2.3V$ to $2.7V$		$V_{CCB}=1.65V$ to $1.95V$		$V_{CCB}=1.4V$ to $1.6V$		$V_{CCB}=1.1V$ to $1.3V$	Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Typ.	
$t_{PLH}, t_{PHL}$	A to B	0.2	4.1	0.4	4.5	0.5	5.6	0.8	6.9	7.0	ns
	B to A	0.3	4.2	0.4	4.5	0.5	5.5	0.5	6.5	4.8	ns
$t_{PZL}, t_{PZH}$	/OE to A, /OE to B		1.7		1.7		1.7		1.7	1.7	$\mu s$
$t_{SKEW}$	A Port, B Port <sup>(11)</sup>		0.5		0.5		0.5		1.0	1.0	ns

$V_{CCA} = 1.65V$  to  $1.95V$ ,  $T_A = -40$  to  $85^\circ C$

Symbol	Parameter	$V_{CCB}=3.0V$ to $3.6V$		$V_{CCB}=2.3V$ to $2.7V$		$V_{CCB}=1.65V$ to $1.95V$		$V_{CCB}=1.4V$ to $1.6V$		$V_{CCB}=1.1V$ to $1.3V$	Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Typ.	
$t_{PLH}, t_{PHL}$	A to B	0.3	5.0	0.5	5.5	0.8	6.7	0.9	7.5	7.5	ns
	B to A	0.5	5.4	0.5	5.6	0.8	6.7	1.0	7.0	5.4	ns
$t_{PZL}, t_{PZH}$	/OE to A, /OE to B		1.7		1.7		1.7		1.7	1.7	$\mu s$
$t_{SKEW}$	A Port, B Port <sup>(11)</sup>		0.5		0.5		0.5		1.0	1.0	ns

Note:

11. Skew is the variation of propagation delay between output signals and applies only to output signals on the same port ( $A_n$  or  $B_n$ ) and switching with the same polarity (LOW-to-HIGH or HIGH-to-LOW) (see Figure 11). Skew is guaranteed, but not tested.

**AC Characteristics** (Continued) $V_{CC}=1.4V$  to  $1.6V$ ,  $T_A=-40$  to  $85^\circ C$ 

Symbol	Parameter	$V_{CCB}=3.0V$ to $3.6V$		$V_{CCB}=2.3V$ to $2.7V$		$V_{CCB}=1.65V$ to $1.95V$		$V_{CCB}=1.4V$ to $1.6V$		$V_{CCB}=1.1V$ to $1.3V$	Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Typ.	
$t_{PLH}, t_{PHL}$	A to B	0.5	6.0	0.5	6.5	1.0	7.0	1.0	8.5	7.9	ns
	B to A	0.6	6.8	0.8	6.9	0.9	7.5	1.0	8.5	6.1	ns
$t_{PZL}, t_{PZH}$	/OE to A, /OE to B		1.7		1.7		1.7		1.7	1.7	$\mu s$
$t_{SKEW}$	A Port, B Port <sup>(12)</sup>		1.0		1.0		1.0		1.0	1.0	ns

 $V_{CCA}=1.1V$  to  $1.3V$ ,  $T_A=-40$  to  $85^\circ C$ 

Symbol	Parameter	$V_{CCB}=3.0V$ to $3.6V$	$V_{CCB}=2.3V$ to $2.7V$	$V_{CCB}=1.65V$ to $1.95V$	$V_{CCB}=1.4V$ to $1.6V$	$V_{CCB}=1.1V$ to $1.3V$	Units
		Typ.	Typ.	Typ.	Typ.	Typ.	
$t_{PLH}, t_{PHL}$	A to B	4.6	4.8	5.4	6.2	9.2	ns
	B to A	6.8	7.0	7.4	7.8	9.1	ns
$t_{PZL}, t_{PZH}$	/OE to A, /OE to B	1.7	1.7	1.7	1.7	1.7	$\mu s$
$t_{SKEW}$	A Port, B Port <sup>(12)</sup>	1.0	1.0	1.0	1.0	1.0	ns

Note:

12. Skew is the variation of propagation delay between output signals and applies only to output signals on the same port ( $A_n$  or  $B_n$ ) and switching with the same polarity (LOW-to-HIGH or HIGH-to-LOW) (see Figure 11). Skew is guaranteed, but not tested.

**Maximum Data Rate**<sup>(13, 14)</sup> $T_A = -40$  to  $85^\circ\text{C}$ 

$V_{CCA}$	$V_{CCB}=3.0\text{V}$ to $3.6\text{V}$	$V_{CCB}=2.3\text{V}$ to $2.7\text{V}$	$V_{CCB}=1.65\text{V}$ to $1.95\text{V}$	$V_{CCB}=1.4\text{V}$ to $1.6\text{V}$	$V_{CCB}=1.1\text{V}$ to $1.3\text{V}$	Units
	Min.	Min.	Min.	Min.	Typ.	
$V_{CCA}=3.00\text{V}$ to $3.60\text{V}$	140	120	100	80	40	Mbps
$V_{CCA}=2.30\text{V}$ to $2.70\text{V}$	120	120	100	80	40	Mbps
$V_{CCA}=1.65\text{V}$ to $1.95\text{V}$	100	100	80	60	40	Mbps
$V_{CCA}=1.40\text{V}$ to $1.60\text{V}$	80	80	60	60	40	Mbps
$V_{CCA}=1.10\text{V}$ to $1.30\text{V}$	Typ.	Typ.	Typ.	Typ.	Typ.	
	40	40	40	40	40	Mbps

**Notes:**

13. Maximum data rate is guaranteed, but not tested.

14. Maximum data rate is specified in megabits per second (*see Figure 10*). It is equivalent to two times the F-toggle frequency, specified in megahertz. For example, 100Mbps is equivalent to 50MHz.**Capacitance**

Symbol	Parameter	Conditions	$T_A = +25^\circ\text{C}$ Typical	Units	
$C_{IN}$	Input Capacitance Control Pin (/OE)	$V_{CCA}=V_{CCB}=\text{GND}$	3	pF	
$C_{I/O}$	Input/Output Capacitance	$V_{CCA}=V_{CCB}=3.3\text{V}$ , /OE= $V_{CCA}$	$A_n$	4	pF
			$B_n$	5	
$C_{pd}$	Power Dissipation Capacitance	$V_{CCA}=V_{CCB}=3.3\text{V}$ , $V_I=0\text{V}$ or $V_{CC}$ , $f=10\text{MHz}$	25	pF	

## I/O Architecture Benefit

The FXLA104 I/O architecture benefits the end user, beyond level translation, in the following three ways:

**Auto Direction** without an external direction pin.

**Drive Capacitive Loads.** Automatically shifts to a higher current drive mode only during “Dynamic Mode” or HL / LH transitions.

**Lower Power Consumption.** Automatically shifts to low-power mode during “Static Mode” (no transitions), lowering power consumption.

The FXLA104 does not require a direction pin. Instead, the I/O architecture detects input transitions on both side and automatically transfers the data to the corresponding output. For example, for a given channel, if both A and B side are at a static LOW, the direction has been established as  $A \rightarrow B$ , and a LH transition occurs on the B port; the FXLA104 internal I/O architecture automatically changes direction from  $A \rightarrow B$  to  $B \rightarrow A$ .

During HL / LH transitions, or “Dynamic Mode,” a strong output driver drives the output channel in parallel with a weak output driver. After a typical delay of approximately 10ns – 50ns, the strong driver is turned off, leaving the weak driver enabled for holding the logic state of the channel. This weak driver is called the “bus

hold.” “Static Mode” is when only the bus hold drives the channel. The bus hold can be over ridden in the event of a direction change. The strong driver allows the FXLA104 to quickly charge and discharge capacitive transmission lines during dynamic mode. Static mode conserves power, where  $I_{CC}$  is typically  $< 5\mu A$ .

### Bus Hold Minimum Drive Current

Specifies the minimum amount of current the bus hold driver can source/sink. The bus hold minimum drive current ( $I_{HOLD}$ ) is  $V_{CC}$  dependent and guaranteed in the DC Electrical tables. The intent is to maintain a valid output state in a static mode, but that can be overridden when an input data transition occurs.

### Bus Hold Input Overdrive Drive Current

Specifies the minimum amount of current required (by an external device) to overdrive the bus hold in the event of a direction change. The bus hold overdrive ( $I_{ODH}$ ,  $I_{ODL}$ ) is  $V_{CC}$  dependent and guaranteed in the DC Electrical tables.

### Dynamic Output Current

The strength of the output driver during LH / HL transitions is *referenced on page 8, Dynamic Output Electrical Characteristics,  $I_{OHD}$ , and  $I_{OLD}$ .*

## Test Diagrams

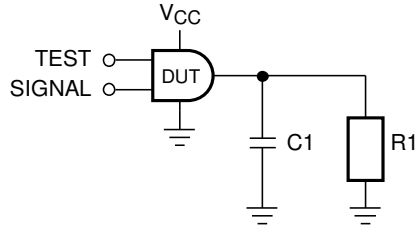


Figure 4. Test Circuit

Table 1. AC Test Conditions

Test	Input Signal	Output Enable Control
$t_{PLH}$ , $t_{PHL}$	Data Pulses	0V
$t_{PZL}$	0V	HIGH to LOW Switch
$t_{PZH}$	$V_{CCI}$	HIGH to LOW Switch

Table 2. AC Load

$V_{CCO}$	C1	R1
$1.2V \pm 0.1V$	15pF	1M $\Omega$
$1.5V \pm 0.1V$	15pF	1M $\Omega$
$1.8V \pm 0.15V$	15pF	1M $\Omega$
$2.5V \pm 0.2V$	15pF	1M $\Omega$
$3.3V \pm 0.3V$	15pF	1M $\Omega$

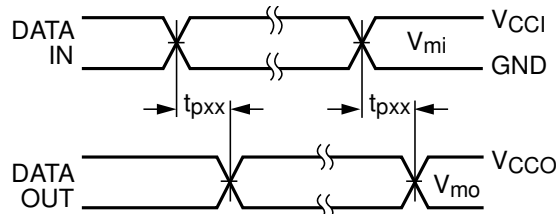
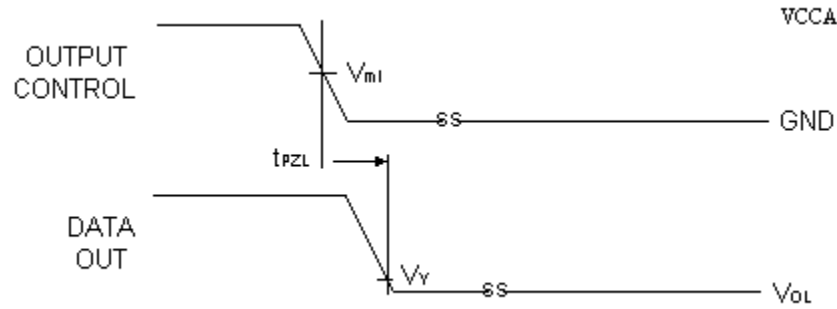


Figure 5. Waveform for Inverting and Non-Inverting Functions

**Notes:**

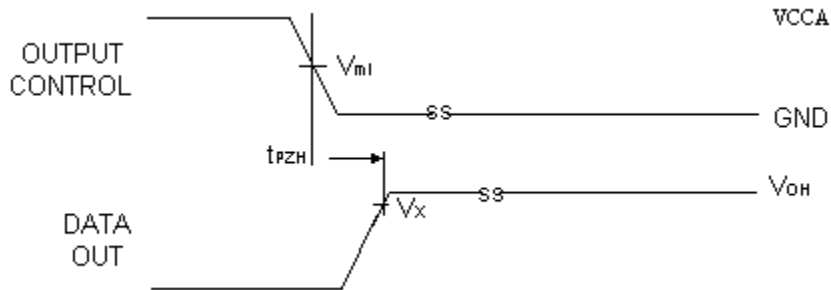
- 15. Input  $t_R = t_F = 2.0ns$ , 10% to 90%.
- 16. Input  $t_R = t_F = 2.5ns$ , 10% to 90%, at  $V_I = 3.0V$  to  $3.6V$  only.



**Figure 6. 3-State Output Low Enable Time for Low Voltage Logic**

**Notes:**

- 17. Input  $t_R = t_F = 2.0\text{ns}$ , 10% to 90%.
- 18. Input  $t_R = t_F = 2.5\text{ns}$ , 10% to 90%, at  $V_I = 3.0\text{V}$  to  $3.6\text{V}$  only.



**Figure 7. 3-State Output High Enable Time for Low Voltage Logic**

**Notes:**

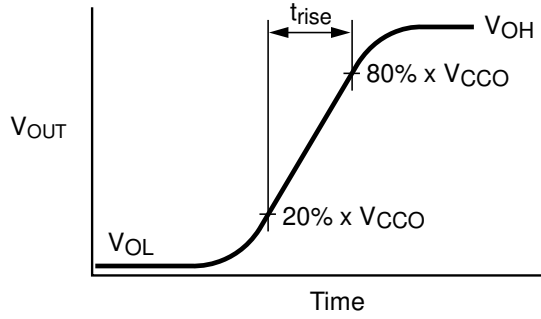
- 19. Input  $t_R = t_F = 2.0\text{ns}$ , 10% to 90%.
- 20. Input  $t_R = t_F = 2.5\text{ns}$ , 10% to 90%, at  $V_I = 3.0\text{V}$  to  $3.6\text{V}$  only.

**Table 3. Test Measure Points**

Symbol	$V_{DD}$
$V_{M1}^{(21)}$	$V_{CCI} / 2$
$V_{MO}$	$V_{CC0} / 2$
$V_X$	$0.9 \times V_{CC0}$
$V_Y$	$0.1 \times V_{CC0}$

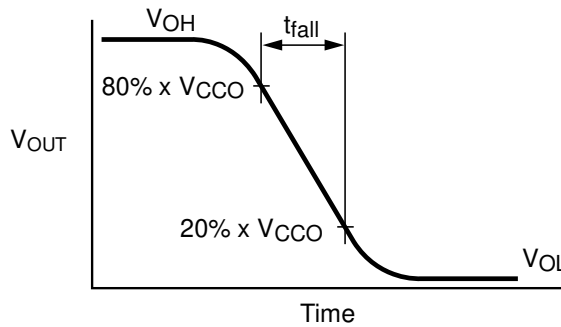
**Note:**

- 21.  $V_{CCI} = V_{CCA}$  for control pin /OE or  $V_{M1}(V_{CCA}/2)$ .



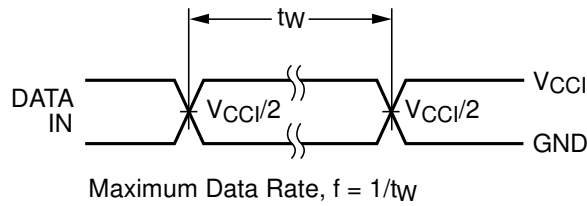
$$I_{OHD} \approx (C_L + C_{I/O}) \times \frac{\Delta V_{OUT}}{\Delta t} = (C_L + C_{I/O}) \times \frac{(20\% - 80\%) \cdot V_{CCO}}{t_{RISE}}$$

**Figure 8. Active Output Rise Time and Dynamic Output Current High**

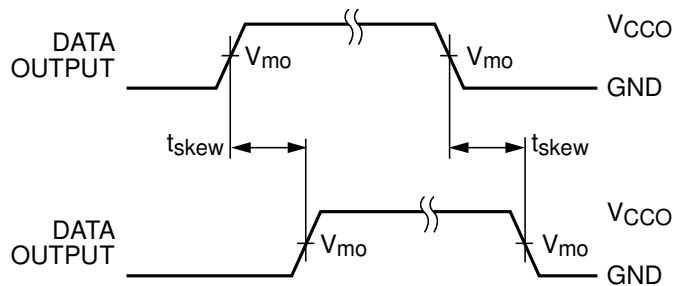


$$I_{OLD} \approx (C_L + C_{I/O}) \times \frac{\Delta V_{OUT}}{\Delta t} = (C_L + C_{I/O}) \times \frac{(80\% - 20\%) \cdot V_{CCO}}{t_{FALL}}$$

**Figure 9. Active Output Fall Time and Dynamic Output Current Low**



**Figure 10. Maximum Data Rate**



**Figure 11. Output Skew Time**

**Note:**

22.  $t_{SKEW} = (t_{pHLmax} - t_{pHLmin})$  OR  $(t_{pLHmax} - t_{pLHmin})$



## Physical Dimensions

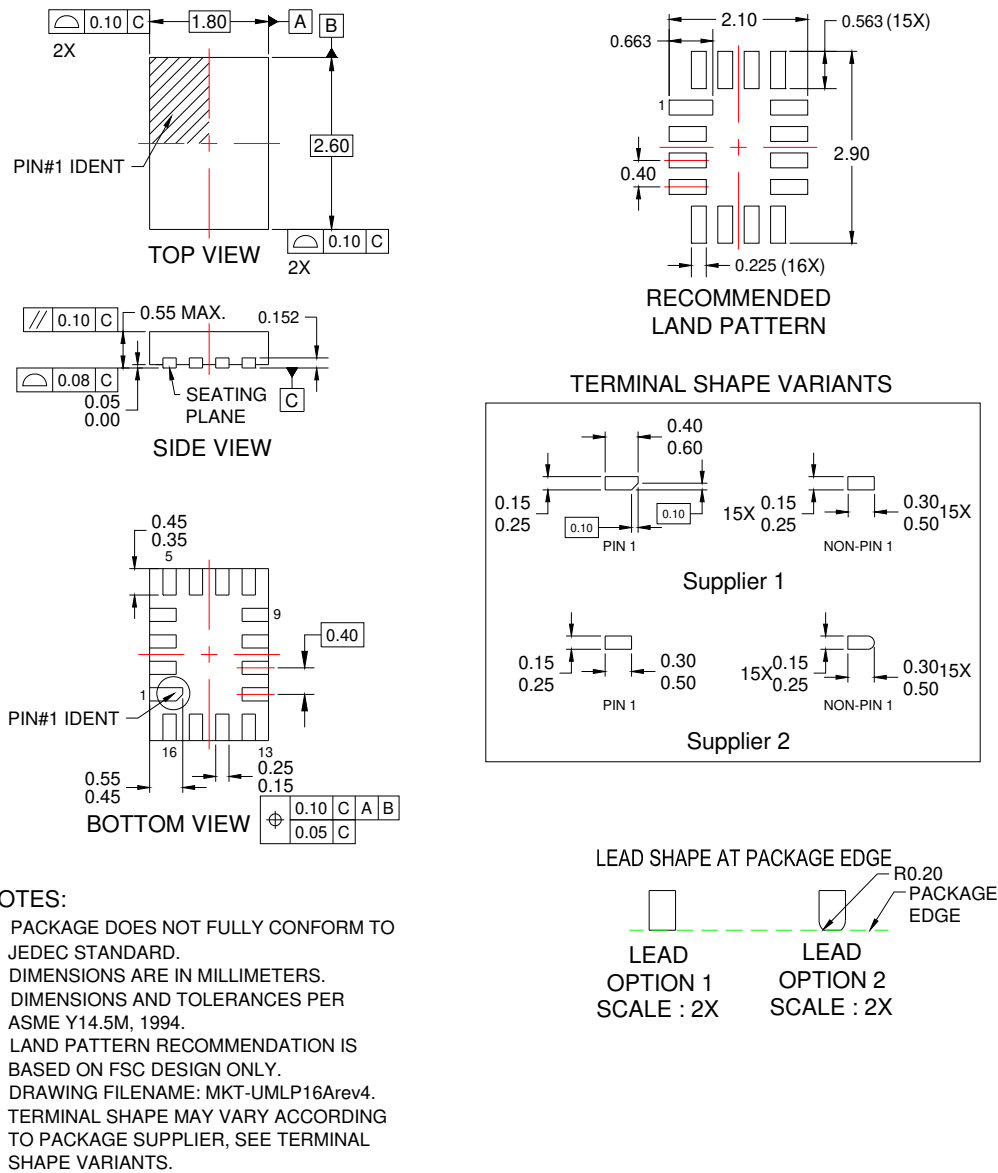


Figure 12.16-Lead, UMLP, QUAD, Ultra-Thin MLP, 1.8 X 2.6mm

## Physical Dimensions

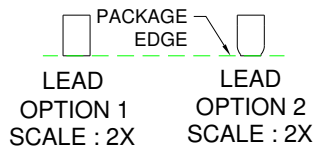
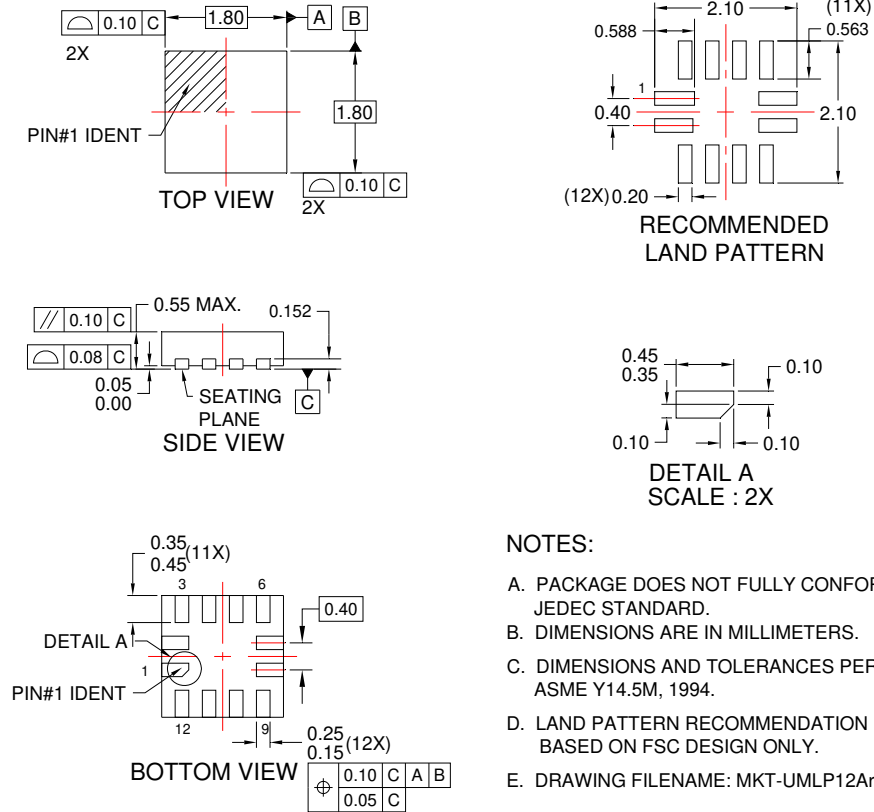



Figure 13.12-Lead, UMLP, QUAD, JEDEC MO-252 1.8 x 1.8mm Package

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