ANALOG DEVICES

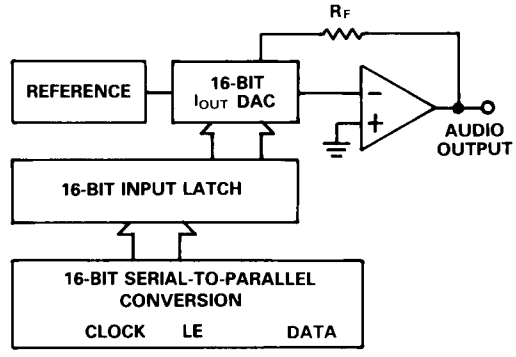
16-Bit PCM Audio DAC

AD1856

FEATURES
0.0025% THD
Fast Settling Permits 2×, 4× or 8× Oversampling
±3V Output
Optional Trim Allows Superlinear Performance
±5V to ±12V Operation
16-Pin Plastic DIP or SOIC Package
Serial Input

APPLICATIONS
Compact Disc Players
Digital Audio Amplifiers
DAT Recorders and Players
Synthesizers and Keyboards

BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD1856 is a monolithic 16-bit PCM Audio DAC. Each device provides a voltage output amplifier, 16-bit DAC, 16-bit serial-to-parallel input register and voltage reference. The digital portion of the AD1856 is fabricated with CMOS logic elements that are provided by Analog Devices' BiMOS II process. The analog portion of the AD1856 is fabricated with bipolar and MOS devices as well as thin film resistors.

This combination of circuit elements, as well as careful design and layout techniques, results in high performance audio playback. Laser trimming of the linearity error affords extremely low total harmonic distortion. An optional linearity trim pin is provided to allow residual differential linearity error at midscale to be eliminated. This feature is particularly valuable for low distortion reconstructions of low amplitude signals. Output glitch is also small contributing to the overall high level of performance. The output amplifier achieves fast settling and high slew rates, providing a full ±3V signal at load currents up to 8mA. The output amplifier is short circuit protected and can withstand indefinite shorts to ground.

The serial input interface consists of the clock, data and latch enable pins. The serial 2s complement data word is clocked into the DAC, MSB first, by the external data clock. The latch enable signal transfers the input word from the internal serial input register to the parallel DAC input register. The input clock can support a 10MHz clock rate. This serial input port is compatible with popular digital filter chips used in consumer audio products. These filters operate at oversampling rates of 2×, 4× and 8× sampling frequency.

The AD1856 can operate with ±5V to ±12V power supplies making it suitable for both the portable and home-use markets. The digital supplies, V_L and $-V_L$, can be separated from the analog supplies, V_S and $-V_S$, for reduced digital crosstalk. Separate analog and digital ground pins are also provided.

Power dissipation is 110mW typical with ±5V supplies and is a typical 300mW when ±12V supplies are used.

The AD1856 is packaged in a 16-pin plastic DIP or SOIC package and incorporates the industry-standard pinout. Operation is guaranteed over the temperature range of −25°C to +70°C and over the voltage supply range of ±4.75 to ±13.2V.

PRODUCT HIGHLIGHTS

1. Total harmonic distortion is 100% tested.
2. MSB trim feature allows superlinear operation.
3. The AD1856 operates with ±5V to ±12V supplies.
4. Serial interface is compatible with digital filter chips.
5. 1.5μs settling time permits 2×, 4× and 8× oversampling.
6. No external components are required.
7. 96dB dynamic range.
8. ±3V or ±1mA output capability.
9. 16-bit resolution.
10. 2s complement serial input words.
11. Low cost.
12. 16-pin plastic DIP or SOIC package.

REV. B

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AD1856—SPECIFICATIONS (typical at T_A = +25°C and ±5V supplies unless otherwise noted)

		Min	Typ	Max	Units
RESOLUTION				**16**	Bits
DIGITAL INPUTS	V_{IH}	2.4		V_L	V
	V_{IL}	0		0.8	V
	I_{IH}, $V_{IH} = V_L$			**1.0**	μA
	I_{IL}, $V_{IL} = 0.4$			**−10**	μA
Clock Input Frequency		**10**			MHz
ACCURACY					
Gain Error			±2.0		%
Bipolar Zero Error			±30		mV
Differential Linearity Error			±0.001		% of FSR
Noise (rms, 20Hz to 20kHz) @ Bipolar Zero			6		μV
TOTAL HARMONIC DISTORTION					
0dB, 990.5Hz	AD1856N-K, R-K		0.002	**0.0025**	%
	AD1856N-J, R-J		0.002	**0.004**	%
	AD1856N, R		0.002	**0.008**	%
−20dB, 990.5Hz	AD1856N-K, R-K		0.018	**0.020**	%
	AD1856N-J, R-J		0.018	**0.040**	%
	AD1856N, R		0.018	**0.040**	%
−60dB, 990.5Hz	AD1856N-K, R-K		1.8	**2.0**	%
	AD1856N-J, R-J		1.8	**4.0**	%
	AD1856N, R		1.8	**4.0**	%
MONOTONICITY			15		Bits
DRIFT (0 to +70°C)					
Total Drift			±25		ppm of FSR/°C
Bipolar Zero Drift			±4		ppm of FSR/°C
SETTLING TIME (to ±0.006% of FSR)					
Voltage Output	6V Step		1.5		μs
	1LSB Step		1.0		μs
	Slew Rate		9		V/μs
Current Output	1mA Step 10Ω to 100Ω Load		350		ns
	1kΩ Load		350		ns
WARM-UP TIME		1			min
OUTPUT					
Voltage Output Configuration					
Bipolar Range			±3		V
Output Current		±8			mA
Output Impedance			0.1		Ω
Short Circuit Duration			Indefinite to Common		
Current Output Configuration					
Bipolar Range (±30%)			1.0		mA
Output Impedance (±30%)			1.7		kΩ
POWER SUPPLY					
Voltage, $+V_L$ and $+V_S$		4.75	5	13.2	V
Voltage, $-V_L$ and $-V_S$		−13.2	−5	−4.75	V
Current, +I, V_L and V_S = +5V, 10MHz Clock			10	**15**	mA
Current, −I, $-V_L$ and $-V_S$ = −5V, 10MHz Clock			−12	**−15**	mA
Current, +I, V_L and V_S = +12V, 10MHz Clock			12		mA
Current, −I, $-V_L$ and $-V_S$ = −12V, 10MHz Clock			−15		mA
POWER DISSIPATION					
V_S and V_L = ±5V, 10MHz Clock			110	**150**	mW
V_S and V_L = ±12V, 10MHz Clock			135		mW
TEMPERATURE RANGE					
Specification		0		+70	°C
Operation		−25		+70	°C
Storage		−60		+100	°C

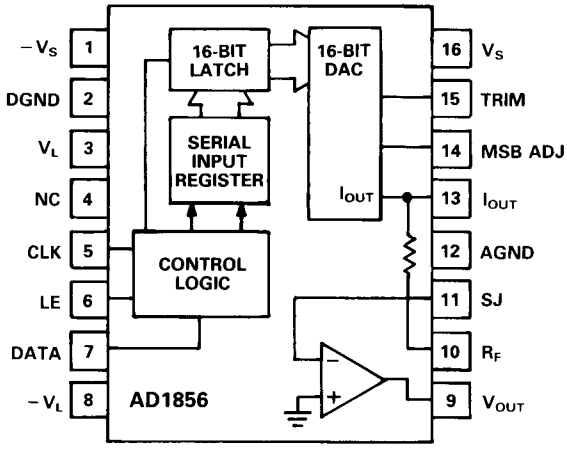
Specifications subject to change without notice.
Specifications shown in **boldface** are tested on all production units at final test.

ABSOLUTE MAXIMUM RATINGS*

V_L to DGND . . . . . 0 to 13.2V
V_S to AGND . . . . . 0 to 13.2V
$-V_L$ to DGND. . . . . -13.2 to 0V
$-V_S$ to AGND . . . . . -13.2 to 0V
Digital Inputs to DGND . . . . . -0.3 to V_L
AGND to DGND . . . . . ± 0.3V
Short Circuit Protection . . . . . Indefinite Short to Ground
Soldering . . . . . +300°C, 10sec
Storage Temperature . . . . . −60°C to +100°C

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CONNECTION DIAGRAM



PIN DESIGNATIONS

Pin	Function	Description
1	$-V_S$	Analog Negative Power Supply
2	DGND	Digital Ground
3	V_L	Logic Positive Power Supply
4	NC	No Connection
5	CLK	Data Clock Input
6	LE	Latch Enable Input
7	DATA	Serial Data Input
8	$-V_L$	Logic Negative Power Supply
9	V_{OUT}	Voltage Output
10	R_F	Feedback Resistor
11	SJ	Summing Junction
12	AGND	Analog Ground
13	I_{OUT}	Current Output
14	MSB ADJ	MSB Adjustment Terminal
15	TRIM	MSB Trimming Potentiometer Terminal
16	V_S	Analog Positive Power Supply

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.

Definition of Specifications

TOTAL HARMONIC DISTORTION

Total Harmonic Distortion (THD) is defined as the ratio of the square root of the sum of the squares of the values of the harmonics to the value of the fundamental input frequency. It is expressed in percent (%) or decibels (dB).

THD is a measure of the magnitude and distribution of linearity error and differential linearity error. The distribution of these errors may be different, depending on the amplitude of the output signal. Therefore, to be most useful, THD should be specified for both large and small signal amplitudes.

SETTLING TIME

Settling Time is the time required for the output to reach and remain within a specified error band about its final value, measured from the digital input transition. It is the primary measure of dynamic performance.

DYNAMIC RANGE

Dynamic Range is the specification that indicates the ratio of the smallest signal the converter can resolve to the largest signal it is able to produce. As a ratio, it is usually expressed in decibels (dB). The theoretical dynamic range of an n-bit converter is approximately (6×n) dB. In the case of the 16-bit AD1856, that is 96dB. The actual dynamic range of a converter is less than the theoretical value due to limitations imposed by noise and quantization and other errors.

BIPOLAR ZERO ERROR

Bipolar Zero Error is the deviation in the actual analog output from the ideal output (0V) when the 2s complement input code representing half scale (all 0s) is loaded in the input register.

DIFFERENTIAL LINEARITY ERROR

Differential Linearity Error is the measure of the variation in analog value, normalized to full scale, associated with a 1LSB change in the digital input. Monotonic behavior requires that the differential linearity error not exceed 1LSB in the negative direction.

MONOTONICITY

A D/A converter is monotonic if the output either increases or remains constant as the digital input increases.

FUNCTIONAL DESCRIPTION

The AD1856 is a complete, monolithic 16-bit PCM audio DAC. No additional external components are required for operation. As shown in the block diagram, each chip contains a voltage reference, an output amplifier, a 16-bit DAC, a 16-bit input latch and a 16-bit serial-to-parallel input register.

The voltage reference consists of a bandgap circuit and buffer amplifier. This circuitry produces an output voltage that is stable over time and temperature changes.

The 16-bit D/A converter uses a combination of segmented decoder and R-2R architectures to achieve consistent linearity and differential linearity. The resistors which form the ladder structure are fabricated with silicon-chromium thin film. Laser trimming of these resistors further reduces linearity error resulting in low output distortion.

The output amplifier uses both MOS and bipolar devices to produce low offset, high slew-rate and optimum settling time. When combined with the on-board feedback resistor, the output op amp can convert the output current of the AD1856 to a voltage output.

ANALOG CIRCUIT CONSIDERATIONS

GROUNDING RECOMMENDATIONS

The AD1856 has two ground pins, designated ANALOG and DIGITAL ground. The analog ground pin is the "high quality" ground reference point for the device. The analog ground pin should be connected to the analog common point in the system. The output load should also be connected to that same point.

The digital ground pin returns ground current from the digital logic portions of the AD1856 circuitry. This pin should be connected to the digital common point in the system.

As illustrated in Figure 1, the analog and digital grounds should be connected together at one point in the system.

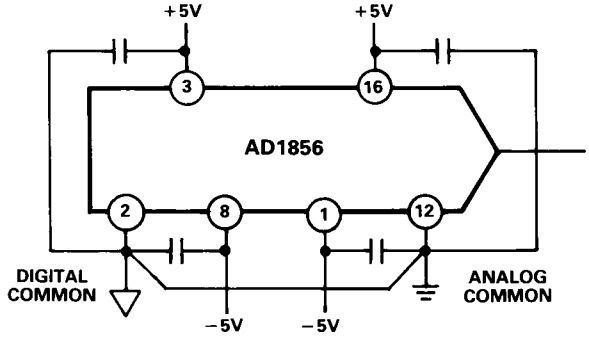


Figure 1. Recommended Circuit Schematic

POWER SUPPLIES AND DECOUPLING

The AD1856 has four power supply input pins. $\pm V_S$ provide the supply voltages to operate the linear portions of the DAC including the voltage reference, output amplifier and control amplifier. The $\pm V_S$ supplies are designed to operate from $\pm 5V$ to $\pm 12V$.

The $\pm V_L$ supplies operate the digital portions of the chip including the input shift register and the input latching circuitry. The $\pm V_L$ supplies are also designed to operate from $\pm 5V$ to $\pm 12V$ subject only to the limitation that $-V_L$ may not be more negative than $-V_S$.

Decoupling capacitors should be used on all power supply pins. Furthermore, good engineering practice suggests that these capacitors be placed as close as possible to the package pins as well as the common points. The logic supplies, $\pm V_L$, should be decoupled to digital common; and the analog supplies, $\pm V_S$, should be decoupled to analog common.

The use of four separate power supplies will reduce feedthrough from the digital portion of the system to the linear portions of the system, thus contributing to good performance. However,

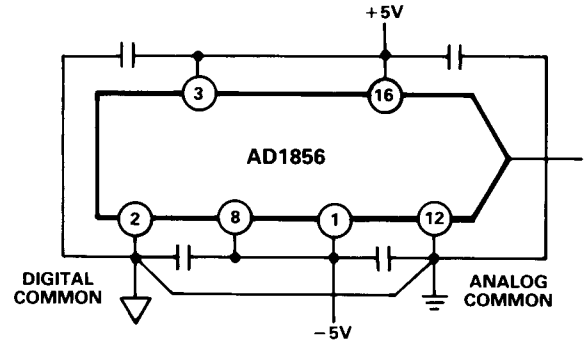


Figure 2. Alternate Recommended Schematic

four separate voltage supplies are not necessary for good circuit performance. For example, Figure 2 illustrates a system where only a single positive and a single negative supply are available. Given that these two supplies are within the range of $\pm 5V$ to $\pm 12V$, they may be used to power the AD1856. In this case, the positive logic and positive analog supplies may both be connected to the single positive supply. The negative logic and negative analog supplies may both be connected to the single negative supply. Performance would benefit from a measure of isolation between the supplies introduced by using simple low-pass filters in the individual power supply leads.

As with most linear circuits, changes in the power supplies will affect the output of the DAC. Analog Devices recommends that well regulated power supplies with less than 1% ripple be incorporated into the design of any system using these devices.

TOTAL HARMONIC DISTORTION

The THD figure of an audio DAC represents the amount of undesirable signal produced during reconstruction and playback of an audio waveform. The THD specification, therefore, provides a direct method to classify and choose an audio DAC for a desired level of performance.

Analog Devices tests and grades all AD1856s on the basis of THD performance. A block diagram of the test setup is shown in Figure 3. In this test setup, a digital data stream, representing a 0db, $-20dB$ or $-60dB$ sine wave is sent to the device under test. The frequency of this waveform is 990.5Hz. Input data is sent to the AD1856 at a $4\times F_S$ rate (176.4kHz). The AD1856 under test produces an analog output signal with the on-board op amp.

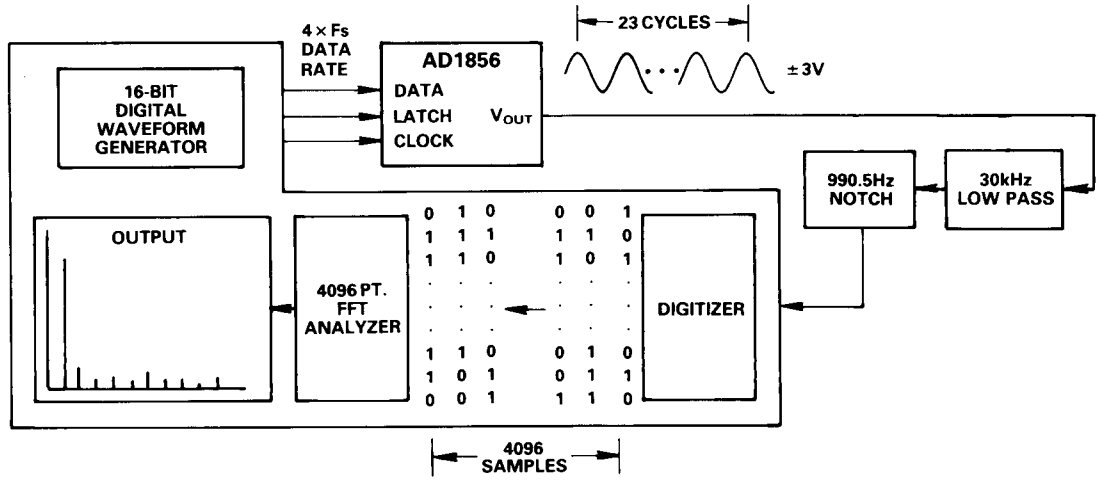


Figure 3. Block Diagram of Distortion Test Circuit

The automatic test equipment digitizes 4096 samples of the output test waveform, incorporating 23 complete cycles of the sine wave. A 4096 point FFT is performed on the results of the test. Based on the first 9 harmonics of the fundamental 990.5Hz output wave, the total harmonic distortion of the device is calculated. Neither a deglitcher nor an MSB trim is used during the THD test.

The circuit design, layout and manufacturing techniques employed in the production of the AD1856 result in excellent THD performance. Figure 4 shows the typical unadjusted THD performance of the AD1856 for various amplitudes of a 1kHz output signal. As can be seen, the AD1856 offers excellent performance, even at amplitudes as low as −60dB. Figure 5 illustrates the typical THD vs. frequency performance.

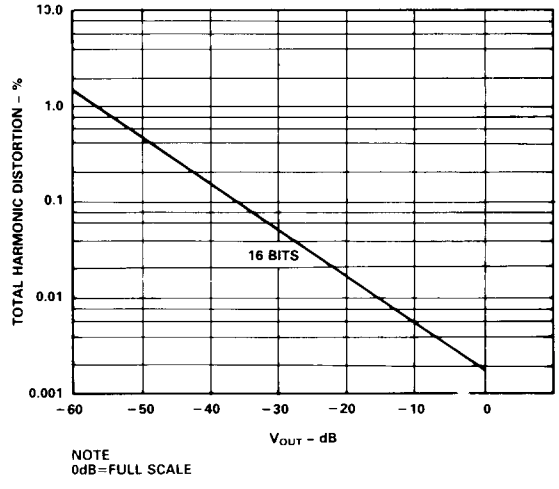


Figure 4. Typical Unadjusted THD vs. Amplitude

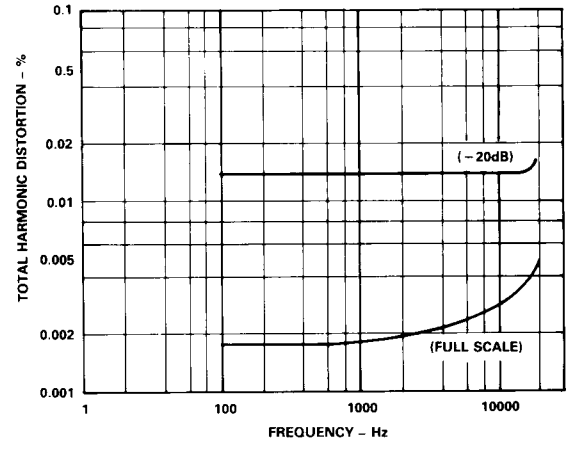


Figure 5. Typical THD vs. Frequency

OPTIONAL MSB ADJUSTMENT

Use of an optional adjustment circuit allows residual differential linearity errors around midscale to be eliminated. These errors are especially important when low amplitude signals are being reproduced. In those cases, as the signal amplitude decreases, the ratio of the midscale differential linearity error to the signal amplitude increases and THD increases.

Therefore, for best performance at low output levels, the optional MSB adjust circuitry shown in Figure 6 may be used. This circuit allows the differential linearity error at midscale to be zeroed out. However, no adjustments are required to meet data sheet specifications.

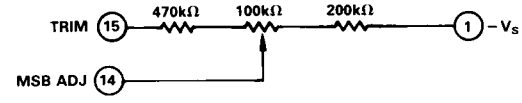


Figure 6. Optional THD Adjust Circuit

DIGITAL CIRCUIT CONSIDERATIONS

Input Data

Data is transmitted to the AD1856 in a bit stream composed of 16-bit words with a serial, MSB first format. Three signals must be present to achieve proper operation: the Data, Clock and Latch Enable signals. Input data bits are clocked into the input register on the rising edge of the Clock signal. The LSB is clocked in on the 16th clock pulse. When all data bits are loaded, a low-going Latch Enable pulse updates the DAC input. Figure 7 illustrates the general signal requirements for data transfer for the AD1856.

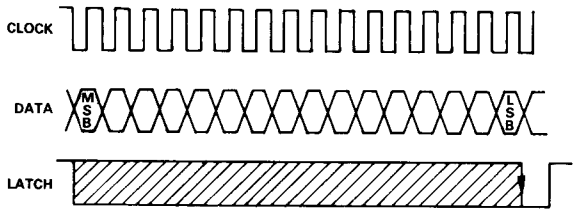


Figure 7. Signal Requirements of AD1856

Figure 8 provides the specific timing requirements that must be met in order for the data transfer to be accomplished properly.

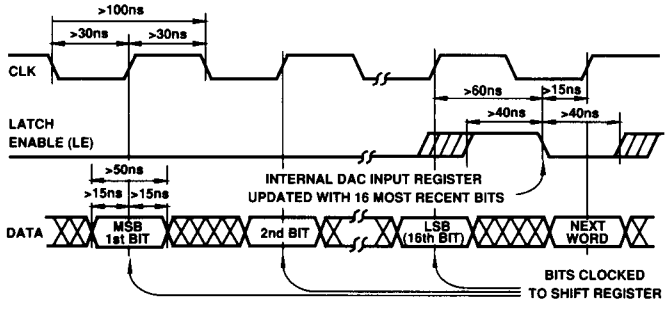


Figure 8. Timing Relationships of Input Signals

The input pins of the AD1856 are both TTL and 5V CMOS compatible, independent of power supply voltages used.

The input requirements illustrated in Figures 7 and 8 are compatible with the data outputs provided by popular DSP filter chips used in digital audio playback systems. The AD1856 input clock can run at a 10MHz rate. This clock rate will allow data transfer rates for 2×, 4× or 8× oversampling reconstruction. The application section of this data sheet contains additional guides for using the AD1856 with various DSP filter chips available from Sony, NPC and Yamaha.

APPLICATIONS OF THE AD1856 PCM AUDIO DAC

The AD1856 is a versatile digital-to-analog converter designed for applications in consumer digital audio equipment. Portable, car and home compact disc player, digital audio-amplifier and DAT systems can all use the AD1856. Various circuit architectures are popular in these systems. They include stereo playback sections featuring one DAC per system, one DAC per audio channel (left/right) or even multiple DACs per channel. Furthermore, these architectures use different output reconstruction rates to accomplish these functions including reproduction at the sample rate F_S (1×), at twice the sample rate (2×F_S), at four times the sample rate (4×F_S) and even at eight times the sample rate (8×F_S). F_S is 44.1kHz for CD and 48kHz for DAT applications.

One DAC per System

Figure 9 shows a circuit using one AD1856 per system to reproduce both stereo channels of a typical first generation digital

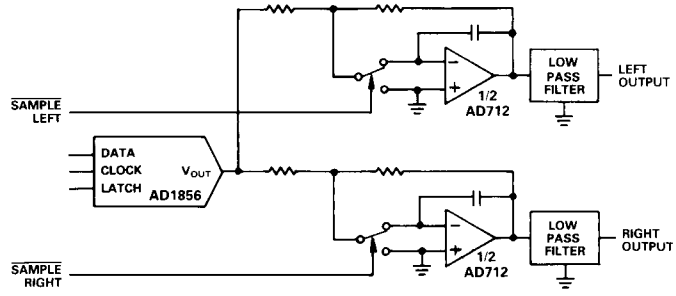


Figure 9. AD1856 in a One DAC per System Architecture

audio system. The input data is fed to the AD1856 in a format which alternates between left channel data and right channel data. The output of the AD1856 is switched between the left channel and right channel output sample/hold amplifiers (SHAs). The SHAs demultiplex and deglitch the output of the AD1856. The timing diagram for the control signals for this circuit is shown in Figure 10.

The architecture illustrated in Figure 9 is suitable for low-end home or portable systems. However, its usefulness in mid- or high-end digital audio reproduction is limited by the phase delay which is introduced in the multiplexed output. This phase delay is due to the fact that the information contained in the input bit stream represents left and right channel audio sampled simultaneously but reconstructed alternately. One obvious solution to this problem may be arrived at by incorporating a third, noninverting SHA to delay the output of one channel to "catch up to" the other channel. This eliminates the phase shift by restoring simultaneous reproduction. This solution is illustrated in Figure 11.

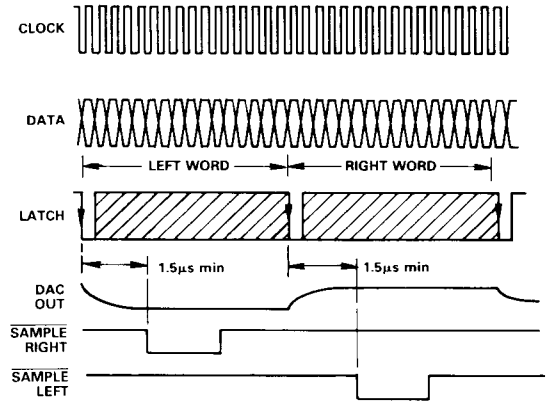


Figure 10. Control Signals for One DAC Circuit

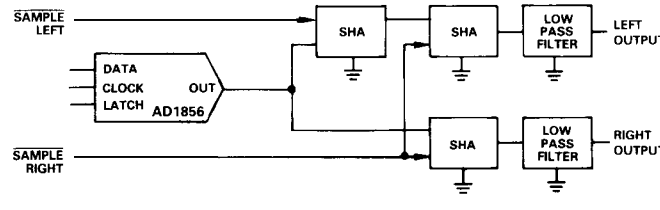


Figure 11. Third SHA Eliminates Phase Delay

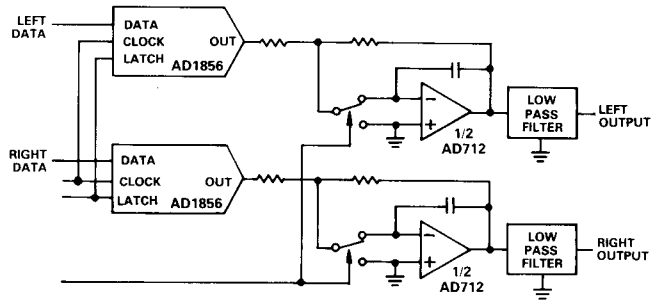


Figure 12. One DAC per Channel Architecture

One DAC per Channel

Another approach used to eliminate phase delay between left and right channels employs one DAC per channel. In this architecture, the input data bit streams for the left channel and the right channel are simultaneously sent and latched into each DAC. This "second generation" approach, shown in Figure 12, is suitable for higher performance digital-audio playback units.

Two DACs per Channel (Four DAC System)

Another architecture uses two DACs per channel. In this scheme, shown in Figure 13, each DAC reproduces one half of the output waveform. The advantage obtained is that midscale differential linearity error no longer effects the zero-crossing points of the waveforms. Its effects are shifted to the points where the output waveform crosses ±3/4 full scale. The result is that THD performance for low amplitude signals is greatly improved. Not shown in Figure 13 is a VLSI circuit required to separate the incoming data into the appropriate form required by each DAC.

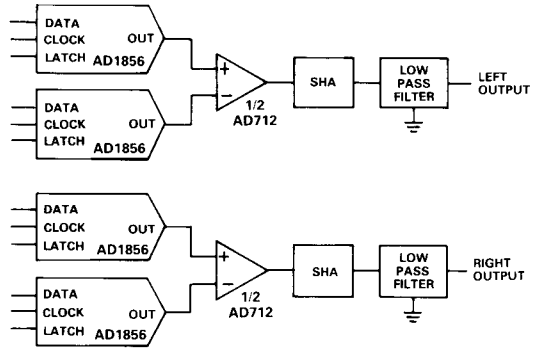


Figure 13. Two DACs per Channel Eliminate Midscale Distortion from the Zero-Crossing Points

DIGITAL FILTERING AND OVERSAMPLING

Oversampling is a term which refers to playback techniques in which the reconstruction frequency used is an integral (2 or more) multiple of the original quantized data rate. For example, in compact disc stereo digital audio playback units, the original quantized data sample rate is 44.1kHz. Popular oversampling rates are 2× or 4× F_S yielding reconstruction rates of 88.2 and 176.4kHz, respectively.

Oversampling is used to ease the performance constraints of the low-pass filters which usually follow the reconstruction DAC. In any signal reconstructed from sampled data, unwanted frequency components are introduced in the output spectrum; these components are centered at the reconstruction frequency.

When a 44.1kHz reconstruction frequency is used, the actual frequency band of interest is 20Hz to 20kHz, and the band of unwanted "image" frequency components extends from 44.1kHz to approximately 24kHz and from 44.1kHz to 64kHz. These unwanted components must be removed with a low-pass filter of very high order. First generation digital audio systems often use low-pass filters of 9, 11 and even 13 poles. Linear implementations of these filters are expensive, difficult to manufacture and can produce distortion due to varying group delay characteristics.

When a 2× reconstruction frequency (88.2kHz) is used, the lowest unwanted frequency components now extend down to approximately 68kHz. A 4× rate (176.4kHz) has unwanted components extending down to approximately 156kHz. The filter response needed to remove these frequency components can now be less steep. This means that a lower order filter may be used resulting in less distortion at lower cost. Linear filters with 3 or 5 poles are adequate to do the job and are quite common in digital audio products employing oversampling techniques.

Oversampling techniques require that the serial input data stream run at the same integral multiple of the original data rate. So, while the constraints on the output low-pass filter are eased, the constraints on the serial digital input port and the settling time of the output stage are not.

The actual oversampling operation takes place in the digital filter chip which is located "upstream" from the DAC. The digital filter accepts data from the media and adds the additional reconstruction points according to the algorithm and coefficients stored in the filter chip. Since the digital filters actually interpolate these additional reconstruction points, they have earned the name "interpolation filters."

The AD1856 is compatible with popular digital filter chips used in digital audio products such as the NPC SM5807, NPC SM5805, Yamaha YM3414, and Sony CXD1136.

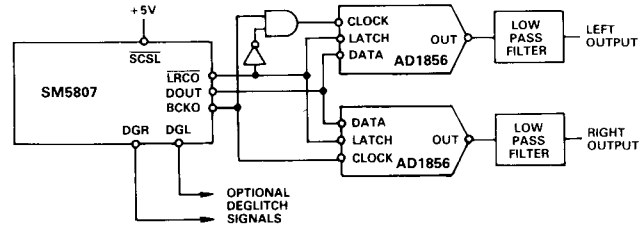


Figure 14. NPC SM5807 and AD1856 Interface

DUAL DAC, 4× F_S OVERSAMPLING ARCHITECTURE

Figure 14 illustrates the use of an NPC digital filter chip with two AD1856 audio DACs. This scheme achieves four times oversampling reconstruction with a dedicated DAC per channel. In this example of a typical compact disc player application, the digital filter chip accepts serial input words from the digital decoder/processor at a 44.1kHz sample rate. Through the use of oversampling, the SM5807 transmits data to the two DACs at a 176.4kHz rate. The serial DAC input data is sent out of the DOUT pin to the serial inputs of the DACs. Left channel and right channel data are sent alternately down the same wire. The Left/Right Channel Output signal, $\overline{LRCO}$ and two logic gates demultiplex the data clock signals from BCKO. In this example,

the BCKO rate is 192×F_S. However, a 196×F_S clock can be used if $\overline{SCSL}$ is wired to a logic zero. Finally, left and right channel deglitching signals are provided. At the user's option, these signals may be used to control external sample-hold amplifiers in order to obtain optimal performance.

ACHIEVING 8× F_S OVERSAMPLING WITH AD1856S AND YAMAHA YM3414

Figure 15 illustrates the combination of a Yamaha YM3414 digital filter chip and two AD1856 audio DACs. In this scheme, the use of a 16.9344MHz clock allows an 8 times oversampling rate for extremely high performance. In addition, a lower-order low-pass filter may be used without sacrificing performance. The DAC input data is simultaneously transmitted to the input registers of the DACs through dedicated left and right channel output pins on the YM3414. As before, optional sample/hold signals are provided.

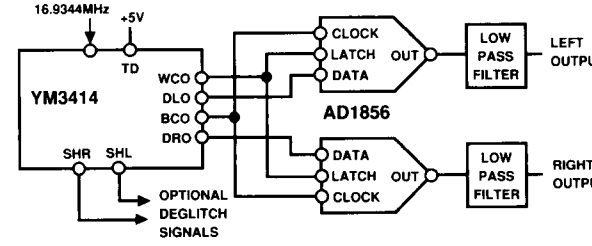


Figure 15. Yamaha YM3414 and AD1856 Interface

C1215c–2.5–1/94

ORDERING GUIDE

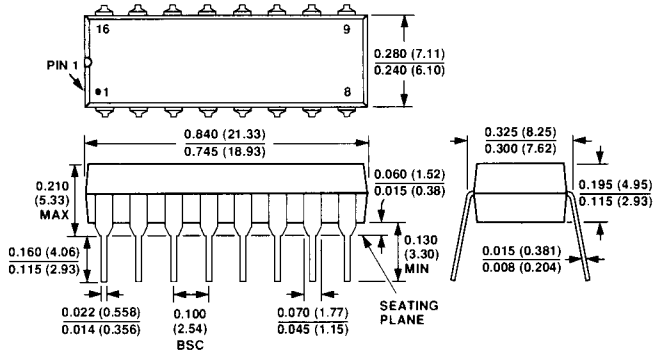
Model	THD @ FS	Package Option*
AD1856N, R	0.008%	N-16, R-16
AD1856N-J, R-J	0.004%	N-16, R-16
AD1856N-K, R-K	0.0025%	N-16, R-16

*N = Plastic DIP; R = Small Outline IC.

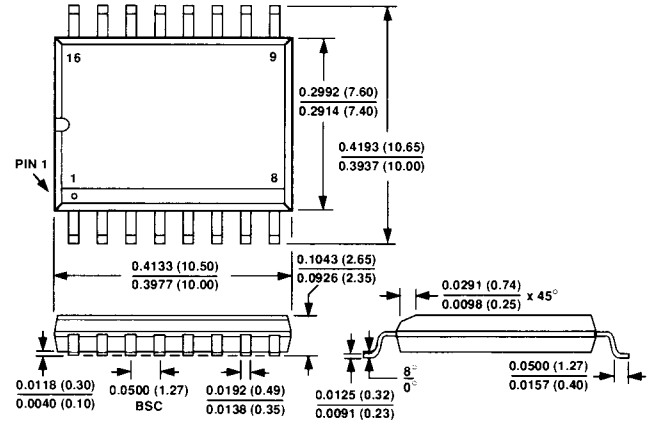
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

16-Pin Plastic DIP (N) Package



16-Pin SOIC (R) Package



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