Development Board EPC9055 Quick Start Guide

Half Bridge with Gate Drive for EPC2106

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EFFICIENT POWER CONVERSION

DESCRIPTION

This development board is in a monolithic half bridge topology with onboard gate drives, featuring the EPC2106 eGaN (Enhancement-mode Gallium Nitride) Integrated Dual FET. The purpose of these development boards is to simplify the evaluation process of these eGaN FETs by including all the critical components on a single board that can be easily connected into any existing converter.

The development board is 2" x 1.5" and contains a dual integrated eGaN FET, in a half bridge configuration using the Texas Instruments LM5113 gate driver, supply and bypass capacitors. The board contains all critical components and layout for optimal switching performance. There are also various probe points to facilitate simple waveform measurement and efficiency calculation. A complete block diagram of the circuit is given in Figure 1.

For more information on the EPC2106 eGaN Integrated Dual FET, please refer to the datasheets available from EPC at www.epc-co.com. The datasheet should be read in conjunction with this quick start guide.

Table 1: Performance Summary (T_A = 25°C)

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNITS
V_{DD}	Gate Drive Input Supply Range		7	12	V
V_{IN}	Bus Input Voltage Range			80	V
V_{OUT}	Switch Node Output Voltage			100	V
I_{OUT}	Switch Node Output Current			3*	A
V_{PWM}	PWM Logic Input Voltage Threshold	Input 'High' Input 'Low'	3.5 0	6 1.5	V V
	Minimum 'High' State Input Pulse Width	V_{PWM} rise and fall time < 10ns	60		ns
	Minimum 'Low' State Input Pulse Width	V_{PWM} rise and fall time < 10ns	100#		ns

*Assumes inductive load, maximum current depends on die temperature – actual maximum current with be subject to switching frequency, bus voltage and thermals cooling.
Limited by time needed to 'refresh' high side bootstrap supply voltage.

QUICK START PROCEDURE

The EPC9055 development board is easy to set up to evaluate the performance of the eGaN-IC monolithic half bridge. The board allows the on-board placement of buck output filter components. Refer to Figure 2 for proper connect and measurement setup and follow the procedure below:

1. With power off, connect the input power supply bus to $+V_{IN}$ (J5, J6) and ground / return to $-V_{IN}$ (J7, J8).
2. With power off, connect the switch node of the half bridge OUT (J3, J4) to your circuit as required.
3. With power off, connect the gate drive input to $+V_{DD}$ (J1, Pin-1) and ground return to $-V_{DD}$ (J1, Pin-2).
4. With power off, connect the input PWM control signal to PWM (J2, Pin-1) and ground return to any of the remaining J2 pins.
5. Turn on the gate drive supply – make sure the supply is between 7 V and 12 V range.
6. Turn on the bus voltage to the required value (do not exceed the absolute maximum voltage on V_{OUT} of 100 V)
7. Turn on the controller / PWM input source and probe switching node to see switching operation.
8. Once operational, adjust the bus voltage and load PWM control within the operating range and observe the output switching behavior, efficiency and other parameters.
9. For shutdown, please follow steps in reverse.

NOTE. When measuring the high frequency content switch node (OUT), care must be taken to avoid long ground leads. Measure the switch node (OUT) by placing the oscilloscope probe tip through the large via on the switch node (designed for this purpose) and grounding the probe directly across the GND terminals provided. See Figure 3 for proper scope probe technique.

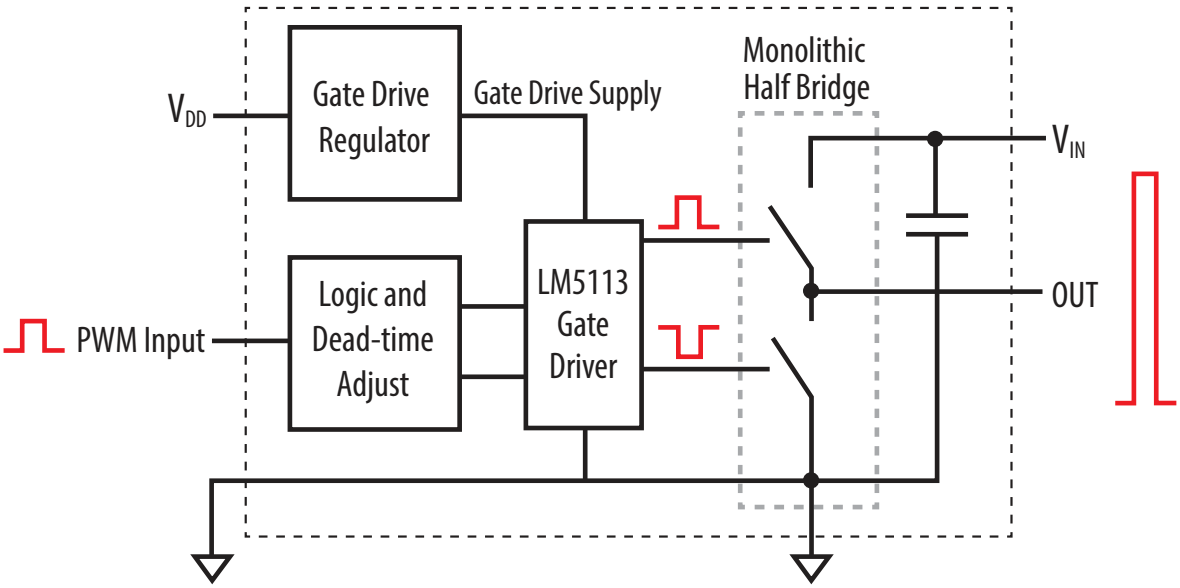

Figure 1: Block Diagram of Development Board

QUICK START PROCEDURE

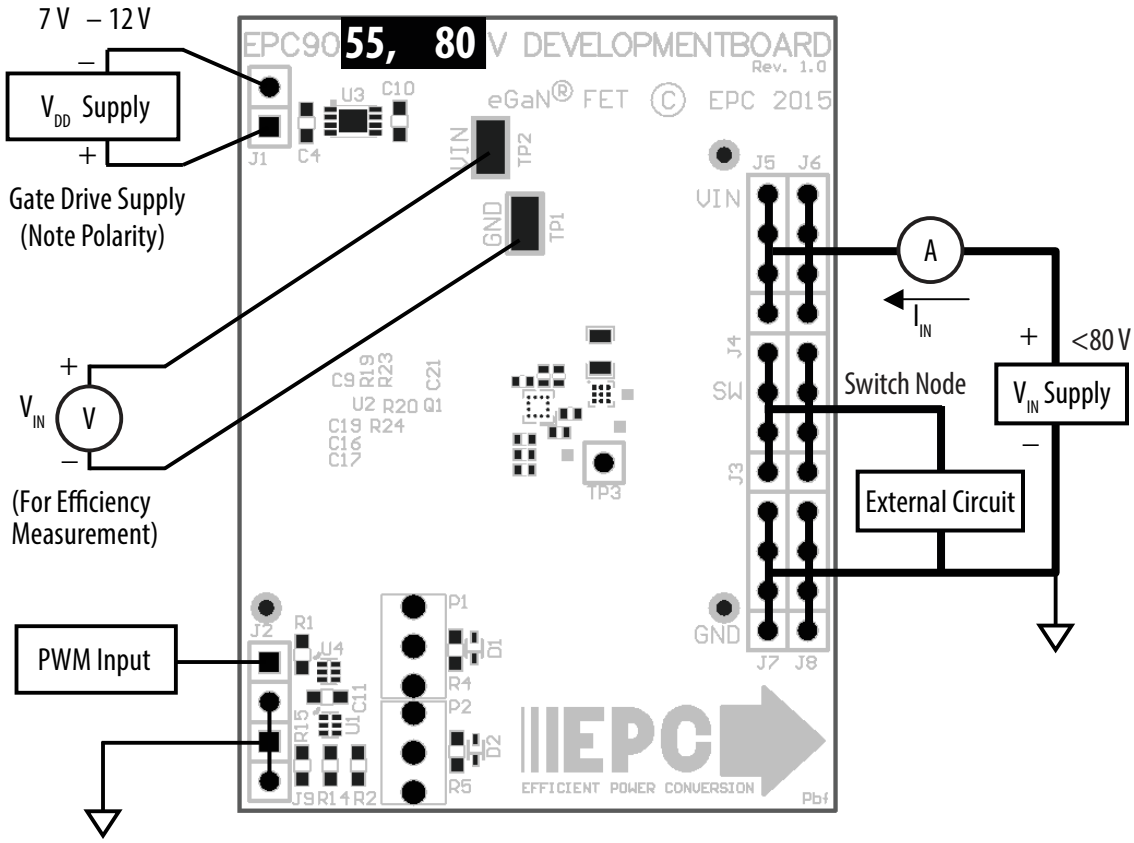

Figure 2: Proper Connection and Measurement Setup

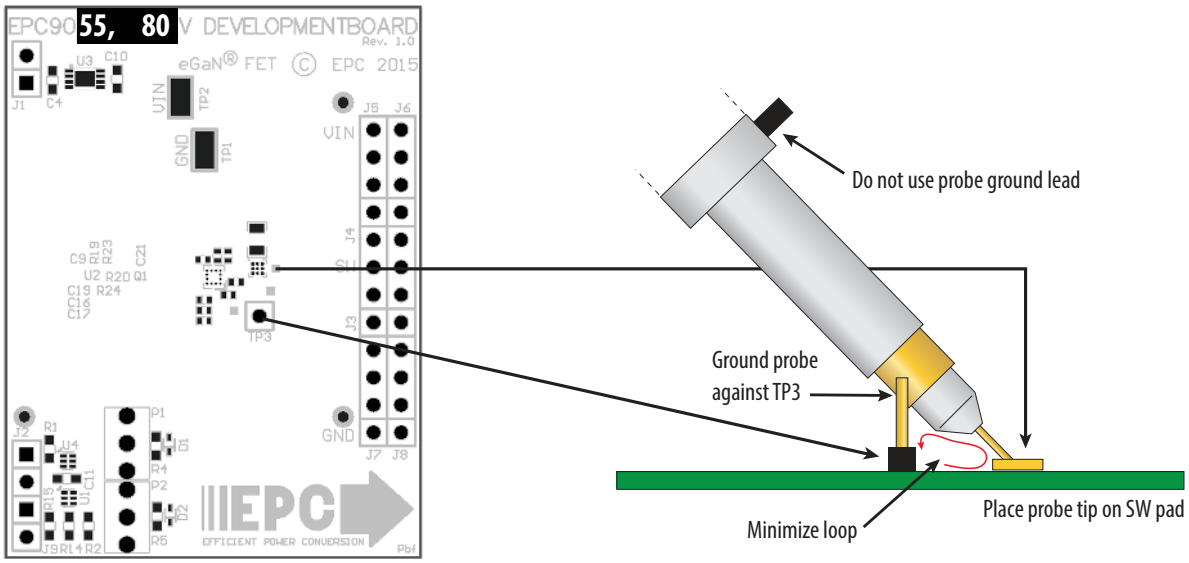

Figure 3: Proper Measurement of Switch Node – OUT

THERMAL PERFORMANCE

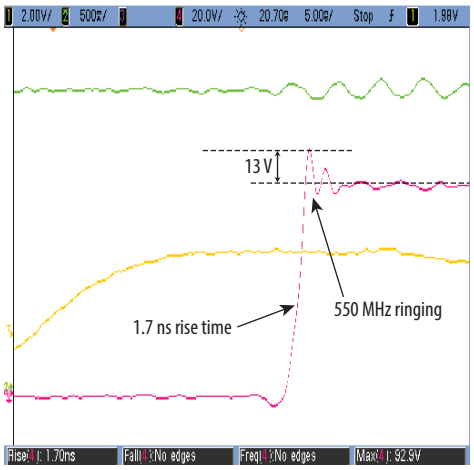

Figure 4 (a) – Rising Edge

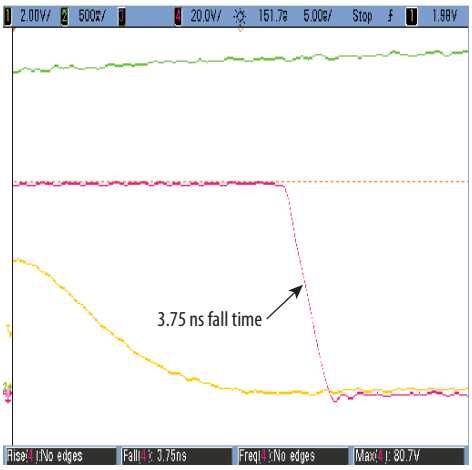

Figure 4 (b) – Falling Edge

Figure 4: Typical Waveforms for EPC9055. V_{IN} = 80 V to 5 V/3 A (500 kHz) Buck converter showing rising and falling edges, CH1: (V_{PWM}) Input logic signal – CH2: (I_{OUT}) Output inductor current – CH4: (V_{OUT}) Switch node voltage

The EPC9055 development boards showcase the EPC2106 eGaN FETs. These development boards are intended for bench evaluation with low ambient temperature and convection cooling. The addition of heat-sinking and forced air cooling can significantly increase the current rating of these devices, but care must be taken to not exceed the absolute maximum die temperature of 150°C.

NOTE. The EPC9055 development boards do not have any current or thermal protection on board.

Table 2: Bill of Materials

Item	Qty	Reference	Part Description	Manufacturer / Part #
1	3	C4, C10, C11,	Capacitor, 1 µF, 10%, 25 V, X5R	Murata, GRM188R61E105KA12D
2	2	C9, C19	Capacitor, 0.1 µF, 10%, 25 V, X5R	TDK, C1005X5R1E104K
3	2	C16, C17	Capacitor, 100 pF, 5%, 50 V, NP0	Kemet, C0402C101K5GACTU
4	1	C21	Capacitor, 1 µF, 10%, 100 V, X7R	TDK, CGA4J3X7S2A105K125AE
5	2	D1, D2	Schottky diode, 30 V	Diodes Inc., SDM03U40-7
6	3	J1, J2, J9	Connector	2pins of Tyco, 4-103185-0
7	1	J3, J4, J5, J6, J7, J8	Connector	FCI, 68602-224HLF
8	1	Q1	eGaN-IC monolithic half bridge	EPC, EPC2106
9	1	R1	Resistor, 10.0 K, 5%, 1/8 W	Stackpole, RMCF0603FT10K0
10	2	R2, R15	Resistor, 0 Ohm, 1/8 W	Stackpole, RMCF0603ZT0R00
11	1	R4	Resistor, 22 Ohm, 1%, 1/8 W	Stackpole, RMCF0603FT22R0
12	1	R5	Resistor, 47 Ohm, 1%, 1/8 W	Stackpole, RMCF0603FT47R0
13	4	R19, R20, R23, R24	Resistor, 1 Ohm, 1/16 W	Stackpole, RMCF0402FT1R00
14	2	TP1, TP2	Test point	Keystone Elect, 5015
15	1	TP3	Connector	1/40th of Tyco, 4-103185-0
16	1	U1	I.C., logic	Fairchild, NC7SZ00L6X
17	1	U2	I.C., gate driver	Texas Instruments, LM5113
18	1	U3	I.C., regulator	Microchip, MCP1703T-5002E/MC
19	1	U4	I.C., logic	Fairchild, NC7SZ08L6X
20	0	R14	Optional resistor	
21	0	D3	Optional diode	
22	0	P1, P2	Optional potentiometer	

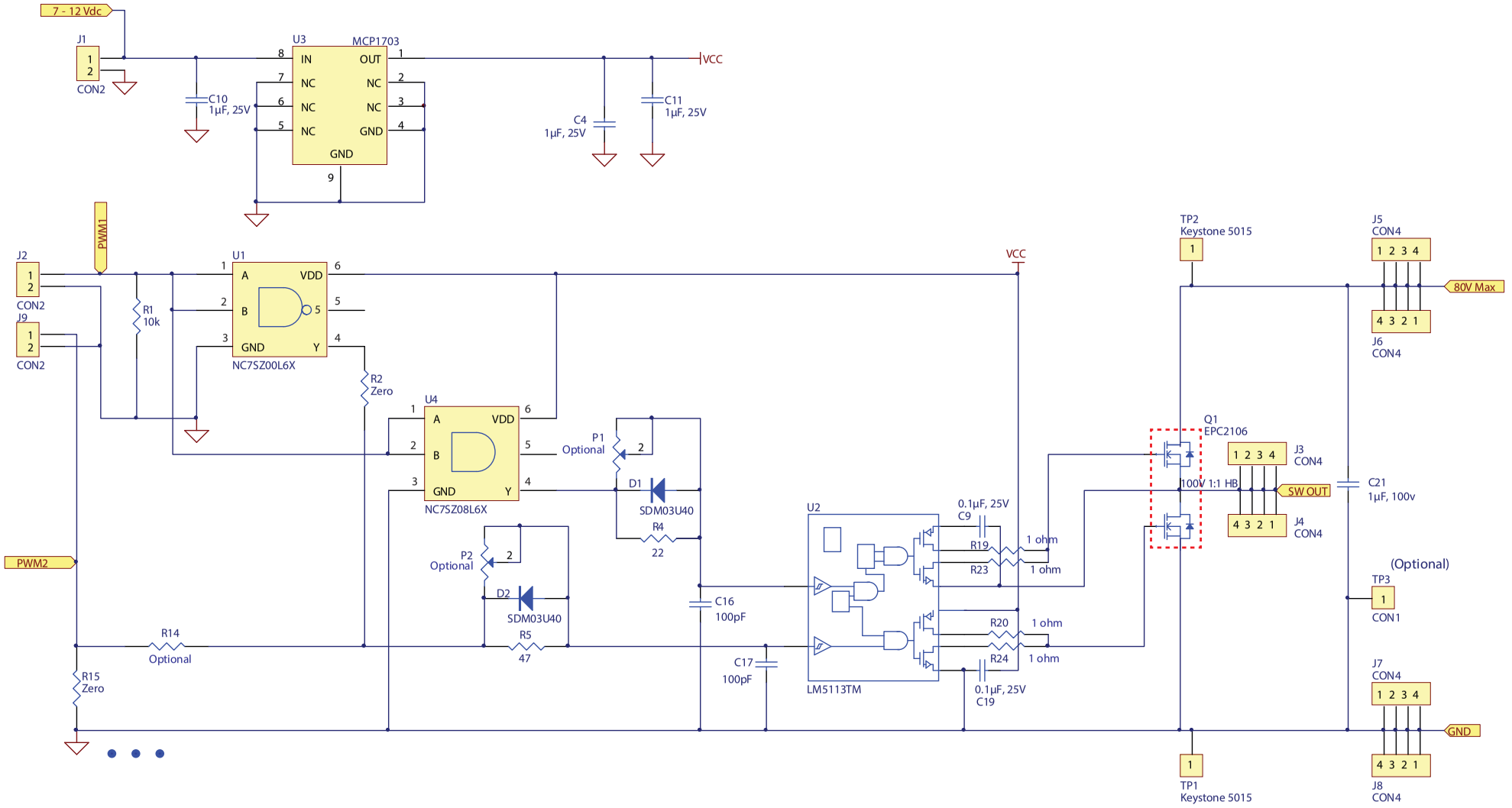

Figure 5: Development Board Schematic