

## 54F/74F657 Octal Bidirectional Transceiver with 8-Bit Parity Generator/Checker and TRI-STATE® Outputs

### General Description

The 'F657 contains eight non-inverting buffers with TRI-STATE® outputs and an 8-bit parity generator/checker. It is intended for bus-oriented applications. The buffers have a guaranteed current sinking capability of 24 mA (20 mA mil) at the A port and 64 mA (48 mA mil) at the B port.

### Features

- 300 Mil 24-pin slimline DIP
- Combines 'F245 and 'F280A functions in one package
- TRI-STATE outputs
- B Outputs sink 64 mA (48 mA mil)
- 12 mA source current, B side
- Input diodes for termination effects

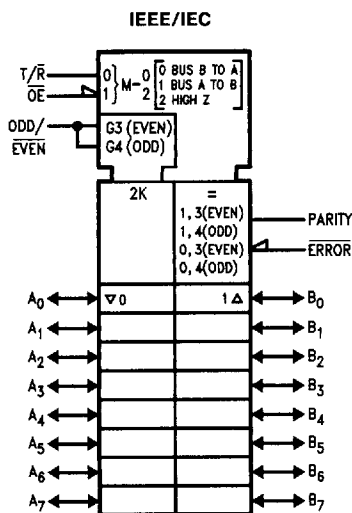
### Ordering Code: See Section 11

Commercial	Military	Package Number	Package Description
74F657SPC		N24C	24-Lead (0.300" Wide) Molded Dual-In-Line
	54F657SDM (Note 2)	J24F	24-Lead (0.300" Wide) Ceramic Dual-In-Line
75F657SC (Note 1)		M24B	24-Lead (0.300" Wide) Molded Small Outline, JEDEC
	54F657FM (Note 2)	W24C	24-Lead Cerpack
	54F657LM (Note 2)	E28A	24-Lead Ceramic Leadless Chip Carrier, Type C

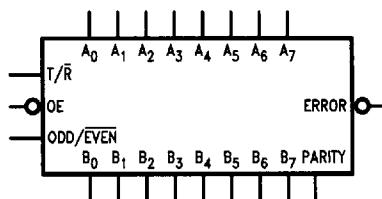
**Note 1:** Devices also available in 13" reel. Use suffix = SCX.

**Note 2:** Military grade device with environmental and burn-in processing. Use suffix = DMQB, FMQB and LMQB.

### Logic Symbols

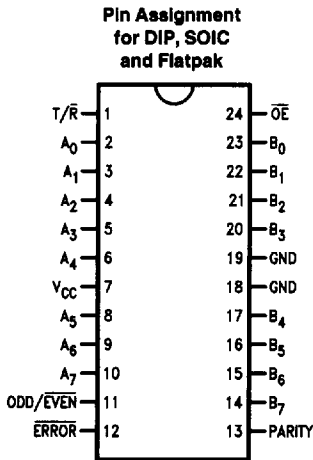


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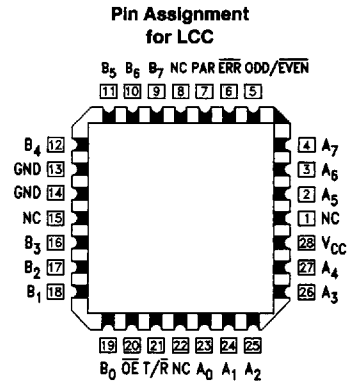


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## Connection Diagrams



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TL/F/9584-3

**Unit Loading/Fan Out:** See Section 2 for U.L. definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input I <sub>H</sub> /I <sub>L</sub> Output I <sub>OH</sub> /I <sub>OL</sub>
A <sub>0</sub> -A <sub>7</sub>	Data Inputs/ TRI-STATE Outputs	4.5/0.15 150/40 (33.3)	90 $\mu$ A / - 90 $\mu$ A -3 mA/24 mA (20 mA)
B <sub>0</sub> -B <sub>7</sub>	Data Inputs/ TRI-STATE Outputs	3.5/0.117 600/106.6 (80)	70 $\mu$ A / - 70 $\mu$ A -12 mA/64 mA (48 mA)
T/ $\bar{R}$	Transmit/Receive Input	2.0/0.067	40 $\mu$ A / - 40 $\mu$ A
$\bar{O}E$	Enable Input	2.0/0.067	40 $\mu$ A / - 40 $\mu$ A
PARITY	Parity Input/ TRI-STATE Output	3.5/0.117 600/106.6 (80)	70 $\mu$ A / - 70 $\mu$ A -12 mA/64 mA (48 mA)
ODD/ $\bar{E}VEN$	ODD/ $\bar{E}VEN$ Parity Input	1.0/0.033	20 $\mu$ A / - 20 $\mu$ A
ERROR	Error Output	600/106.6 (80)	-12 mA/64 mA (48 mA)

## Functional Description

The Transmit/Receive (T/ $\bar{R}$ ) input determines the direction of the data flow through the bidirectional transceivers. Transmit (active HIGH) enables data from the A port to the B port; Receive (active LOW) enables data from the B port to the A port.

The Output Enable ( $\bar{O}E$ ) input disables the parity and ERROR outputs and both the A and B ports by placing them in a HIGH-Z condition when the Output Enable input is HIGH.

When transmitting (T/ $\bar{R}$  HIGH), the parity generator detects whether an even or odd number of bits on the A port are HIGH and compares these with the condition of the pari-

ty select (ODD/ $\bar{E}VEN$ ). If the Parity Select is HIGH and an even number of A inputs are HIGH, the Parity output is HIGH.

In receiving mode (T/ $\bar{R}$  LOW), the parity select and number of HIGH inputs on port B are compared to the condition of the Parity input. If an even number of bits on the B port are HIGH, the parity select is HIGH, and the PARITY input is HIGH, then ERROR will be HIGH to indicate no error. If an odd number of bits on the B port are HIGH, the parity select is HIGH, and the PARITY input is HIGH, the ERROR will be LOW indicating an error.

Function Table

Number of Inputs That Are High	Inputs			Input/Output	Outputs	
	OE	T/R	ODD/EVEN	Parity	ERROR	Outputs Mode
0, 2, 4, 6, 8	L	H	H	H	Z	Transmit
	L	H	L	L	Z	Transmit
	L	L	H	H	H	Receive
	L	L	H	L	L	Receive
	L	L	L	H	L	Receive
	L	L	L	L	H	Receive
1, 3, 5, 7	L	H	H	L	Z	Transmit
	L	H	L	H	Z	Transmit
	L	L	H	H	L	Receive
	L	L	H	L	H	Receive
	L	L	L	H	H	Receive
	L	L	L	L	L	Receive
Immaterial	H	X	X	Z	Z	Z

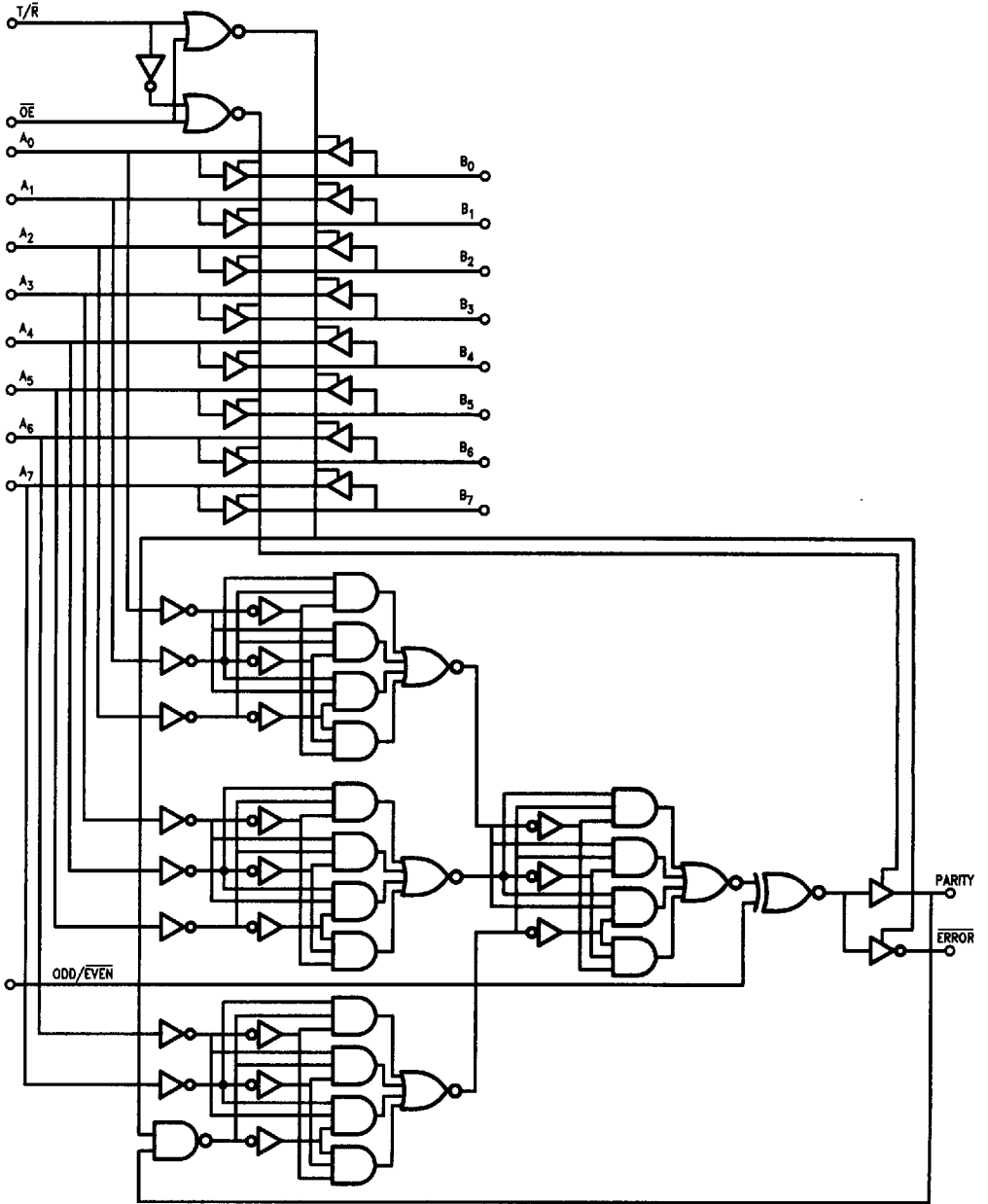
H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Immaterial  
Z = High Impedance

Function Table

Inputs		Outputs
OE	T/R	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	High-Z State

H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Immaterial

### Functional Block Diagram



2 GROUND PINS  
1 V<sub>CC</sub> PIN

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## Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +175°C
Plastic	-55°C to +150°C
V <sub>CC</sub> Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	
Standard Output	-0.5V to V <sub>CC</sub>
TRI-STATE Output	-0.5V to +5.5V

Current Applied to Output in LOW State (Max)

twice the rated I<sub>OL</sub> (mA)

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

## Recommended Operating Conditions

Free Air Ambient Temperature	
Military	-55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

## DC Electrical Characteristics

Symbol	Parameter		54F/74F			Units	V <sub>CC</sub>	Conditions
			Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage					V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage					V	Min	I <sub>IN</sub> = -18 mA
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub> 54F 10% V <sub>CC</sub> 54F 10% V <sub>CC</sub> 74F 10% V <sub>CC</sub> 74F 10% V <sub>CC</sub> 74F 10% V <sub>CC</sub> 74F 5% V <sub>CC</sub> 74F 5% V <sub>CC</sub>	2.5 2.4 2.0 2.5 2.4 2.0 2.7 2.7			V	Min	I <sub>OH</sub> = -1 mA (A <sub>n</sub> ) I <sub>OH</sub> = -3 mA (A <sub>n</sub> , B <sub>n</sub> , Parity, ERROR) I <sub>OH</sub> = -12 mA (B <sub>n</sub> , Parity, ERROR) I <sub>OH</sub> = -1 mA (A <sub>n</sub> ) I <sub>OH</sub> = -3 mA (A <sub>n</sub> , B <sub>n</sub> , Parity, ERROR) I <sub>OH</sub> = -15 mA (B <sub>n</sub> , Parity, ERROR) I <sub>OH</sub> = -1 mA (A <sub>n</sub> ) I <sub>OH</sub> = -3 mA (A <sub>n</sub> , B <sub>n</sub> , Parity, ERROR)
V <sub>OL</sub>	Output LOW Voltage	54F 10% V <sub>CC</sub> 54F 10% V <sub>CC</sub> 74F 10% V <sub>CC</sub> 74F 10% V <sub>CC</sub>		0.5 0.55 0.5 0.55		V	Min	I <sub>OL</sub> = 20 mA (A <sub>n</sub> ) I <sub>OL</sub> = 48 mA (B <sub>n</sub> , Parity, ERROR) I <sub>OL</sub> = 24 mA (A <sub>n</sub> ) I <sub>OL</sub> = 64 mA (B <sub>n</sub> , Parity, ERROR)
I <sub>IH</sub>	Input HIGH Current		20 40			μA	Max	V <sub>IN</sub> = 2.7V (ODD/EVEN) V <sub>IN</sub> = 2.7V (T/R, OE)
I <sub>BVI</sub>	Input HIGH Current Breakdown Test		100			μA	V <sub>CC</sub> = 0	V <sub>IN</sub> = 7.0V (T/R, OE, ODD/EVEN)
I <sub>BVIT</sub>	Input HIGH Current Breakdown Test (I/O)		1.0 2.0			mA	Max	V <sub>IN</sub> = 5.5V (Parity, B <sub>n</sub> ) V <sub>IN</sub> = 5.5V (A <sub>n</sub> )
I <sub>IL</sub>	Input LOW Current		-20 -40			μA	Max	V <sub>IN</sub> = 0.5V (ODD/EVEN) V <sub>IN</sub> = 0.5V (T/R, OE)
I <sub>OZH</sub>	Output Leakage Current		50			μA	Max	V <sub>OUT</sub> = 2.7V (ERROR)
I <sub>OZL</sub>	Output Leakage Current		-50			μA	Max	V <sub>OUT</sub> = 0.5V (ERROR)
I <sub>IH</sub> + I <sub>OZH</sub>	Output Leakage Current		70 90			μA	Max	V <sub>I/O</sub> = 2.7V (B <sub>n</sub> , Parity) V <sub>I/O</sub> = 2.7V (A <sub>n</sub> )
I <sub>IL</sub> + I <sub>OZL</sub>	Output Leakage Current		-70 -90			μA	Max	V <sub>I/O</sub> = 0.5V (B <sub>n</sub> , Parity) V <sub>I/O</sub> = 0.5V (A <sub>n</sub> )
I <sub>OS</sub>	Output Short-Circuit Current		-60 -100	-150 -225		mA	Max	V <sub>OUT</sub> = 0V (A <sub>n</sub> ) V <sub>OUT</sub> = 0V (B <sub>n</sub> , Parity, ERROR)
I <sub>CEX</sub>	Output HIGH Leakage Current		250 1.0 2.0			μA mA mA	Max Max Max	V <sub>OUT</sub> = V <sub>CC</sub> (ERROR) V <sub>OUT</sub> = V <sub>CC</sub> (B <sub>n</sub> , Parity) V <sub>OUT</sub> = V <sub>CC</sub> (A <sub>n</sub> )
I <sub>ZZ</sub>	Bus Drainage Test		500			μA	0.0V	V <sub>OUT</sub> = 5.25V (A <sub>n</sub> , B <sub>n</sub> , Parity, ERROR)
I <sub>COH</sub>	Power Supply Current		101 125			mA	Max	V <sub>O</sub> = HIGH
I <sub>COL</sub>	Power Supply Current		112 150			mA	Max	V <sub>O</sub> = LOW
I <sub>CCZ</sub>	Power Supply Current		109 145			mA	Max	V <sub>O</sub> = HIGH Z

## AC Electrical Characteristics: See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F			54F		74F		Units	Fig. No.
		T <sub>A</sub> = +25°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 50 pF			T <sub>A</sub> , V <sub>CC</sub> = Mil C <sub>L</sub> = 50 pF		T <sub>A</sub> , V <sub>CC</sub> = Com C <sub>L</sub> = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
t <sub>PLH</sub>	Propagation Delay	2.5	4.5	8.0	2.5	9.5	2.5	9.0	ns	2-3
t <sub>PHL</sub>	A <sub>n</sub> to B <sub>n</sub> , B <sub>n</sub> to A <sub>n</sub>	3.0	4.9	7.5	3.0	8.5	3.0	8.0		
t <sub>PLH</sub>	Propagation Delay	6.5	10.1	14.0	5.5	18.0	6.0	16.0	ns	2-3
t <sub>PHL</sub>	A <sub>n</sub> to PARITY	7.0	10.9	15.0	5.5	20.5	6.0	16.5		
t <sub>PLH</sub>	Propagation Delay	4.5	7.8	11.0	4.0	14.0	4.0	13.0	ns	2-3
t <sub>PHL</sub>	ODD/EVEN to PARITY	4.5	8.8	12.0	4.5	16.5	4.5	13.5		
t <sub>PLH</sub>	Propagation Delay	4.5	7.5	11.0	4.0	14.0	4.0	13.0	ns	2-3
t <sub>PHL</sub>	ODD/EVEN to ERROR	4.5	8.2	12.0	4.5	16.5	4.5	13.5		
t <sub>PLH</sub>	Propagation Delay	8.0	14.0	20.5	7.5	27.0	7.5	23.0	ns	2-3
t <sub>PHL</sub>	B <sub>n</sub> to ERROR	8.0	15.0	21.5	7.5	28.5	7.5	23.5		
t <sub>PLH</sub>	Propagation Delay	7.0	10.8	15.5	6.0	20.0	6.0	17.0	ns	2-3
t <sub>PHL</sub>	PARITY to ERROR	7.5	11.8	16.5	6.5	22.0	7.5	18.5		
t <sub>PZH</sub>	Output Enable Time	3.0	5.0	8.0	2.5	11.0	2.5	9.5	ns	2-5
t <sub>PZL</sub>	$\overline{OE}$ to A <sub>n</sub> /B <sub>n</sub>	4.0	6.5	10.0	3.5	13.5	3.5	11.0		
t <sub>PHZ</sub>	Output Disable Time	1.0	4.5	8.0	1.0	9.5	1.0	9.0	ns	2-5
t <sub>PLZ</sub>	$\overline{OE}$ to A <sub>n</sub> /B <sub>n</sub>	1.0	4.9	7.5	1.0	8.5	1.0	8.0		
t <sub>PZH</sub>	Output Enable Time	3.0	5.0	8.0	2.5	11.0	2.5	9.5	ns	2-5
t <sub>PZL</sub>	$\overline{OE}$ to ERROR (Note 1)	4.0	7.7	10.0	3.5	13.5	3.5	11.0		
t <sub>PHZ</sub>	Output Disable Time	1.0	4.5	8.0	1.0	9.5	1.0	9.0	ns	2-5
t <sub>PLZ</sub>	$\overline{OE}$ to ERROR	1.0	4.9	7.5	1.0	8.5	1.0	8.0		
t <sub>PZH</sub>	Output Enable Time	3.0	5.0	8.0	2.5	11.0	2.5	9.5	ns	2-5
t <sub>PZL</sub>	$\overline{OE}$ to PARITY	4.0	7.7	10.0	3.5	13.5	3.5	11.0		
t <sub>PHZ</sub>	Output Disable Time	1.0	4.6	8.0	1.0	9.5	1.0	9.0	ns	2-5
t <sub>PLZ</sub>	$\overline{OE}$ to PARITY	1.0	5.1	7.5	1.0	8.5	1.0	8.0		

**Note 1:** These delay times reflect the TRI-STATE recovery time only and not the signal time through the buffers or the parity check circuitry. To assure VALID information at the ERROR pin, time must be allowed for the signal to propagate through the drivers (B to A), through the parity check circuitry (same as A to PARITY), and to the ERROR output after the ERROR pin has been enabled (Output Enable times). VALID data at the ERROR pin  $\geq$  (A to PARITY) + (Output Enable Time).