NCP1603

PFC/PWM Combo Controller with Integrated High Voltage Startup and Standby Capability

The NCP1603 is a Power Factor Correction (PFC) and Pulse Width Modulation (PWM) combo controller. It offers extremely low no−load standby power consumption that is suitable for the low−power consumer markets. The key features of the device are listed below.

Features

- Pb−Free Package is Available*

PFC Features

- Near−Unity Power Factor in Discontinuous and Critical Mode (DCM and CRM)
- Voltage−Mode Operation
- Low Startup and Shutdown Current Consumption
- Programmable Switching Frequency for DCM
- Synchronization Capability
- Overvoltage Protection (107% of Nominal Output Level)
- Undervoltage Protection or Shutdown (8% of Nominal Output Level)
- Programmable Overcurrent Protection
- Thermal Shutdown with Hysteresis (95/140°C)
- Undervoltage Lockout with Hysteresis (9.0/10.5 V)

PWM Features

- Integrated Lossless High Voltage Startup Current Source
- 100 kHz PWM Current−Mode Operation with Skipping Cycle Capability During Standby Condition
- PFC Bias Voltage is Disabled in Standby Condition to Achieve Extremely Low No−Load Standby Power Consumption
- Fault Protection Implemented by a Timer and Independent of Badly Coupled Auxiliary Transformer Winding
- Primary Overcurrent Protection and Latched Overvoltage Protection
- Internal 2.5 ms Soft−Start
- ±6.4% Frequency Jittering for Improved EMI Performance
- Latched Thermal Shutdown with Hysteresis (140/165°C)
- Undervoltage Lockout with Hysteresis (5.6/7.7/12.6 V)

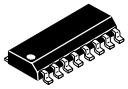
Applications

- Notebook Adapters
- TV/Monitors

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

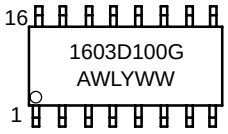
ON Semiconductor®

http://onsemi.com



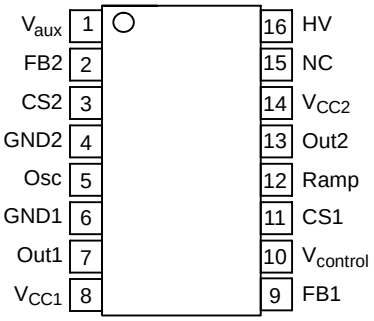
SO−16
D SUFFIX
CASE 751B

MARKING DIAGRAM



A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

PIN CONNECTIONS

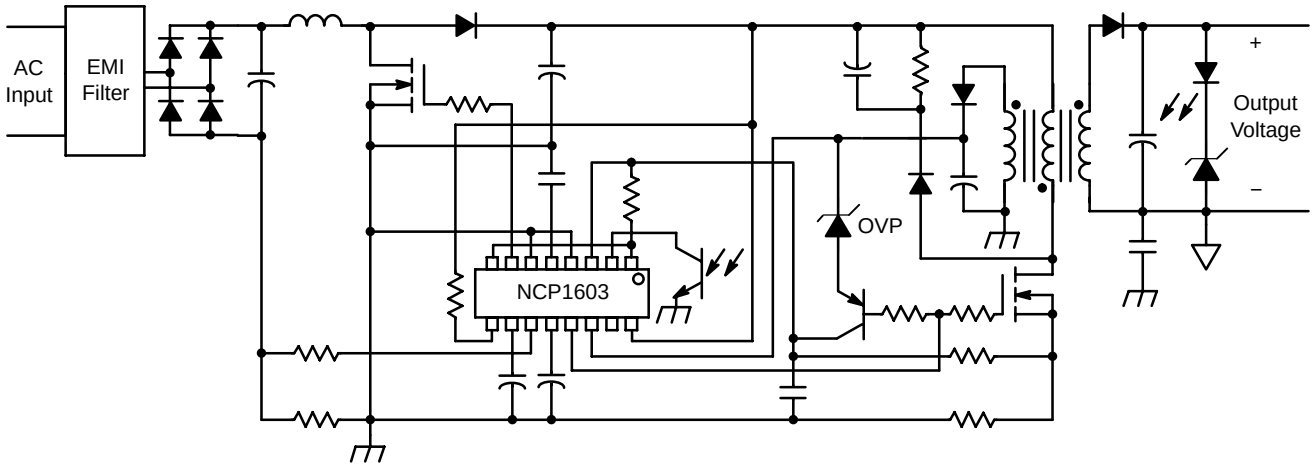


(Top View)

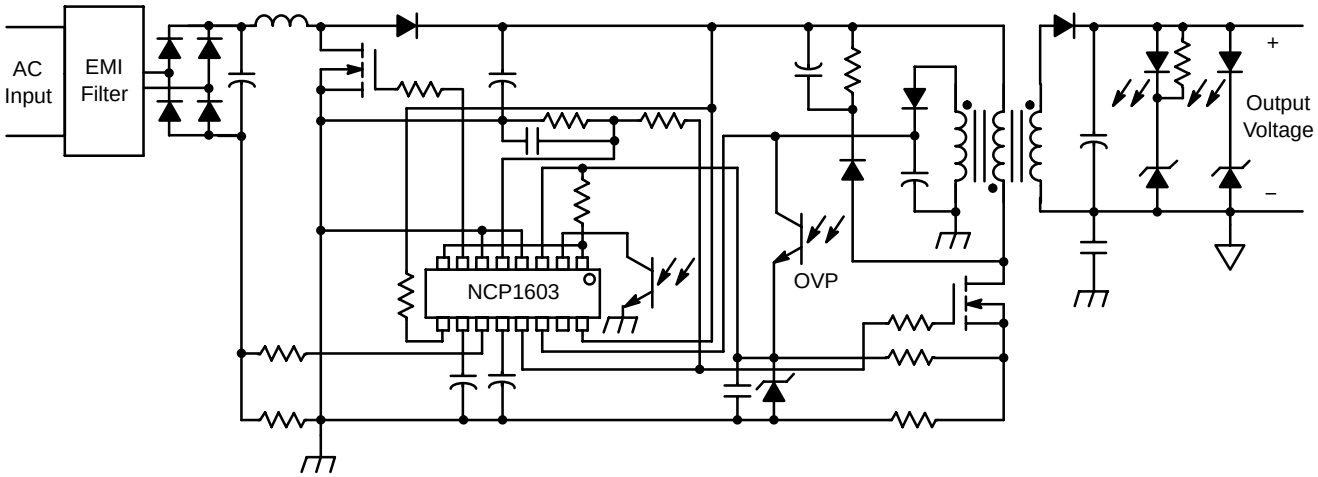
ORDERING INFORMATION

Device	Package	Shipping†
NCP1603D100R2	SO−16	2500 Tape & Reel
NCP1603D100R2G	SO−16 (Pb−Free)	2500 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.



Not Synchronized and V_{CC} OVP Latch Implemented



Synchronized and Output OVP Latch Implemented

Figure 1. Typical Application Circuits

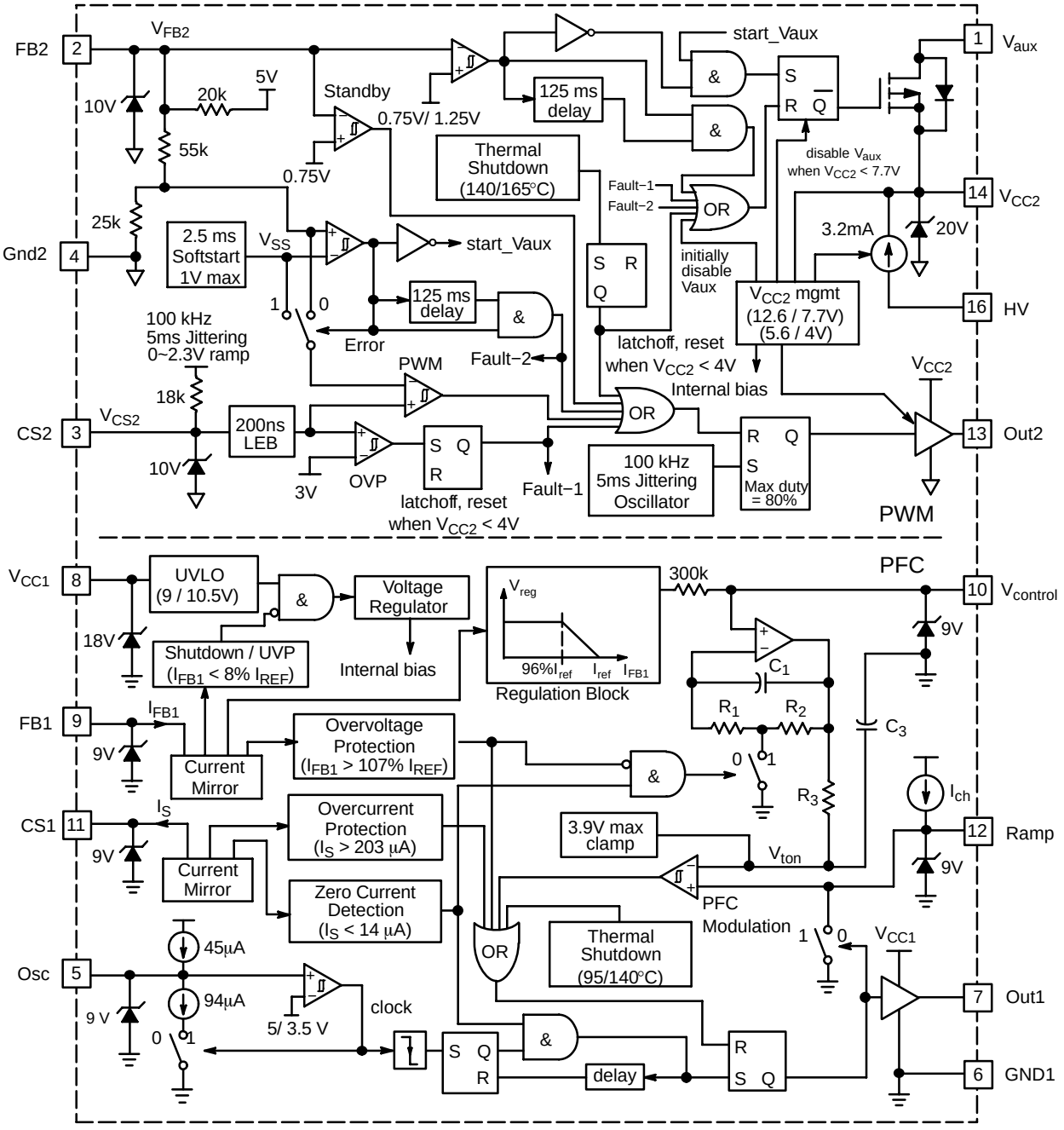


Figure 2. Functional Block Diagram

PIN FUNCTION DESCRIPTION

Pin	Symbol	Function	Description
1	V_{aux}	Auxiliary Supply	This pin connects to the V_{CC1} pin externally. It delivers a bias voltage from the V_{CC2} to the PFC section. The V_{aux} is disabled when either one of the following conditions occurs: (1) V_{aux} is initially off; (2) Fault (V_{FB2} > 3.0 V for more than 125 ms); (3) Standby (V_{FB2} < 0.75 V and then V_{FB2} is smaller than 1.25 V for more than 125 ms); (4) Overvoltage protection latch activated from CS2 pin; (5) Thermal shutdown latch in the PWM section; (6) Insufficient supply voltage (V_{CC2} < 7.7 V). The transistor turns on (or V_{aux} is enabled) when V_{FB2} is within the normal mode regulation window (0.75 V < V_{FB2} < 3.0 V).
2	FB2	PWM Feedback	An external optocoupler collector pulls the voltage of this pin V_{FB2} down to regulate the output voltage. The PWM regulation window between V_{FB2} = 0.75 V and V_{FB2} = 3.0 V. When V_{FB2} drops below 0.75 V, the controller enters standby operation. When no feedback signal is received from the optocoupler, V_{FB2} is internally pulled to be higher than 3.0 V. If this condition lasts for longer than 125 ms, the controller enters double−hiccup fault condition.
3	CS2	PWM Current Sense	This pin cumulates three different functions: current−mode PWM regulation, primary overcurrent protection and overvoltage protection (OVP). If the voltage of this pin is above 3.0 V for OVP, the circuit is latched off until V_{CC2} resets. The PWM Drive Output is disabled. An external noise decoupling pF−order capacitor is connected to the pin to prevent the latch protection activated due to noise.
4	GND2	PWM Ground	−
5	Osc	PFC Oscillator	In oscillator mode, this pin is connected to an external capacitor to set the oscillator frequency in DCM operation. In synchronization mode, this pin is connected to an external driving signal. However, if the PFC−stage inductor current is non−zero at the end of a switching period, the PFC−stage circuit will be forced to CRM and the Out1 is out of synchronization to the Osc pin signal.
6	GND1	PFC Ground	−
7	Out1	PFC Drive Output	This pin provides an output to an external MOSFET in the PFC section.
8	V_{CC1}	PFC Supply Voltage	This pin is the positive supply of the PFC section. the operating range is between 9.0 V and 18 V with UVLO start threshold 10.5 V.
9	FB1	PFC Feedback	This pin receives a current I_{FB1} that represents the PFC circuit output voltage. The current is for the output regulation, PFC section overvoltage protection (OVP) and PFC section output undervoltage protection (UVP). When I_{FB1} goes above 107% I_{ref}, OVP is activated and the Drive Output is disabled. When I_{FB1} goes below 14 μA, the PFC section enters a low−current consumption shutdown mode.
10	$V_{control}$	PFC Control Voltage	The control voltage $V_{control}$ directly controls the input impedance and hence the power factor of the circuit. This pin is connected to an external capacitor to limit the control voltage bandwidth typically below 20 Hz to achieve Power Factor Correction purpose.
11	CS1	PFC Current Sense	This pin receives a current I_S that is proportional to the inductor current. The current is for overcurrent protection (OCP), and zero current detection. When I_S goes above 200 μA, OCP is activated and the Drive Output (Out1) is disabled. When I_S goes below 14 μA, it is recognized to be a zero current for feedback regulation and DCM or CRM operation in the PFC oscillator section.
12	Ramp	PFC Ramp	This pin is connected to an external capacitor to set a ramp signal. The capacitor value directly affects the input impedance of the PFC circuit and its maximum input power.
13	Out2	PWM Drive Output	This pin provides an output to an external MOSFET in the PWM section.
14	V_{CC2}	PWM Supply Voltage	This pin is basically the positive supply of the PWM section. It is also the positive supply of the whole device because the PFC section is also supplied from this pin indirectly through V_{aux} pin (Pin 1). The operating range is between 7.7 V and 18 V. The circuit resets when V_{CC2} drops below 4.0 V.
15	NC	No Connected	This pin is for high voltage clearance of the HV pin.
16	HV	High Voltage	This pin connects to the bulk DC voltage to deliver power to the controller in startup or fault condition. The internal startup circuit is disabled in normal and standby condition for power saving purpose. The UVLO stop and start thresholds of the startup circuit are V_{CC2} = 12.6 V and V_{CC2} = 5.6 V.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
V_{aux} Pin (Pin 1) Maximum Voltage Range Maximum Continuous Current	 V_{max} I_{max}	 −0.3 to +18 35	 V mA
FB2 and CS2 Pin (Pins 2−3) Maximum Voltage Range Maximum Current	 V_{max} I_{max}	 −0.3 to +10 100	 V mA
Ramp, CS1, $V_{control}$, FB1, and Osc Pins (Pins 5, 9−12) Maximum Voltage Range Maximum Current	 V_{max} I_{max}	 −0.3 to +9.0 100	 V mA
Out1 Pin (Pin 7) Maximum Voltage Range Maximum Current	 V_{max} I_{max}	 −0.3 to +18 −500 to +750	 V mA
V_{CC1} and V_{CC2} Pins (Pins 8, 14) Maximum Voltage Range Maximum Current	 V_{max} I_{max}	 −0.3 to +18 100	 V mA
Out2 Pin (Pin 13) Maximum Voltage Range Maximum Current	 V_{max} I_{max}	 −0.3 to +17.5 1.0	 V A
HV Pin (Pin 16) Maximum Voltage Range Maximum Current	 V_{max} I_{max}	 −0.3 to +500 100	 V mA
Power Dissipation and Thermal Characteristics Maximum Power Dissipation (T_A = 25°C) Thermal Resistance, Junction−to−Air	 P_D $R_{\theta JA}$	 770 111	 mW °C/W
Operating Junction Temperature Range	T_J	−40 to +125	°C
Maximum Storage Temperature Range	T_{stg}	−60 to +150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. This device contains ESD protection and exceeds the following tests:
   Pin 1−14: Human Body Model 2000 V per Mil−Std−883, Method 3015.
   Machine Model Method 200 V.
   Pin 16 is the HV startup of the device and is rated to the maximum rating of the part, or 500 V.
2. This device contains latchup protection and exceeds 100 mA per JEDEC Standard JESD78.

ELECTRICAL CHARACTERISTICS (For typical values T_J = 25°C, for min/max values, T_J = −40°C to +125°C, V_{CC2} = 13 V, HV = 30 V, V_{CC1} = 15 V, $V_{control}$ = 100 nF, Ramp = 330 pF, Osc = 220 pF unless otherwise specified).

Characteristic (PWM Section)	Pin	Symbol	Min	Typ	Max	Unit
PWM OSCILLATOR						
Oscillation Frequency (T_J = 25°C) (Note 3) Oscillation Frequency (T_J = 0°C to +125°C) Oscillation Frequency (T_J = −40°C to +125°C)	−	f_{osc2}	93 90 85	100 − −	107 110 110	kHz
Oscillator Modulation Swing, in Percentage of f_{osc2}	−	−	−	±6.4	−	%
Oscillator Modulation Swing Period	−	−	−	5.0	−	ms
Maximum Duty Ratio (V_{CS2} = 0 V, V_{FB2} = 2.0 V)	−	D_{max}	75	80	85	%
PWM GATE DRIVE						
Gate Drive Resistor Output High (V_{CC2} = 13 V, Out2 = 300 Ω to GND2) Output Low (Out2 = 1.0 V, V_{FB2} = 0 V)	13	 R_{OH2} R_{OL2}	 6.0 3.0	 12.3 7.5	 25 18	 Ω Ω
Gate Drive Rise Time from 10% to 90% (Out2 = 1.0 nF to GND2)	13	t_{r2}	−	40	−	ns
Gate Drive Fall Time from 90% to 10% (Out2 = 1.0 nF to GND2)	13	t_{f2}	−	15	−	ns
PWM CURRENT SENSE/OVERVOLTAGE PROTECTION						
Maximum Current Threshold (T_J = 25°C) Maximum Current Threshold (T_J = −40°C to +125°C)	3	I_{Limit}	0.991 0.96	1.043 −	1.095 1.106	V
Soft−Start Duration	−	t_{SS}	−	2.5	−	ms
Leading Edge Blacking Duration	3	t_{LEB}	100	200	350	ns
Propagation Delay from CS Detected to Turn Out2 Off	−	$T_{delay(CS)}$	−	90	180	ns
Overvoltage Protection Threshold	3	V_{OVP}	2.7	3.0	3.3	V
Internal Compensation Ramp (Peak−to−Peak) (Note 4)	3	V_{comp}	−	2.3	−	V
Internal Resistor to Ramp (Note 4)	3	R_{comp}	9.0	18	36	kΩ
PWM STANDBY THRESHOLDS/FEEDBACK						
Standby Thresholds Feedback Voltage V_{FB2} to Start Standby Feedback Voltage V_{FB2} to Stop Standby	2	 V_{stby} $V_{stby−out}$	 0.6 1.0	 0.75 1.25	 0.9 1.5	 V V
Validation Time for Leaving Standby	2	$t_{stby−aux}$	−	125	−	ms
Validation Time for Recognize a Fault	2	t_{fault}	−	125	−	ms
Feedback Pin Sinking Capability (V_{FB2} = 0.75 V)	2	I_{FB2}	200	235	270	μA
AUXILIARY SUPPLY						
V_{aux} MOSFET Resistance (V_{CC2} = 13 V, V_{FB} = 2.0 V, V_{aux} = 20 mA Sinking)	1	R_{aux}	6.0	11.7	23	Ω
PWM THERMAL SHUTDOWN						
Thermal Shutdown Threshold (Note 4)	−	T_{SD2}	150	165	−	°C
Thermal Shutdown Hysteresis	−	T_{H2}	−	25	−	°C
PWM STARTUP CURRENT SOURCE						
High−Voltage Current Source Startup (V_{CC2} = $V_{CC2(on)}$−0.2 V, V_{FB2} = 2.0 V, HV = 30 V) Startup (V_{CC2} = 0 V, HV = 30 V) Leakage (V_{CC2} = 13 V, HV = 700 V)	16	 I_{HV1} I_{HV2} I_{HV3}	 1.8 1.8 10	 3.2 4.4 30	 4.2 5.6 80	 mA mA μA
Minimum Startup Voltage (V_{CC2} = $V_{CC2(on)}$−0.2 V, I_{HV} = 0.5 mA)	16	$V_{start(min)}$	−	20	23	V

3. Consult factory for other frequency options.
4. Guaranteed by design.

ELECTRICAL CHARACTERISTICS (For typical values T_J = 25°C, for min/max values, T_J = −40°C to +125°C, V_{CC2} = 13 V, HV = 30 V, V_{CC1} = 15 V, $V_{control}$ = 100 nF, Ramp = 330 pF, Osc = 220 pF unless otherwise specified).

Characteristic (PFC Section)	Pin	Symbol	Min	Typ	Max	Unit
PWM SUPPLY SECTION						
Supply Voltage Startup Threshold, V_{CC2} Increasing Minimum Operating Valley Voltage after Turn−On Undervoltage Lockout Threshold Voltage, V_{CC2} Decreasing Logic Reset Level	14	 $V_{CC2(on)}$ $V_{CC2(off)}$ $V_{CC2(latch)}$ $V_{CC2(reset)}$	 11.6 7.0 5.0 −	 12.6 7.7 5.6 4.0	 13.6 8.4 6.2 −	 V V V V
Supply Current Operating (V_{CC2} = 13 V, Out2 = Open, V_{FB2} = 2.0 V) Operating (V_{CC2} = 13 V, Out2 = 1.0 nF to GND2, V_{FB2} = 2.0 V) Latch−Off Phase (V_{CC2} = 6.5 V, V_{FB2} = 2.0 V)	14	 $I_{CC2(op1)}$ $I_{CC2(op2)}$ $I_{CC2(latch)}$	 0.6 1.3 400	 1.1 2.2 680	 1.8 3.0 1000	 mA mA μA
PFC OSCILLATOR						
Oscillator Frequency (Osc = 220 pF to GND)	5	f_{osc1}	52	58	64	kHz
Internal Capacitance of the Oscillator Pin	5	$C_{osc(int)}$	−	36	−	pF
Maximum Oscillator Switching Frequency	5	$f_{osc1(max)}$	−	405	−	kHz
Oscillator Discharge Current (Osc = 5.5 V)	5	I_{odch}	40	49	60	μA
Oscillator Charge Current (Osc = 3.0 V)	5	I_{och}	40	45	60	μA
Comparator Lower Threshold (Osc = 220 pF to GND) (Note 5)	5	$V_{sync(L)}$	3.0	3.5	4.0	V
Comparator Upper Threshold (Osc = 220 pF to GND)	5	$V_{sync(H)}$	4.5	5.0	5.5	V
Synchronization Pulse Width for Detection	5	$t_{sync(min)}$	500	–	–	ns
Synchronization Propagation Delay	5	$t_{sync(d)}$	−	371	–	ns
PFC GATE DRIVE						
Gate Drive Resistor Output High and Draw 100 mA out of Out1 Pin (I_{source} = 100 mA) Output Low and Insert 100 mA into Out1 Pin (I_{sink} = 100 mA)	7	 R_{OH1} R_{OL1}	 5.0 2.0	 11.6 7.2	 20 18	 Ω Ω
Gate Drive Rise Time from 1.5 V to 13.5 V (Out1 = 1.0 nF to GND)	7	t_{r1}	−	53	−	ns
Gate Drive Fall Time from 13.5 V to 1.5 V (Out1 = 1.0 nF to GND)	7	t_{f1}	−	32	−	ns
PFC FEEDBACK/OVERVOLTAGE PROTECTION/UNDERVOLTAGE PROTECTION						
Reference Current	9	I_{ref}	192	203	208	μA
Regulation Block Ratio	9	I_{regL}/I_{ref}	95	96	97	%
Vcontrol Pin Internal Resistor	10	$R_{control}$	−	300	−	kΩ
Maximum Control Voltage (I_{FB1} = 100 μA)	10	$V_{control(max)}$	0.95	1.05	1.15	V
Feedback Pin Voltage (I_{FB1} = 100 μA)	9	$V_{FB1-100}$	−	3.0	−	V
Overvoltage Protection Current Ratio	9	I_{OVP}/I_{ref}	104	107	–	%
Overvoltage Protection Current Threshold	9	I_{OVP}	−	217	225	μA
Undervoltage Protection Current Threshold	9	I_{UVP}/I_{ref}	4.0	8.0	15	%

5. Comparator lower threshold is also the synchronization threshold.

ELECTRICAL CHARACTERISTICS (continued) (For typical values T_J = 25°C, for min/max values, T_J = −40°C to +125°C, V_{CC2} = 13 V, HV = 30 V, V_{CC1} = 15 V, $V_{control}$ = 100 nF, Ramp = 330 pF, Osc = 220 pF unless otherwise specified).

Characteristic (PFC Section)	Pin	Symbol	Min	Typ	Max	Unit
PFC CURRENT SENSE						
Current Sense Pin Offset Voltage (I_S = 100 μA)	11	V_S	−	4.0	−	mV
Overcurrent Protection Level	11	$I_{S(OCP)}$	190	203	210	μA
Current Sense Pin Offset Voltage at Overcurrent Level	11	$V_{S(OCP)}$	0	3.2	20	mV
Zero Current Detection Level	11	$I_{S(ZCD)}$	9	14	19	μA
Current Sense Pin Offset Voltage at Zero Current Level	11	$V_{S(ZCD)}$	0	7.5	20	mV
Zero Current Sense Resistor ($R_{S(ZCD)} = V_{S(ZCD)}/I_{S(ZCD)}$)	11	$R_{S(ZCD)}$	−	0.536	1.0	kΩ
PFC RAMP						
Charging Current (Ramp = 0 V)	12	I_{ch}	95	100	105	μA
Maximum Power Resistance ($R_{power} = V_{control(max)}/I_{ch}$)	12	R_{power}	9.5	10	11.5	kΩ
Internal Clamping of Voltage V_{ton}	−	$V_{ton(max)}$	−	3.9	−	V
Internal Capacitance of the Ramp Pin	12	$C_{ramp(int)}$	−	22	−	pF
Ramp Pin Sink Resistance (Osc = 0 V, Ramp = 1.0 mA sourcing)	12	R_{ramp}	−	71.5	−	Ω
PFC THERMAL SHUTDOWN						
Thermal Shutdown Threshold (Note 6)	−	T_{SD1}	140	170	−	°C
Thermal Shutdown Hysteresis	−	T_{H1}	−	45	−	°C
PFC SUPPLY SECTION						
Supply Voltage Startup Threshold (UVLO) Minimum Voltage for Operation after Turn−On UVLO Hysteresis	8	 $V_{CC1(on)}$ $V_{CC1(off)}$ V_{H1}	 9.6 8.25 1.0	 10.5 9.0 1.5	 11.4 9.75 −	 V V V
Supply Current Start−Up ($V_{CC1} = V_{CC1(on)}$–0.2 V) Operating (V_{CC1} = 15 V, Out1 = Open, Osc = 220 pF) Operating (V_{CC1} = 15 V, Out1 = 1.0 nF to GND1, Osc = 220 pF) Shutdown (V_{CC1} = 15 V, I_{FB} = 0 A)	8	 $I_{CC1(stup)}$ $I_{CC1(op1)}$ $I_{CC1(op2)}$ $I_{CC1(stdn)}$	 − − − −	 17 2.7 3.7 24	 40 5.0 5.0 50	 μA mA mA μA

6. Guaranteed by design.

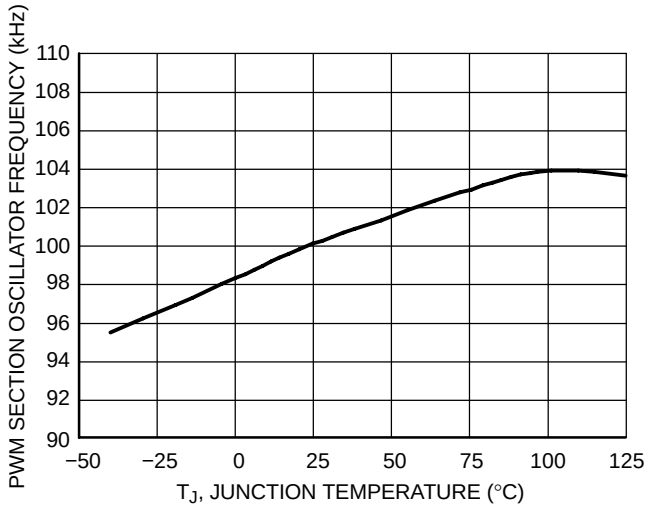


Figure 3. PWM Section Oscillator Frequency vs. Temperature

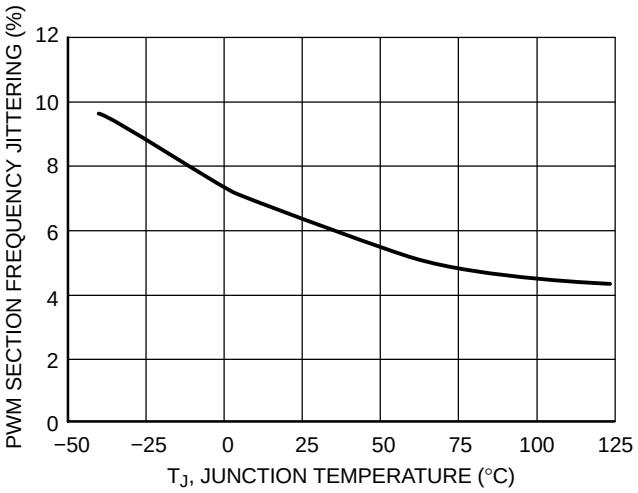


Figure 4. PWM Section Oscillator Frequency Jittering vs. Temperature

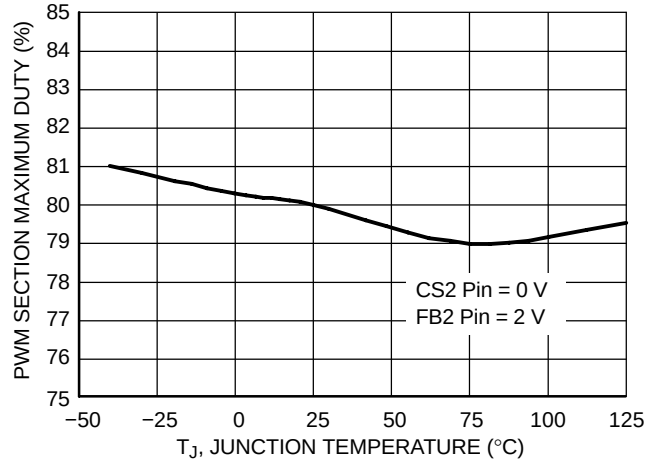


Figure 5. PWM Section Maximum Duty vs. Temperature

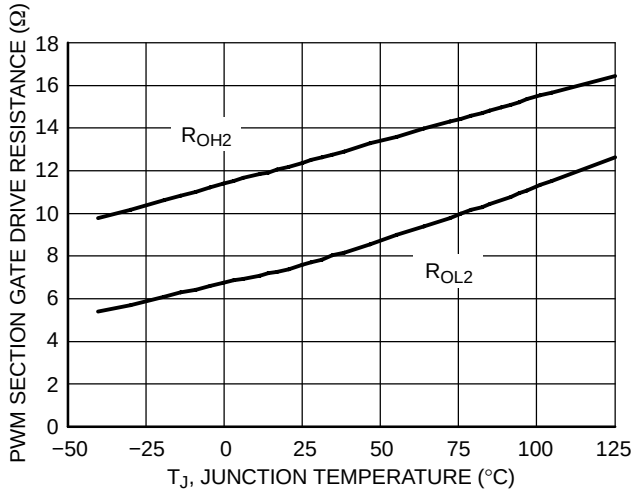


Figure 6. PWM Section Gate Drive Resistance vs. Temperature

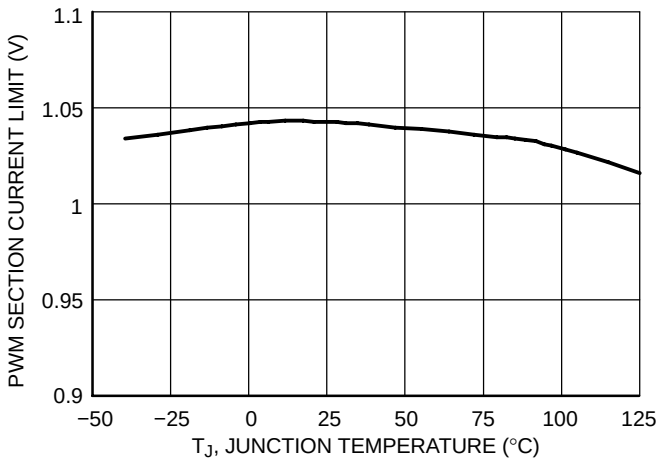


Figure 7. PWM Section Current Limit vs. Temperature

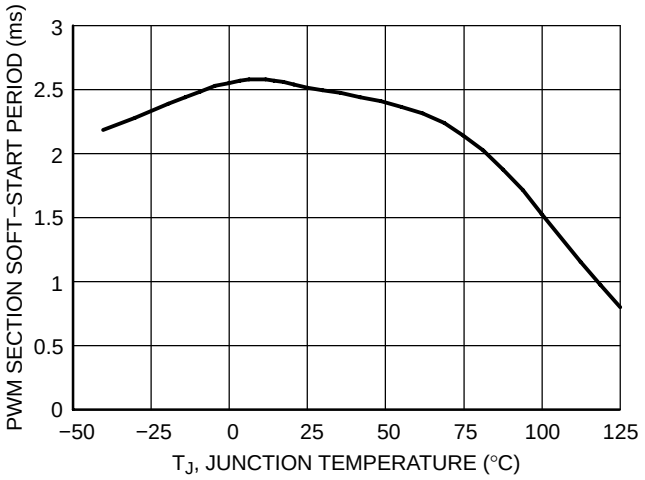


Figure 8. PWM Section Soft−Start Period vs. Temperature

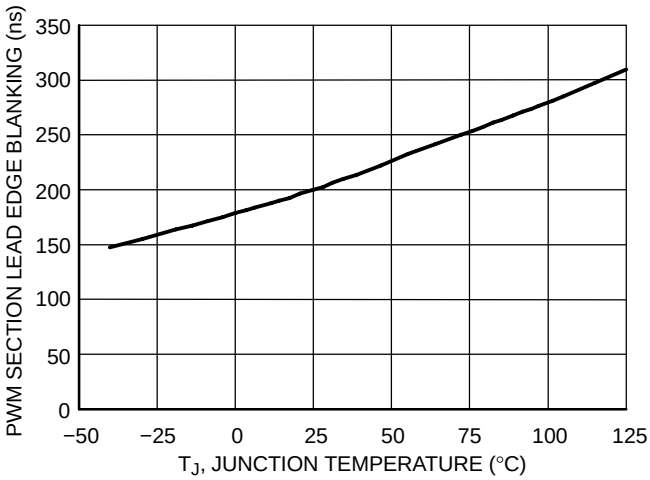


Figure 9. PWM Section Lead Edge Blanking vs. Temperature

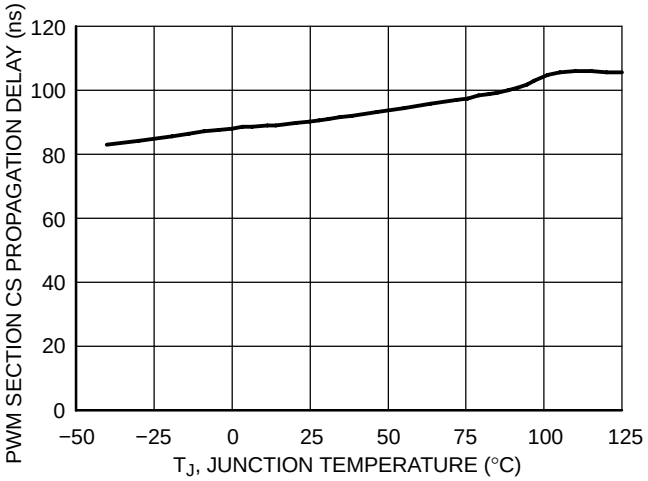


Figure 10. CS2 Pin Propagation Delay vs. Temperature

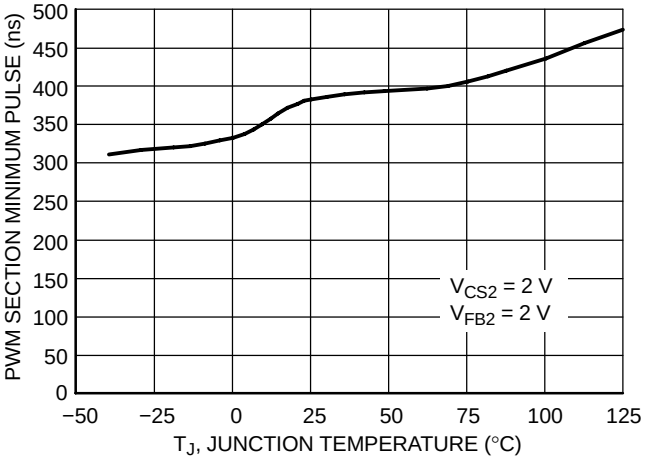


Figure 11. PWM Section Minimum Output Pulse vs. Temperature

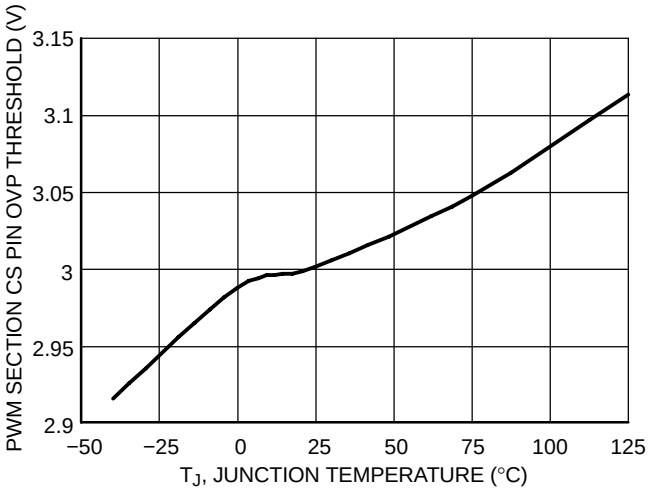


Figure 12. CS2 Pin Overvoltage Protection Threshold vs. Temperature

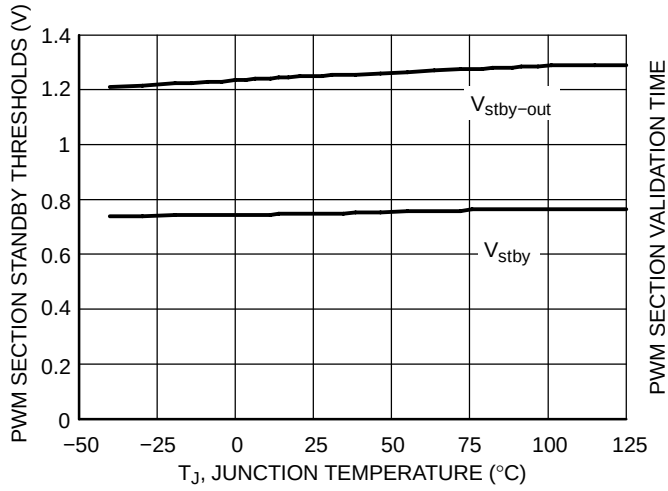


Figure 13. PWM Section Standby Thresholds vs. Temperature

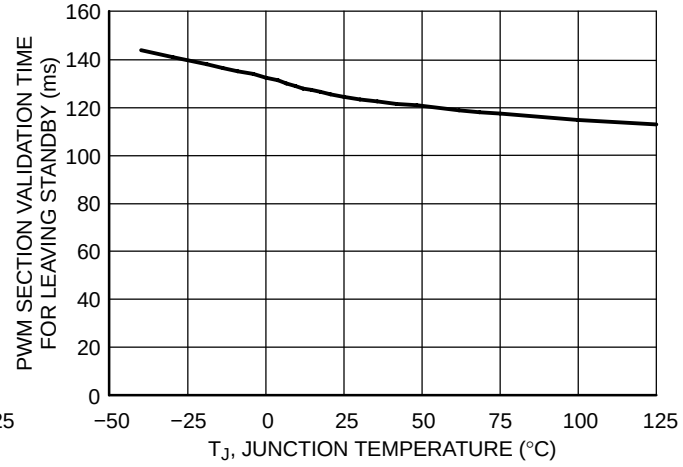


Figure 14. PWM Section Validation Time for Leaving Standby vs. Temperature

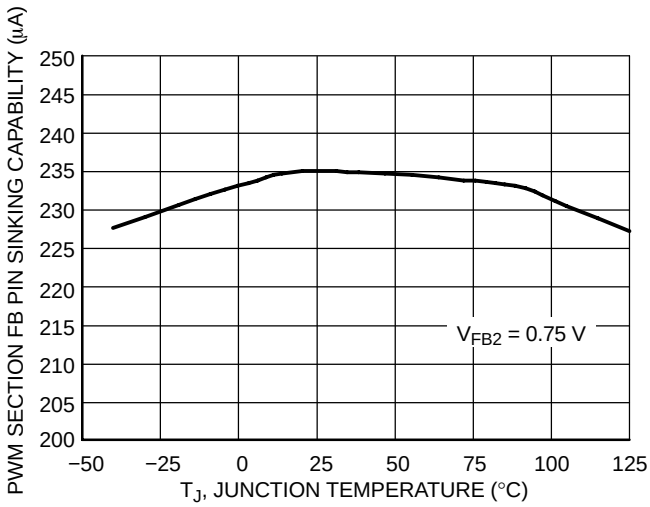


Figure 15. FB2 Pin Sinking Capability vs. Temperature

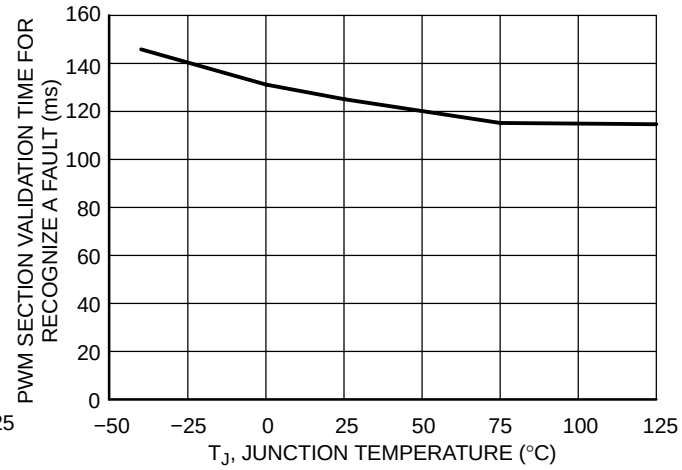


Figure 16. PWM Section Validation Time for Recognizing a Fault vs. Temperature

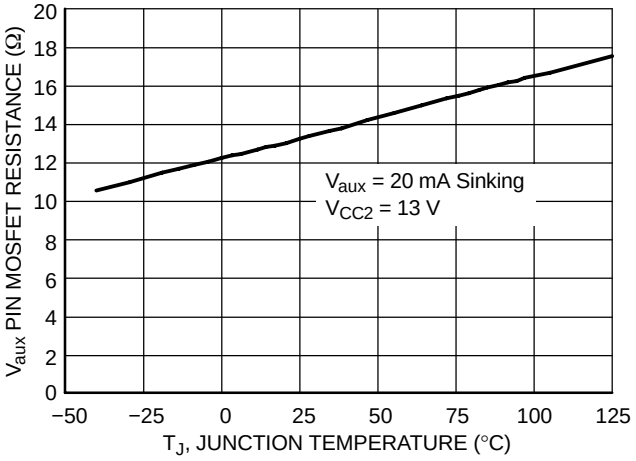


Figure 17. V_{aux} Pin Internal MOSFET Resistance vs. Temperature

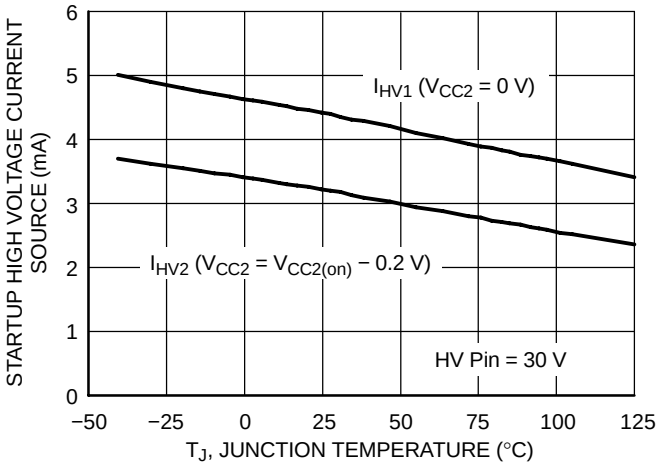


Figure 18. PWM Section High Voltage Startup Current Source vs. Temperature

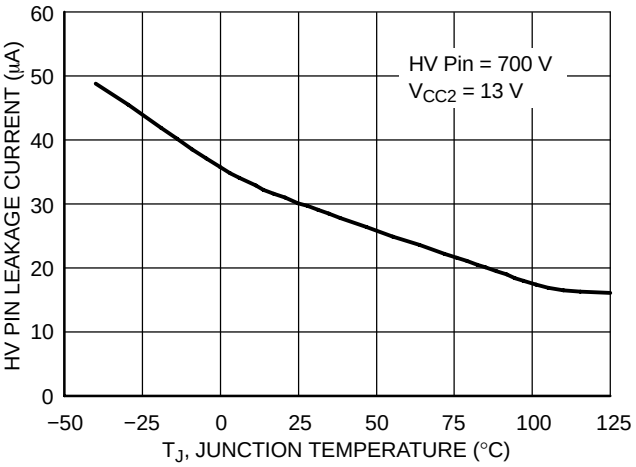


Figure 19. PWM Section HV Pin Leakage Current vs. Temperature

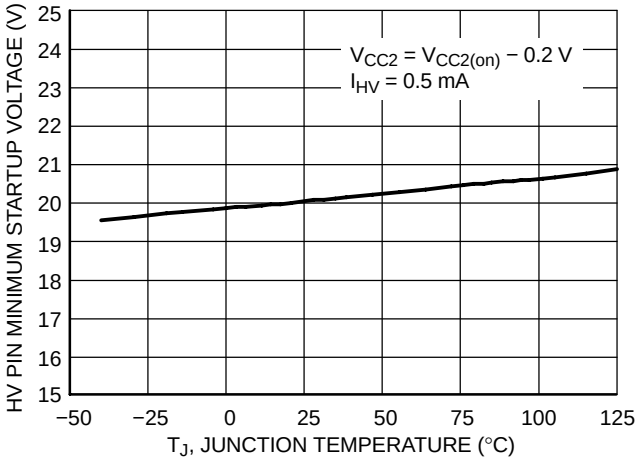


Figure 20. PWM Section HV Pin Minimum Operating Voltage vs. Temperature

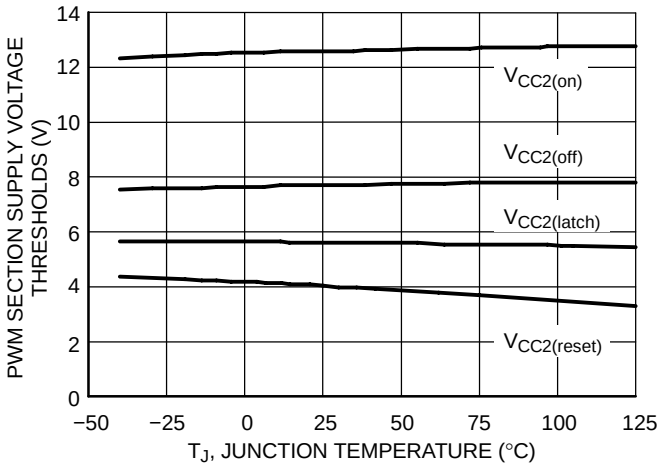


Figure 21. PWM Section Supply Voltage Thresholds vs. Temperature

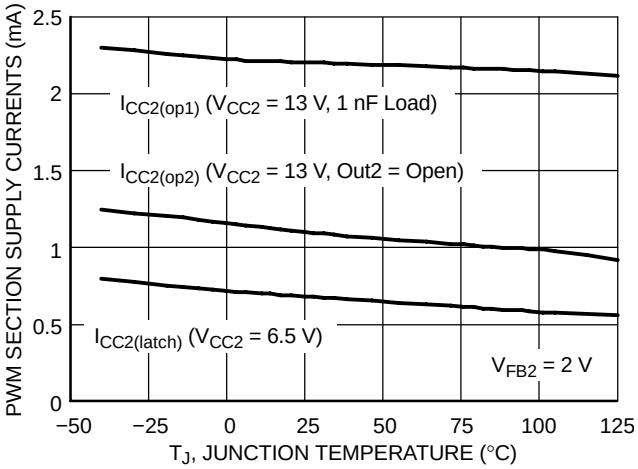


Figure 22. PWM Section Supply Currents vs. Temperature

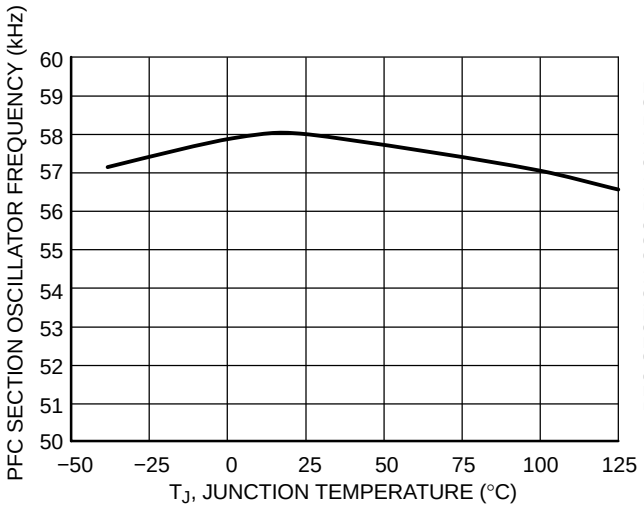


Figure 23. PFC Section Oscillator Frequency vs. Temperature

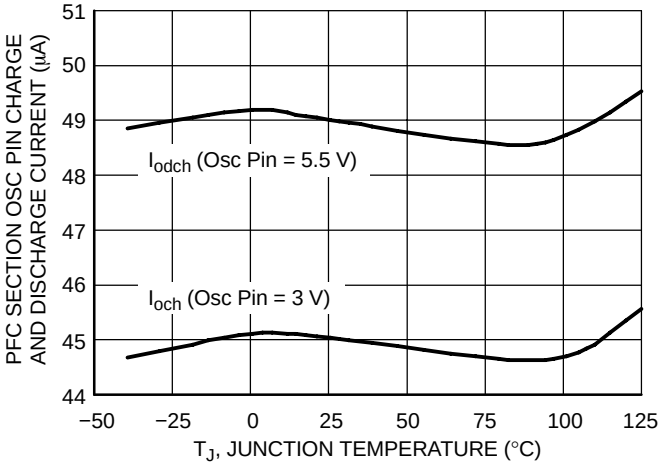


Figure 24. PFC Section Osc Pin Charge and Discharge Current vs. Temperature

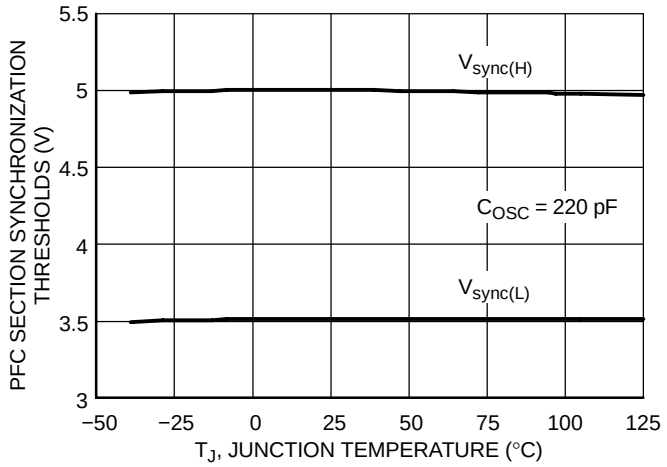


Figure 25. PFC Section Synchronization Thresholds vs. Temperature

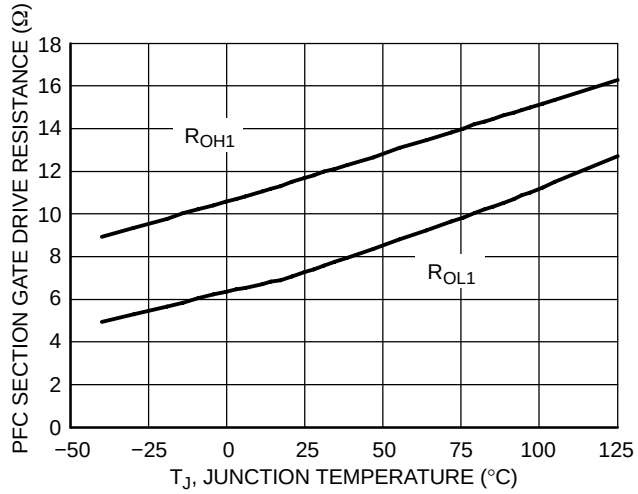


Figure 26. PFC Section Gate Drive Resistance vs. Temperature

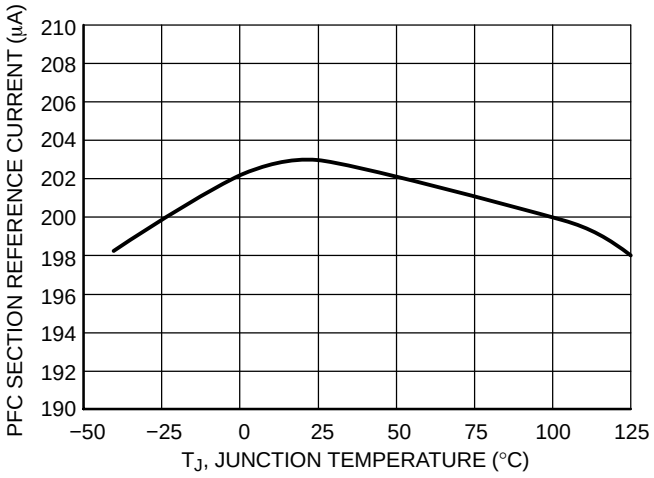


Figure 27. PFC Section Reference Current vs. Temperature

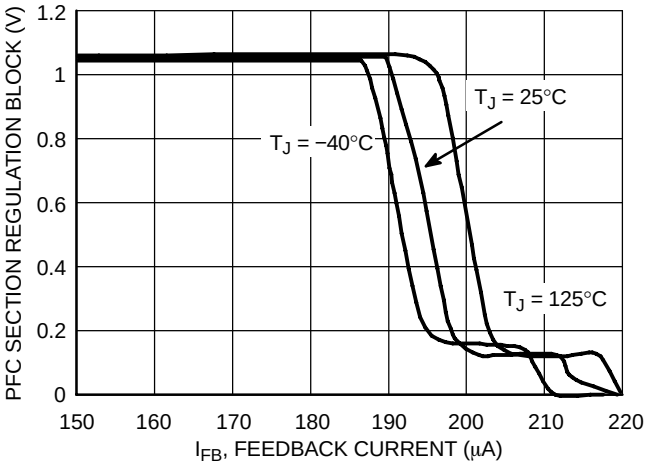


Figure 28. PFC Section Regulation Block Transfer Function

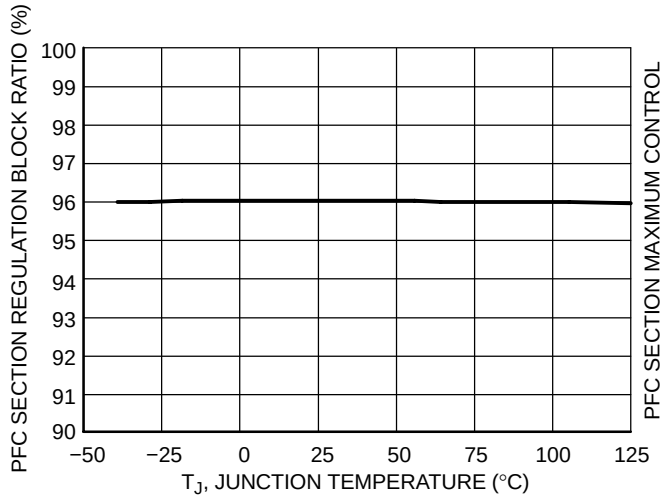


Figure 29. PFC Section Regulation Block vs. Temperature

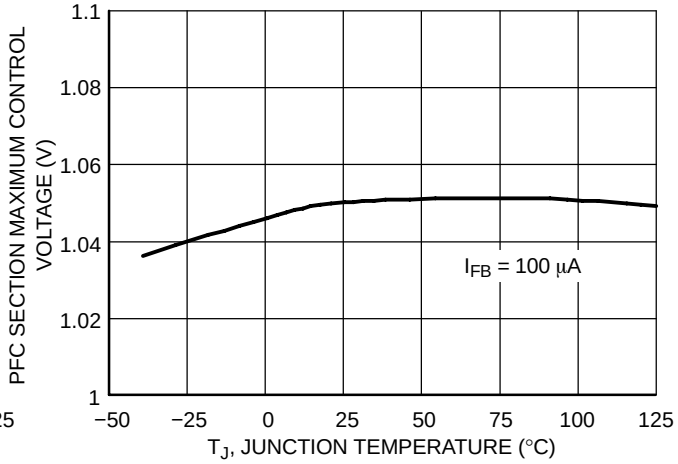


Figure 30. PFC Section Maximum Control Voltage vs. Temperature

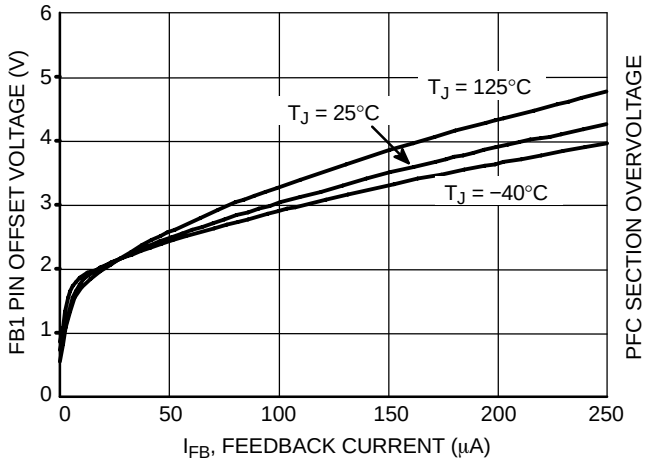


Figure 31. Feedback Pin Voltage vs. Feedback Current

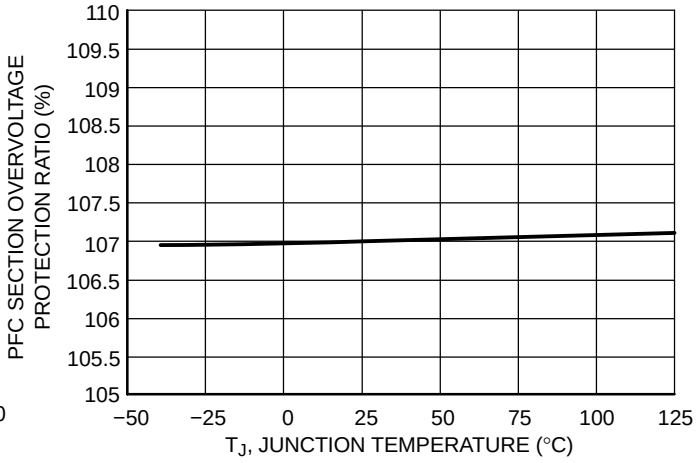


Figure 32. PFC Section Overvoltage Protection Ratio vs. Temperature

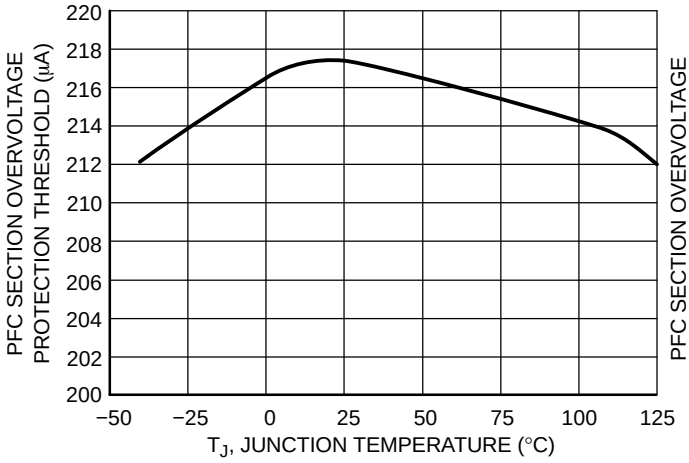


Figure 33. PFC Section Overvoltage Protection Threshold vs. Temperature

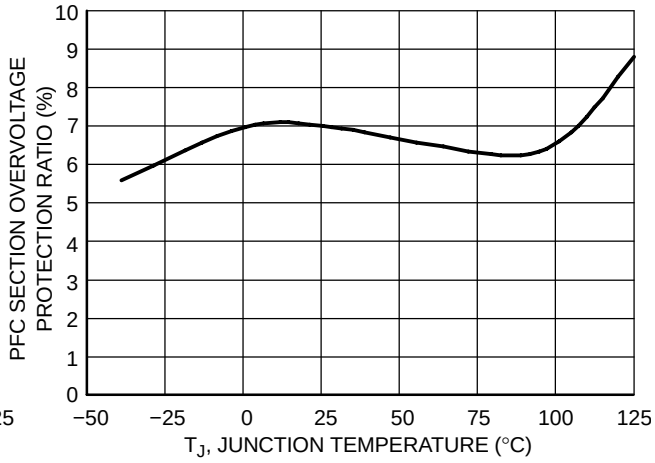


Figure 34. PFC Section Overvoltage Protection Ratio vs. Temperature

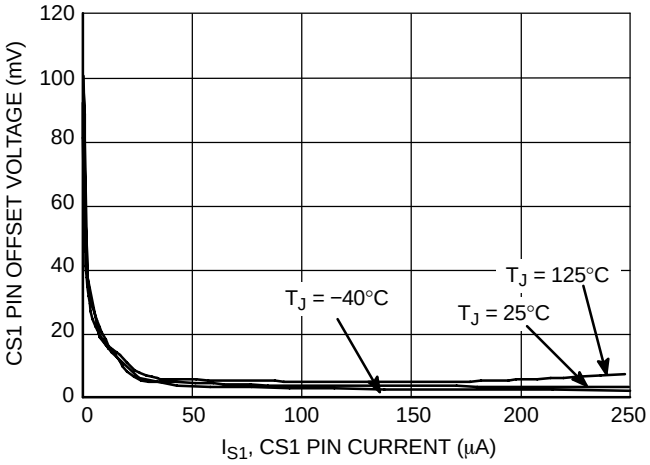


Figure 35. CS1 Pin Offset Voltage vs. Current

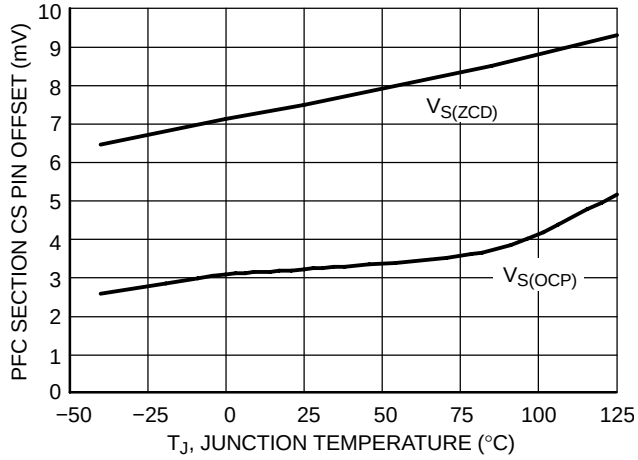


Figure 36. PFC Section CS Pin Offset vs. Temperature

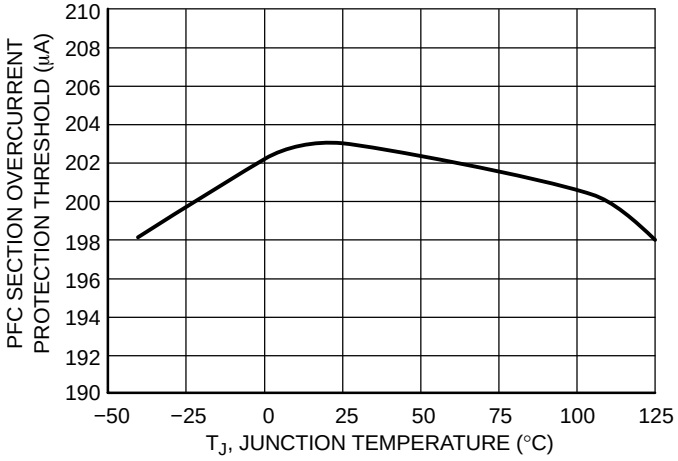


Figure 37. PFC Section Overcurrent Protection Threshold vs. Temperature

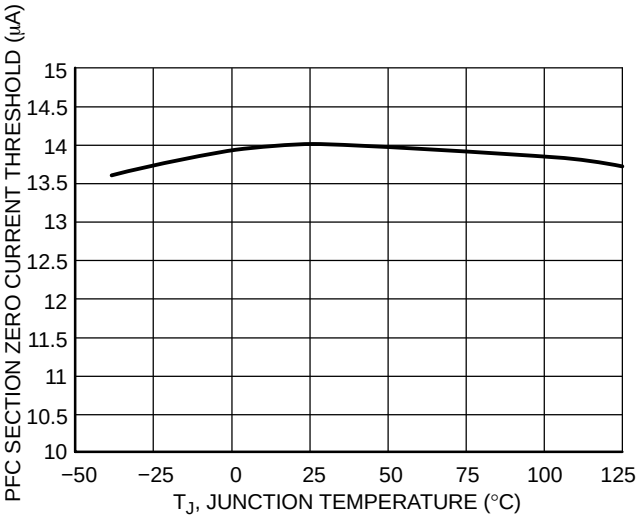


Figure 38. PFC Section Zero Current Threshold vs. Temperature

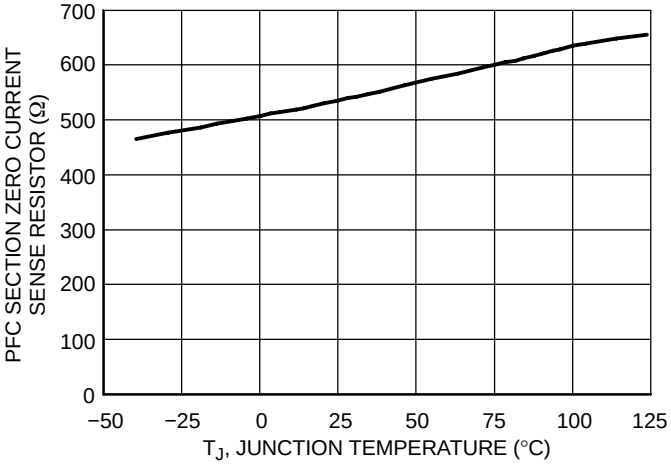


Figure 39. PFC Section Zero Current Sense Resistance vs. Temperature

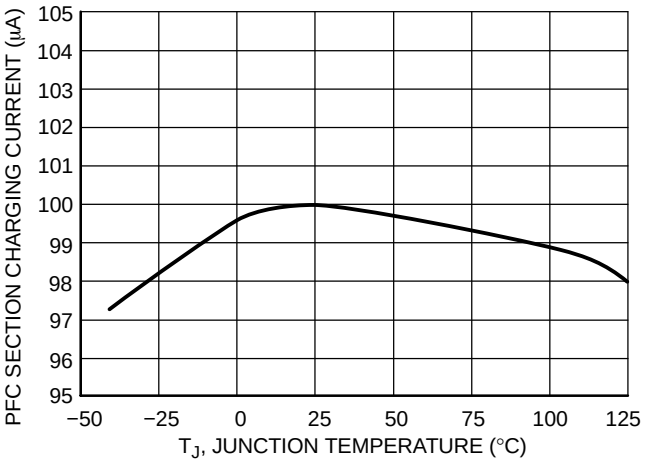


Figure 40. PFC Section Charging Current vs. Temperature

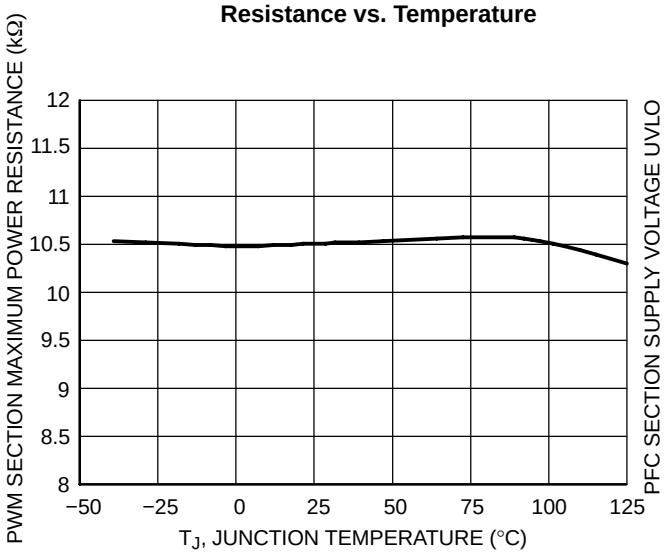


Figure 41. PFC Section Maximum Power Resistance vs. Temperature

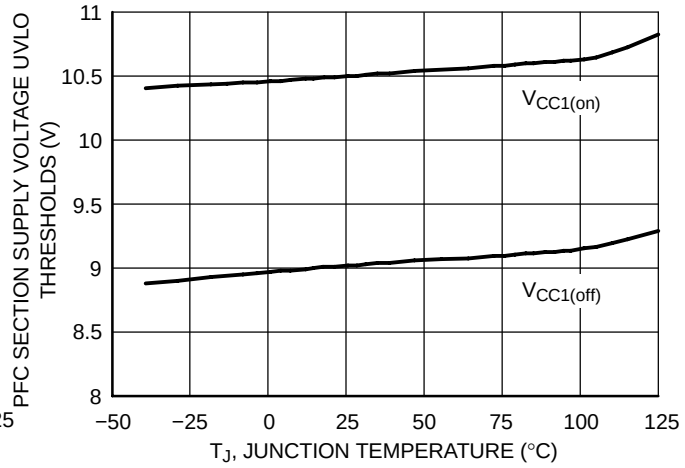


Figure 42. PFC Section Supply Voltage Undervoltage Lockout Thresholds vs. Temperature

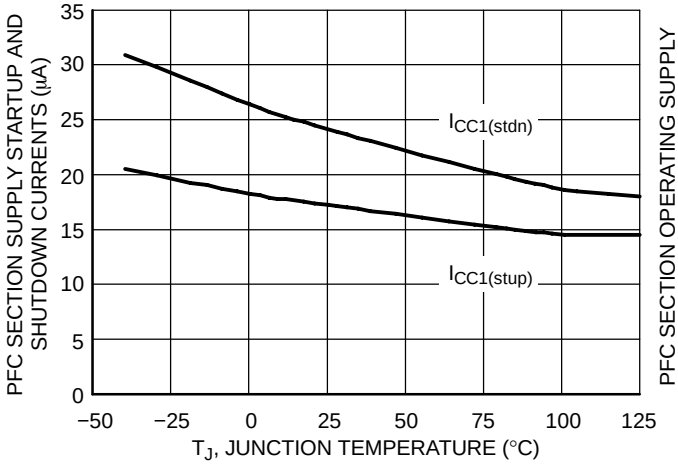


Figure 43. PFC Section Supply Current in Startup and Shutdown Conditions vs. Temperature

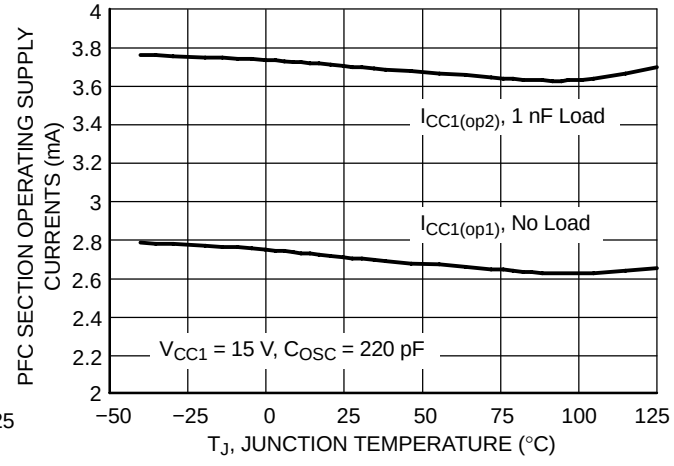


Figure 44. PFC Section Operating Supply Currents vs. Temperature

OPERATING DESCRIPTION

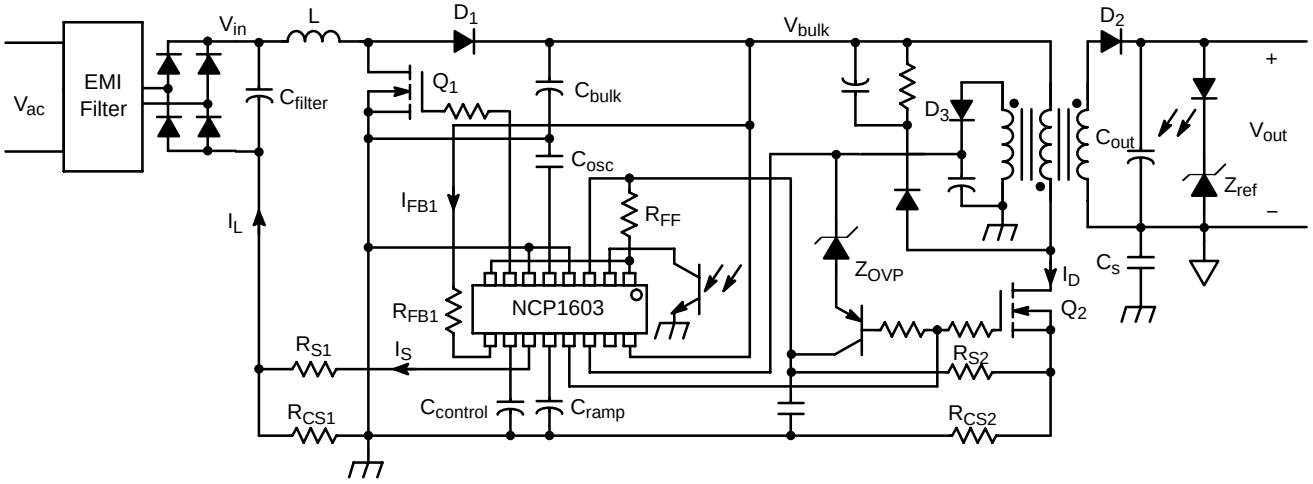


Figure 45. Typical Application Circuit

Introduction

The NCP1603 is a PWM/PFC combo controller for two−stages PFC low−power application. A typical application circuit is listed in Figure 45. The first−stage PFC boost circuit draws a near−unity power factor current from the input but it also steps up the rectified input voltage V_{in} to a high bulk voltage V_{bulk} in the bulk capacitor C_{bulk}. Then, the second−stage PWM flyback circuit converts the bulk voltage V_{bulk} to a usable low voltage and isolated output voltage V_{out}. The controllers of the two stages are combined to become a single PWM/PFC combo controller. The advantages of NCP1603 are the following:

1. Integrated maximum 500 V lossless high voltage startup circuit that saves area and power loss.
2. Low standby power consumption because of PFC shutdown and skipping cycle operation.
3. Proprietary PFC methodology limits the maximum switching frequency and frequency jittering feature of the second−stage make the easier front−ended EMI filter design.
4. Internal ramp compensation for stability improvement in the second stage converter.
5. Minimum number of external components.
6. Optional synchronization capability between the PFC and PWM sections for bulk capacitor ripple current reduction.
7. Safety protection features.

NCP1603 is a co−package of two individual IC dies. (NCP1601 and NCP1230, 100 kHz) The PFC die links up pin 5 to pin 12 that are in the lower half of Figure 46. The PWM die links up the other pins that are in the upper half of Figure 46. For simplicity, the PFC pins are named with suffix one that stands for the first stage and the PWM pins are named with suffix two that stands for the second stage.

This dual−dies architecture allows the PFC die to be completely powered off in the standby low−power condition. It makes the power supply an excellent low−power no load standby performance.

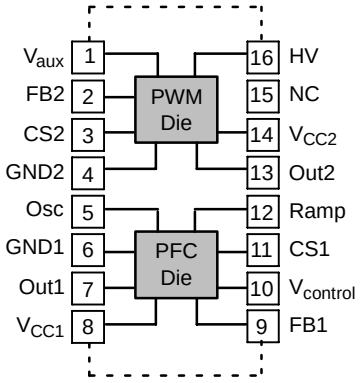


Figure 46. Internal Connection

Biasing the Controller

The PWM section is the master section that always operates. The PFC section is the slave section that is powered off in standby condition for power saving. It is implemented by connecting V_{aux} pin (Pin 1) and V_{CC1} pin (Pin 8) together externally. The V_{CC1} pin generally requires a small decoupling external capacitor (0.1 μF) or nothing. The PWM section powers the PFC section. The V_{CC} of the whole device refers to V_{CC2} (Pin 14) in the PWM section (i.e., $V_{CC} = V_{CC2}$).

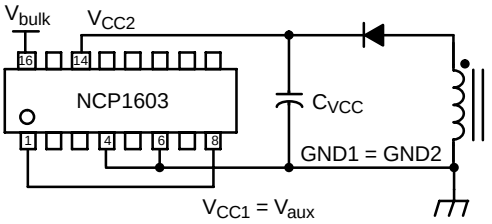


Figure 47. Bias Supply Schematic

The recommended biasing schematic of the controller is in Figure 47 while a typical completed application schematic can be referred to Figure 45. These two dies have their own individual supply voltages at Pin 8 and Pin 14. The grounds of the two dies are physically connected through the package substrate but they are needed to be connected externally. The bias voltage to the NCP1603 comes from the bulk voltage V_{bulk} through the HV pin (Pin 16) during startup. After startup, a second−stage flyback transformer auxiliary winding delivers the supply voltage to V_{CC}.

Lossless High Voltage Startup Circuit

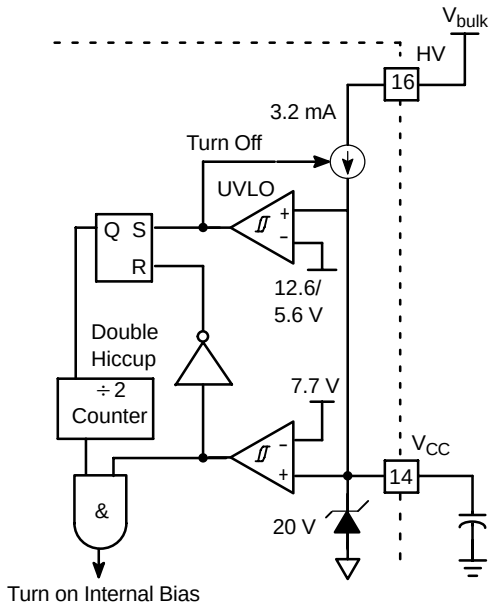


Figure 48. V_{CC2} Management

The HV pin (Pin 16) is capable of the maximum 500 V so that this pin can be directly connected to the bulk voltage V_{bulk} and delivers startup supply voltage to the controller. Figure 48 illustrates the block diagram of the startup circuit. An UVLO comparator monitors the V_{CC} at Pin 14. A startup current source is activated and deactivated whenever the voltage reaches $V_{CC2(latch)}$ (5.6 V typical) and $V_{CC2(on)}$ (12.6 V typical) thresholds respectively. Therefore, the V_{CC} never drops below $V_{CC2(latch)}$ after powering up unless the circuit is unplugged (i.e., V_{bulk} disappears or smaller than its minimum required operating threshold $V_{start(min)}$ (20 V typical)). This feature makes the controller memorize the external latch off function implemented in Pin 3.

This in−chip startup circuit can minimize the number of external components and Printed Circuit Board (PCB) area. It also minimizes the loss due to startup resistor because startup resistor always dissipates power but this startup circuit can be turned off when the V_{CC} voltage is sufficient. Actually, there is a small leakage current I_{HV3} (30 μA typical at HV = 700 V) when the startup circuit is off.

The V_{CC} capacitor is recommended to be at least 47 μF to ensure that V_{CC} is always above the minimum operating voltage $V_{CC2(off)}$ (7.7 V typical) in the startup phase. For example, the PWM die consumes $I_{CC2(op2)}$ (2.2 mA typical), a 47 μF V_{CC} capacitor can maintain the V_{CC} above 7.7 V for 105 ms. It is the available time to establish a V_{CC} voltage from the flyback transformer auxiliary winding.

$$t_{startup} = \frac{C_{VCC}\Delta V}{I_{CC2(op2)}} = \frac{47\ \mu F \cdot (12.6\ V - 7.7\ V)}{2.2\ mA} = 105\ ms \quad \text{(eq. 1)}$$

A large enough V_{CC} capacitor can also help to maintain V_{CC2} always above $V_{CC2(off)}$ to prevent the IC accidentally powered off during the standby condition where the low−frequency ripple of V_{CC2} can be very high.

The PFC section does not consume any current in the startup phase since V_{aux} is disabled initially (i.e., V_{aux} = V_{CC1} = 0 V).

When V_{CC2} falls below $V_{CC2(off)}$ (7.7 V typical) for whatever reason, the PWM section sleeps and it consumes $I_{CC2(latch)}$ (680 μA typical) until V_{CC2} reaches $V_{CC2(latch)}$ (5.6 V typical). When V_{CC2} reaches $V_{CC2(latch)}$ (5.6 V typical), the startup current source activates and V_{CC2} rises again.

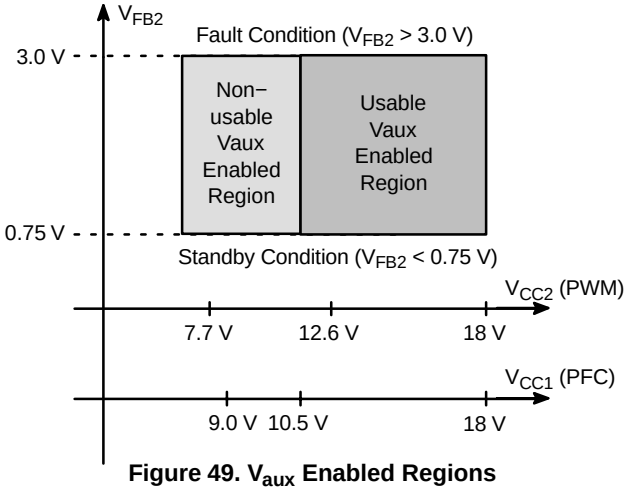


Figure 49. V_{aux} Enabled Regions

Auxiliary Supply V_{aux}

The V_{aux} pin (Pin 1) connects to the V_{CC1} pin (Pin 8) externally. Internally, the V_{aux} pin is connected to V_{CC2} through an internal MOSFET. The MOSFET on−resistance is R_{aux} (11.7 Ω typical). It delivers a supply voltage from the PWM section to the PFC section. The V_{aux} is disabled when one of the following conditions occurs.

1. V_{aux} is initially disabled because of no feedback signal (V_{FB2} > 3.0 V) initially.
2. Fault condition (V_{FB2} > 3.0 V for more than 125 ms).
3. Standby condition (V_{FB2} < V_{stby} (0.75 V typical) and then V_{FB2} < $V_{stby−out}$ (1.25 V typical) for more than 125 ms).
4. Insufficient operating supply voltage (V_{CC2} < $V_{CC2(off)}$ (7.7 V typical)).
5. Overvoltage protection (OVP) latch activated from CS2 pin (Pin 3) (V_{CS2} > V_{OVP} (3.0 V typical)).
6. Thermal shutdown latch in the PWM section activated when the junction temperature is over typical 150°C.

The UVLO start thresholds of V_{CC1} is $V_{CC1(on)}$ (10.5 V typical) and the maximum allowable limit is 18 V. On the other hand, the V_{aux} is enabled when V_{CC2} is over $V_{CC2(off)}$ (7.7 V typical). Hence, there are two possible operating regions in Figure 49. In the non−usable region the V_{aux} is not high enough to turn on the PFC section. **Therefore, the flyback transformer auxiliary winding must be between $V_{CC1(on)}$ (10.5 V typical) and 18 V**.

Regulation in the PWM Section

The PWM section (or the second stage) of the NCP1603 is NCP1230 that is a current−mode fixed−frequency PWM flyback controller with internal compensation ramp. The simplified block diagram of the duty cycle regulation section is in Figure 50. A 100 kHz clock oscillator is modulated by adding a frequency jittering feature. This modulated 100 kHz clock signal turns the Out2 (pin 13) high in each switching cycle. The Out2 goes low when the current−loop feedback signal intersects with the output voltage−loop feedback signal. A duty cycle is therefore generated. The maximum duty ratio is limited to D_{max} (80% typical).

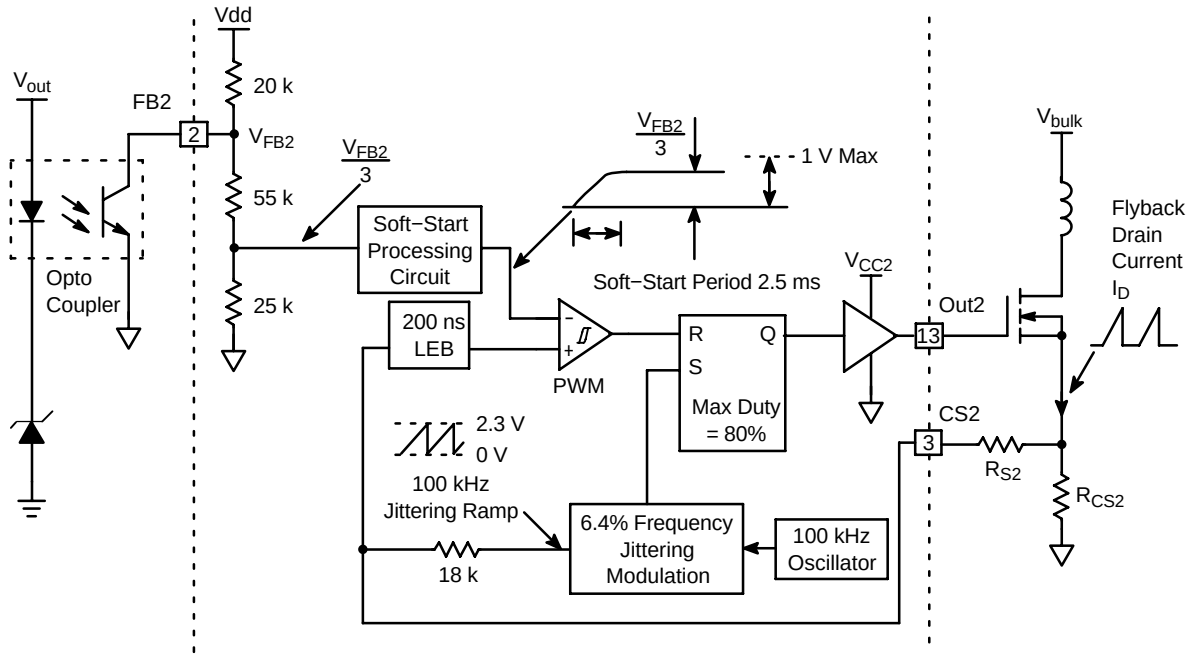


Figure 50. Block Diagram of Duty Cycle Regulation in the PWM Section

The current−loop feedback circuit consists of a typical 200 ns Leading Edge Blanking (LEB) that is to prevent a premature reset of the output due to noise, a pair of sense resistors R_{CS2} and R_{S2} that sense the flyback drain current I_D, and a 0−to−2.3 V jittering ramp that adds a ramp compensation for a stability improvement to the current−mode control possibly in continuous mode operation.

The V_{FB2} is approximately divided by 3 by an internal pair of resistors (55 kΩ and 25 kΩ). The soft−start processing circuit reduces the initial voltage−loop feedback signal (V_{FB2} / 3) for 2.5 ms. After this 2.5 ms, the soft−start disappears. As a result, the startup envelope of the peak drain current (or duty ratio) ramps up gradually for 2.5 ms. It is noted that the 2.5 ms is counted when the PWM die circuit is reset that is when V_{CC2} reaches $V_{CC2(on)}$ (12.6 V typical). This soft−start feature offers a reduced transient voltage and current stress on the power circuit during the startup.

Excessive output voltage causes more the optocoupler current. It pulls down the V_{FB2} through FB2 pin (Pin 2) and generates a lower duty ratio. The output voltage reduces. Insufficient output voltage reduces the optocoupler current. If the current is too small, the V_{FB2} is eventually pulled high than 3.0 V (3.8 V typical). The (V_{FB2} /3) signal is then clamped to an internal 1.0 V limit. If the ramp is ignored (i.e., R_{S2} = 0), the maximum possible drain current is derived as:

$$I_{D(max)} = \frac{1\ V}{R_{CS2}} \qquad \text{(eq. 2)}$$

It is noted that resistor R_{S2} will affect the percentage of the ramp getting compared for the modulation. Hence, a large value of the R_{S2} increase the ramp and will reduce the possible maximum duty ratio.

Frequency Jittering

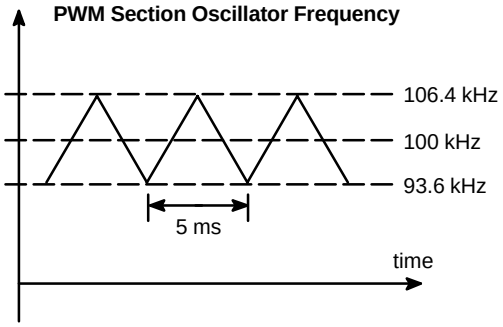


Figure 51. Frequency Jittering of PWM Oscillator

Frequency jittering is a method used to soften the EMI signature by spreading the energy in the vicinity of the main switching component. The PWM Section offers a typical ±6.4% deviation on the nominal switching frequency (100 kHz typical). A sweep sawtooth modulates the 100 kHz clock up and down with a 5.0 ms period. Figure 51 illustrates the ±6.4% variation of the jittering oscillator frequency versus time.

Fault Condition

Figure 52 illustrates the fault detection circuitry and its timing diagram. When fault (or output short circuit) happens, the output voltage collapses and the optocoupler is opened. V_{FB2} is internally pulled to be higher than 3.0 V (3.8 V typical). Then, the controller activates an error flag when (V_{FB2}/3) is greater than the soft−start voltage V_{SS} that is 1.0 V after the 2.5 ms from startup.

When the circuit is powering up in the beginning, the output voltage is not yet established and FB2 pin (Pin 2) is opened. Therefore, there is a 125 ms timer to allow the circuit to establish an initial output voltage. Then, a fault (or short circuit) condition is recognized when an error flag ($V_{FB2} \geqslant 3.0$ V) can last for 125 ms. When a fault is detected, Out2 (Pin 13) goes low. The power supply stops delivering power to the output. On the other hand, the V_{aux} (= V_{CC1}) also goes low. The V_{aux} will restore immediately when the error flag disappears.

This fault detection method offers advantage of getting rid of the auxiliary winding information that cannot truely represent the output voltage when the flyback transformer is badly coupled.

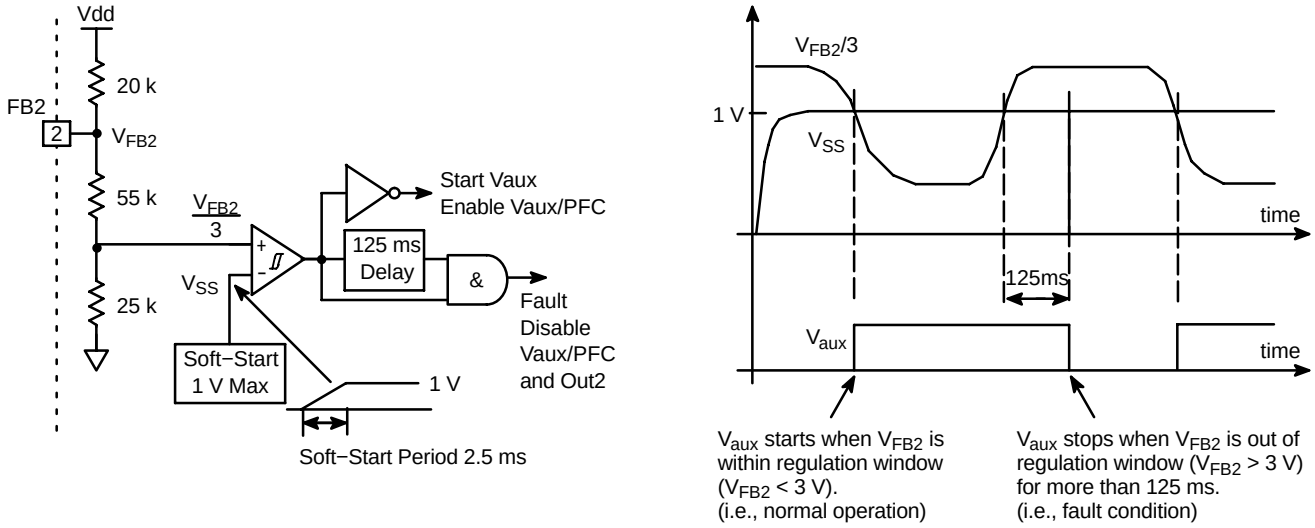


Figure 52. Block Diagram and Timing Diagram of Fault Detection

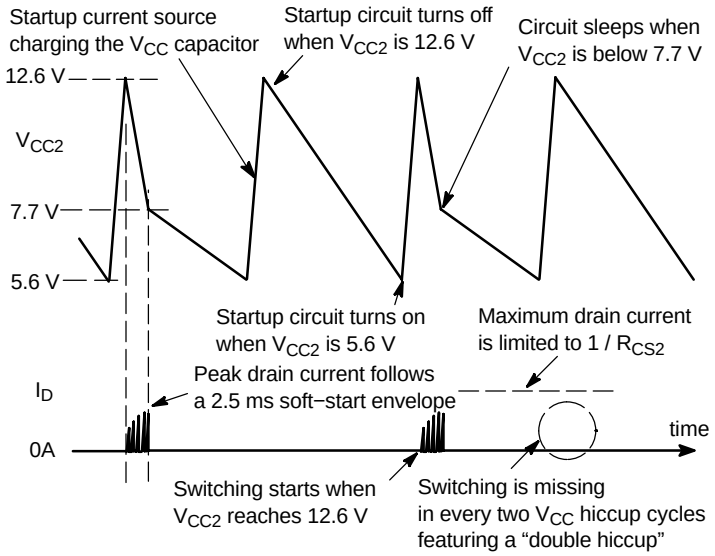


Figure 53. Timing Diagram of Fault Condition

Figure 53 illustrates the timing diagram of V_{CC2} and the second−stage drain current I_D in fault condition. The V_{CC} drops because output voltage collapses. When V_{CC} drops below $V_{CC(off)}$ (7.7 V typical), the Drive Output signal disappears and the V_{CC} continues to drop. When bias voltage V_{CC} drops to $V_{CC(latch)}$ (5.6 V typical), the startup current source activates and charge up the V_{CC} until V_{CC} reaches $V_{CC(on)}$ (12.6 V typical). The internal 2.5 ms soft−start activates after V_{CC} reaches $V_{CC(on)}$ (12.6 V typical). The peak drain current follows its 2.5 ms envelope. The power supply dissipates some power due to the switching signal of Out2 and waits for possible auto−recovery of operation when the fault is cleared.

As shown in Figure 53, NCP1603 has a “double hiccup” feature that allows the drain current in every two V_{CC} hiccup cycle in fault condition. The “double hiccup” feature offers fewer power dissipation during fault condition comparing to “single hiccup”.

If the fault is cleared (V_{FB2} < 3.0 V_{SS}) and V_{CC} remains above $V_{CC2(off)}$ (7.7 V typical), the circuit will resume its operation. Otherwise, the V_{CC} will continue this 12.6−7.7−5.6−12.6 V hiccup mode until the fault or bulk voltage is cleared.

Standby Condition

The output voltage rises up excessively in standby condition and the V_{FB2} drops. A set point of 25% of the maximum of V_{FB2} (i.e., 3.0 V) is defined to be the standby threshold. Hence, the standby threshold is V_{stby} = 25% × 3.0 V = 0.75 V.

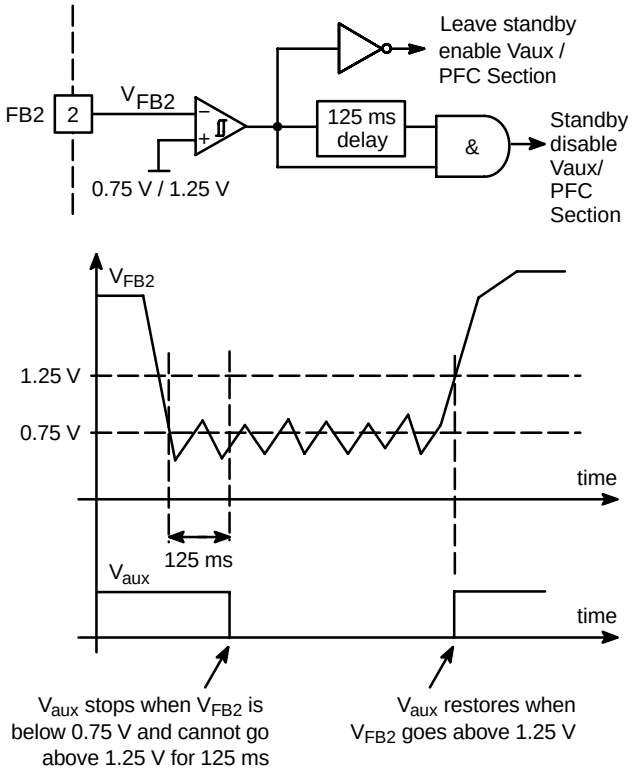


Figure 54. Block Diagram and Timing Diagram of Standby Detection

Figure 54 illustrates the standby detection circuitry and its timing diagram. When standby condition happens (i.e., V_{FB2} < 0.75 V), the controller will wait for a typical 125 ms to ensure that the output power remains low for a while. Then, the V_{aux} is disabled to shut down the PFC section for power saving. The V_{aux} (or the PFC) restores when V_{FB2} goes above 1.25 V immediately because V_{FB2} can be possibly above the 0.75 V threshold during standby operation (referring to Figure 55) and the PFC section is needed after the circuit restores from standby condition.

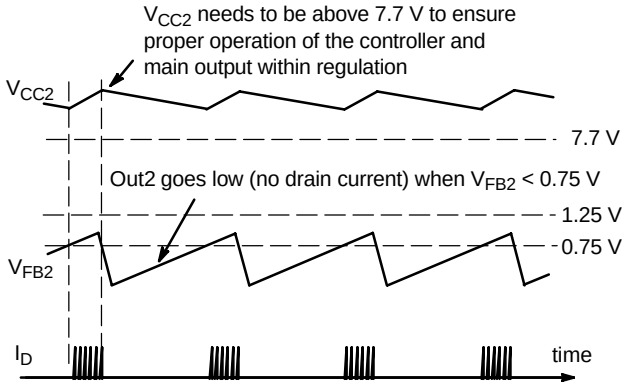


Figure 55. Timing Diagram in Standby Condition

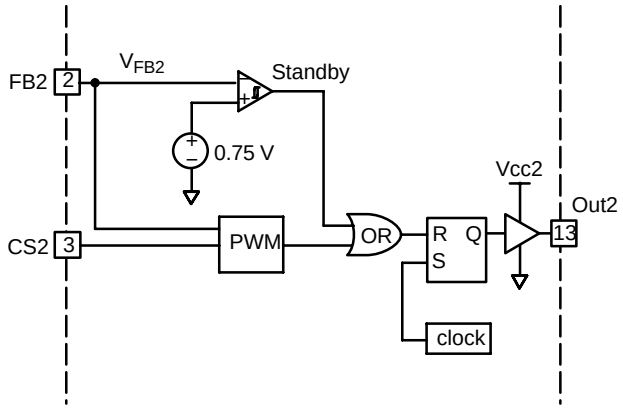


Figure 56. Block Diagram in Standby Operation in PWM Section

Figure 55 and 56 show the timing diagram and block diagram of the standby operation respectively. A skipping cycle behavior of the drain current is made by reset the latch whenever V_{FB2} is smaller than 0.75 V. When V_{FB2} is greater than 0.75 V, the duty ratio is modulated by the PWM block that is illustrated in Figure 50.

PFC in Discontinuous/Critical Mode

The PFC section of the NCP1603 is NCP1601 that is designed for low−power PFC boost circuit in DCM or CRM and takes advantages on both operating modes. DCM limits the maximum switching frequency. It simplifies the front−ended EMI filter design. CRM limits the maximum currents of diode, MOSFET and inductor. It reduces the costs and improves the reliability of the circuit. This device substantially exhibits unity power factor while operating in DCM and CRM. It minimizes the number of external components.

The PFC section primarily designed to operate in fixed−frequency DCM. In the most stressful conditions, CRM can be an alternative option that is without power factor degradation. On the other hand, the PFC section can be viewed as a CRM controller with a frequency clamp (maximum switching frequency limit) alternative option that is also without power factor degradation. In summary, the PFC section can cover both CRM and DCM without power factor degradation. Based on the selections of the boost inductor and the oscillator frequency, the circuit is capable of the following three applications.

1. CRM only by setting the oscillator frequency higher than the CRM frequency range.
2. CRM and DCM by setting the oscillator frequency somewhere within the CRM frequency range.
3. DCM only by setting the oscillator frequency lower than the CRM frequency range.

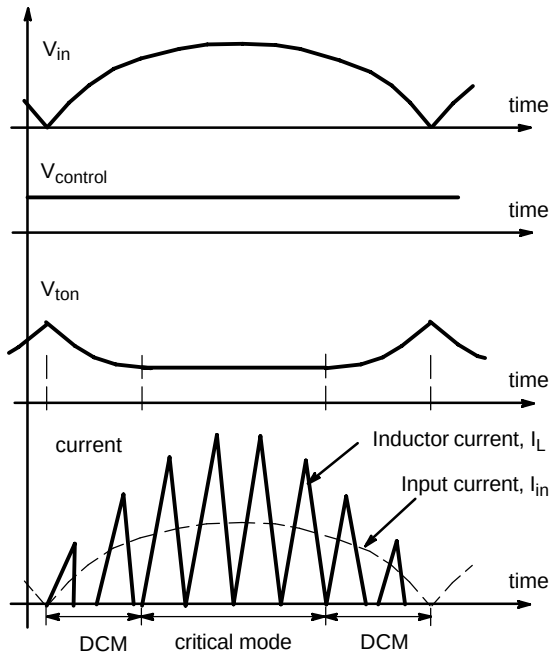


Figure 57. Timing Diagram of the PFC Stage

DCM needs higher peak inductor current comparing to CRM in the same averaged input current. Hence, CRM is generally preferred at around the sinusoidal peak for lower the maximum current stress but DCM is also preferred at the non−peak region to avoid excessive switching frequencies. Because of the variable−frequency feature of the CRM and constant−frequency feature of DCM, switching frequency is the maximum in the DCM region and hence the minimum switching frequency will be found at the moment of the sinusoidal peak.

DCM PFC Circuit

A DCM/CRM PFC boost converter is shown in Figure 58. Input voltage is a rectified 50 or 60 Hz sinusoidal signal. The MOSFET is switching at a high frequency (typically around 100 kHz) so that the inductor current I_L basically consists of high−frequency and low−frequency components.

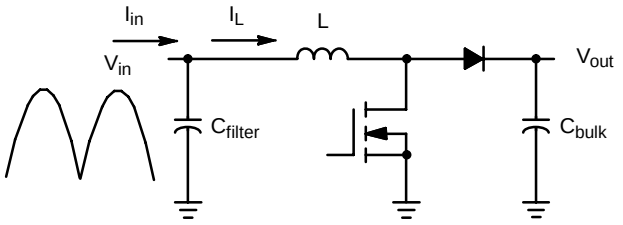


Figure 58. DCM/CRM PFC Boost Converter

Filter capacitor C_{filter} is an essential and very small value capacitor in order to eliminate the high−frequency content of the DCM inductor current I_L. This filter capacitor cannot be too bulky because it can pollute the power factor by distorting of the rectified sinusoidal input voltage.

PFC Methodology

The PFC section uses a proprietary PFC methodology particularly designed for both DCM and CRM operation. The PFC methodology is described in this section.

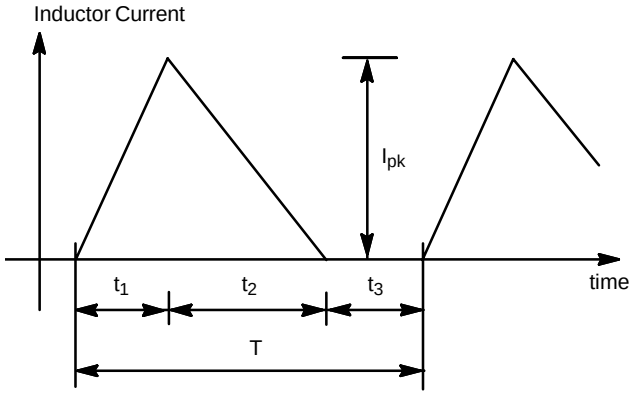


Figure 59. Inductor Current in DCM

As shown in Figure 59, the inductor current I_L of each switching cycle starts from zero in DCM. CRM is a special case of DCM when $t_3 = 0$. When the PFC boost converter MOSFET is on, the inductor current I_L increases from zero to I_{pk} for a time duration t_1 with inductance L and input voltage V_{in}. Equation 3 is formulated.

$$V_{in} = L\frac{I_{pk}}{t_1} \qquad \text{(eq. 3)}$$

The input filter capacitor C_{filter} and the front−ended EMI filter absorb the high−frequency component of inductor current. It makes the input current I_{in} a low−frequency signal.

$$I_{in} = \frac{I_{pk}\,(t_1 + t_2)}{2\,T} \quad \text{for DCM} \qquad \text{(eq. 4)}$$

$$I_{in} = \frac{I_{pk}}{2} \quad \text{for CRM} \qquad \text{(eq. 5)}$$

From Equations 3, 4, and 5, the input impedance Z_{in} is formulated.

$$Z_{in} = \frac{V_{in}}{I_{in}} = \frac{2TL}{t_1(t_1 + t_2)} \quad \text{for DCM} \qquad \text{(eq. 6)}$$

$$Z_{in} = \frac{V_{in}}{I_{in}} = \frac{2L}{t_1} \quad \text{for CRM} \qquad \text{(eq. 7)}$$

Power factor is corrected when the input impedance Z_{in} in Equations 6 and 7 are constant or slowly varying.

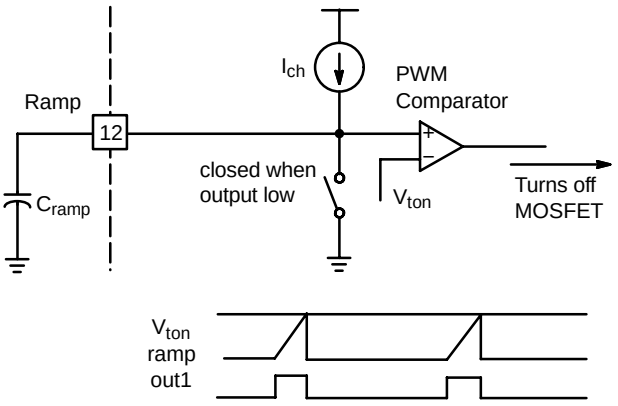


Figure 60. PFC Modulation Circuit and Timing Diagram

The MOSFET on time t_1 of PFC modulation duty is generated by a feedback signal V_{ton} and a ramp. The PFC modulation circuit and timing diagram are shown in Figure 60. A relationship in Equation 8 is obtained.

$$t_1 = \frac{C_{ramp}\,V_{ton}}{I_{ch}} \qquad \text{(eq. 8)}$$

The charging current I_{ch} is constant 100 μA current and the ramp capacitor C_{ramp} is constant for a particular design. Hence, according to Equation 8, the MOSFET on time t_1 is proportional to V_{ton}.

In order to protect the PFC modulation comparator, the maximum voltage of V_{ton} is limited to internal clamp $V_{ton(max)}$ (3.9 V typical) and the ramp pin (Pin 12) is with

a 9.0 V ESD zener diode. The 3.9 V maximum limit of this V_{ton} indirectly limits the maximum on time.

The $V_{control}$ processing circuit generates V_{ton} from control voltage $V_{control}$ and time information of zero inductor current. The circuit in Figure 61 makes Equations 9 and 10 where the value of resistor R_1 is much higher than the value of resistor R_2 ($R_1 >> R_2$).

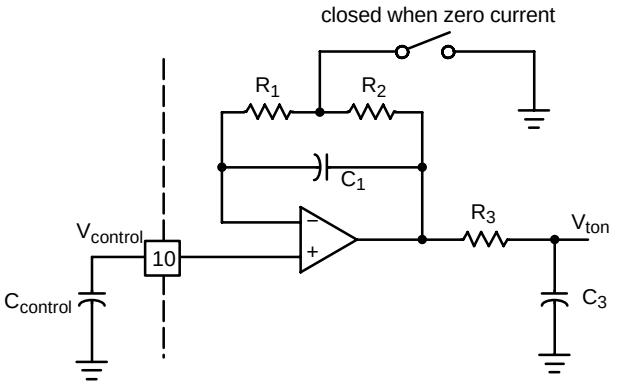


Figure 61. $V_{control}$ Processing Circuit

$$V_{ton} = \frac{T\,V_{control}}{t_1 + t_2} \quad \text{for DCM} \qquad \text{(eq. 9)}$$

$$V_{ton} = V_{control} \quad \text{for CRM} \qquad \text{(eq. 10)}$$

It is noted that V_{ton} is always greater than or equal to $V_{control}$ ($V_{ton} \geq V_{control}$).

In summary, the input impedance Z_{in} in Equation 11 is obtained from Equations 3 through 10.

$$Z_{in} = \frac{V_{in}}{I_{in}} = \frac{2LI_{ch}}{C_{ramp}\,V_{control}} \qquad \text{(eq. 11)}$$

Control voltage $V_{control}$ comes from the PFC boost circuit output voltage (i.e., bulk voltage V_{bulk}) that is a slowly varying signal. The bandwidth of $V_{control}$ can be additionally limited by inserting an external capacitor $C_{control}$ to the $V_{control}$ pin (Pin 10) in Figure 62. The internal 300 kΩ resistor and the capacitor $C_{control}$ create a low−pass filter that has a bandwidth $f_{control}$ in Equation 12. It is generally recommended to limit the bandwidth below 20 Hz to achieve power factor correction. Typical value of $C_{control}$ is 0.1 μF.

$$C_{control} > \frac{1}{2\pi 300k\Omega\, f_{control}} \qquad \text{(eq. 12)}$$

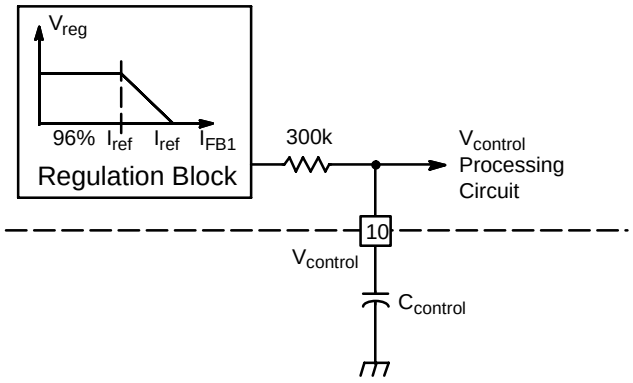


Figure 62. $V_{control}$ Low−Pass Filtering

If the bandwidth of $V_{control}$ is much less than the 50 or 60 Hz line frequency, the input impedance Z_{in} is slowly varying or roughly constant. Then, the power factor correction is achieved in DCM and CRM.

Maximum Power in PFC Section

Input and output power (P_{in} and P_{out}) are derived in Equations 13 and 14 when the circuit efficiency η is obtained or assumed. The variable V_{ac} stands for the RMS input voltage.

$$P_{in} = \frac{V_{ac}^2}{Z_{in}} = \frac{V_{ac}^2 C_{ramp} V_{control}}{2LI_{ch}} \qquad \text{(eq. 13)}$$

$$P_{out} = \eta\, P_{in} = \frac{\eta V_{ac}^2 C_{ramp} V_{control}}{2LI_{ch}} \qquad \text{(eq. 14)}$$

From Equations 13 and 14, control voltage $V_{control}$ controls the amount of output power, input power, or input impedance. The maximum value of the control voltage $V_{control}$ is 1.05 V (i.e., $V_{control(max)}$ = 1.05 V). A parameter called maximum power resistor R_{power} (10.5 kΩ typical) is defined in Equation 18 and restricted to have a maximum ±10% variation (i.e., 9.5 kΩ ≤ R_{power} ≤ 11.5 kΩ) for defining the maximum power in an application.

$$R_{power} = \frac{V_{control(max)}}{I_{ch}} = \frac{1.05\ V}{100\ \mu A} = 10.5\ k\Omega \qquad \text{(eq. 15)}$$

It means that the maximum input and output power ($P_{in(max)}$ and $P_{out(max)}$) are limited to ±10% variation.

$$P_{in(max)} = \frac{V_{ac}^2 C_{ramp} R_{power}}{2\ L} \qquad \text{(eq. 16)}$$

$$P_{out(max)} = \frac{\eta V_{ac}^2 C_{ramp} R_{power}}{2\ L} \qquad \text{(eq. 17)}$$

The maximum input current $I_{ac(max)}$ to deliver the maximum input power $P_{in(max)}$ is also derived in (eq.14). The suffix ac stands for RMS value.

$$I_{ac(max)} = \frac{P_{in(max)}}{V_{ac}} = \frac{V_{ac} C_{ramp} R_{power}}{2\ L} \qquad \text{(eq. 18)}$$

Feedback in PFC Section

The output voltage of the PFC circuit (i.e., bulk voltage V_{bulk}) is sensed as a feedback current I_{FB1} flowing into the FB1 pin (Pin 9) of NCP1603. The FB1 pin voltage V_{FB1} is typically smaller than 5.0 V referring to Figure 31. It is much lower than V_{bulk} that is typically 400 V. Therefore, V_{FB1} is generally neglected.

$$I_{FB1} = \frac{V_{bulk} - V_{FB1}}{R_{FB1}} \approx \frac{V_{bulk}}{R_{FB1}} \qquad \text{(eq. 19)}$$

where R_{FB1} is the feedback resistor connected the FB1 pin (Pin 9) and the output voltage referring to Figure 45.

Then, the feedback current I_{FB1} represents the bulk voltage V_{bulk} and will be used in the PFC section voltage regulation, undervoltage protection (UVP), and overvoltage protection (OVP).

Bulk Voltage Regulation in PFC Section

PFC−stage feedback current I_{FB1}, that presents bulk voltage V_{bulk} or the PFC−stage output voltage, is regulated with a reference current (I_{ref} = 203 μA typical) as shown in Figure 63. When I_{FB1} is lower than 96% of I_{ref}, the V_{reg} that is the output of the regulation block is as high as $V_{control(max)}$ (1.05 V typical) that it gives the maximum value on V_{ton} and the maximum MOSFET on time and V_{bulk} increases. When I_{FB1} is higher than I_{ref}, the V_{reg} becomes 0 V that gives no MOSFET on time and V_{bulk} decreases. As a result, the bulk voltage V_{bulk} is regulated around the range between 96% and 100% of the nominal value of $R_{FB1} \times I_{ref}$.

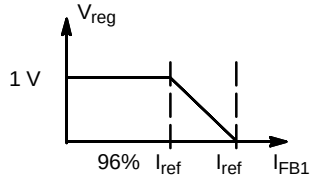


Figure 63. Regulation Block

Based on Equations 13 and 14 for a particular power level, the $V_{control}$ is inversely proportional to V_{ac}^2. Hence, in high V_{ac} condition $V_{control}$ is lower. It means that I_{FB1} or output voltage is higher based on the regulation block characteristic in Figure 63. In other words, the $V_{control}$ in the low V_{ac} condition is much higher than the high V_{ac} condition. In order to not over−design the circuit in the application, the $V_{control}$ in the low V_{ac} condition is usually very closed to $V_{control(max)}$. It makes the output voltage be almost 96% of the nominal value of $R_{FB1} \times I_{ref}$ in high V_{ac} condition.

The feedback resistor R_{FB1} consists of two or three high precision resistors in order to set the nominal V_{bulk} precisely and for safety purpose.

The regulation block output V_{reg} is connected to control voltage $V_{control}$ through an internal resistor $R_{control}$ (300 kΩ typical) for the low−pass filter in Figure 62. The $V_{control}$ and the time information of zero current are collected in the $V_{control}$ processing circuit to generate V_{ton} that is then compared to a ramp signal to generate the MOSFET on time t_1 for power factor correction.

Current Sense in PFC Section

The PFC section senses the inductor current I_L by the current sense scheme in Figure 64. This scheme has the advantages of: (1) the inrush current limitation by the resistor. R_{CS1}. and (2) the overcurrent protection and zero current detection implemented in the same pin.

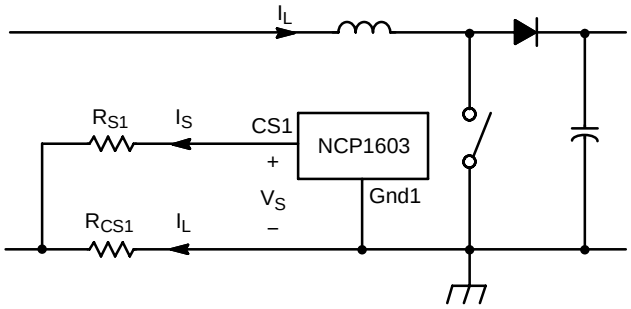


Figure 64. Current Sense in PFC Section

Inductor current I_L passes through R_{CS1} and creates a negative voltage. This voltage is measured by a current I_S flowing out of the CS1 pin (Pin 11). CS1 pin has an offset voltage V_S. This offset voltage is studied in the setting of zero inductor current $I_{L(ZCD)}$ and the maximum inductor current $I_{L(OCP)}$ (i.e., overcurrent protection threshold). A typical variation of offset voltage V_S versus sense current I_S is shown in Figure 35. Based on Figure 64, Equation 20 is derived.

$$V_S - R_{S1} I_S = -R_{CS1} I_L \qquad \text{(eq. 20)}$$

Zero Current Detection (ZCD) in PFC Section

The device recognizes zero inductor current when CS1 pin (Pin 11) sense current I_S is smaller than $I_{S(ZCD)}$ (14 μA typical). The offset voltage of the CS1 pin in this condition is $V_{S(ZCD)}$ (7.5 mV typical). The inductor current $I_{L(ZCD)}$ at the ZCD condition is derived in Equation 21.

$$I_{L(ZCD)} = \frac{R_{S1} I_{S(ZCD)} - V_{S(ZCD)}}{R_{CS1}} \qquad \text{(eq. 21)}$$

It is obvious that the $I_{L(ZCD)}$ is not always zero. In order to make it reasonably close to zero, the setting of R_{S1} and R_{CS1} are crucial.

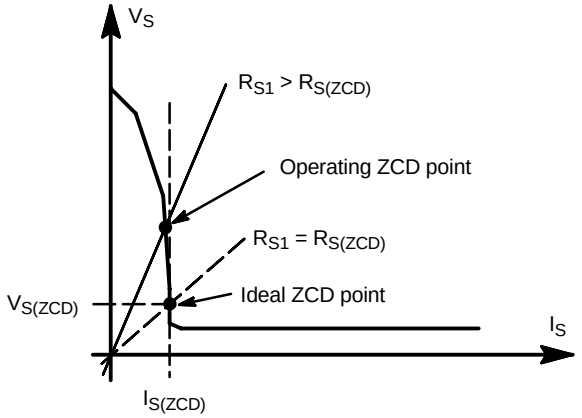


Figure 65. CS Pin Characteristic when $I_L = 0$

Based on the CS pin (Pin 4) characteristics in Figure 35, Figure 65 is studied here. When the inductor current is exactly zero (i.e., $I_{L(ZCD)} = 0$), the ideal ZCD point in the Figure 65 is reached where R_{S1} is $R_{S(ZCD)}$ (536 Ω typical). Considering the tolerance, the actual sense resistor R_{S1} is needed to be higher than the ideal value of $R_{S(ZCD)}$ to ensure that zero current signal is generated when sense current is smaller than the ZCD threshold (i.e., $I_S < I_{S(ZCD)}$). That is,

$$R_S > R_{S(ZCD)} = \frac{V_{S(ZCD)}}{I_{S(ZCD)}} \qquad \text{(eq. 22)}$$

The higher value of R_{S1} makes the bigger distance between the operating and ideal ZCD points in Figure 65. Hence, R_{S1} has to be as low value as possible. The best recommended value of R_{S1} is therefore the maximum of $R_{S(ZCD)}$ that is 1.0 kΩ.

Now that the R_{S1} is set at a particular value that is greater than $R_{S(ZCD)}$. From Equation 20, the operating lines in Equation 23 with different inductor currents I_L of Equation 20 are studied.

$$V_S = R_{S1}I_S - R_{CS1}I_L \qquad \text{(eq. 23)}$$

These operating lines are added in Figure 65 to formulate Figure 66. When the inductor current I_L is smaller than $I_{L(ZCD)}$, the sense current I_S is smaller than $I_{S(ZCD)}$ and hence the zero current signal is generated.

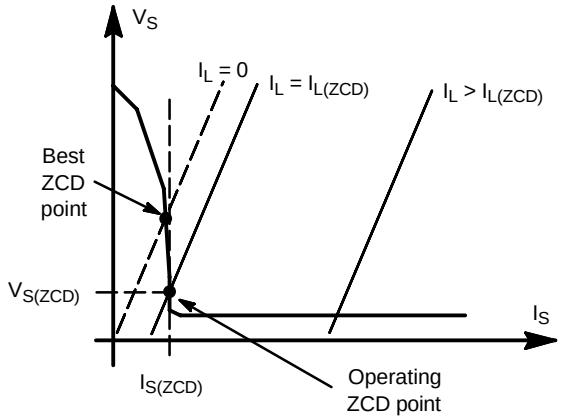


Figure 66. CS Pin Characteristic with Different Inductor Current

It is noted in Figure 66 and Equation 23 that when the (R_{CS1} I_L) term is smaller the error or distance between the lines to the line $I_L = 0$ is smaller. Therefore, the value of the current sense resistor R_{CS1} is also recommended to be as small as possible to minimize the error in the zero current detection.

Overcurrent Protection (OCP) in PFC Section

Overcurrent protection is reached when I_S is larger than $I_{S(OCP)}$ (200 μA typical). The offset voltage of the CS pin is $V_{S(OCP)}$ (3.2 mV typical) in this condition. That is:

$$I_{L(OCP)} = \frac{R_{S1}I_{S(OCP)} - V_{S(OCP)}}{R_{CS1}} \qquad \text{(eq. 24)}$$

When overcurrent protection threshold is reached, the Drive Output of the device goes low.

Oscillator/Synchronization Block in PFC Section

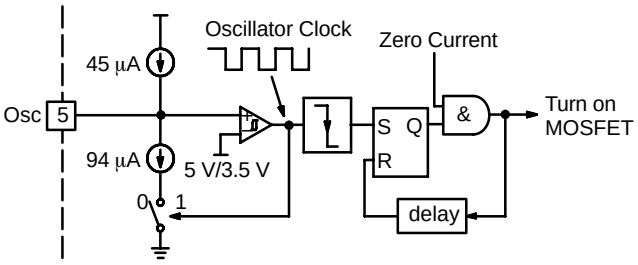


Figure 67. Oscillator / Synchronization Block in PFC Section

The PFC section is designed to operate in either DCM or CRM. In order to keep the operation in DCM and CRM only, the Drive Output cannot turn on as long as there is some inductor current flowing through the circuit. Hence, the zero current signal is provided to the oscillator/ synchronization block in Figure 67. An input comparator monitors the Osc pin (Pin 5) voltage and generates a clock signal. The negative edge of the clock signal is stored in a RS latch. When zero current is detected, the RS latch will be reset and a set signal is sent to the output drive latch that turns on the MOSFET in the PFC boost circuit. Figure 68 illustrates a typical timing diagram of the oscillator block.

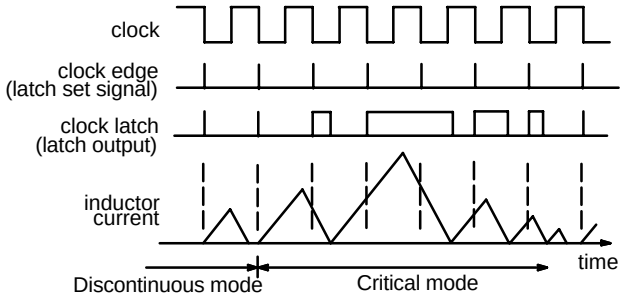


Figure 68. Oscillator Block Timing Diagram

Oscillator Mode in PFC Section

In oscillator mode, the Osc pin (Pin 5) is connected to an external capacitor C_{osc}. When the voltage of this pin is above $V_{sync(H)}$ (5.0 V typical), the pin sinks a current I_{odch} (94–45 = 49 μA typical) and the external capacitor C_{osc} discharges. When the voltage reaches $V_{sync(L)}$ (3.5 V typical), the pin sources a current I_{och} (45 μA typical) and the external capacitor C_{osc} is charged. It is noted that there is a typical 300 ns propagation delay and the 3.5 V and 5.0 V threshold conditions are measured on 220 pF C_{osc} capacitor. Hence, the actual oscillator hysteresis is a little bit smaller.

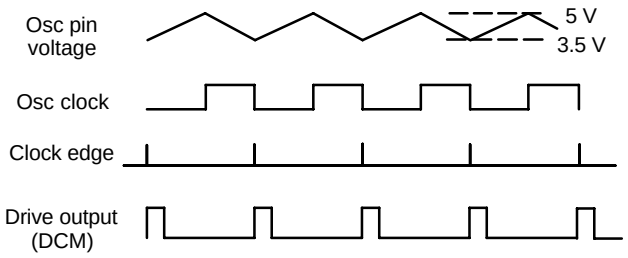


Figure 69. Oscillator Mode Timing Diagram in DCM

There is an internal capacitance $C_{osc(int)}$ (36 pF typical) in the oscillator pin and the oscillator frequency is to $f_{osc(max)}$ (405 kHz typical) when the Osc pin is opened. Hence, the oscillator switching frequency can be formulated in Equation 25 and represented in Figure 70.

$$C_{osc} = \frac{36\ pF \cdot 405\ kHz}{f_{osc}} - 36\ pF \qquad \text{(eq. 25)}$$

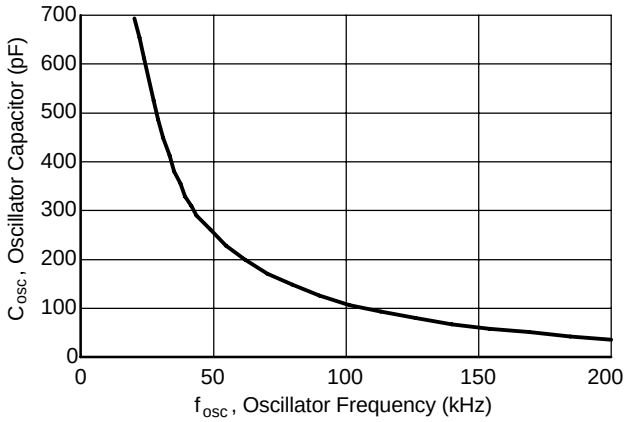


Figure 70. Osc Pin Frequency Setting

Synchronization Option

In synchronization mode, the Osc pin (Pin 5) receives an external digital signal with level high defined to be higher than $V_{sync(H)}$ (5.0 V typical) and level low defined to be lower than $V_{sync(L)}$ (3.5 V typical). An internal 9.0 V ESD Zener diode is connected to the Osc pin and hence the maximum allowable synchronization voltage is 9.0 V. The circuit recognizes a synchronization frequency by the time difference between two falling edge instants when the synchronization signal across the 3.5 V threshold point. The actual synchronization threshold point is a little bit higher than the 3.5 V threshold point. The minimum synchronization pulse width is 500 ns.

There is a typical 350 ns propagation delay from synchronization threshold point to the moment of output goes high and there is also a typical 300 ns propagation delay from the synchronization threshold point to the moment of crossing 3.5 V. Hence, the output goes high apparently when the sync signal turns to 3.5 V. A timing diagram of synchronization mode is summarized in Figure 71.

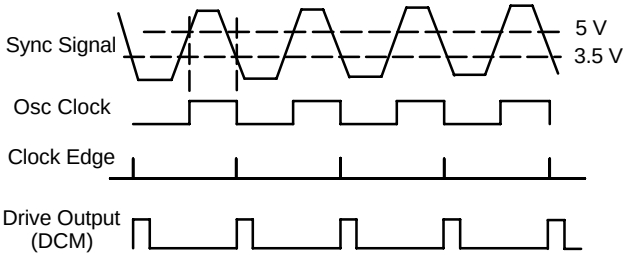


Figure 71. Synchronization Mode Timing Diagram in DCM

The PWM and PFC Section can be synchronized together in order to minimize some of the ripple current in the bulk capacitor as shown in Figure 72 and 73. The Out2 pin (Pin 13) is the external synchronization signal in Figure 71 to the PFC Section. When the Out2 is in high state, the voltage is potentially higher than the maximum allowable voltage in Osc pin (Pin 5). Hence, a pair of resistors divides the voltage from Out2 reduces the voltage

entering Osc pin and a capacitor is added to remove some possible noise As a result, the current in Figure 73 may not necessarily passes through the bulk capacitor for fewer ripple current there.

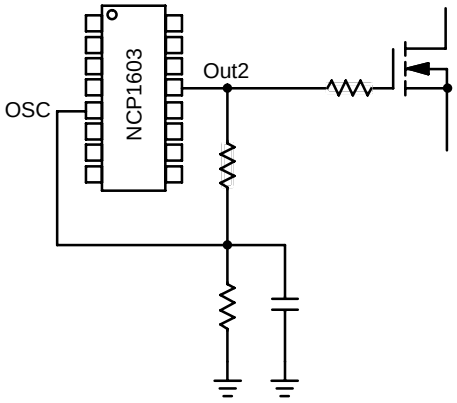


Figure 72. Synchronization Configuration

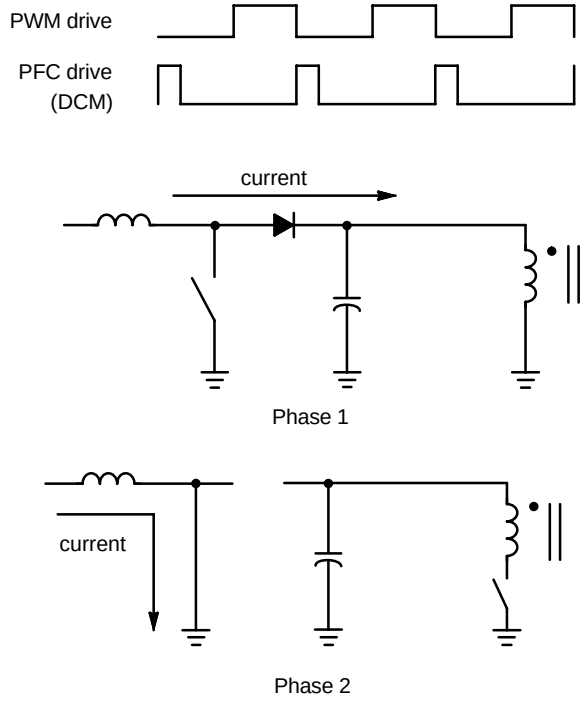


Figure 73. Synchronization Timing Diagram

Output Drive

The output stages of the PFC section and PWM section are designed for direct drive of power MOSFET. However, it is recommended to connect a current limiting resistor to the gate of the power MOSFET. The PFC section output is capable of up to −500 mA and +750 mA peak drive current and has a typical rise and fall time of 53 and 32 ns with a 1.0 nF load while the PWM section output is capable of up to ±1.0 A peak drive current and has a typical rise and fall time of 40 ns and a fall time of 15 ns with a 1.0 nF capacitive load.

Safety Features of NCP1603

(1) Bulk Voltage Overvoltage Protection (OVP)

When the PFC feedback current I_{FB1} is higher than 107% of the reference current I_{ref} (i.e., the bulk voltage V_{bulk} is higher than 107% of its nominal value), the PFC Drive Output pin (Pin 7) of the device goes low for protection and the switch of the $V_{control}$ processing circuit is kept off. The circuit automatically resumes operation when the output voltage is lower than 107%.

The maximum OVP threshold is limited to 225 μA that corresponds to 225 μA × 1.95 MΩ + 5.0 V = 443.75 V when R_{FB1} = 1.95 MΩ (e.g., 910 kΩ + 910 kΩ + 130 kΩ) and V_{FB1} = 5.0 V (for the worst case referring to Figure 31). Hence, it is generally recommended to use 450 V rating output capacitor to allow some design margin.

(2) Bulk Voltage Undervoltage Protection (UVP)

When the PFC feedback current I_{FB1} is smaller than 8% of the reference current I_{ref}, the PFC section is shutdown and consumes less than 50 μA. In normal situation of the boost converter configuration, the output bulk voltage V_{bulk} is always higher than input voltage V_{in} and the I_{FB1} is higher than 8% of the reference current. It enables the PFC section to operate. Hence, UVP happens when the bulk voltage V_{bulk} is abnormally under−voltage, the FB1 pin (Pin 9) is opened, or the FB1 pin (Pin 9) is manually pulled low.

(3) PFC−Stage Overcurrent Protection

When the PFC sense current I_{S1} is higher than typically 200 μA, the PFC Drive Output (Pin 7) goes low. It represents the PFC−stage inductor current i_L exceeds a user−defined value. The operation automatically resumes when the inductor current becomes lower than this user−defined value at the next clock cycle.

(4) PWM−Stage Short−Circuit Protection

When V_{FB2} remains higher than 3.0 V for 125 ms, a fault is recognized. The PFC−stage (i.e., V_{aux}) will be disabled and the V_{CC2} will operate a double hiccup shown in Figure 53. The operation will be self−recovered if V_{CC2} is above 7.7 V and V_{FB2} is below 3.0 V. This fault protection is implemented by a timer and independent of badly coupled auxiliary transformer winding.

(5) Latched V_{CC} Overvoltage Protection

The normal operating voltage range of the CS2 pin (Pin 3) is between 0 V and I_{limit} (1.0 V typical). When the voltage is above 1.0 V, the Out2 (Pin 13) goes low. When the voltage increases above 3.0 V, the Out2 goes low and stays latched off until the circuit is reset by unplugging from main supply to make V_{CC2} drop below $V_{CC(reset)}$ (4.0 V typical). This feature also offers the designer the flexibility to implement an externally pull−high latched protection or latched shutdown circuit.

In order to prevent wrongly triggering the latch protection function, it is generaly recommended to put a pF−order decoupling ceramic capacitor across the CS2 pin to remove possible high−frequency noise there.

To set the V_{CC} overvoltage protection, the circuit is configured in Figure 74. A PNP bipolar transistor is added to open the Zener diode Z_{OVP} when Out2 is high in order to stop any interference of the normal operation of current sense. It is because the Zener diode easily pulls high the CS2 pin voltage to 1.0 V and that interferes with the normal operation of the current sense when the output is high. The OVP threshold $V_{CC2(OVP)}$ is expressed in Equation 26.

$$V_{CC2(OVP)} = V_{ZOVP} + 3\ V \qquad \text{(eq. 26)}$$

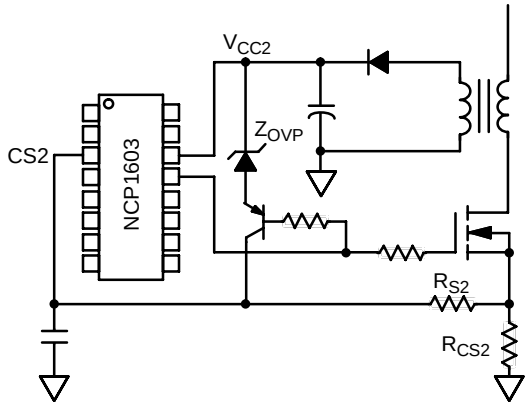


Figure 74. V_{CC} Latched OVP Application Circuit

(6) Latched Overvoltage Protection (OVP)

As long as an external protection on CS2 pin (Pin 3) does not affect the normal regulation operation of current sense, the protection can be implemented. An alternative is to implement the output overvoltage protection by an optocoupler in Figure 75. The leakage current of the added circuit is up to the zener diode at the output voltage. When there is no overvoltage, the leakage is small and it does not affect the normal operation. A resistor paralleled to the optocoupler is added to share the potential increasing leakage current of the zener diode due to temperature variation. The Zener diode at the output voltage is recommended to be a 1 mA operating current at the threshold voltage. Then, this current is coupled through the optocoupler and inserts a similar order of current (depending on the current−transfer−ratio CTR of the optocoupler) into CS2 pin. The CS2 pin is capable of up to 100 mA and with an internal 9 V anti−parallel ESD diode but it is recommended to put a 8.2 V Zener diode there to further protect the pin.

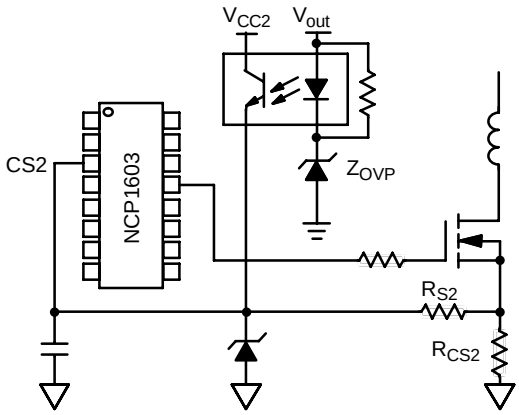


Figure 75. Output Latched OVP Application Circuit

(7) Dual Thermal Shutdown (TSD)

The NCP1603 consists of two individual dies that incorporates their individual thermal shutdown. The PFC thermal circuitry disables the PFC gate drive Out1 and then keeps the power switch off when its junction temperature exceeds 170 °C typically. The PFC gate drive Out1 is then enabled once the temperature drops below typically 125°C (i.e., 45°C hysteresis).

The PWM thermal circuitry disables the PWM gate drive Out2 and then keeps the power switch off when its junction temperature exceeds 165°C typically. The PWM gate drive Out2 is then enabled once the temperature drops below typically 140°C and the circuit is unplugged (to make V_{CC2} drops below 4.0 V).

PFC Toggling

The variation of the duty ratio in the PWM stage between the PFC−on or PFC−off can be very large. When the NCP1603 circuit is operating at some conditions between PFC on and off boundary, the duty ratio variation can lead to unwanted on/off toggling in the PFC stage. A current feedforward resistor R_{FF} is hence recommended to added between V_{aux} and CS2 pin (pins 1 and 3) in Figure 76 to prevent the toggling. The value of R_{FF} is much larger than current sense feedback resistor R_{S2} and plays very little effect when V_{aux} = 0 (or PFC is off). When V_{aux} is available (or PFC is on), the R_{FF} creates a positive offset on the CS2 pin voltage and it allows the feedback voltage V_{FB2} to only shift slightly but provide a dramatic duty cycle reduction in Figure 77. It slight movement of the feedback voltage can reduce the change to reach the PFC stage on/off threshold. Hence, the current feedforward resistor can help to improve the toggling.

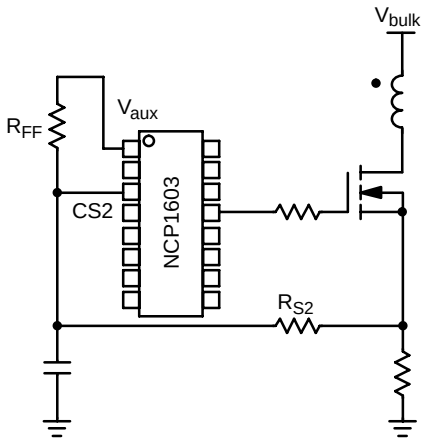


Figure 76. Feedforward Resistor R_{FF} Added

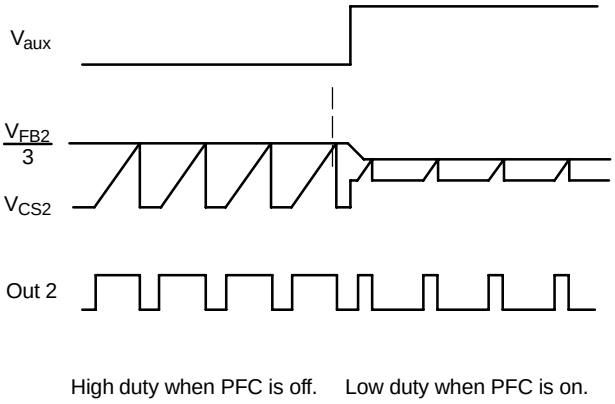


Figure 77. Timing Diagram of PWM Stage When R_{FF} is Added

PACKAGE DIMENSIONS

SO−16
D SUFFIX
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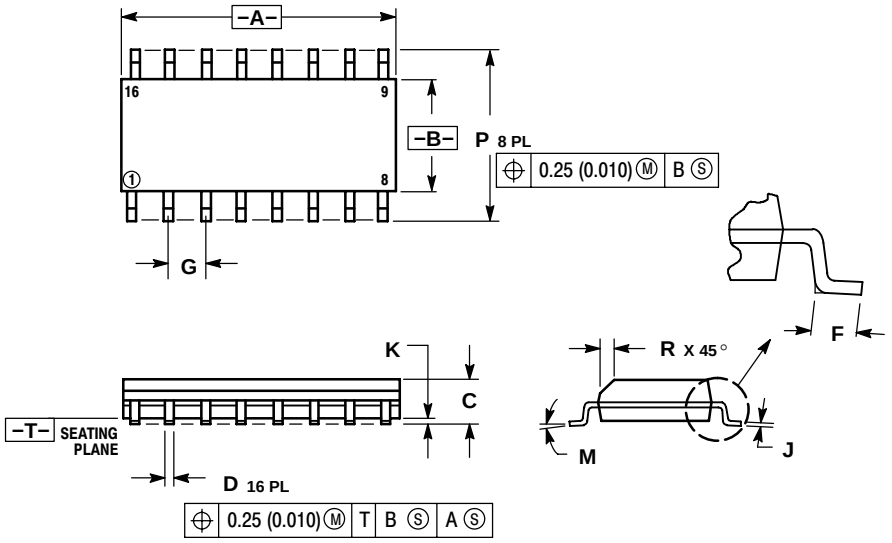

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

The products described herein (NCP1603), may be covered by one or more of the following U.S. patents: 6,271,735, 6,362,067, 6,385,060, 6,597,221, 6,970,365. There may be other patents pending.

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