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**Datasheet for:**

# **MicroSD Card 3.0**

PSFUSDxxxxCxxxx

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## Revision History

| Date     | Revision | Description                                                                     | Checked by |
|----------|----------|---------------------------------------------------------------------------------|------------|
| 11/13/18 | A        | Initial release based on<br>PSFUSDxxxxQxxxx_C (9/04/18)<br>Add VAFUSD128GCEZVH2 |            |
|          |          |                                                                                 |            |
|          |          |                                                                                 |            |

## Ordering Information

| Spec   | Viking P/N       | Grade | NAND Process | Density GB | Temperature |
|--------|------------------|-------|--------------|------------|-------------|
| SD 3.0 | VAFUSD016GCE1WT3 | C     | TSB 3D TLC   | 16         | 0 to 70°C   |
| SD 3.0 | VAFUSD032GCE5WT3 | C     | TSB 3D TLC   | 32         | 0 to 70°C   |
| SD 3.0 | VAFUSD032GCEBVH2 | C     | SK Hynix MLC | 32         | 0 to 70°C   |
| SD 3.0 | VAFUSD064GCEAVH2 | C     | SK Hynix MLC | 64         | 0 to 70°C   |
| SD 3.0 | VAFUSD128GCEZVH2 | C     | SK Hynix MLC | 128        | 0 to 70°C   |

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# 1 Introduction

Viking SSD's offer the highest flash storage reliability and performance as well as support for many functional features.

## 1.1 Features

- Bus Speed Mode
  - UHS-I
  - Non-UHS
- Speed Class
  - Class 2/6/10
- Power Consumption<sup>Note</sup>
  - Power Up Current < 250uA
  - Standby Current < 1000uA
  - Read Current < 400mA
  - Write Current < 400mA
- CPRM (Content Protection for Recordable Media)
- Advanced Flash Management
  - Static and Dynamic Wear Leveling
  - Bad Block Management
- Write Protect with mechanical switch
- Supply Voltage 2.7 ~ 3.6V
- Temperature Range
  - Operation: 0°C ~ 70°C
  - Storage: -40°C ~ 85°C
- RoHS compliant
- EMI compliant

NOTE: Please see Chapter on Power Consumption for details



- Performance Overview

| Capacity | Class | UHS-I           | Flash    | TestMetrix Test Test 500MB |              |
|----------|-------|-----------------|----------|----------------------------|--------------|
|          |       |                 | Density  | Read (MB/s)                | Write (MB/s) |
| 0.512GB  | CL6   | Non-UHS         | .512Gb*1 | 23                         | 17           |
| 1GB      | CL6   | Non-UHS         | .512Gb*2 | 23                         | 22           |
| 2GB      | CL6   | Non-UHS         | .512Gb*4 | 23                         | 22           |
| 4GB      | CL10  | UHS-I (Grade 1) | 4Gb*1    | 35                         | 35           |
| 8GB      | CL10  | UHS-I (Grade 1) | 4Gb*2    | 35                         | 35           |
| 16GB     | CL10  | UHS-I (Grade 1) | 8Gb*2    | 35                         | 35           |
| 32GB     | CL10  | UHS-I (Grade 1) | 8Gb*4    | 35                         | 35           |
| 64GB     | CL10  | UHS-I (Grade 1) | 16Gb*2   | 35                         | 35           |
| 128GB    | CL10  | UHS-I (Grade 1) | 32Gb*2   | 35                         | 35           |

## 1.2 General Description

The Micro Secure Digital (MicroSD) card version 3.0 is fully compliant with the standards released by the SD Card Association. The Command List supports [Part 1 Physical Layer Specification Ver3.01 Final] definitions. Card capacities of non-secure area and secure area support [Part 3 Security Specification Ver3.0 Final]

The MicroSD 3.0 card has a 9-pin interface, designed to operate at a maximum frequency of 208MHz. It can alternate communication protocol between the SD mode and SPI mode. It performs data error detection and correction with very low power consumption. The Card capacity could be more than 64GB and up to 2TB in the future with ex-FAT file system, which is called SDXC (Extended Capacity SD Memory Card). Secure Digital 3.0 cards are one of the most popular cards today due to its high performance, good reliability and wide compatibility.

## 1.3 Flash Management

### 1.3.1 Error Correction Code (ECC)

Flash memory cells will deteriorate with use, which might generate random bit errors in the stored data. Thus, Viking MicroSD cards apply the BCH ECC Algorithm, which can detect and correct errors occur during Read process, ensure data been read correctly, as well as protect data from corruption.

### 1.3.2 Wear Leveling

NAND Flash devices can only undergo a limited number of program/erase cycles, and in most cases, the flash media are not used evenly. If some area get updated more frequently than

others, the lifetime of the device would be reduced significantly. Thus, Wear Leveling technique is applied to extend the lifespan of NAND Flash by evenly distributing write and erase cycles across the media.

Viking provides advanced Wear Leveling algorithm, which can efficiently spread out the flash usage through the whole flash media area. Moreover, by implementing both dynamic and static Wear Leveling algorithms, the life expectancy of the NAND Flash is greatly improved.

### **1.3.3 Bad Block Management**

Bad blocks are blocks that include one or more invalid bits, and their reliability is not guaranteed. Blocks that are identified and marked as bad by the manufacturer are referred to as “Initial Bad Blocks”. Bad blocks that are developed during the lifespan of the flash are named “Later Bad Blocks”. Viking implements an efficient bad block management algorithm to detect the factory-produced bad blocks and manages any bad blocks that appear with use. This practice further prevents data being stored into bad blocks and improves the data reliability.

## 2 PRODUCT SPECIFICATIONS

### 2.1 Summary

- Support MicroSD system specification version 3.0
- Card capacity of non-secure area and secure area support  
[Part 3 Security Specification Ver3.0 Final] Specifications
- Support MicroSD SPI mode
- Designed for read-only and read/write cards
- Bus Speed Mode (use 4 parallel data lines)
  - Non-UHS Mode
    - Default speed mode: 3.3V signaling, frequency up to 25MHz, up to 12.5 MB/sec
    - High speed mode: 3.3V signaling, frequency up to 50MHz, up to 25 MB/sec
  - UHS Mode
    - SDR12: SDR up to 25MHz, 1.8V signaling
    - SDR25: SDR up to 50MHz, 1.8V signaling
    - SDR50: 1.8V signaling, frequency up to 100MHz, up to 50 MB/sec
    - SDR104: 1.8V signaling, frequency up to 208MHz, up to 104MB/sec
    - DDR50: 1.8V signaling, frequency up to 50MHz, sampled on both clock edges, up to 50MB/sec

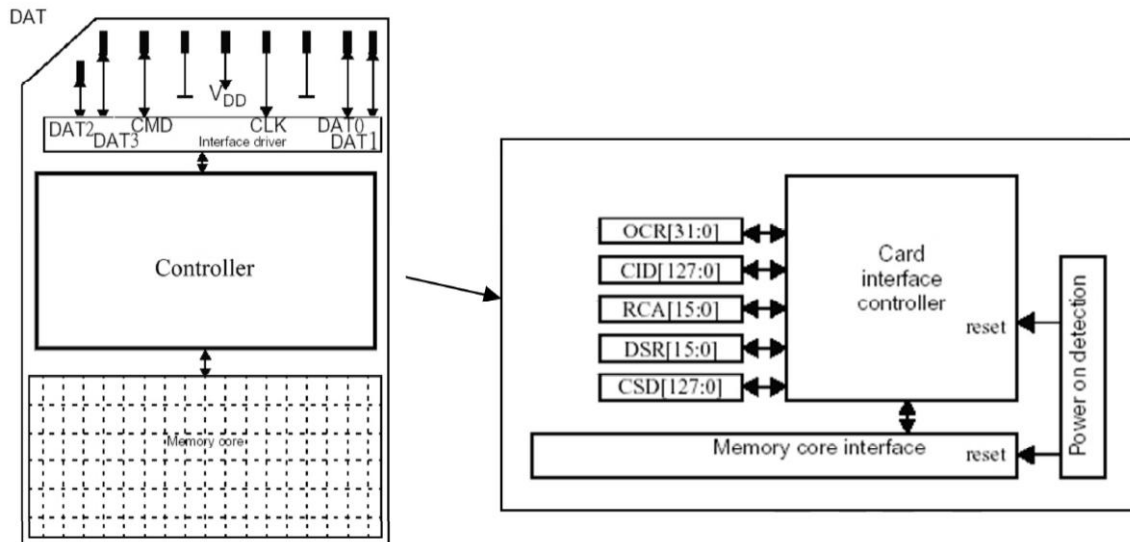
#### NOTES:

1. Timing in 1.8V signaling is different from that of 3.3V signaling.
2. To properly run the UHS mode, please ensure the device supports UHS-I mode.

- The command list supports  
[Part 1 Physical Layer Specification Ver3.1 Final] definitions
- Copyrights Protection Mechanism
  - Compliant with the highest security of DPRM standard
- Support CPRM (Content Protection for Recordable Media) of MicroSD Card
- Card removal during read operation will never harm the content
- Password Protection of cards (optional)
- Write Protect feature using mechanical switch
- Built-in write protection features (permanent and temporary)
- Electrostatic Discharge (ESD)
  - ESD protection in contact pads (contact discharge)
  - ESD protection in non-contact pads (air discharge)
- Operation voltage range: 2.7 ~ 3.6V
- Support Dynamic and Static Wear Leveling

## 2.2 Block Diagram

Figure 2-1: High-Level Block Diagram



## 2.3 MicroSD CARD COMPARISON

**Table 2-1: Comparing SD3.0 Standard, SD3.0 SDHC and SD3.0 SDXC**

|                                            | SD3.0 SDSC (Backward compatible to 2.0 host) | SD3.0 SDHC (Backward compatible to 2.0 host) | SD3.0 SDXC                       |
|--------------------------------------------|----------------------------------------------|----------------------------------------------|----------------------------------|
| File System                                | FAT 12/16                                    | FAT32                                        | exFAT                            |
| Addressing Mode                            | Byte (1 byte unit)                           | Block (512 byte unit)                        | Block (512 byte unit)            |
| HCS/CCS bits of ACMD41                     | Support                                      | Support                                      | Support                          |
| CMD8 (SEND_IF_COND)                        | Support                                      | Support                                      | Support                          |
| CMD16 (SET_BLOCKLEN)                       | Support                                      | Support (Only CMD42)                         | Support (Only CMD42)             |
| Partial Read                               | Support                                      | Not Support                                  | Not Support                      |
| Lock/Unlock Function                       | Mandatory                                    | Mandatory                                    | Mandatory                        |
| Write Protect Groups                       | Optional                                     | Not Support                                  | Not Support                      |
| Supply Voltage 2.7v – 3.6v (for operation) | Support                                      | Support                                      | Support                          |
| Total Bus Capacitance for each signal line | 40pF                                         | 40pF                                         | 40pF                             |
| CSD Version (CSD_STRUCTURE Value)          | 1.0 (0x0)                                    | 2.0 (0x1)                                    | 2.0 (0x1)                        |
| Speed Class                                | Optional                                     | Mandatory (Class 2 / 4 / 6 / 10)             | Mandatory (Class 2 / 4 / 6 / 10) |

**Table 2-2: Comparing UHS Speed Grade Symbols**

|                     | U1 ( UHS Speed Grade 1 )                                                                    | U3 ( UHS Speed Grade 3 )         |
|---------------------|---------------------------------------------------------------------------------------------|----------------------------------|
| Operable Under      | *UHS-I Bus I/F, UHS-II Bus I/F                                                              |                                  |
| MicroSD Memory Card | SDHC UHS-I and UHS-II, SDXC UHS-I and UHS-II                                                |                                  |
| Performance         | 10 MB/s minimum write speed                                                                 | 30 MB/s minimum write speed      |
| Applications        | Full higher potential of recording real-time broadcasts and capturing large-size HD videos. | Capable of recording 4K2K video. |

\*UHS (Ultra High Speed), , defines bus-interface speeds up to 312 Megabytes per second for greater device performance. It is available on SDXC and SDHC memory cards and devices.

### 3 ENVIRONMENTAL SPECIFICATIONS

#### 3.1 Environmental Conditions

##### 3.1.1 Temperature and Humidity

Table 3-1: Temperature Specifications

| Conditions                | Operating     | Shipping      | Storage       |
|---------------------------|---------------|---------------|---------------|
| Temperature- Ambient      | -40 to 85°C   | -40 to 85°C   | -40 to 85°C   |
| Humidity (non-condensing) | 95% under 25C | 93% under 40C | 93% under 40C |

##### 3.1.2 Shock and Vibration

Table 3-2: Shock and Vibration Specifications

| Stimulus  | Description                                                         |
|-----------|---------------------------------------------------------------------|
| Shock     | 1500G, 0.5ms                                                        |
| Vibration | 20 – 80 Hz/1.52mm, 80 – 2000 Hz/20G, (X,Y,Z axis / 30 min for each) |

##### 3.1.1 Electromagnetic Immunity and EMI Compliance

- FCC: CISPR22
- CE: EN55022
- BSMI 13438

##### 3.1.2 Drop

Table 3-3: Drop Specifications

|              | Height of Drop  | Number of Drop                 |
|--------------|-----------------|--------------------------------|
| MicroSD card | 150cm free fall | Direction: 6 face; 1 time/face |

Result: No any abnormality is detected when power on

### 3.1.3 Bend

**Table 3-4: Bend Specifications**

|              | Force             | Action                        |
|--------------|-------------------|-------------------------------|
| MicroSD card | $\geq 10\text{N}$ | Hold for 1min; total 5 times. |

Result: No any abnormality is detected when power on

### 3.1.4 Toque

**Table 3-5: Torque Specifications**

|              | Force                    | Action                                   |
|--------------|--------------------------|------------------------------------------|
| MicroSD card | 0.15N-m or $\pm 2.5$ deg | Hold 30 second/direction, Total 5 cycles |

Result: No any abnormality is detected when power on

### 3.1.5 Switch

**Table 3-6: Switch Specifications**

|              | Force       | Number of Switch Cycle |
|--------------|-------------|------------------------|
| MicroSD card | 0.4N-m~5N-m | 1000 cycles            |

Result: No any abnormality is detected when power on

### 3.1.6 Card Socket Insertions

**Table 3-7: Card Socket Insertions**

|              | Number of Mating Cycles | Result |
|--------------|-------------------------|--------|
| MicroSD card | 10000 cycles            | Pass   |

### 3.1.7 Electrostatic Discharge (ESD)

**Table 3-8: Electrostatic Discharge (ESD)**

|              | Condition                                 | Result |
|--------------|-------------------------------------------|--------|
| MicroSD card | Contact: $\pm 4\text{KV}$ ; 5 times/Pin   | Pass   |
|              | Air: $\pm 15\text{KV}$ ; 5 times/Position | Pass   |

## 3.2 Power Consumption

The table below is the power consumption of MicroSD card with different bus speed modes.

**Table 3-9: Power Consumption**

| Bus Speed Mode     | Max. Power Up Current (uA) | Max. Standby Current (uA) | Max. Read Current (mA) | Max. Write Current (mA) |
|--------------------|----------------------------|---------------------------|------------------------|-------------------------|
| Default Speed Mode | 250                        | 1000                      | 150 @ 3.6V             | 150 @ 3.6V              |
| High Speed Mode    | 250                        | 1000                      | 200 @ 3.6V             | 200 @ 3.6V              |

**NOTES:**

- 1) Power consumptions are measured at room temperature (25C). Standby current might rise to 1600 under 85C.
- 2) Power consumption of Max. Standby Current is for MicroSD cards under and including 64GB only. For 128GB and 256GB, the power consumption is to be determined.

## 3.3 DC Characteristic

### 3.3.1 Bus Operation Conditions for 3.3V Signaling

**Table 3-10: Threshold Level for High Voltage Range**

| Parameter           | Symbol          | Min.      | Max       | Unit | Condition                     |
|---------------------|-----------------|-----------|-----------|------|-------------------------------|
| Supply Voltage      | VDD             | 2.7       | 3.6       | V    |                               |
| Output High Voltage | V <sub>OH</sub> | 0.75*VDD  |           | V    | I <sub>OH</sub> =-2mA VDD Min |
| Output Low Voltage  | V <sub>OL</sub> |           | 0.125*VDD | V    | I <sub>OL</sub> =2mA VDD Min  |
| Input High Voltage  | V <sub>IH</sub> | 0.625*VDD | VDD+0.3   | V    |                               |
| Input Low Voltage   | V <sub>IL</sub> | VSS-0.3   | 0.25*VDD  | V    |                               |
| Power Up Time       |                 |           | 250       | ms   | From 0V to VDD min            |



**Table 3-11: Peak Voltage and Leakage Current**

| Parameter                 | Symbol | Min  | Max.    | Unit | Remarks |
|---------------------------|--------|------|---------|------|---------|
| Peak voltage on all lines |        | -0.3 | VDD+0.3 | V    |         |
| All Inputs                |        |      |         |      |         |
| Input Leakage Current     |        | -10  | 10      | uA   |         |
| All Outputs               |        |      |         |      |         |
| Output Leakage Current    |        | -10  | 10      | uA   |         |

**Table 3-12: Threshold Level for 1.8V Signaling**

| Parameter           | Symbol            | Min.                 | Max  | Unit | Condition                    |
|---------------------|-------------------|----------------------|------|------|------------------------------|
| Supply Voltage      | V <sub>DD</sub>   | 2.7                  | 3.6  | V    |                              |
| Regulator Voltage   | V <sub>DDIO</sub> | 1.7                  | 1.95 | V    | Generated by V <sub>DD</sub> |
| Output High Voltage | V <sub>OH</sub>   | 1.4                  | -    | V    | I <sub>OH</sub> =-2mA        |
| Output Low Voltage  | V <sub>OL</sub>   | -                    | 0.45 | V    | I <sub>OL</sub> =2mA         |
| Input High Voltage  | V <sub>IH</sub>   | 1.27                 | 2    | V    |                              |
| Input Low Voltage   | V <sub>IL</sub>   | V <sub>SS</sub> -0.3 | 0.58 | V    |                              |

**Table 3-13: Input Leakage Current for 1.8V Signaling**

| Parameter             | Symbol | Min | Max. | Unit | Remarks                      |
|-----------------------|--------|-----|------|------|------------------------------|
| Input Leakage Current |        | -2  | 2    | uA   | DAT3 pull-up is disconnected |

### 3.3.2 Bus Signal Line Load

Figure 3-1: Bus Circuitry Diagram

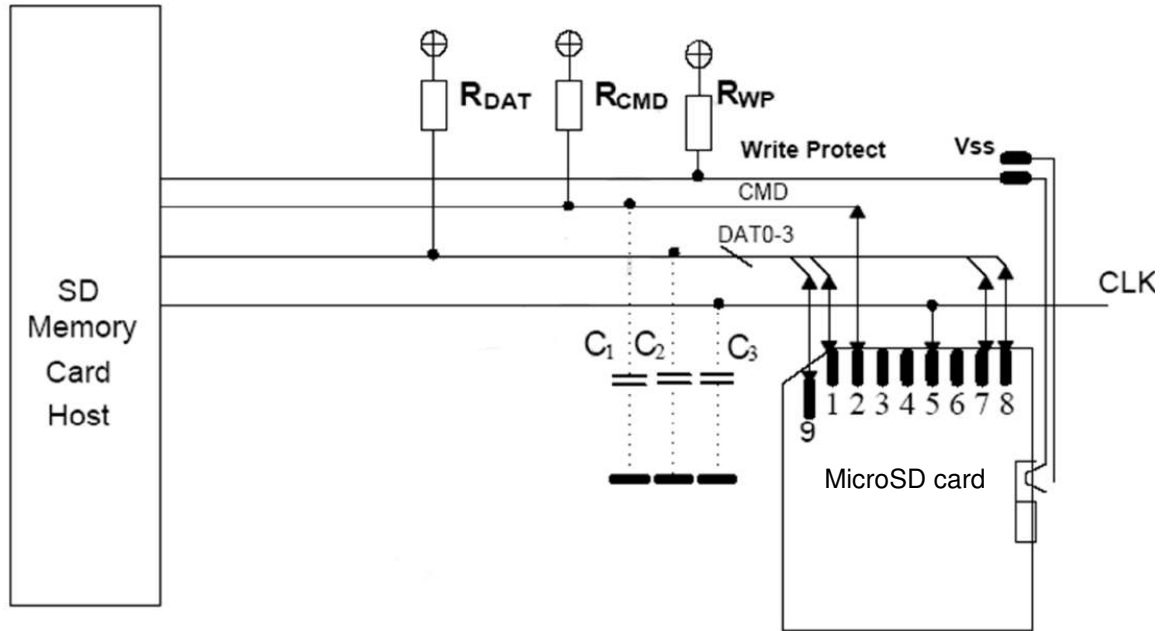


Table 3-14: Bus Operation Conditions – Signal Line’s Load

| Parameter                                  | Symbol                 | Min | Max | Unit       | Remark                                           |
|--------------------------------------------|------------------------|-----|-----|------------|--------------------------------------------------|
| Pull-up resistance                         | $R_{CMD}$<br>$R_{DAT}$ | 10  | 100 | k $\Omega$ | To prevent bus floating                          |
| Total bus capacitance for each signal line | $C_L$                  |     | 40  | pF         | 1 card $C_{HOST}+C_{BUS}$ shall not exceed 30 pF |
| Card Capacitance for each signal pin       | $C_{CARD}$             |     | 10  | pF         |                                                  |
| Maximum signal line inductance             |                        |     | 16  | nH         |                                                  |
| Pull-up resistance inside card (pin1)      | $R_{DAT3}$             | 10  | 90  | k $\Omega$ | May be used for card detection                   |
| Capacity Connected to Power Line           | $C_C$                  |     | 5   | $\mu$ F    | To prevent inrush current                        |

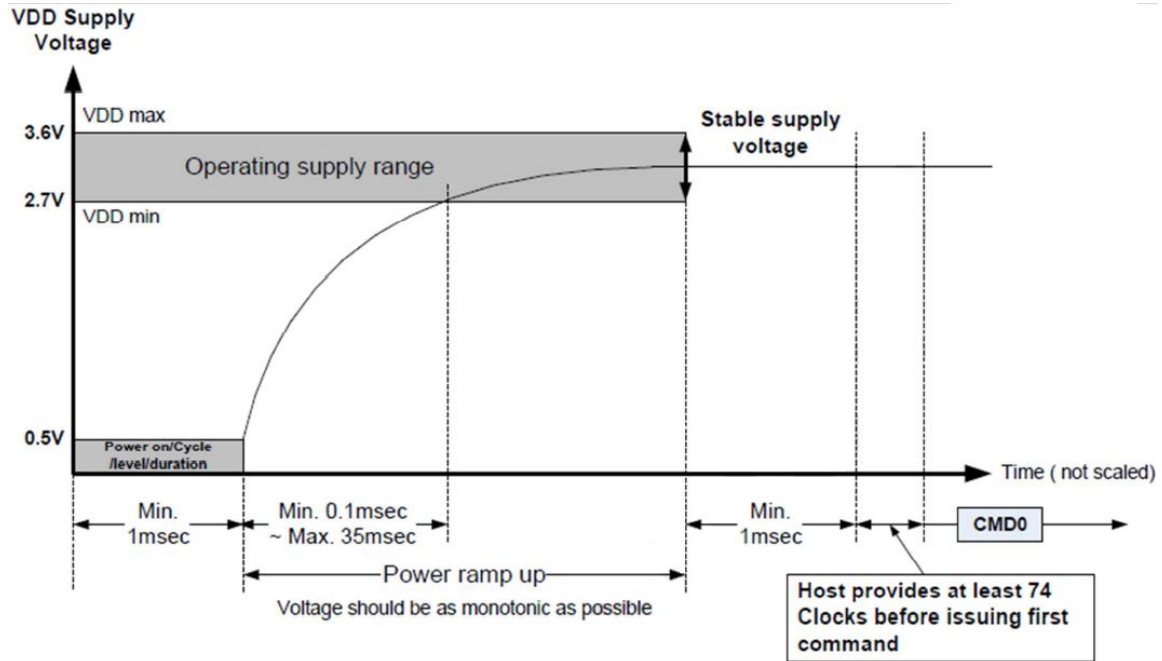
**Notes:**

Total Bus Capacitance =  $C_{HOST} + C_{BUS} + N C_{CARD}$

### 3.3.3 Power Up Time of Host

Host needs to keep power line level less than 0.5V and more than 1ms before power ramp up.

Figure 3-2: Power Up Time of Host



## **Power On or Power Cycle**

Followings are requirements for Power on and Power cycle to assure a reliable MicroSD Card hard reset.

1. Voltage level shall be below 0.5V
2. Duration shall be at least 1ms.

## **Power Supply Ramp Up**

The power ramp up time is defined from 0.5V threshold level up to the operating supply voltage which is stable between VDD (min.) and VDD (max.) and host can supply SDCLK.

Followings are recommendations of Power ramp up:

1. Voltage of power ramp up should be monotonic as much as possible.
2. The minimum ramp up time should be 0.1ms.
3. The maximum ramp up time should be 35ms for 2.7-3.6V power supply.
4. Host shall wait until VDD is stable.
5. After 1ms VDD stable time, host provides at least 74 clocks before issuing the first command.

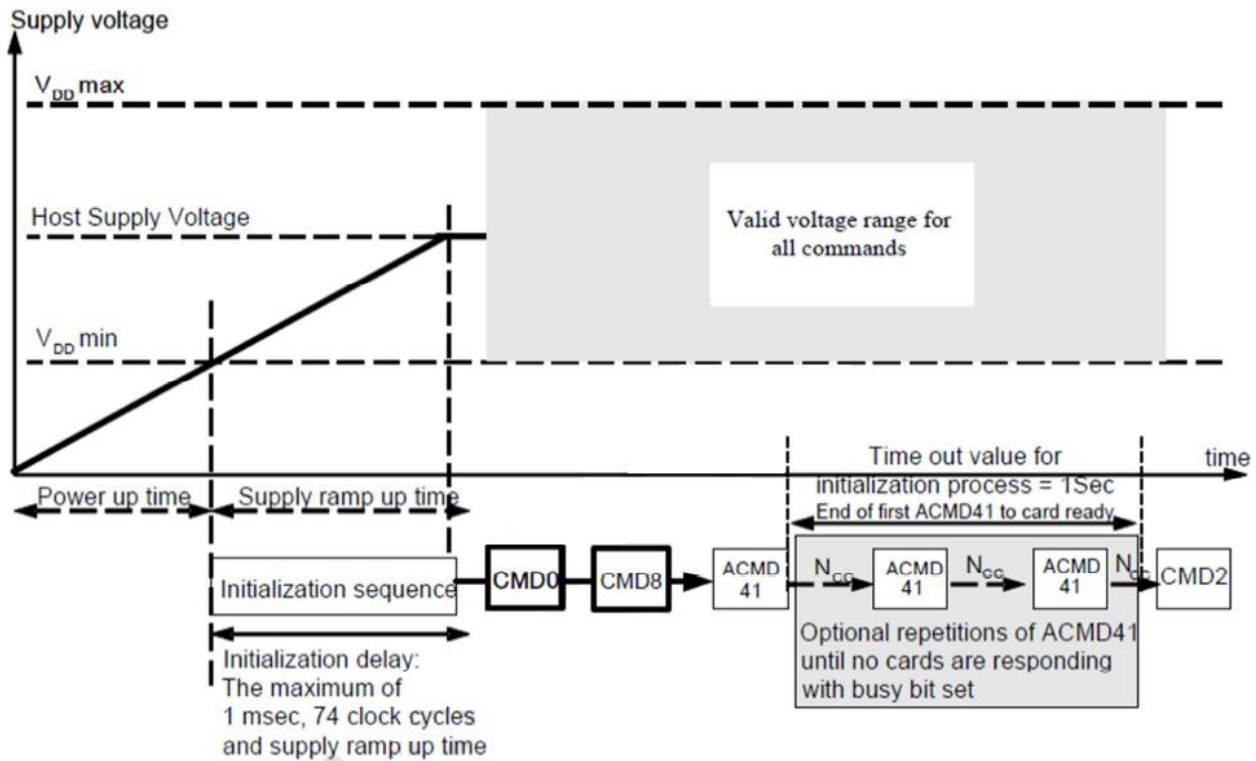
## **Power Down and Power Cycle**

1. When the host shuts down the power, the card VDD shall be lowered to less than 0.5Volt for a minimum period of 1ms. During power down, DAT, CMD, and CLK should be disconnected or driven to logical 0 by the host to avoid a situation that the operating current is drawn through the signal lines.
2. If the host needs to change the operating voltage, a power cycle is required. Power cycle means the power is turned off and supplied again. Power cycle is also needed for accessing cards that are already in Inactive State. To create a power cycle the host shall follow the power down description before power up the card (i.e. the card VDD shall be once lowered to less than 0.5Volt for a minimum period of 1ms).

### 3.3.4 Power Up Time of Card

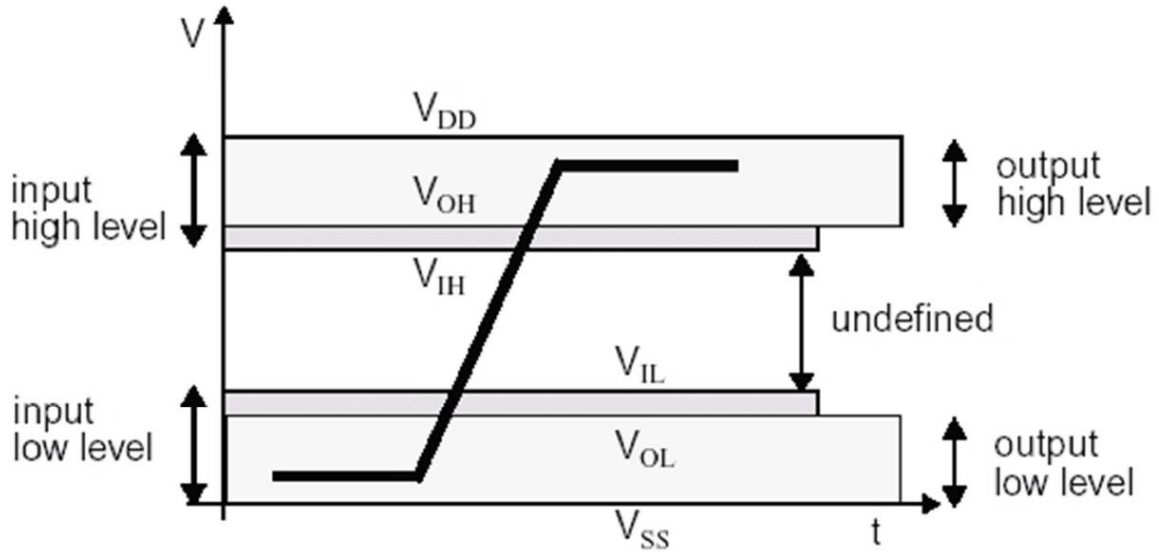
A device shall be ready to accept the first command within 1ms from detecting VDD min. Device may use up to 74 clocks for preparation before receiving the first command.

**Figure 3-3: Power Up Time of Card**



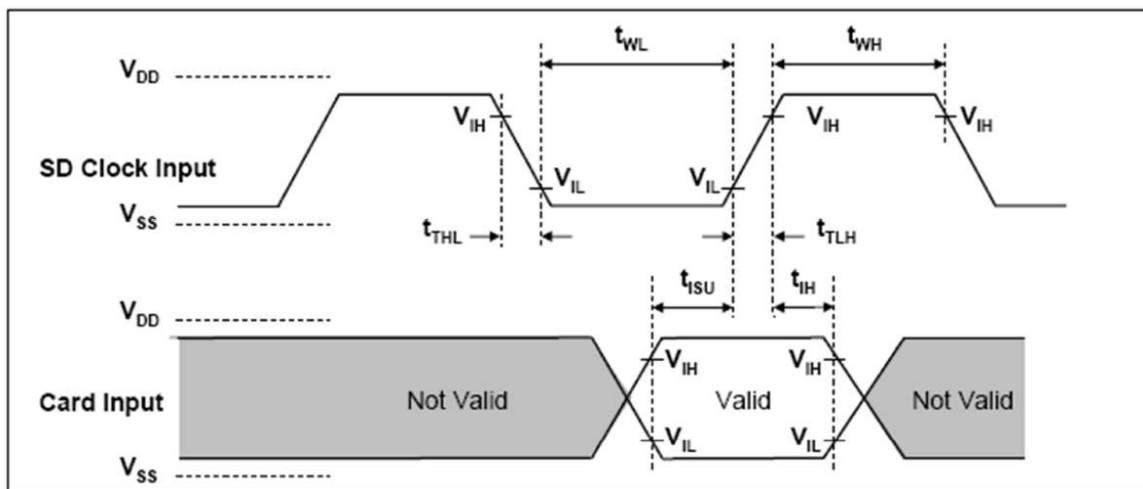
### 3.4 AC Characteristic

Figure 3-4: Voltage Levels

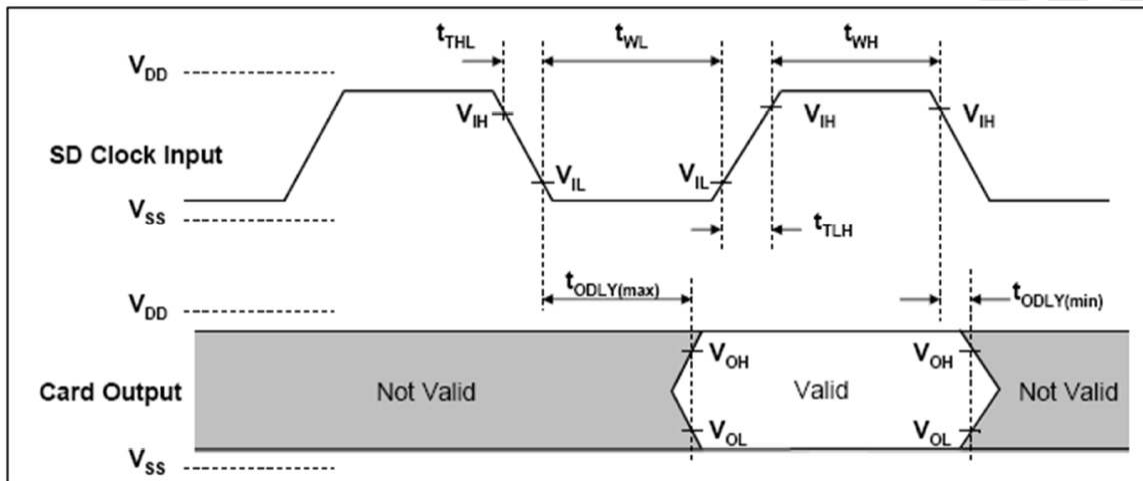


#### 3.4.1 MicroSD Interface Timing (Default)

Figure 3-5: Card Input Timing (Default Speed Card)



**Figure 3-6: Card Output Timing (Default Speed Card)**



**Table 3-15: Timing Specifications**

| Parameter                                                           | Symbol            | Min      | Max | Unit | Remark                             |
|---------------------------------------------------------------------|-------------------|----------|-----|------|------------------------------------|
| <b>Clock CLK</b> (All values are referred to min(VIH) and max(VIL)) |                   |          |     |      |                                    |
| Clock frequency Data Transfer Mode                                  | f <sub>PP</sub>   | 0        | 25  | MHz  | C <sub>card</sub> ≤ 10 pF (1 card) |
| Clock frequency Identification Mode                                 | f <sub>OD</sub>   | 0(1)/100 | 400 | kHz  | C <sub>card</sub> ≤ 10 pF (1 card) |
| Clock low time                                                      | t <sub>WL</sub>   | 10       |     | ns   | C <sub>card</sub> ≤ 10 pF (1 card) |
| Clock high time                                                     | t <sub>WH</sub>   | 10       |     | ns   | C <sub>card</sub> ≤ 10 pF (1 card) |
| Clock rise time                                                     | t <sub>TLH</sub>  |          | 10  | ns   | C <sub>card</sub> ≤ 10 pF (1 card) |
| Clock fall time                                                     | t <sub>THL</sub>  |          | 10  | ns   | C <sub>card</sub> ≤ 10 pF (1 card) |
| <b>Inputs CMD, DAT</b> (referenced to CLK)                          |                   |          |     |      |                                    |
| Input set-up time                                                   | t <sub>ISU</sub>  | 5        |     | ns   | C <sub>card</sub> ≤ 10 pF (1 card) |
| Input hold time                                                     | t <sub>IH</sub>   | 5        |     | ns   | C <sub>card</sub> ≤ 10 pF (1 card) |
| <b>Outputs CMD, DAT</b> (referenced to CLK)                         |                   |          |     |      |                                    |
| Output Delay time during Data Transfer Mode                         | t <sub>ODLY</sub> | 0        | 14  | ns   | C <sub>card</sub> ≤ 40 pF (1 card) |
| Output Delay time during Identification Mode                        | t <sub>ODLY</sub> | 0        | 50  | ns   | C <sub>card</sub> ≤ 40 pF (1 card) |

**Notes:**

1) 0Hz means to stop the clock. The given minimum frequency range is for cases where continuous clock is required.



### 3.4.2 MicroSD Interface Timing (High-Speed Mode)

Figure 3-7: Card Input Timing (High Speed Card)

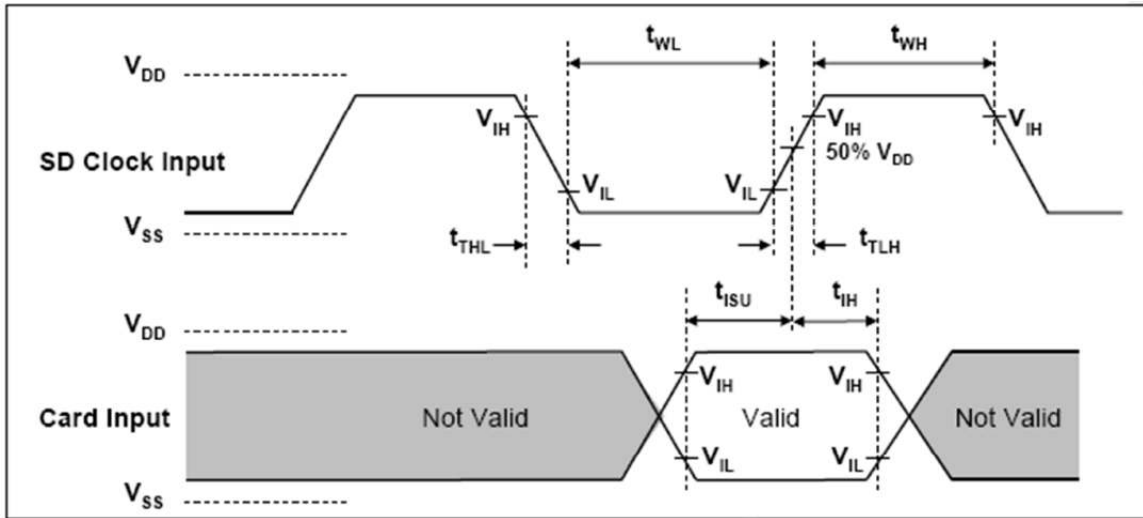
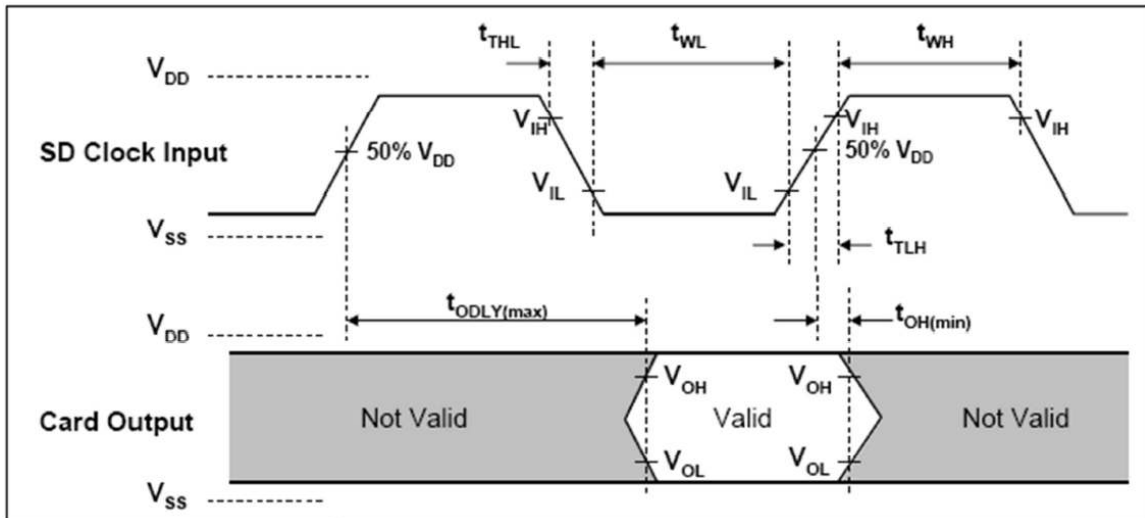


Figure 3-8: Card Output Timing (High Speed Card)



**Table 3-16: Card Output Timing (High Speed Card)**

| Parameter                                                           | Symbol     | Min | Max | Unit | Remark                         |
|---------------------------------------------------------------------|------------|-----|-----|------|--------------------------------|
| <b>Clock CLK</b> (All values are referred to min(VIH) and max(VIL)) |            |     |     |      |                                |
| Clock frequency Data Transfer Mode                                  | $f_{PP}$   | 0   | 50  | MHz  | $C_{card} \leq 10$ pF (1 card) |
| Clock low time                                                      | $t_{WL}$   | 7   |     | ns   | $C_{card} \leq 10$ pF (1 card) |
| Clock high time                                                     | $t_{WH}$   | 7   |     | ns   | $C_{card} \leq 10$ pF (1 card) |
| Clock rise time                                                     | $t_{TLH}$  |     | 3   | ns   | $C_{card} \leq 10$ pF (1 card) |
| Clock fall time                                                     | $t_{THL}$  |     | 3   | ns   | $C_{card} \leq 10$ pF (1 card) |
| <b>Inputs CMD, DAT</b> (referenced to CLK)                          |            |     |     |      |                                |
| Input set-up time                                                   | $t_{ISU}$  | 6   |     | ns   | $C_{card} \leq 10$ pF (1 card) |
| Input hold time                                                     | $t_{IH}$   | 2   |     | ns   | $C_{card} \leq 10$ pF (1 card) |
| <b>Outputs CMD, DAT</b> (referenced to CLK)                         |            |     |     |      |                                |
| Output Delay time during Data Transfer Mode                         | $t_{ODLY}$ | 0   | 14  | ns   | $C_{card} \leq 40$ pF (1 card) |
| Output hold time                                                    | $t_{OH}$   | 2.5 |     | ns   | $C_{card} \leq 15$ pF (1 card) |
| Total System capacitance of each                                    | $C_L$      | 0   | 40  | ns   | $C_{card} \leq 15$ pF (1 card) |

**Notes:**

1) In order to satisfy severe timing, the host shall drive only one card.

### 3.4.3 MicroSD Interface Timing (SDR12, SDR25 and SDR50 Modes)

Figure 3-9: Clock Signal Timing (Input)

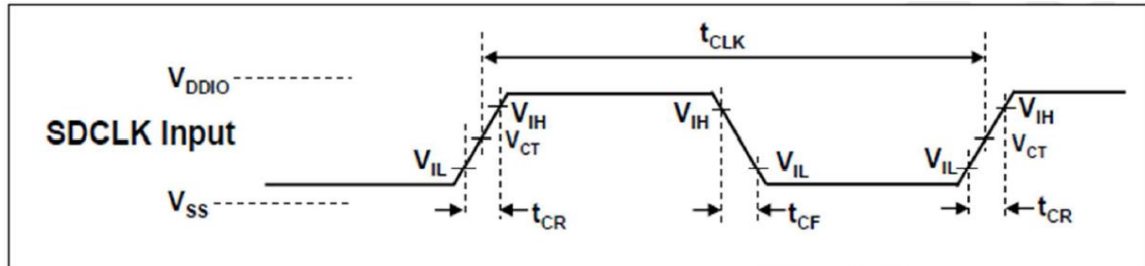
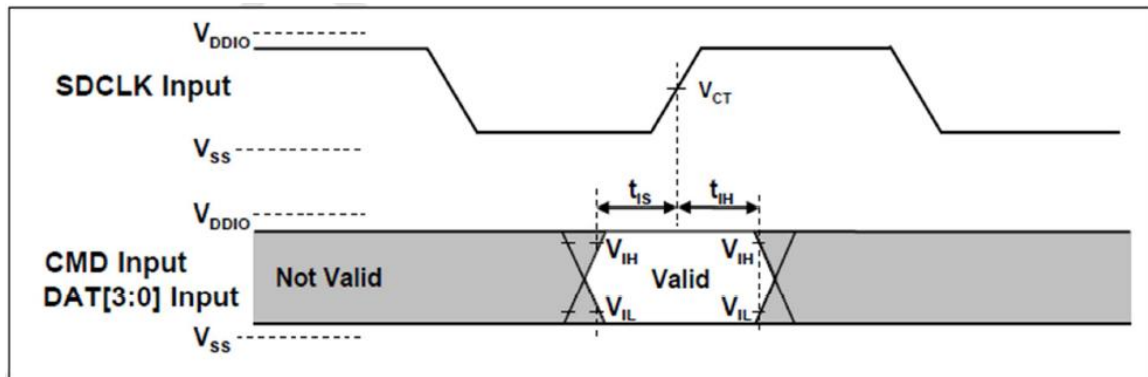


Table 3-17: Clock Signal Timing

| Symbol           | Min | Max             | Unit | Remark                                                                                                                                             |
|------------------|-----|-----------------|------|----------------------------------------------------------------------------------------------------------------------------------------------------|
| $t_{CLK}$        | 4.8 | -               | ns   | 208MHz (Max.), Between rising edge, $V_{CT} = 0.975V$                                                                                              |
|                  |     |                 |      | $t_{CR}, t_{CF} < 0.96ns$ (max.) at 208MHz, $C_{CARD} = 10pF$                                                                                      |
| $t_{CR}, t_{CF}$ | -   | $0.2 * t_{CLK}$ | ns   | $t_{CR}, t_{CF} < 2.00ns$ (max.) at 100MHz, $C_{CARD} = 10pF$ The absolute maximum value of $t_{CR}, t_{CF}$ is 10ns regardless of clock frequency |
| Clock Duty       | 30  | 70              | %    |                                                                                                                                                    |

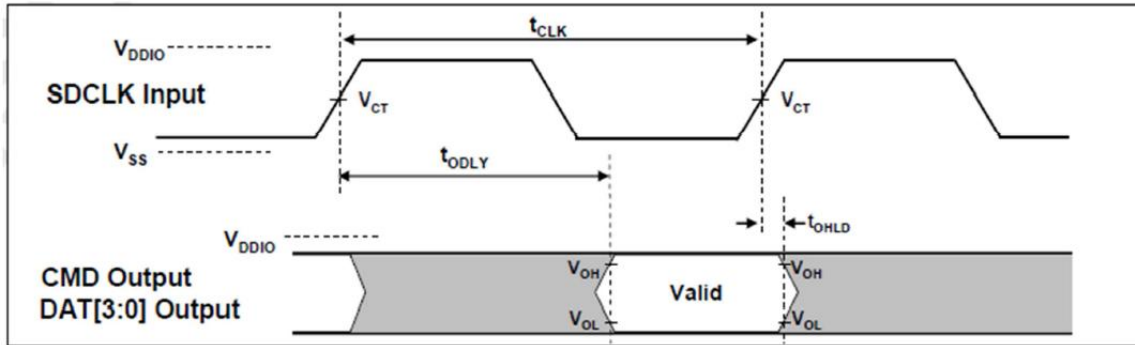
**Figure 3-10: SDR50 and SDR104 Card Input Timing**



**Table 3-18: SDR50 and SDR104 Card Input Timing**

| Symbol   | Min              | Max | Unit | SDR104 Mode                                         |
|----------|------------------|-----|------|-----------------------------------------------------|
| $t_{IS}$ | 1.4              | -   | ns   | $C_{CARD} = 10\text{pF}$ , $V_{CT} = 0.975\text{V}$ |
| $t_{IH}$ | 0.8 <sup>1</sup> | -   | ns   | $C_{CARD} = 5\text{pF}$ , $V_{CT} = 0.975\text{V}$  |
| Symbol   | Min              | Max | Unit | SDR104 Mode                                         |
| $t_{IS}$ | 3.00             | -   | ns   | $C_{CARD} = 10\text{pF}$ , $V_{CT} = 0.975\text{V}$ |
| $t_{IH}$ | 0.8 <sup>1</sup> | -   | ns   | $C_{CARD} = 5\text{pF}$ , $V_{CT} = 0.975\text{V}$  |

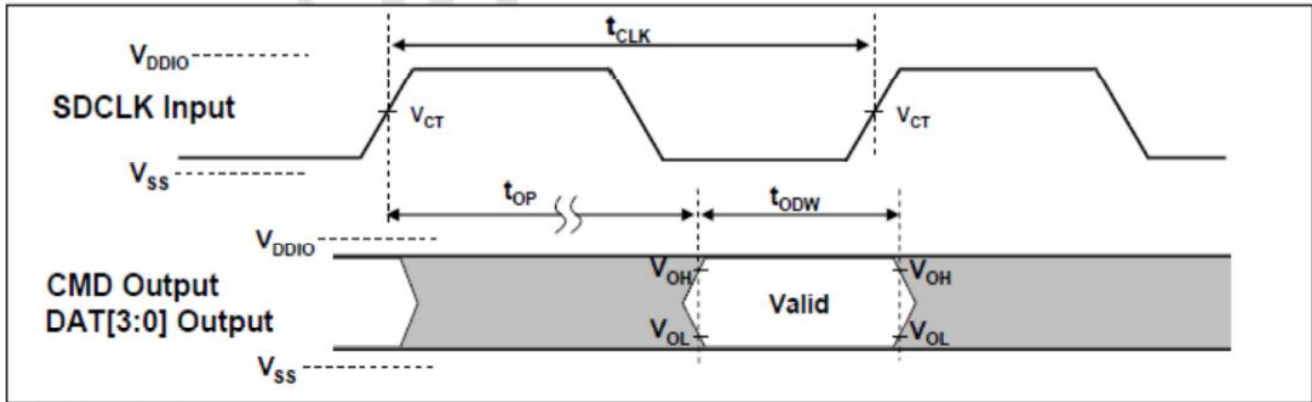
**Figure 3-11: Clock Signal Timing (Output Timing of Fixed Data)**



**Table 3-19: Output Timing of Fixed Data Window (SDR12, SDR25, SDR50)**

| Symbol     | Min | Max | Unit | Remark                                                                          |
|------------|-----|-----|------|---------------------------------------------------------------------------------|
| $t_{ODLY}$ | -   | 7.5 | ns   | $t_{CLK} \geq 10.0ns$ , $C_L = 30pF$ , using driver Type B, for SDR50           |
| $t_{ODLY}$ | -   | 14  | ns   | $t_{CLK} \geq 20.0ns$ , $C_L = 40pF$ , using driver Type B, for SDR25 and SDR12 |
| $T_{OH}$   | 1.5 | -   | ns   | Hold time at the $t_{ODLY}$ (min.), $C_L = 15pF$                                |

**Figure 3-12: Output Timing of Variable Window (SDR104)**



**Table 3-20: Output Timing of Variable Window (SDR104)**

| Symbol          | Min  | Max   | Unit | Remark                                                |
|-----------------|------|-------|------|-------------------------------------------------------|
| $t_{OP}$        | 0    | 2     | UI   | Card Output Phase                                     |
| $\Delta t_{OP}$ | -350 | +1550 | ps   | Delay variable due to temperature change after tuning |
| $t_{ODW}$       | 0.6  | -     | UI   | $t_{ODW} = 2.88\text{ns}$ at 208MHz                   |

### 3.4.4 MicroSD Interface Timing (DDR50 Mode)

Figure 3-13: Clock Signal Timing

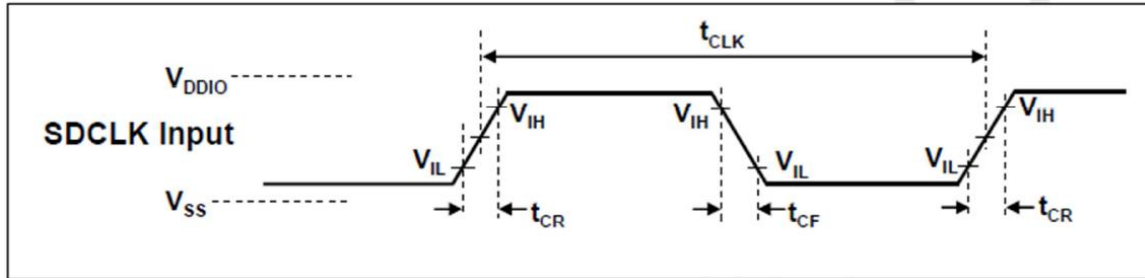
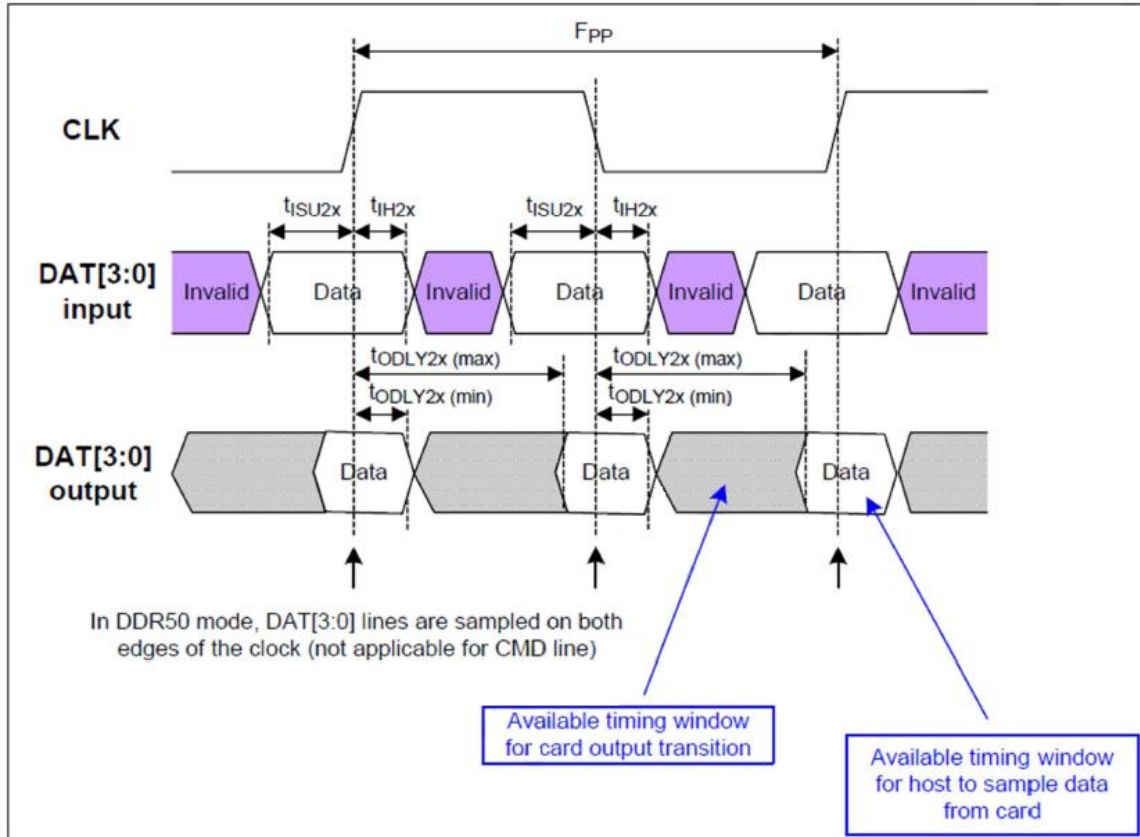


Table 3-21: Clock Signal Timing

| Symbol           | Min | Max             | Unit | Remark                                                                   |
|------------------|-----|-----------------|------|--------------------------------------------------------------------------|
| $t_{CLK}$        | 20  | -               | ns   | 50MHz (Max.), Between rising edge                                        |
| $t_{CR}, t_{CF}$ | -   | $0.2 * t_{CLK}$ | ns   | $t_{CR}, t_{CF} < 4.00\text{ns}$ (max.) at 50MHz, $C_{CARD}=10\text{pF}$ |
| Clock Duty       | 45  | 55              | %    |                                                                          |

Figure 3-14: Timing Diagram DAT Inputs/Outputs Referenced to CLK in DDR50 Mode





**Table 3-22: Bus Timings – Parameters Values (DDR50 Mode)**

| Parameter                                   | Symbol       | Min | Max  | Unit | Remark                         |
|---------------------------------------------|--------------|-----|------|------|--------------------------------|
| <b>Inputs CMD (referenced to CLK)</b>       |              |     |      |      |                                |
| Input set-up time                           | $t_{ISU}$    | 3   | -    | ns   | $C_{card} \leq 10$ pF (1 card) |
| Input hold time                             | $t_{IH}$     | 0.8 | -    | ns   | $C_{card} \leq 10$ pF (1 card) |
| <b>Outputs CMD (referenced to CLK)</b>      |              |     |      |      |                                |
| Output Delay time during Data Transfer Mode | $t_{ODLY}$   | 0   | 13.7 | ns   | $C_L \leq 30$ pF (1 card)      |
| Output hold time                            | $t_{OH}$     | 1.5 |      | ns   | $C_L \geq 15$ pF (1 card)      |
| <b>Inputs DAT (referenced to CLK)</b>       |              |     |      |      |                                |
| Input set-up time                           | $t_{ISU2x}$  | 3   | -    | ns   | $C_{card} \leq 10$ pF (1 card) |
| Input hold time                             | $t_{IH2x}$   | 0.8 | -    | ns   | $C_{card} \leq 10$ pF (1 card) |
| <b>Outputs DAT (referenced to CLK)</b>      |              |     |      |      |                                |
| Output Delay time during Data Transfer Mode | $t_{ODLY2x}$ | 0   | 13.7 | ns   | $C_L \leq 25$ pF (1 card)      |
| Output hold time                            | $t_{OH2x}$   | 1.5 |      | ns   | $C_L \geq 15$ pF (1 card)      |

## 4 INTERFACE

### 4.1 Pad Assignment and Descriptions

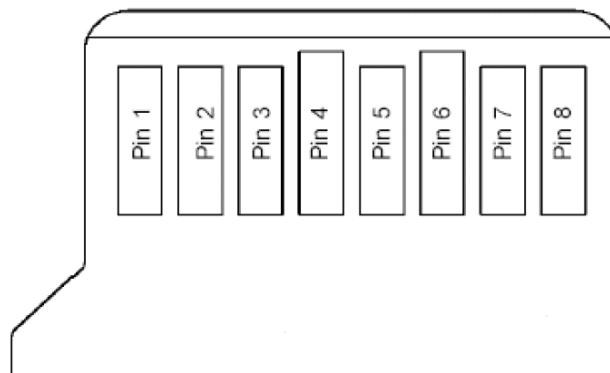
#### 4.1.1 MicroSD Bus Pin Assignment

**Table 4-1: MicroSD Bus Pin Assignment**

| Pin # | SD Mode  |                   |                        | SPI Mode |                   |                        |
|-------|----------|-------------------|------------------------|----------|-------------------|------------------------|
|       | Name     | Type <sup>1</sup> | Description            | Name     | Type <sup>1</sup> | Description            |
| 1     | DAT2     | I/O/PP            | Data Line[Bit2]        | RSV      |                   |                        |
| 2     | CD/ DAT3 | I/O/PP            | Card Detect Line[Bit3] | CS       | I                 | Chip Select (neg true) |
| 3     | CMD      | PP                | Command/Response       | DI       | I                 | Data In                |
| 4     | Vdd      | S                 | Supply Voltage         | Vdd      | S                 | Supply Voltage         |
| 5     | CLK      | I                 | Clock                  | SCLK     | I                 | Clock                  |
| 6     | VSS      | S                 | Supply voltage ground  | VSS      | S                 | Supply voltage ground  |
| 7     | DAT0     | I/O/PP            | Data Line[Bit0]        | DO       | O/PP              | Data Out               |
| 8     | DAT1     | I/O/PP            | Data Line[Bit1]        | RSV      | -                 | Reserved (*)           |

**Notes:**

- 1) S: power supply; I: input; O: output using push-pull drivers; PP: I/O using push-pull drivers;
- 2) The extended DAT lines (DAT1-DAT3) are input on power up. They start to operate as DAT lines after SET\_BUS\_WIDTH command. The Host shall keep its own DAT1-DAT3 lines in input mode, as well, while they are not used.
- 3) At power up this line has a 50KOhm pull up enabled in the card. This resistor serves two functions Card detection and Mode Selection. For Mode Selection, the host can drive the line high or let it be pulled high to select MicroSD mode. If the host wants to select SPI mode it should drive the line low. For Card detection, the host detects that the line is pulled high. This pull-up should be disconnected by the user, during regular data transfer, with SET\_CLR\_CARD\_DETECT (ACMD42) command



**Figure 4-1: MicroSD Pin Assignment (Back View of the Card)**

**Table 4-2: Registers**

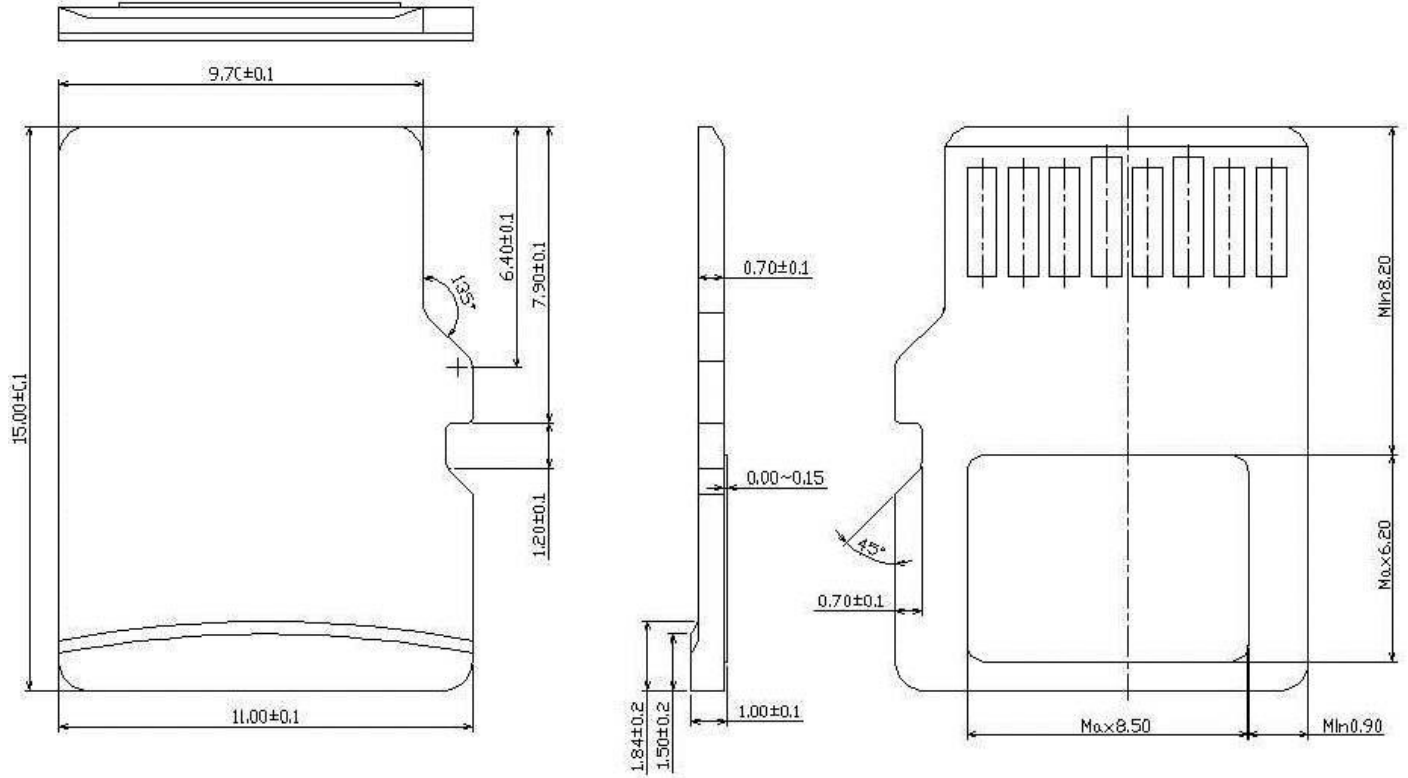
| Name             | Width  | Description                                                                                                                                               |
|------------------|--------|-----------------------------------------------------------------------------------------------------------------------------------------------------------|
| CID              | 128bit | Card identification number; card individual number for identification. <b>Mandatory</b>                                                                   |
| RCA <sup>1</sup> | 16bit  | Relative card address; local system address of a card, dynamically suggested by the card and approved by the host during initialization. <b>Mandatory</b> |
| DSR              | 16bit  | Driver Stage Register; to configure the card's output drivers. <b>Optional</b>                                                                            |
| CSD              | 128bit | Card Specific Data; information about the card operation conditions. <b>Mandatory</b>                                                                     |
| SCR              | 64bit  | SD Configuration Register; information about the MicroSD Memory Card's Special Features capabilities. <b>Mandatory</b>                                    |
| OCR              | 32bit  | Operation conditions register. <b>Mandatory</b>                                                                                                           |
| SSR              | 512bit | SD Status; information about the card proprietary features. <b>Mandatory</b>                                                                              |
| OCR              | 32bit  | Card Status; information about the card status. <b>Mandatory</b>                                                                                          |

**Notes:**

1) RCA register is not used (available) in SPI mode

## 5 Mechanical Information

Figure 5-1: MicroSD Case Dimensions



Note: All dimension in mm. Drawing is not to scale