

TS7329K - 100W Asymmetric Peak Power GaN Broadband SPDT Switch

1.0 Features

- Low insertion loss (TX/RX): 0.4/0.6dB @ 2600MHz
- High isolation (RX Path): 40dB @ 2600MHz
- High peak power handling capability
- No external DC blocking capacitors on RF lines
- All RF ports OFF state
- Versatile 2.6-5.5V power supply
- Operating frequency: 500MHz to 5GHz

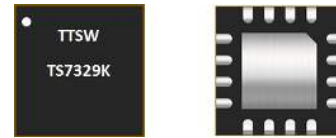


Figure 1 Device Image
(16 Pin 3×3×0.8mm QFN Package)

2.0 Applications

- 4G, 5G systems
- RX protection
- Cellular infrastructure
- Small cells
- LTE relays and microcells
- Radar



RoHS/REACH/Halogen Free Compliance

3.0 Description

The TS7329K is an asymmetrical reflective Single Pole Dual Throw (SPDT) switch designed for broadband, high peak power switching applications. Its broadband behavior from 500MHz to 5GHz frequencies makes the TS7329K an excellent switch for all applications requiring low insertion loss, high isolation and high linearity within a small package size.

The TS7329K is packaged into a compact Quad Flat No lead (QFN) 3x3mm 16 leads plastic package.

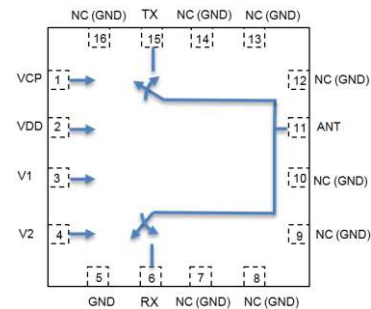


Figure 2 Function Block Diagram
(Top View)

4.0 Ordering Information

Table 1 Ordering Information

| Base Part Number | Package Type | Form | Qty | Reel Diameter | Reel Width | Orderable Part Number |
|------------------|----------------------|---------------|------|---------------|------------|-----------------------|
| TS7329K | 16 Pin 3×3×0.8mm QFN | Tape and Reel | 3000 | 13" (330mm) | 18mm | TS7329KMTRPBF |
| Evaluation Board | | | | | | TS7329K-EVB |

5.0 Pin Description

Table 2 Pin Definition

| Pin Number | Pin Name | Description |
|------------------------|----------|--|
| 1 | VCP | Internal charge pump voltage output. Connect a 1nF capacitor to GND on this pin to improve switching time. |
| 2 | VDD | DC power supply |
| 3 | V1 | Switch control input 1 |
| 4 | V2 | Switch control input 2 |
| 6 | RX | RX port |
| 5,7,8,9,10,12,13,14,16 | NC | No internal connection, Can be grounded |
| 11 | ANT | Antenna port |
| 15 | TX | TX port |

Note: The backside ground (thermal) pad of the package must be grounded directly to the ground plane of PCB with multiple vias to ensure proper operation and thermal management.

6.0 Absolute Maximum Ratings

Table 3 Absolute Maximum Ratings @ $T_A=+25^{\circ}\text{C}$ Unless Otherwise Specified

| Parameter | Symbol | Value | Unit |
|---|-----------------|--------------|-----------------------------|
| Electrical Ratings | | | |
| Power Supply Voltage | VDD | 2.6 to 5.5 | V |
| Storage Temperature Range | T_{st} | -55 to +125 | $^{\circ}\text{C}$ |
| Operating Temperature Range | T_{op} | -40 to +85 | $^{\circ}\text{C}$ |
| Maximum Junction Temperature | T_J | +140 | $^{\circ}\text{C}$ |
| RF Input Power CW, 800MHz, $T_J=+85^{\circ}\text{C}$ | TX-ANT | 42 | dBm |
| RF Input Power CW, 800MHz, $T_J=+105^{\circ}\text{C}$ | TX-ANT | 41 | dBm |
| Thermal Ratings | | | |
| Thermal Resistance (junction-to-case) – Bottom side | $R_{\theta JC}$ | 25 | $^{\circ}\text{C}/\text{W}$ |
| Thermal Resistance (junction-to-top) | $R_{\theta JT}$ | 36 | $^{\circ}\text{C}/\text{W}$ |
| Soldering Temperature | T_{SOLD} | 260 | $^{\circ}\text{C}$ |
| ESD Ratings | | | |
| Human Body Model (HBM) | Level 1B | 500 to <1000 | V |
| Charged Device Model (CDM) | Level C3 | ≥ 1000 | V |
| Moisture Rating | | | |
| Moisture Sensitivity Level | MSL | 1 | - |

Attention:

Maximum ratings are absolute ratings. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Exceeding one or a combination of the absolute maximum ratings may cause permanent and irreversible damage to the device and/or to surrounding circuit.

7.0 Electrical Specifications

Table 4 Electrical Specifications @T_A=+25°C Unless Otherwise Specified; VDD=+3.3V; 50Ω Source/Load.

| Parameter | Condition | Minimum | Typical | Maximum | Unit |
|-------------------------------|---|---------|---------|---------|------|
| Operating Frequency | | 500 | | 5000 | MHz |
| Insertion Loss, TX | 800MHz | | 0.30 | 0.40 | dB |
| | 1.95GHz | | 0.35 | 0.45 | |
| | 2.6GHz | | 0.40 | 0.55 | |
| | 3.8GHz | | 0.40 | | |
| | 5.0GHz (with match. See page 4) | | 0.45 | | |
| Insertion Loss, RX | 800MHz | | 0.50 | 0.65 | dB |
| | 1.95GHz | | 0.55 | 0.70 | |
| | 2.6GHz | | 0.60 | 0.75 | |
| | 3.8GHz | | 0.70 | | |
| | 5.0GHz (with match. See page 4) | | 0.85 | | |
| Isolation ANT-TX | 800MHz | 39 | 42 | | dB |
| | 1.95GHz | 30 | 33 | | |
| | 2.6GHz | 27 | 30 | | |
| | 3.8GHz | | 27 | | |
| | 5.0GHz (with match. See page 4) | | 23 | | |
| Isolation ANT-RX | 800MHz | 52 | 55 | | dB |
| | 1.95GHz | 42 | 45 | | |
| | 2.6GHz | 37 | 40 | | |
| | 3.8GHz | | 35 | | |
| | 5.0GHz (with match. See page 4) | | 30 | | |
| Return Loss ANT-TX, RX | 800MHz | | 30 | | dB |
| | 1.95GHz | | 25 | | |
| | 2.6GHz | | 23 | | |
| | 3.8GHz | | 22 | | |
| | 5.0GHz (with match) | | 18 | | |
| Isolation @ Peak Power | Peak power=49.2dBm, Isolation RX @3.8GHz | | 35 | | dB |
| Harmonic distortion | | | | | |
| H2 | 800MHz, Pin=35dBm | | -40 | | dBm |
| H3 | 800MHz, Pin=35dBm | | -45 | | dBm |
| IIP3 | 800MHz | | 70 | | dBm |
| P0.1dB ^[1] TX | 700MHz~3.8GHz, CW | 42 | | | dBm |
| Peak P0.1dB TX ^[2] | 700MHz~3.8GHz, pulsed power | 49.2 | 50 | | dBm |
| P0.1dB ^[1] RX | 700MHz~3.8GHz, CW | 39 | | | dBm |
| Switching Time | 50% ctrl to 10/90% of the RF value is settled. C1=1nF (refer to Figure 3) | | 0.35 | | μs |
| Control Voltage | Power supply VDD | 2.6 | 3.3 | 5.5 | V |
| | All control pins high, V _{ih} | 1.0 | 3.3 | 5.25 | V |
| | All control pins low, V _{il} | -0.3 | | 0.5 | V |
| Control Current | All control pins low, I _{il} | | 0 | | μA |
| | All control pins high, I _{ih} | | | 7.5 | μA |
| Current Consumption, IDD | Active mode | | 160 | 200 | μA |

Note:

[1] P0.1dB is a figure of merit.

[2] 1% duty cycle and 10μs pulse width.

[3] No external DC blocking capacitors required on RF pins unless DC voltage is applied on a RF pin.

8.0 Switch Truth Table

Table 5 Switch Truth Table

| V1 | V2 | Active RF Path |
|----|----|----------------|
| 0 | 1 | All OFF |
| 0 | 0 | ANT-TX |
| 1 | 0 | ANT-RX |

Attention:

- [1] VDD should be applied first before V1 and V2, otherwise may cause damage to the device.
- [2] There are internal pull-downs to ground on both V1 and V2 control pins, the state at start-up without any control voltage applied will be ANT-TX ON.
- [3] If all OFF state is not used, the switch can be operated with single control pin V1.

9.0 Evaluation Board

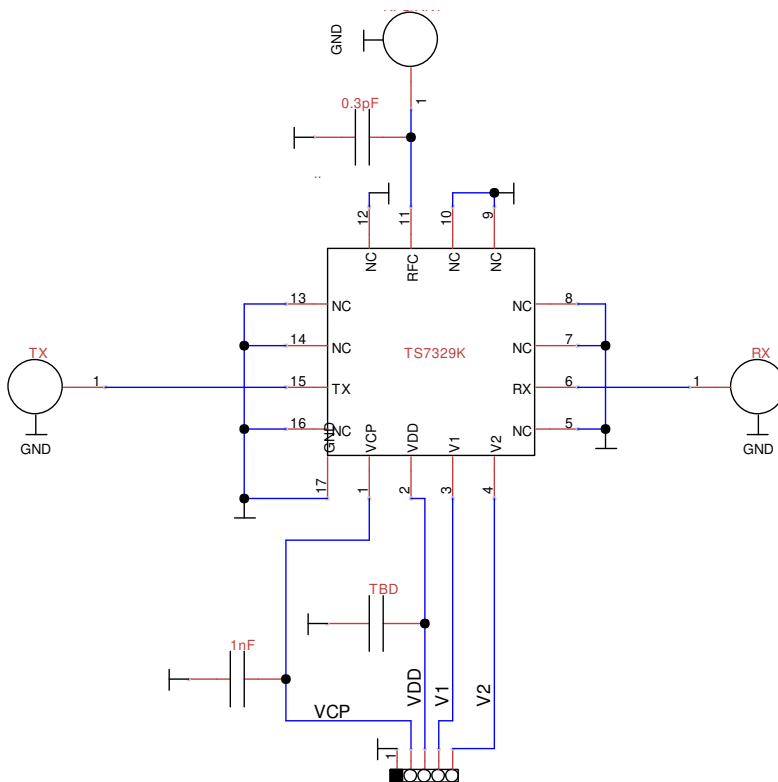


Figure 3 Evaluation Board Schematic

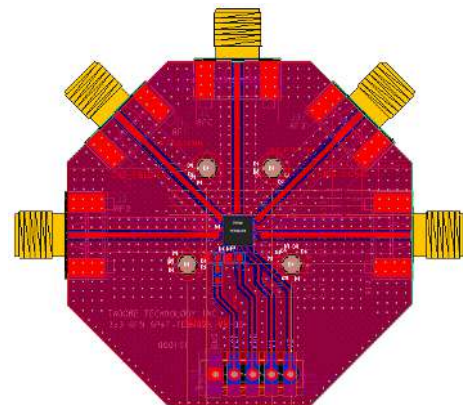


Figure 4 Evaluation Board Image

Attention:

- [1] 17 refers to the center pad of the device.
- [2] The purpose of connection between VCP and connector N1 is to monitor VCP, do not apply external voltage to VCP.
- [3] Below 4GHz, no match required on ANT port.
- [4] For 4.4~5GHz : Add 0.3pF (Passive Plus 0402N0R3AW251) to GND close to RFC pin.

10.0 Typical Characteristics
10.1 With No Match

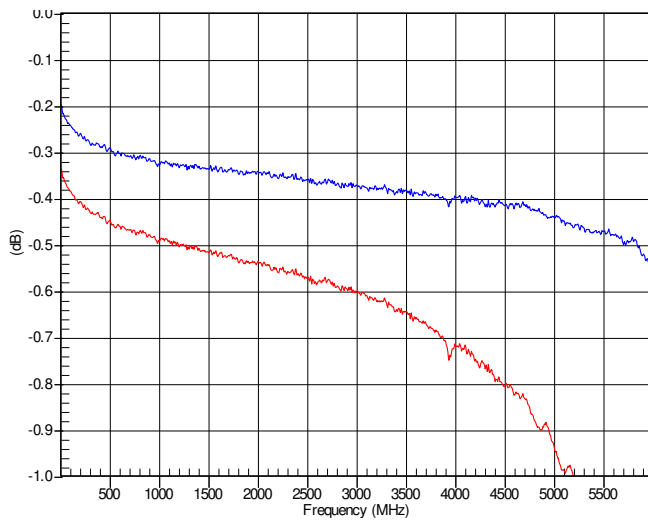


Figure 5 TX, RX Insertion Loss

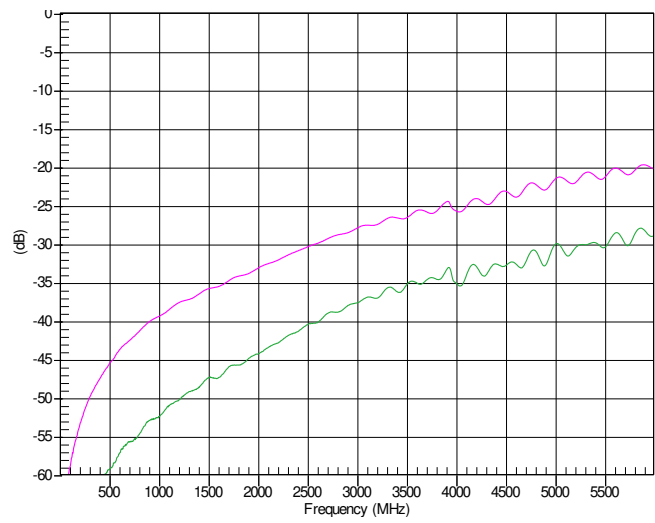


Figure 6 TX, RX Isolation

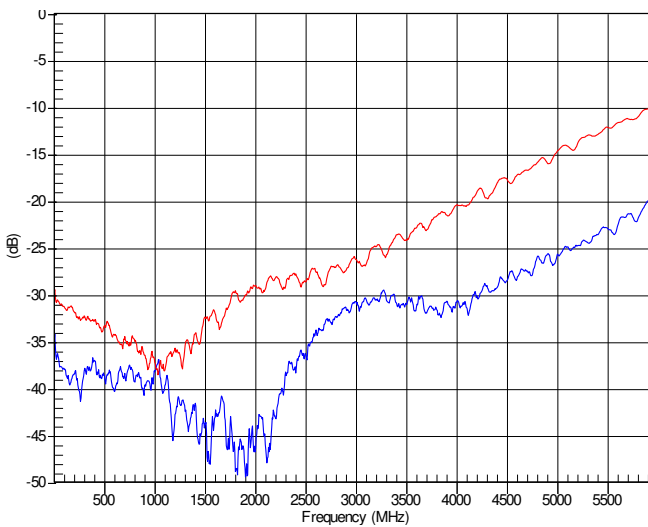


Figure 7 TX, RX Return Loss

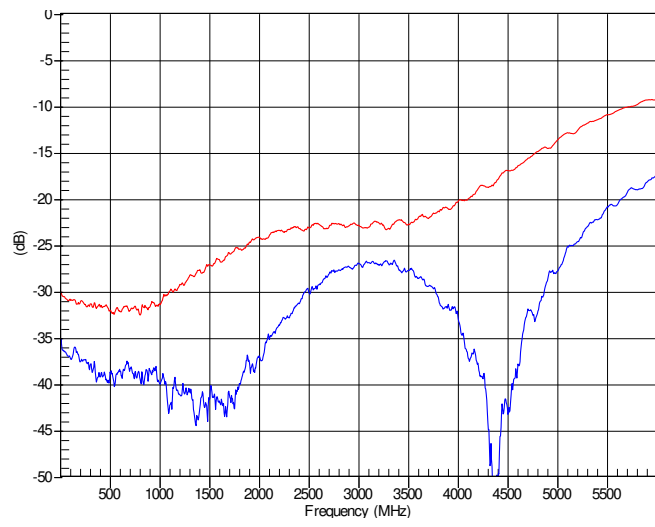


Figure 8 ANT Return Loss

10.2 With Match Tuned for 4.4~5GHz

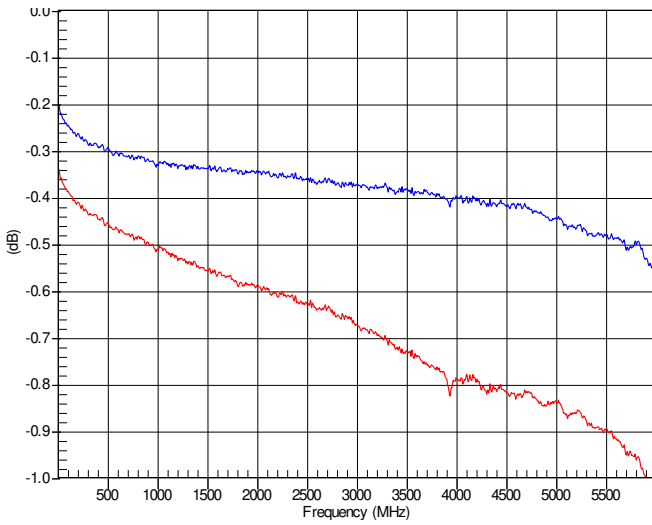


Figure 9 TX, RX Insertion Loss

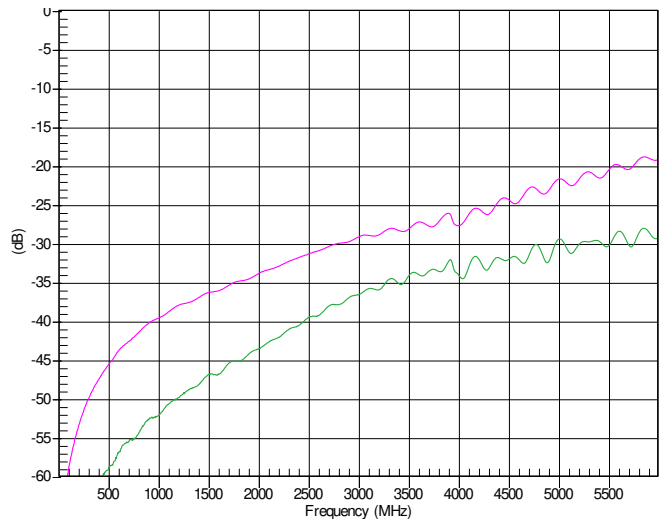


Figure 10 TX, RX Isolation

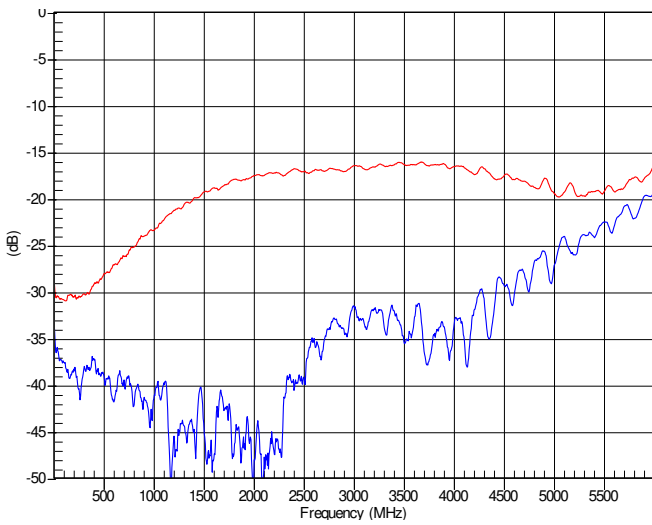


Figure 11 TX, RX Return Loss

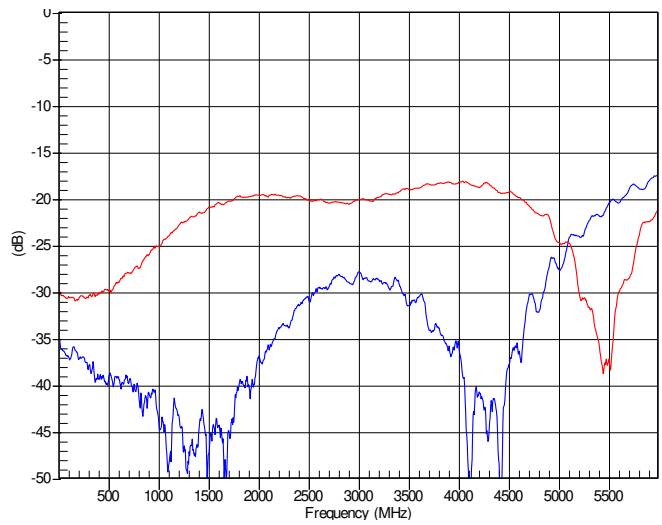


Figure 12 ANT Return Loss

11.0 Device Package Information

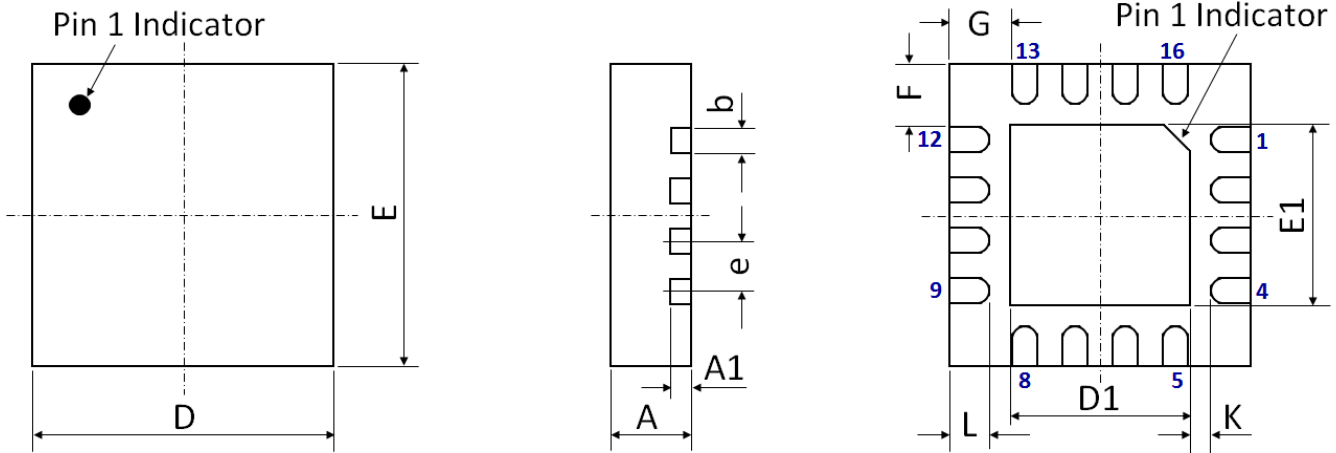


Figure 13 Device Package Drawing
(All dimensions are in mm)

Table 6 Device Package Dimensions

| Dimension (mm) | Value (mm) | Tolerance (mm) | Dimension (mm) | Value (mm) | Tolerance (mm) |
|----------------|------------|----------------|----------------|------------|----------------|
| A | 0.80 | ±0.05 | E | 3.00 BSC | ±0.05 |
| A1 | 0.203 | ±0.02 | E1 | 1.70 | ±0.05 |
| b | 0.25 | ±0.05 | F | 0.625 | ±0.05 |
| D | 3.00 BSC | ±0.05 | G | 0.625 | ±0.05 |
| D1 | 1.70 | ±0.05 | L | 0.25 | ±0.05 |
| e | 0.50 BSC | ±0.05 | K | 0.40 | ±0.05 |

Note: Lead finish: Pure Sn without underlayer; Thickness: 7.5µm ~ 20µm (Typical 10µm ~ 12µm)

Attention:

Please refer to application notes [TN-001](#) and [TN-002](#) at <http://www.tagoretech.com> for PCB and soldering related guidelines.

12.0 PCB Land Design

Guidelines:

- [1] 4 layer PCB is recommended.
- [2] Via diameter is recommended to be 0.2mm to prevent solder wicking inside the vias.
- [3] Thermal vias shall only be placed on the center pad.
- [4] The maximum via number for the center pad is $3(X) \times 3(Y) = 9$.

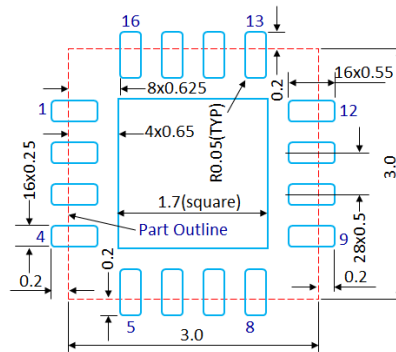


Figure 14 PCB Land Pattern
(Dimensions are in mm)

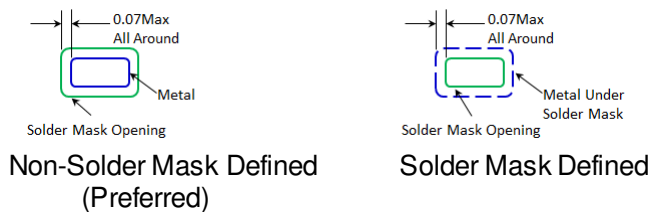


Figure 15 Solder Mask Pattern
(Dimensions are in mm)

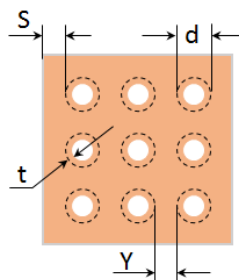


Figure 16 Thermal Via Pattern
(Recommended Values: $S \geq 0.15\text{mm}$; $Y \geq 0.20\text{mm}$; $d = 0.2\text{mm}$; Plating Thickness $t = 25\mu\text{m}$ or $50\mu\text{m}$)

13.0 PCB Stencil Design

Guidelines:

[1] Laser-cut, stainless steel stencil is recommended with electro-polished trapezoidal walls to improve the paste release.

[2] Stencil thickness is recommended to be 125µm.

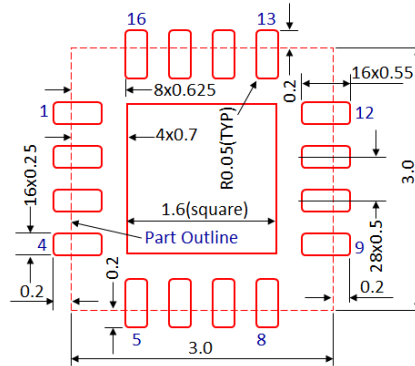


Figure 17 Stencil Openings
(Dimensions are in mm)

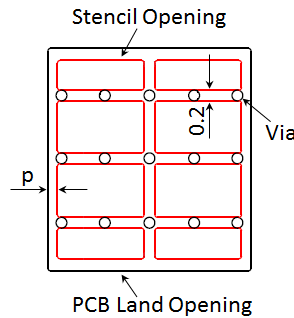


Figure 18 Stencil Openings Shall not Cover Via Areas If Possible
(Dimensions are in mm)

14.0 Tape and Reel Information

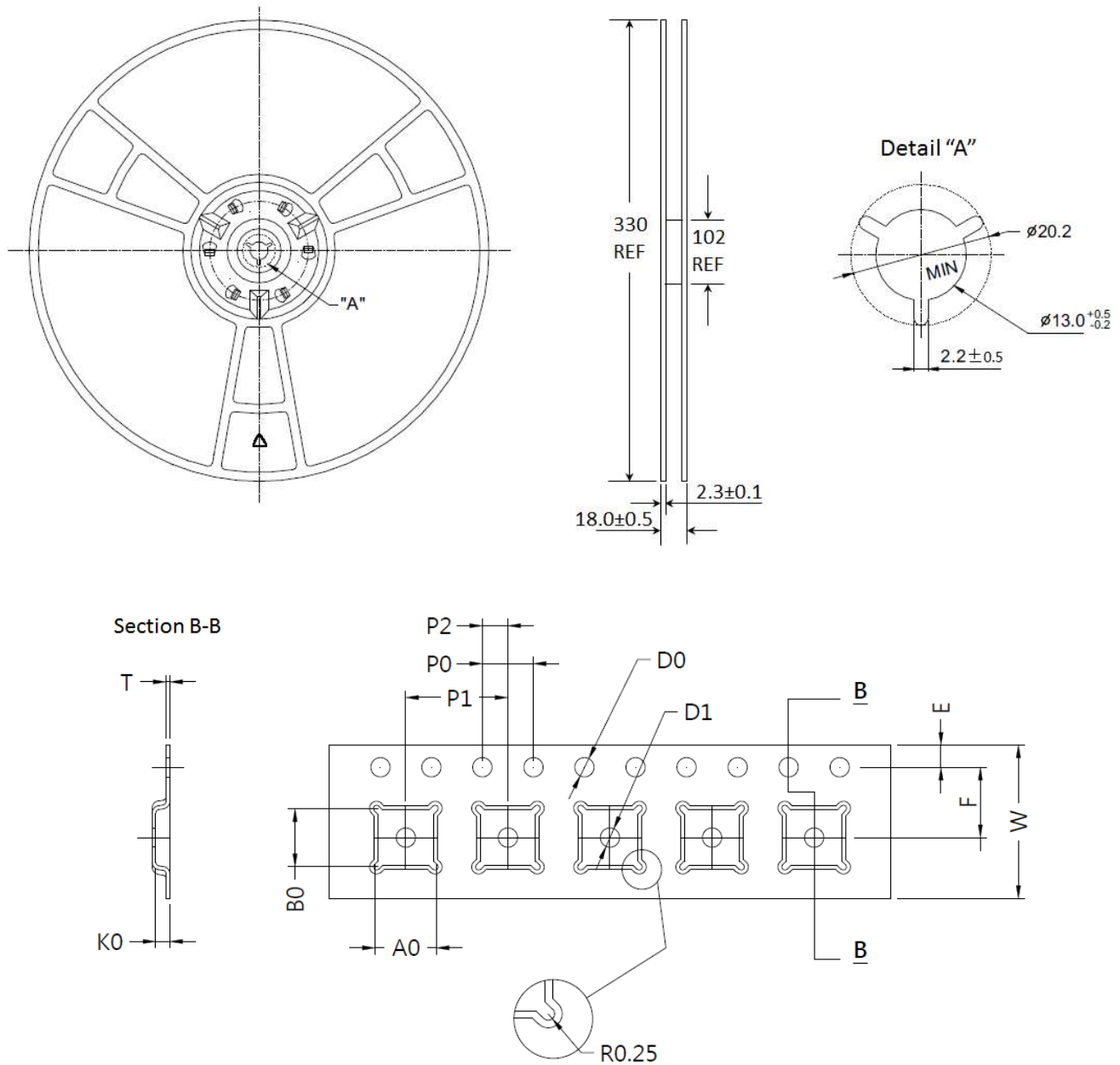


Figure 19 Tape and Reel Drawing

Table 7 Tape and Reel Dimensions

| Dimension (mm) | Value (mm) | Tolerance (mm) | Dimension (mm) | Value (mm) | Tolerance (mm) |
|----------------|------------|----------------|----------------|------------|----------------|
| A0 | 3.35 | ±0.10 | K0 | 1.10 | ±0.10 |
| B0 | 3.35 | ±0.10 | P0 | 4.00 | ±0.10 |
| D0 | 1.50 | +0.10/-0.00 | P1 | 8.00 | ±0.10 |
| D1 | 1.50 | +0.10/-0.00 | P2 | 2.00 | ±0.05 |
| E | 1.75 | ±0.10 | T | 0.30 | ±0.05 |
| F | 5.50 | ±0.05 | W | 12.00 | ±0.30 |

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