2.1MHz, 20A Multi-Phase Step-Down Converter with I^2C Interface

General Description

The RTQ2134 is a multi-phase, programmable power management IC that integrates with four high efficient, synchronous step-down converter cores. The RTQ2134 can be 2 + 2 and 2 + 1 + 1 output by OTP. It also features wide output voltage range and the capability to configure the corresponding power stages, which make the device optimized to meet power management requirements for low-power processors, such as core power for CPUs and GPUs. The RTQ2134 supports many programmable functions including voltage level, slew rate of voltage change, and slew rate of soft-start via an I2C interface capable of operating up to 3.4MHz. The RTQ2134 also supports remote-sense function to get accurate output voltage at large loading. Moreover, the device has interrupt and fault-detection function to report error status. The RTQ2134 is available in a WET-WQFN-30L 4.5x5 (FC) package.

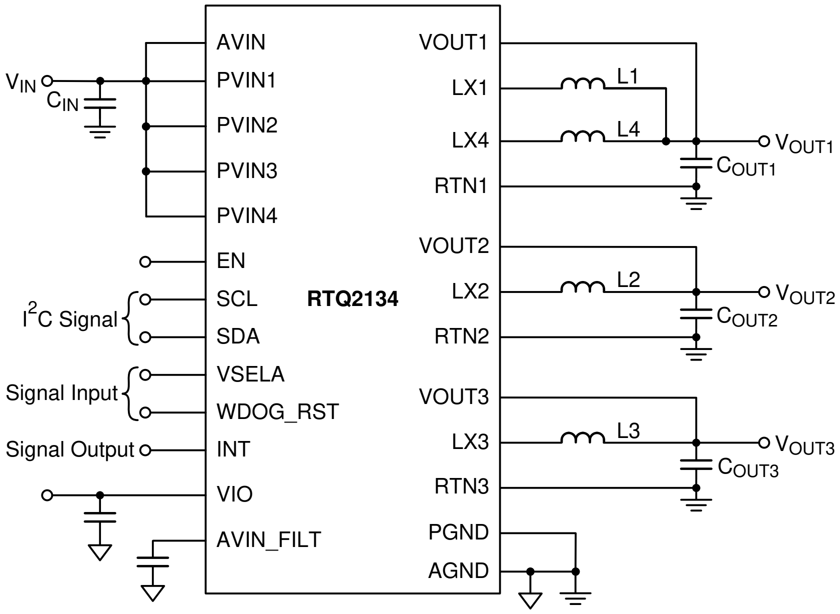
Applications

- Automotive Systems

Features

- **FMEA Compliant PinOut**
- **AEC-Q100 Grade1 Qualified**
- **2 + 2 / 2 + 1 + 1 Phase Output**
- **I^2C Programmable Output Voltage : 0.3V to 1.85V**
- **Maximum Output Current : Total 20A, 5.5A per Phase**
- **Output Remote Sense**
- **Fast Transient Response**
- **Input Supply Voltage Range : 3V to 6V**
- **Selectable Automatic Phase Shielding and Power Saving Mode Enables Higher Light Load Efficiency**
- **Dynamic Voltage Scaling (DVS) with Programmable Slew Rate for Each Output**
- **Programmable Soft-Start Function**
- **Interrupt Function and Fault Detection**
- **Watchdog Function**
- **Input Under-Voltage Lockout (UVLO)**
- **Cycle by Cycle Current Limit**
- **Output Under-Voltage Protection**
- **Over-Temperature Protection**
- **WET-WQFN-30L 4.5x5 (FC)**

Simplified Application Circuit



Ordering Information

Part Number	I^2C Address	Default VOUT and Delay Time	Lead Plating System	Package Type	Grade
Program to 2 + 1 + 1 phase operation					
RTQ2134GQWTF-21-QA-00	0x18	(1) VOUTx = 1V (2) No Enable/Disable delay time	G : Green (Halogen Free and Pb Free)	QWTF : WET-WQFN-30L 4.5x5 (FC) (W-Type)	QA : AEC-Q100 Qualified and Screened by High Temperature
RTQ2134GQWTF-21-QA-01	0x18	(1) VOUTx = 1V (2) Enable delay time : VOUT1/2/3 = 0/4/4ms (3) Disable delay time : VOUT1/2/3 = 4/0/0ms			
RTQ2134GQWTF-21-QA-02	0x19	(1) VOUTx = 1V (2) No Enable/Disable delay time			
RTQ2134GQWTF-21-QA-03	0x18	(1) VOUT1/2/3 = 0.75V/1.125V/0.6V (2) Enable delay time : VOUT1/2/3 = 3/2/8ms (3) Disable delay time : VOUT1/2/3 = 4/8/0ms			
Program to 2 + 2 phase operation					
RTQ2134GQWTF-22-QA-00	0x18	(1) VOUTx = 1V (2) No Enable/Disable delay time	G : Green (Halogen Free and Pb Free)	QWTF : WET-WQFN-30L 4.5x5 (FC) (W-Type)	QA : AEC-Q100 Qualified and Screened by High Temperature
RTQ2134GQWTF-22-QA-01	0x18	(1) VOUTx = 1V (2) Enable delay time : VOUT1/2 = 4/0ms (3) Disable delay time : VOUT1/2 = 0/4ms			
RTQ2134GQWTF-22-QA-02	0x18	(1) VOUTx = 1V (2) Enable delay time : VOUT1/2 = 3/0ms (3) Disable delay time : VOUT1/2 = 0/3ms			
RTQ2134GQWTF-22-QA-03	0x18	(1) VOUT1/2 = 1.15V/1.06V (2) No Enable/Disable delay time			
RTQ2134GQWTF-22-QA-N0	0x18	(1) VOUT1 = 1V, VOUT2 = Disable (2) No Enable/Disable delay time			
RTQ2134GQWTF-22-QA-N1	0x19	(1) VOUTx = 1V (2) No Enable/Disable delay time			

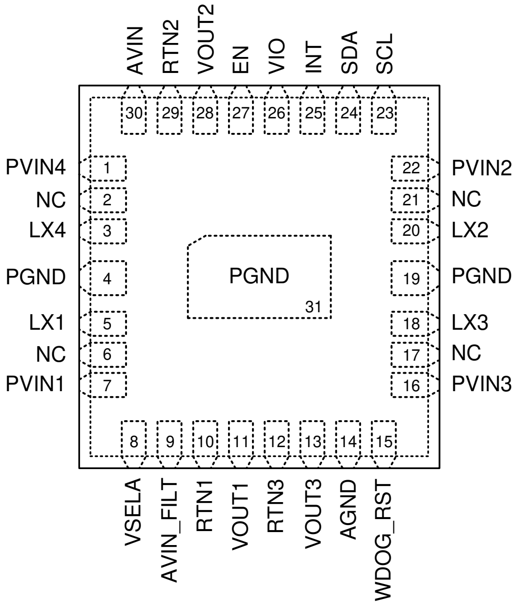
Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Pin Configuration

(TOP VIEW)



WET-WQFN-30L 4.5x5 (FC)

Marking Information

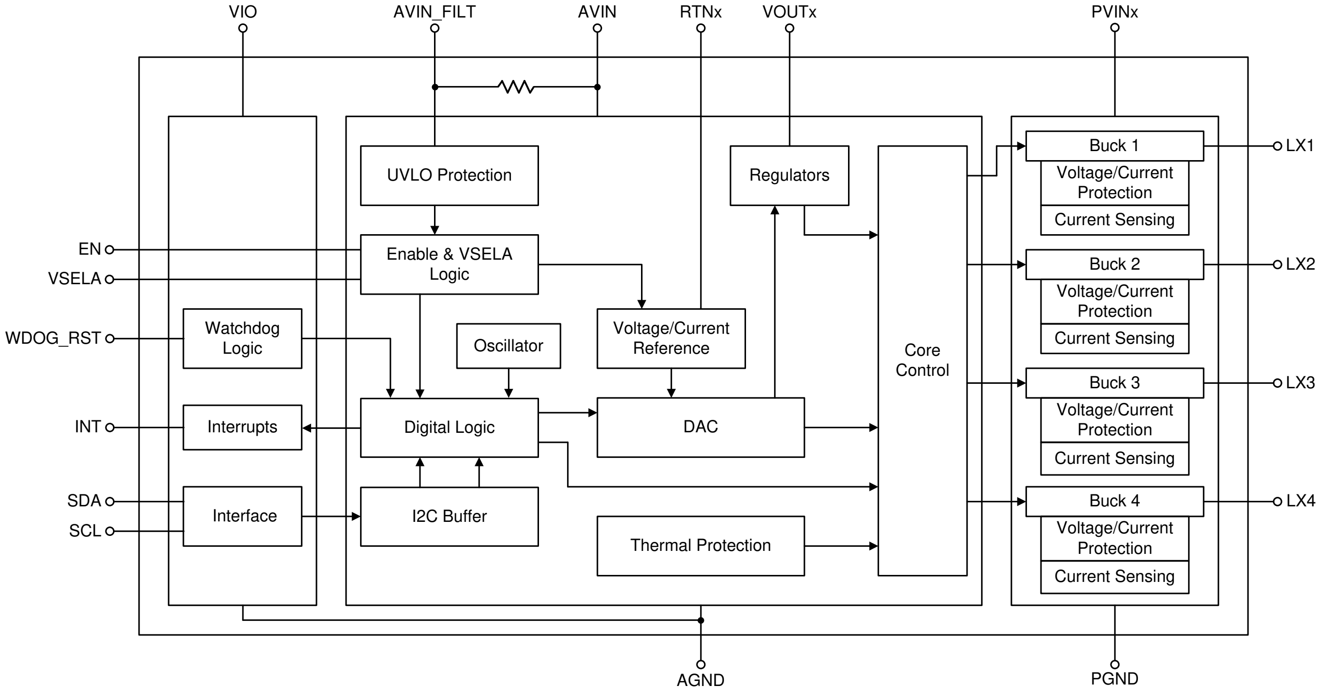
For marking information, contact our sales representative directly or through a Richtek distributor located in your area.

Functional Pin Description

Pin No.	Pin Name	Pin Function
1	PVIN4	Power input for power stage 4. It is recommended to use a 10-μF, X7R capacitor.
2, 6, 17, 21	NC	No internal connection.
3	LX4	Switching node for power stage 4.
4, 19	PGND	Power ground for power stage.
5	LX1	Switching node for power stage 1.
7	PVIN1	Power input for power stage 1. It is recommended to use a 10-μF, X7R capacitor.
8	VSELA	VSEL input pin for all channels. Using corresponding register to define action. "Do Not" leave this pin floating.
9	AVIN_FILT	Filtered analog supply voltage. It is recommended to use a 1-μF, X7R capacitor.
10	RTN1	Remote ground sense for Buck1.
11	VOUT1	Output voltage sense for Buck1.
12	RTN3	Remote ground sense for Buck3.
13	VOUT3	Output voltage sense for Buck3.
14	AGND	Analog GND.

Pin No.	Pin Name	Pin Function
15	WDOG_RST	Control input for output voltage reset. Reset each Buck output voltage, DVSx, and ENDVSx registers to factory default setting value when this pin is pulled low. Connect this pin to be higher than 70% of VIO pin voltage if this pin is not used. "Do Not" leave this pin floating. The minimum watchdog debounce time is 100μs. Note that the factory default setting value in watchdog register (0x25) is 0x00h (Disabled).
16	PVIN3	Power input for power stage 3. It is recommended to use a 10-μF, X7R capacitor.
18	LX3	Switching node for power stage 3.
20	LX2	Switching node for power stage 2.
22	PVIN2	Power input for power stage 2. It is recommended to use a 10-μF, X7R capacitor.
23	SCL	Clock input for I^2C interface. The pull-up voltage supply must be the same as VIO voltage for correct operation. Connect this pin to AGND if I^2C interface is not used. "Do Not" leave this pin floating.
24	SDA	Data line for I^2C interface. The pull-up voltage supply must be the same as VIO voltage for correct operation. Connect this pin to AGND if I^2C interface is not used. "Do Not" leave this pin floating.
25	INT	Interrupt indicator. When INT function is used, set 0x33[6] = 1, 0x34[6] = 1 and 0x35[6] = 1.
26	VIO	I/O supply voltage for digital communications. Connect this pin to 1.8V for normal operation. "Do Not" leave this pin floating.
27	EN	Master chip enable. A logic-high enables the converter; a logic-low forces the device into shutdown mode. "Do Not" leave this pin floating.
28	VOUT2	Output voltage sense for Buck2.
29	RTN2	Remote ground sense for Buck2.
30	AVIN	Analog input voltage.
31(Exposed PAD)	PGND	Exposed pad. The exposed pad is connected to PGND and must be soldered to a large PCB copper area for maximum power dissipation.

Functional Block Diagram



Operation

The RTQ2134 is a power management IC that integrates four high efficiency Buck converters, and is capable of providing multiphase or single phase operation. Each of the four converters provides up to 5.5A of maximum output current over an input supply voltage range of 3.3V to 6V.

The RTQ2134 utilizes the proprietary Advanced Constant On-Time (ACOT®) control architecture. The ultrafast ACOT® control enables the use of small ceramic capacitors (MLCC) to save the PCB size.

During normal operation, the internal high-side power switch (HSFET) is turned on for a fixed interval determined by a one-shot timer at the beginning of each clock cycle. When the HSFET is turned off, the internal low-side power switch (LSFET) is turned on. The output voltage is sensed remotely at VOUTx and RTNx for high accuracy and is compared to an internal reference voltage. Hence, the error signal is obtained and internally compensated. The compensated error signal is then compared to an internal ramp signal. When the minimum off-time one-shot (100ns, max.) has timed out and the inductor current is below the current-limit threshold, the one-shot is triggered again if the internal ramp signal falls below the compensated error signal. The ACOT® control architecture features ultrafast transient response. When a load is suddenly increased, the output voltage drops quickly, and triggers a new on-time to rise inductor current again.

Dynamic Voltage Scaling (DVS)

The RTQ2134 provides wide output voltage range with 8-bit resolution and each Buck converter has two independently programmable voltage setting. They are called DVS0 and DVS1. Take Buck1 as two-phase configuration for example, register 0x48[8:0] can set voltage of DVS0 while 0x4A[8:0] is used to set voltage of DVS1. There are two methods to select the DVS. For the first method, it can be changed by software from register 0x52[1:0]. Control DVS0 by setting 0x52[1:0]=00 and DVS1 by setting 0x52[1:0]=01. For the second method, selecting the DVS can be from external hardware pin when setting 0x52[1:0]=10. VSELA pin can be this role and its polarity is defined by 0x52[2]. When setting 0x52[2]=0, pull VSELA high to put DVS0 in use and pull VSELA low to put DVS1 in use. Conversely, when setting 0x52[2]=1, pull VSELA high to put DVS1 in use and pull VSELA low to put DVS0 in use.

The RTQ2134 also supports DVS speed configuration, whether the slew rate of voltage changes in the same DVSx or between DVS0 and DVS1. Take Buck1 as two-phase configuration for example, when output voltage is set from low to high or high to low, register 0x54[6:4] defines slew rate of DVS up while 0x54[2:0] is used to define slew rate of DVS down. In order to have better performance during voltage changing operation, the master/slave enters PWM operation and keeps 200μs after the voltage achieves target even when IC is set to Auto mode. Figure 1 and Figure 2 show the DVS up and down operation.

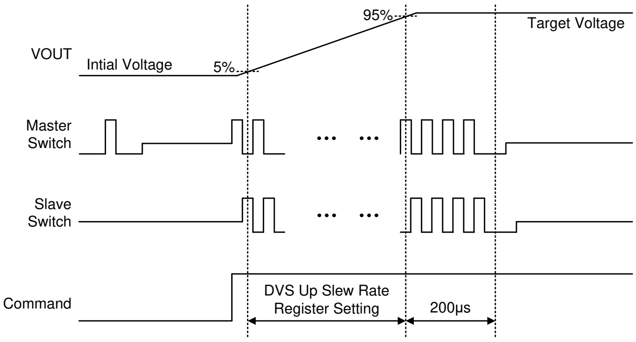


Figure 1. DVS Up Operation

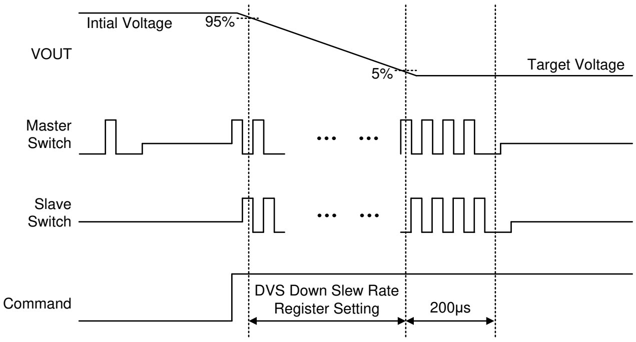


Figure 2. DVS Down Operation

MODE Selection

Whether it is DVS0 or DVS1, there are two modes of operation: forced continuous conduction mode (FCCM) and automatic power saving mode (Auto mode). It is set in the following registers: 0x49[5], 0x4B[5], 0x63[5], 0x65[5], 0x7D[5] and 0x7F[5]. For example, to set DVS0 of Buck1 to FCCM, just write "1" at 0x49[5].

Auto Mode with Automatic Phase Adding/Shedding

Auto mode enables high efficiency at light load. At low load current, the inductor current can drop to zero and become negative. This is detected by internal zero current-detect circuitry utilizing the LSFET $R_{DS(ON)}$ to sense the inductor current. The LSFET is turned off when the inductor current drops to zero, resulting in discontinuous operation (DCM). Both HSFET and LSFET remain off with the output capacitor supplying the load current until the feedback voltage falls below the feedback reference voltage. DCM operation maintains high efficiency at light load, while setting MODE to Forced PWM (FCCM) operation helps meet tight voltage regulation accuracy requirements. For multiphase outputs, the RTQ2134 automatically increases the number of operating phases as the load continues to increase above 3A (typ). The two phases are interleaved with 180 degrees apart. Interleaving reduces ripple current at the input and output. Therefore, the input and output capacitors are also reduced. Conversely, when the load current per phase drops below 2.6A (typ), the RTQ2134 automatically sheds the number of phases.

FCCM Mode

Setting MODE to Forced PWM (FCCM) operation helps meet stringent voltage regulation accuracy requirements. Users must enable all the set outputs before setting into the FCCM.

UVLO, Enable Control and Soft-Start

The RTQ2134 implements under-voltage lockout protection (UVLO) to prevent operation without fully turn on the internal HSFET and LSFET. The UVLO monitors the voltage of AVIN. When the AVIN voltage is lower than UVLO threshold, IC stops switching and resets all digital functions.

The RTQ2134 provides an EN pin, as an external chip enable control, to enable or disable the device. If V_{EN} is held below a logic-low threshold voltage (V_{ENL}) of the enable input (EN), the converter will enter into shutdown mode and reset all digital function (I^2C); that is, the converter is disabled even if the VIN voltage is above VIN under-voltage lockout threshold (V_{UVLO}). During shutdown mode, the supply current can be reduced to I_{SHDN} (20μA or below). If the EN voltage rises above the logic-high threshold voltage (V_{ENH}), the device starts switching. When appropriate voltages are present on the VIN, AVIN, VIO and EN pins, the RTQ2134 will begin digital function, switching and initiate a soft-start ramp of the output voltage. After the device is turned on and VIO is ready, all digital functions including I^2C communication start to work in a boot time with 230μs (typ.). The voltage of VIO can be used to supply power to digital function and it is recommended that enable the device after VIO voltage is ready. The RTQ2134 supports enable delay time setting (factory setting) and soft-start slew rate setting for each Buck. The soft-start function is used to prevent large inrush current while the converter is powered up. Register 0x55[5:4], 0x6F[5:4] and 0x89[5:4] let soft-start time of each be programmable. The start-up sequence is shown in Figure 3. IC also implements enable control by software, it can be set in the registers: 0x49[0], 0x4B[0], 0x63[0], 0x65[0], 0x7D[0] and 0x7F[0]. If the output voltage of Buck is default disable which is only set by factory, the output voltage starts to ramp up by software and the Figure 4 shows the start-up sequence. For disable function, the device supports disable delay time setting (factory setting) by external EN pin and the output voltage ramps down with default discharge resistor. The discharge resistor can be controlled to on or off by register 0x42[0], 0x5F[0] and 0x79[0] when the converter is disabled by software. The power-off sequence is shown in Figure 5 and Figure 6.

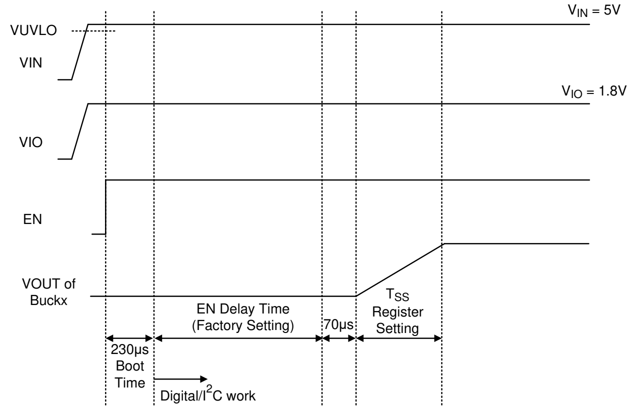


Figure 3. Start-up Sequence

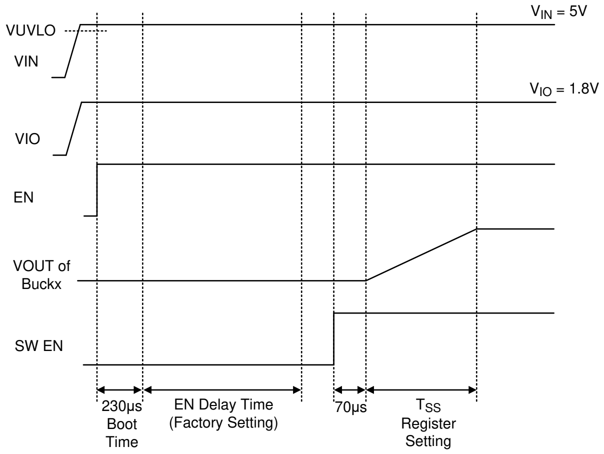


Figure 4. Start-up Sequence by Software

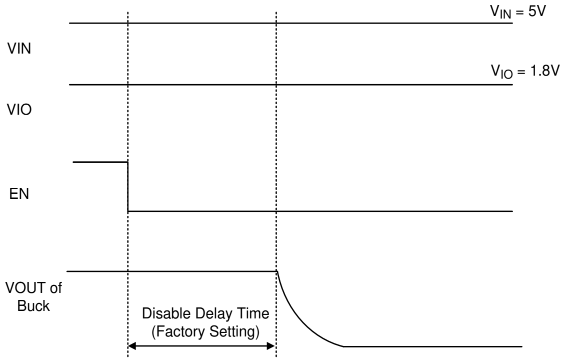


Figure 5. Power-off Sequence

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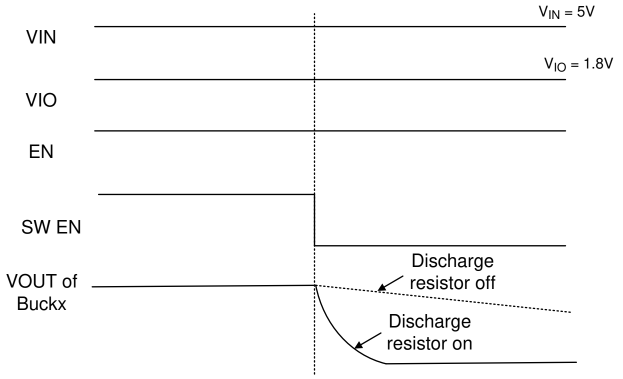


Figure 6. Power-off Sequence by Software

Power Good Indication

The RTQ2134 provides a power good indication and this function shows the status of output voltage. When output voltage is between 110% and 90% of setting voltage for each Buck, the PG indication bit goes high. The relative registers are 0x14[7], 0x15[7] and 0x16[7].

Fault Detection and Interrupt Pin

The RTQ2134 alerts the host when a warning, like Boot and Hot Die, or fault events, like over-voltage, under-voltage and over-temperature conditions have occurred. Registers 0x13, 0x14, 0x15 and 0x16 can help host to know if the fault or waning event happens. These bits relative to events can be read and cleared. Moreover, the RTQ2134 provides an interrupt pin with the push-pull output capability and this pin shows these events by using active low. When INT function is used, set 0x33[6] = 1, 0x34[6] = 1 and 0x35[6] = 1. The pull high output voltage of INT pin will be VIO voltage. Register 0x32, 0x33, 0x34 and 0x35 can also set the mask function to mask or pass the event flag output to external interrupt pin. The overall detection function is shown in Figure 7.

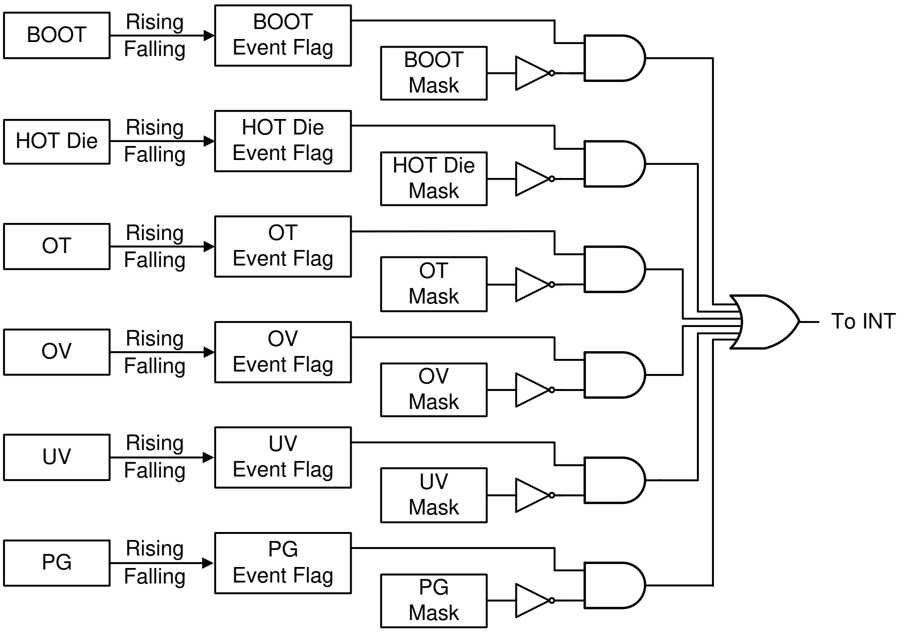


Figure 7. Overall Detection Function

Watchdog Function

The RTQ2134 implements a watchdog function which resets each Buck output voltage, DVSx, and ENDVSx registers to factory default setting value. Register 0x25 can enable or disable watchdog function of each Buck and provide the debounce time for selection. The minimum watchdog debounce time is 100μs when 0x25[2:0] is set to 000. The operation of watchdog reset is shown in Figure 8. Table 1 shows the registers will be reset when WDOG_RST pin is pulled low. The I^{2}C command needs to be after the WDOG_RST is pulled high.

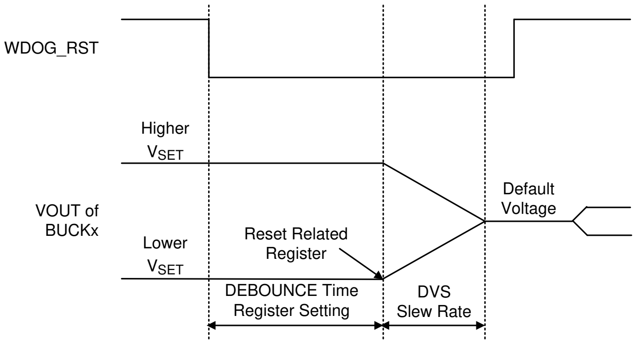


Figure 8. Watchdog Reset Operation

Table 1. Watchdog Reset Register

BUCK1_WDT	BUCK2_WDT	BUCK3_WDT
0x48	0x62	0x7C
0x49[0]	0x63[0]	0x7D[0]
0x4A	0x64	0x7E
0x4B[0]	0x65[0]	0x7F[0]
0x52	0x6C	0x86

Over-Current Protection

The RTQ2134 features cycle-by-cycle current-limit protection on both HSFET and LSFET to prevent the device from the catastrophic damage in output short-circuit, over-current or inductor saturation conditions.

The HSFET over-current protection is achieved by an internal current comparator that monitors the current in the HSFET during each on-time. The switch current is compared with the HSFET peak-current limit (I_{LIM_H}) after a certain amount of delay when the HSFET is turned on each cycle. If an over-current condition occurs, the converter will immediately turn off the HSFET and turn on the LSFET to prevent the inductor current from exceeding the HSFET current limit.

The LSFET over-current protection is achieved by measuring the inductor current through the LSFET during the LSFET on-time. Once the current rises above the LSFET valley current limit (I_{LIM_L}), the on-time one-shot will be inhibited until the inductor current ramps down to the current limit level (I_{LIM_L}), that is, another on-time can only be triggered when the inductor current goes below the LSFET current limit. If the output load current exceeds the available inductor current (clamped by the LSFET current limit), the output capacitor needs to supply the extra current so that the output voltage will begin to drop. If it drops below the output under-voltage protection trip threshold, the IC will stop switching to avoid excessive heat.

Output Under-Voltage Protection

The RTQ2134 includes output under-voltage protection (UVP) against over-load or short-circuited condition by constantly monitoring the output voltage V_{OUT}. If V_{OUT} drops below the under-voltage protection trip threshold (typically 50% of the internal reference voltage), both HSFET and LSFET will stop switching. Register 0x37[3], 0x38[3] and 0x39[3] can select hiccup or latch protection behavior of each Buck converter when converter is in UV condition. For hiccup behavior, both HSFET and LSFET keep low state in a 1ms and then IC starts to switch. If the output voltage is not greater than UV threshold after internal soft-start end signal is triggered, both HSFET and LSFET will still keep low state again for next cycle. When each Buck is set to latch mode, UVP will let converter enter shutdown mode unless resetting IC by external EN pin or falling to UVLO low threshold.

Over-Temperature Protection

The RTQ2134 includes an over-temperature protection (OTP) circuitry to prevent overheating due to excessive power dissipation. The OTP shuts down switching operation when junction temperature exceeds a thermal shutdown threshold T_{SD}. Once the junction temperature cools down by a thermal shutdown hysteresis (ΔT_{SD}), the IC resumes normal operation with a complete soft-start. It can select not to shut down IC when OTP happens by using register 0x30[3].

Note that the over-temperature protection is intended to protect the device during momentary overload conditions. The protection is activated outside of the absolute maximum range of operation as a secondary fail-safe and therefore should not be relied upon operationally. Continuous operation above the specified absolute maximum operating junction temperature may impair device reliability or permanently damage the device.

Absolute Maximum Ratings (Note 1)

- Supply Input Voltage ---------- –0.3V to 6.5V
- LX Pin Switch Voltage---------- –0.3V to 7.3V
  < 100ns ---------- –5V to 9V
- Other I/O Pin Voltages ---------- –0.3V to 7.3V
- Power Dissipation, P_D @ T_A = 25°C
  WET-WQFN-30L 4.5x5 (FC) ---------- 2.87W
- Package Thermal Resistance (Note 2)
  WET-WQFN-30L 4.5x5 (FC), θ_{JA} ----------34.8°C/W
  WET-WQFN-30L 4.5x5 (FC), $\theta_{JC(Top)}$----------18.2°C/W
  WET-WQFN-30L 4.5x5 (FC), θ_{JB} ----------13.2°C/W
- Lead Temperature (Soldering, 10 sec.)---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 4)

- Supply Input Voltage (for 2 + 2 application)---------- 3.3V to 6V
- Supply Input Voltage (for 2 + 1 + 1 application) ---------- 3V to 6V
- VIO Input Voltage ---------- 1.7V to V_{IN}
- Junction Temperature Range ---------- –40°C to 150°C

Electrical Characteristics

(V_{IN} = 3.7V, T_J = –40°C to 125°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Analog Input Voltage	V_{AVIN}	For 2 + 2 application	3.3	--	6	V
Power Input Voltage	V_{PVIN}	For 2 + 2 application	3.3	--	6	V
Shutdown Current	I_{SHDN}	EN = 0V, Digital circuit doesn't work	--	1	20	μA
Buck Off Current	I_{SDBO}	EN = VIO = 1.8V, disable all Buck by software	--	20	80	μA
1Phase no Switching Current	I_{SLP}	V_{OUT} = 1.2 x $V_{OUT\_SETTING}$	--	70	120	μA
Under-Voltage Lockout Threshold	V_{UVLO}	V_{IN} rising	2.1	2.32	2.45	V
Under-Voltage Lockout Hysteresis	ΔV_{UVLO}		--	300	--	mV
High-Side Switch On-Resistance	$R_{DS(ON)\_H}$	V_{IN} = 5V	18	25	45	mΩ
Low-Side Switch On-Resistance	$R_{DS(ON)\_L}$	V_{IN} = 5V	8	15	25	mΩ

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
SDA, SCL, VSELA, WDOG_RST	Logic-High	V_{IH}	$3V \le V_{IN} \le 6V$	0.7 x VIO	--	--	V
	Logic-Low	V_{IL}	$3V \le V_{IN} \le 6V$	--	--	0.3 x VIO	
EN Threshold	Logic-High	V_{ENH}		1.2	--	--	V
	Logic-Low	V_{ENL}		--	--	0.4	
External Supply Voltage for I/O Pin		$V_{IN\_I/O}$		1.7	1.8	V_{IN}	V
V_{OUT} DC Accuracy			Auto PFM/PWM, $V_{OUT} = 1V$ (Note 5)	–2.5	--	2.5	%
			Forced PWM, $0.6V \le V_{OUT} \le 1.85V$	–1.5	--	1.5	%
Load Regulation		ΔV_{LOAD}	$I_{OUT(DC)}$ = 1 to 5A (Note 5)	--	–0.08	--	%/A
Line Regulation		ΔV_{LINE}	$3V \le V_{IN} \le 6V$, $I_{OUT(DC)} = 1.5A$ (Note 5)	--	0.2	--	%/V
Load Transient Response			2phase operation, 0.1 to 4A, $t_R = t_F = 1\mu s$, $L = 0.33\mu H$, $C_{OUT} = 44\mu F$/phase (Note 5)	--	±40	--	mV
			1phase operation, 0.1 to 2A, $t_R = t_F = 1\mu s$, $L = 0.33\mu H$, $C_{OUT} = 44\mu F$/phase (Note 5)	--	±40	--	mV
Line Transient Response			4V to 5V, $t_R = t_F = 10\mu s$ (Note 5)	--	±40	--	mV
Current Balance			Load = 10A, $\lvert I_{Avg} - I_{LX\_1 \text{ or } 4} \rvert$	--	--	0.5	A
Phase Adding Level			From 1phase to 2phase (Note 5)	--	3	--	A
Phase Shedding Level			From 2phase to 1phase (Note 5)	--	2.6	--	A
Soft-Start Time		Tstart	Slew Rate = 10mV/μs	–20	--	20	%
High-Side Switch Current Limit per Channel		I_{LIM_H}		5.8	8	11	A
Low-Side Switch Current Limit per Channel		I_{LIM_L}		5.1	7	9	A
Thermal Shutdown		T_{SD}		--	160	--	°C
Thermal Shutdown Hysteresis		ΔT_{SD}		--	30	--	°C
HOT Die Warning			0xAA = 0x02 (Note 5)	--	109	--	°C
HOT Die Hysteresis		T_{HYSHD}	(Note 5)	--	15	--	°C
Discharge Resistor				70	115	180	Ω
Output UVP Flag		V_{UVP_T}	Trigger Level	40	50	60	%
		V_{UVP_R}	Recovery Level	--	57	--	%
Output OVP Flag		V_{OVP_T}	Trigger Level	123	133	143	%
		V_{OVP_R}	Recovery Level	--	125	--	%
Switching Frequency		f_{SW}	$V_{OUT} = 1V$	1850	2100	2500	kHz

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Error Rate of DVS Slew Rate		V_{IN} = 3.7V, V_{OUT} = 0.6V to 1.2V	–20	--	20	%
Digital Output Pin : INT		Output low level, I_{SOURCE} = 2mA	--	--	0.4	V
		Push-pull, I_{SINK} = 2mA	1.6	--	VIO	V
Digital Output Pin : SDA		Output low level Resistor	--	--	40	Ω
I^{2}C Speed			--	--	3.4	MHz
Hold Time (Repeated) Start Condition. After this Period, the First Clock Pulse is Generated	$t_{HD;STA}$	Fast mode (Note5)	0.6	--	--	μs
Low Period of the SCL Clock	t_{LOW}	Fast mode (Note5)	1.3	--	--	μs
High Period of the SCL Clock	t_{HIGH}	Fast mode (Note5)	0.6	--	--	μs
Set-Up Time for a Repeated START Condition	$t_{SU;STA}$	Fast mode (Note5)	0.6	--	--	μs
Data Hold Time	$t_{HD;DAT}$	Fast mode (Note5)	0	--	0.9	μs
Data Set-Up Time	$t_{SU;DAT}$	Fast mode (Note5)	100	--	--	ns
Set-Up Time for STOP Condition	$t_{SU;STO}$	Fast mode (Note5)	0.6	--	--	μs
Bus Free Time between a STOP and START Condition	t_{BUF}	Fast mode (Note5)	1.3	--	--	μs
Rising Time of both SDA and SCL Signals	t_R	Fast mode (Note5)	20	--	300	ns
Falling Time of both SDA and SCL Signals	t_F	Fast mode (Note5)	20	--	300	ns
SDA Output Low Sink Current	I_{OL}	SDA Voltage = 0.4V (Note5)	2	--	--	mA
Detect SDA Low Timeout	$t_{TIMEOUT}$	Fast/High speed mode (Note5)	--	30	--	ms

Note 1. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured in the natural convection at T_A = 25°C on a Four-layer Richtek Evaluation Board. θ_{JC} is measured at the top of the package.

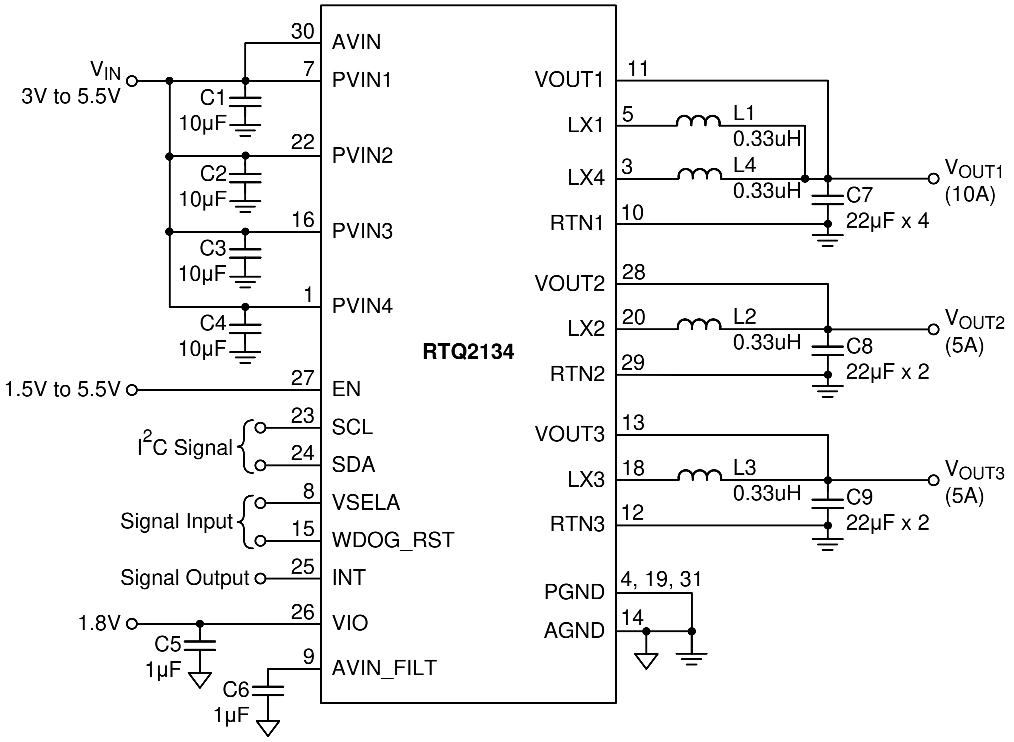
Note 3. Devices are ESD sensitive. Handling precautions are recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

Note 5. Guaranteed by design.

Typical Application Circuit

2 + 1 + 1 Phase



2 + 2 Phase

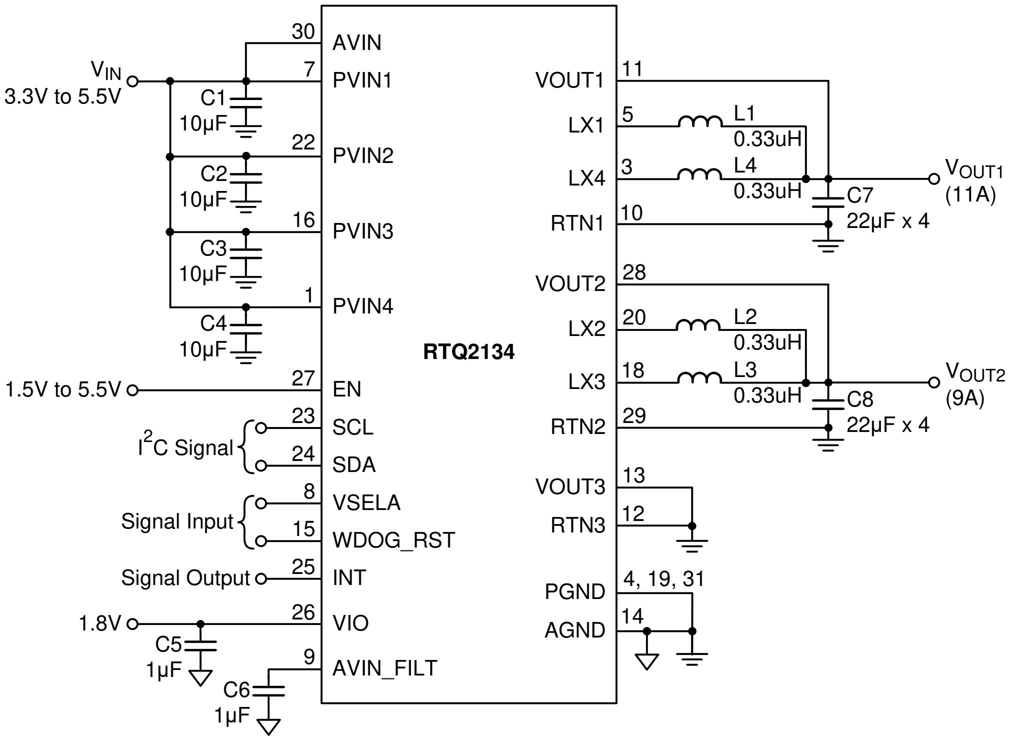


Table 2. Recommended BOM

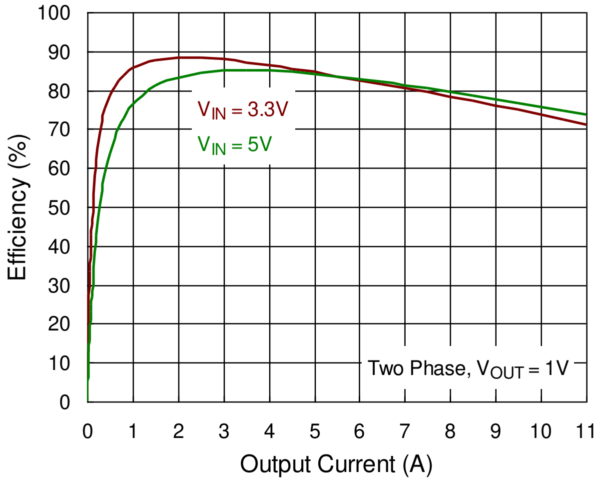
Reference	Qty	Part number	Description	Package	Manufacture
U1	1	RTQ2134	DC-DC Converter	WET-WQFN-30L 4.5x5 (FC)	RICHTEK
C1, C2, C3, C4	4	GRT188C81A106ME	10μF	C-0603	Murata
C5, C6	2	GRT188C8YA105KE	1μF	C-0603	Murata
C7, C8, C9	8	GRT31CR70J226KE	22μF	C-1206	Murata
L1, L2, L3, L4	4	VCTA25201B-R33MS6	0.33μH	2520	Cyntec

Note :

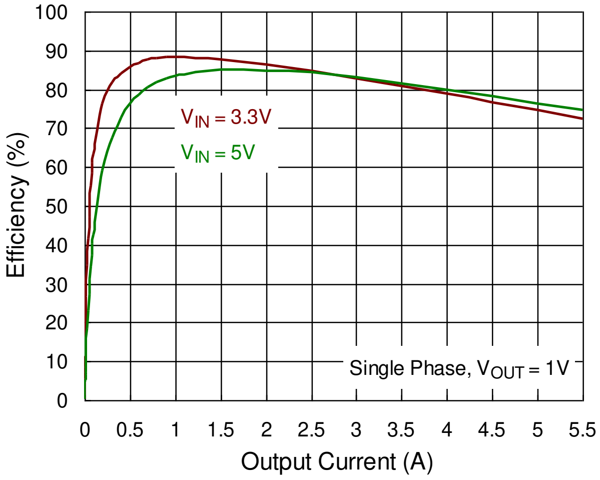
1. C_{OUT} = 44μF per-phase is min. value for the RTQ2134.
2. All the input and output capacitors are the suggested values, referring to the effective capacitances, subject to any de-rating effect, like a DC bias.

Typical Operating Characteristics

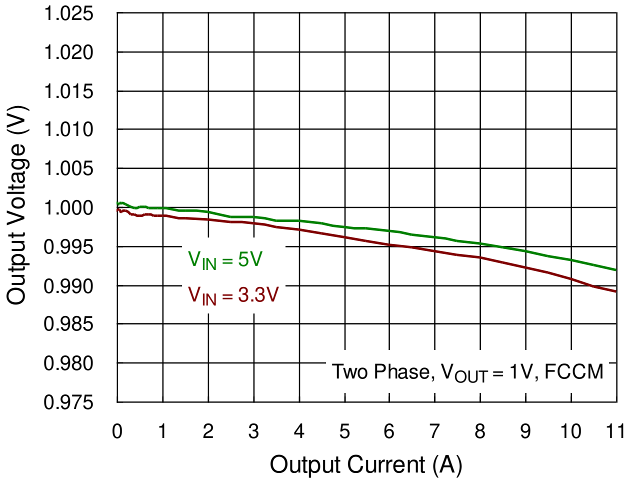
Efficiency vs. Output Current



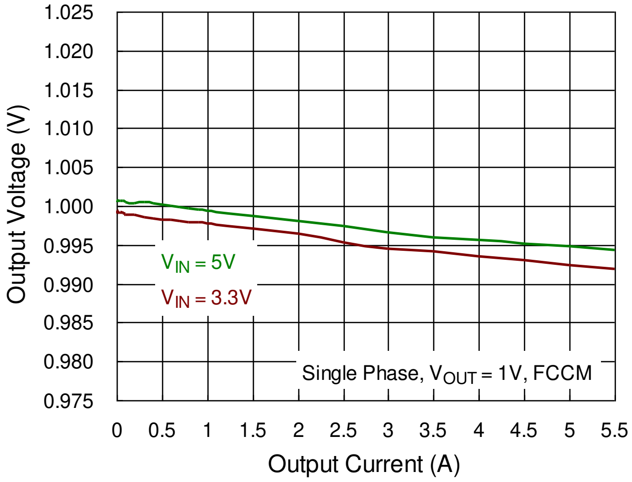
Efficiency vs. Output Current



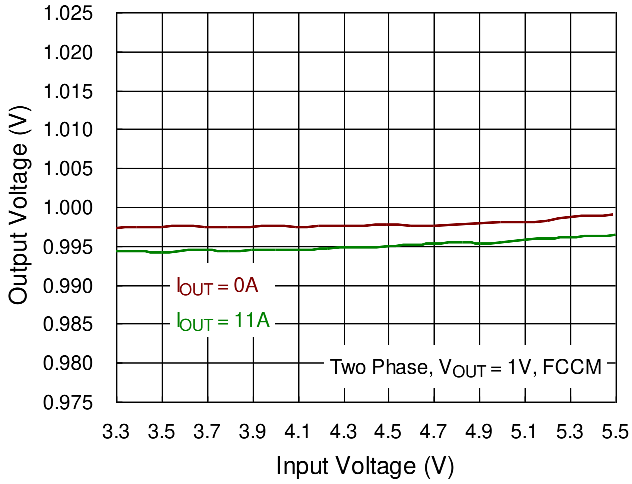
Output Voltage vs. Output Current



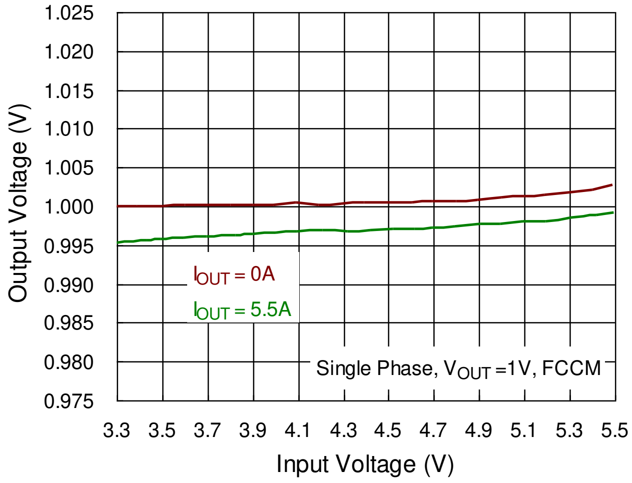
Output Voltage vs. Output Current



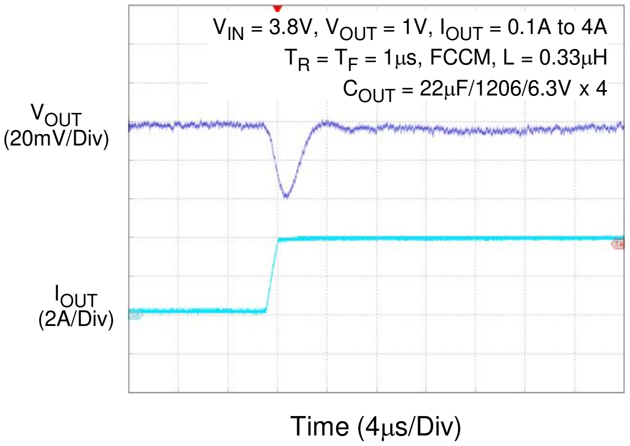
Output Voltage vs. Input Voltage



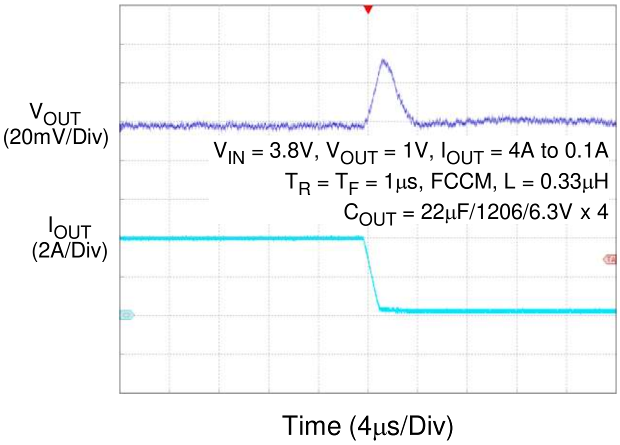
Output Voltage vs. Input Voltage



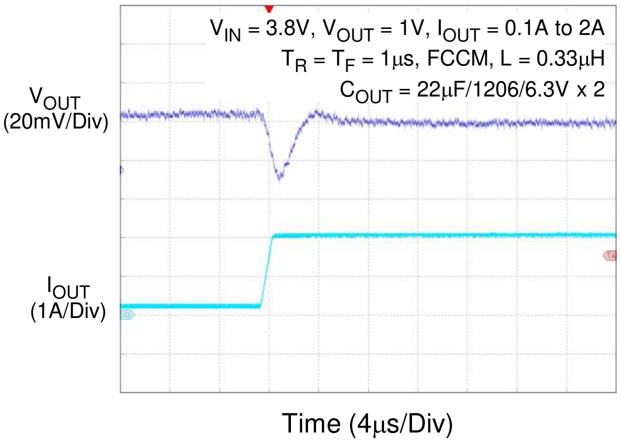
Load Transient Response-Two Phase



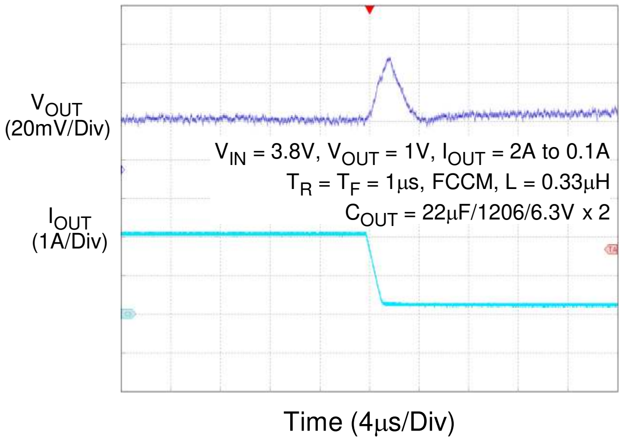
Load Transient Response-Two Phase



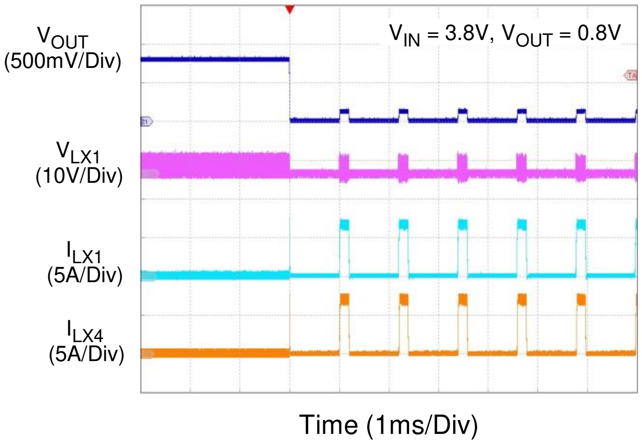
Load Transient Response-Single Phase



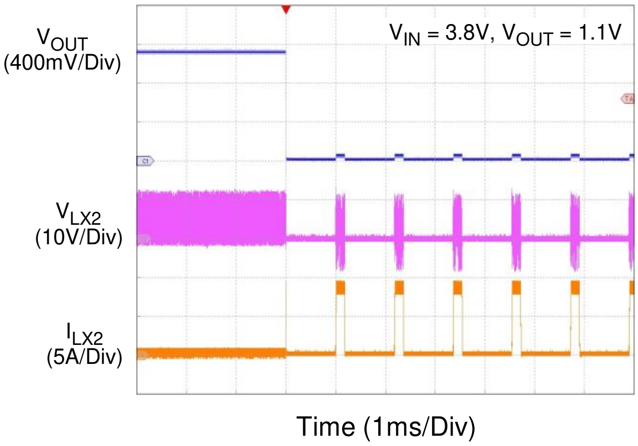
Load Transient Response-Single Phase



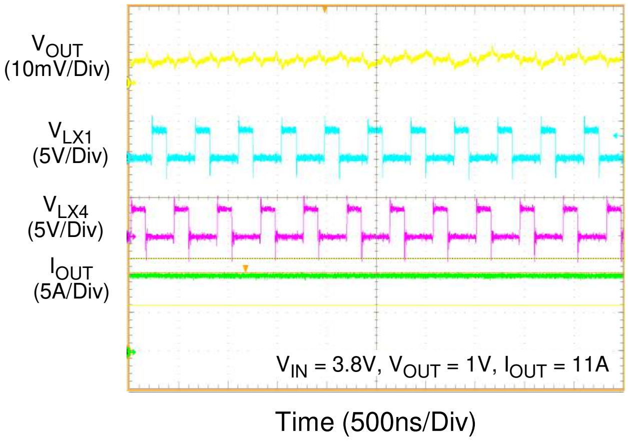
OCP Hiccup - Two Phase



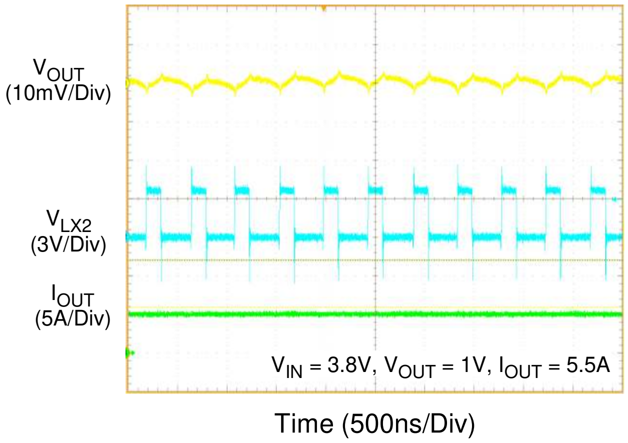
OCP Hiccup - Single Phase



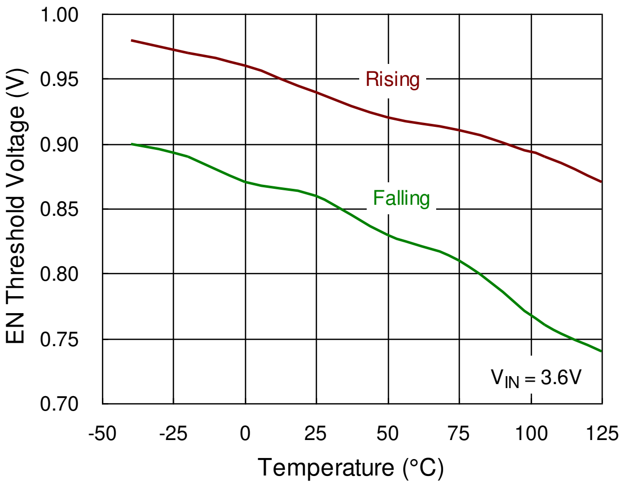
Output Ripple - Two Phase



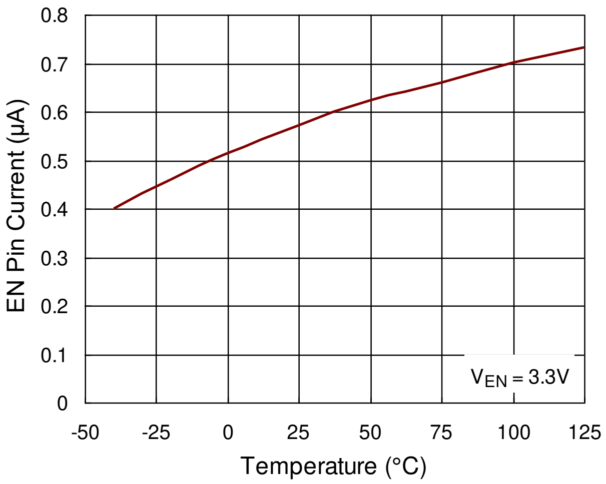
Output Ripple - Single Phase



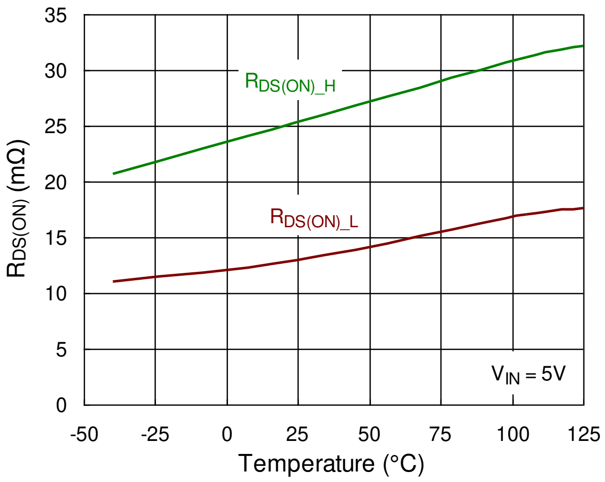
EN Threshold Voltage vs. Temperature



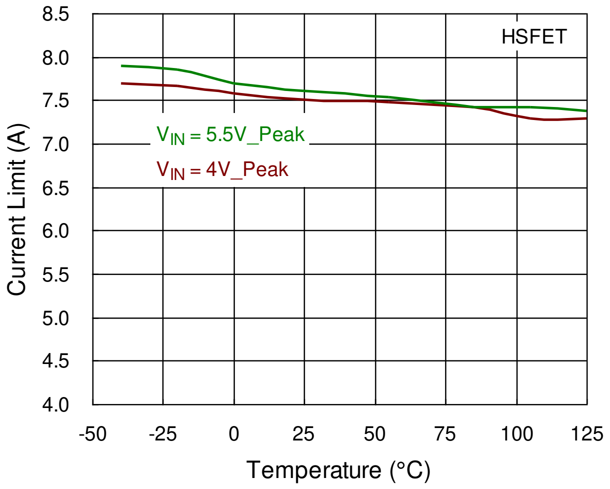
EN Pin Current vs. Temperature

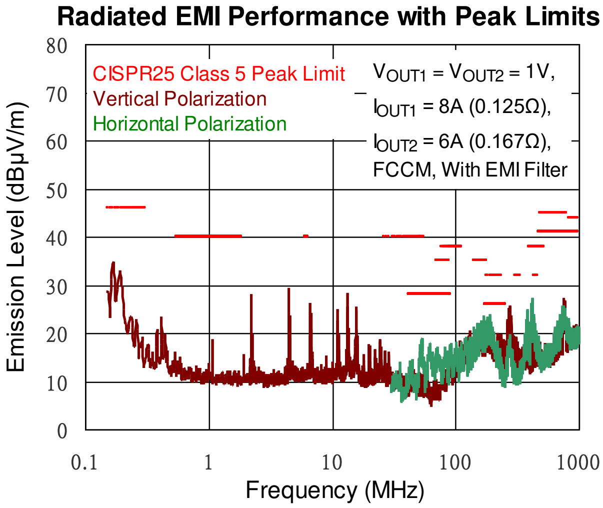


MOSFET $R_{DS(ON)}$ vs. Temperature



Current Limit vs. Temperature




Radiated EMI Performance with Peak Limits
CISPR25 Class 5 Peak Limit
Vertical Polarization
Horizontal Polarization
$V_{OUT1} = V_{OUT2} = 1V$,
$I_{OUT1} = 8A\ (0.125\Omega)$,
$I_{OUT2} = 6A\ (0.167\Omega)$,
FCCM, With EMI Filter
Emission Level (dBµV/m)
80
70
60
50
40
30
20
10
0
0.1
1
10
100
1000
Frequency (MHz)

Application Information

The RTQ2134 is a power management IC that integrates four high efficiency Buck converters, and is capable of multiphase or single-phase operation. The RTQ2134 supports 2 + 1 + 1 and 2 + 2 configuration.

Inductor Selection

The inductor selection are trade-offs among size, cost, efficiency, and transient response requirements. Generally, three key inductor parameters are specified for operation with the device: inductance value (L), inductor saturation current (I_{SAT}), and DC resistance (DCR).

A good compromise between size and loss is a 30% peak-to-peak ripple current to the IC rated current, but it still depends on size consideration. The inductor used in the Typical Application Circuit of this datasheet is recommended. The switching frequency, input voltage, output voltage, and selected inductor ripple current determine the inductor value as follows :

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times \Delta I_L}$$

To enhance the efficiency, choose a low-loss inductor having the lowest possible DCR that fits in the allotted dimensions. The selected inductor should have a saturation current rating greater than the peak current limit of the device. The core must be large enough not to saturate at the peak inductor current (I_{L_PEAK}) :

$$\Delta I_L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times L}$$

$$I_{L\_PEAK} = I_{OUT\_MAX} + \frac{1}{2}\Delta I_L$$

The current flowing through the inductor is the inductor ripple current plus the output current. During power-up, faults, or transient load conditions, the inductor current can increase the peak inductor current level calculated above. In transient conditions, the inductor current can increase up to the switch current limit of the device. For this reason, the most conservative approach is to specify an inductor with a saturation current rating equal to or greater than the switch current limit rather than the peak inductor current.

Input Capacitor Selection

Input capacitance, C_{IN}, is needed to filter the pulsating current at the drain of the HSFET. The C_{IN} should be sized to do this without causing a large variation in input voltage. Several capacitors may also be paralleled to meet size, height and thermal requirements in the design. For low input voltage applications, sufficient bulk input capacitance is needed to minimize transient effects during output load changes.

The input capacitor should be placed as close as possible to each VIN pin with a low inductance connection to the PGND of the IC. It is recommended to connect capacitors between the VIN pin and the PGND pin as shown in the Typical Application Circuit. The larger input capacitance is required when a lower switching frequency is used. The X7R capacitors are recommended for best performance across temperature and input voltage variations.

Output Capacitor Selection

The selection of C_{OUT} is determined by considering to satisfy the voltage ripple and the transient loads. The peak-to-peak output ripple, ΔV_{OUT}, is determined by :

$$\Delta V_{OUT} = \Delta I_L \left(ESR + \frac{1}{8 \times C_{OUT} \times F_{SW}} \right)$$

where the ΔI_L is the peak-to-peak inductor ripple current. The highest output ripple is at maximum input voltage since ΔI_L increases with input voltage. Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirements.

Ceramic capacitors have very low equivalent series resistance (ESR) and provide the best ripple performance. The X7R dielectric capacitor is recommended for the best performance across temperature and input voltage variations. The variation of the capacitance value with temperature, DC bias voltage and switching frequency needs to be taken into consideration. For example, the capacitance value of a capacitor decreases as the DC bias across the capacitor increases. Be careful to consider the voltage coefficient of ceramic capacitors when choosing the value and case size. Most ceramic capacitors lose 50% or more of their rated values when used near their rated voltage.

Transient performance can be improved with a higher value output capacitor. Increasing the output capacitance will also decrease the output voltage ripple.

The recommended output capacitors are shown in Typical Application Circuit section.

Thermal Considerations

In many applications, the RTQ2134 does not generate much heat due to its high efficiency and low thermal resistance of its WQFN- 30L 4.5x5 package. However, in applications where the RTQ2134 runs at a high ambient temperature and high input voltage or high switching frequency, the generated heat may exceed the maximum junction temperature of the part.

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. If the junction temperature reaches approximately 160°C, the RTQ2134 stops switching the power MOSFETs until the temperature cools down by 30°C.

The maximum power dissipation can be calculated by the following formula :

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA(EFFECTIVE)}$$

where

$T_{J(MAX)}$ is the maximum allowed junction temperature of the die. For recommended operating condition specifications, the maximum junction temperature is 125°C. T_A is the ambient operating temperature, $\theta_{JA(EFFECTIVE)}$ is the system-level junction to ambient thermal resistance. It can be estimated from thermal modeling or measurements in the system.

The thermal resistance of the device strongly depends on the surrounding PCB layout and can be improved by providing a heat sink of surrounding copper ground. The addition of backside copper with thermal vias, stiffeners, and other enhancements can also help reduce thermal resistance.

Experiments in the Richtek thermal lab show that simply set $\theta_{JA(EFFECTIVE)}$ as 110% to 120% of the θ_{JA} is reasonable to obtain the allowed $P_{D(MAX)}$.

The power loss of system can be found in the efficiency measurement and the formula below can be used to determine the power loss of IC by removing the loss of inductor including DC loss and AC loss.

Two-phase converter power loss :

$$P_{loss} = (V_{IN} \times I_{IN} - V_{OUT} \times I_{OUT}) - ((\frac{I_{OUT}}{2})^2 \times DCR) \times 2$$
$$- P_{core\_loss} \times 2 - (\frac{V_{OUT}^2 \times ACR}{12 \times L^2 \times f_{SW}^2} \times (1 - \frac{V_{OUT}}{V_{IN}})^2) \times 2$$

Single-phase converter power loss :

$$P_{loss} = (V_{IN} \times I_{IN} - V_{OUT} \times I_{OUT}) - I_{OUT}^2 \times DCR - P_{core\_loss}$$
$$- \frac{V_{OUT}^2 \times ACR}{12 \times L^2 \times f_{SW}^2} \times (1 - \frac{V_{OUT}}{V_{IN}})^2$$

Where

P_{core_loss} and ACR need to be obtained from inductor supplier.

Total loss of IC cannot be larger than maximum power loss. If the application requires a higher ambient temperature and/or higher switching frequency, care should be taken to reduce the temperature rise of the part by using a heat sink or air flow. Note that the over-temperature protection is intended to protect the device during momentary overload conditions. The protection is activated outside of the absolute maximum range of operation as a secondary fail-safe and therefore should not be relied upon operationally. Continuous operation above the specified absolute maximum operating junction temperature may impair device reliability or permanently damage the device.

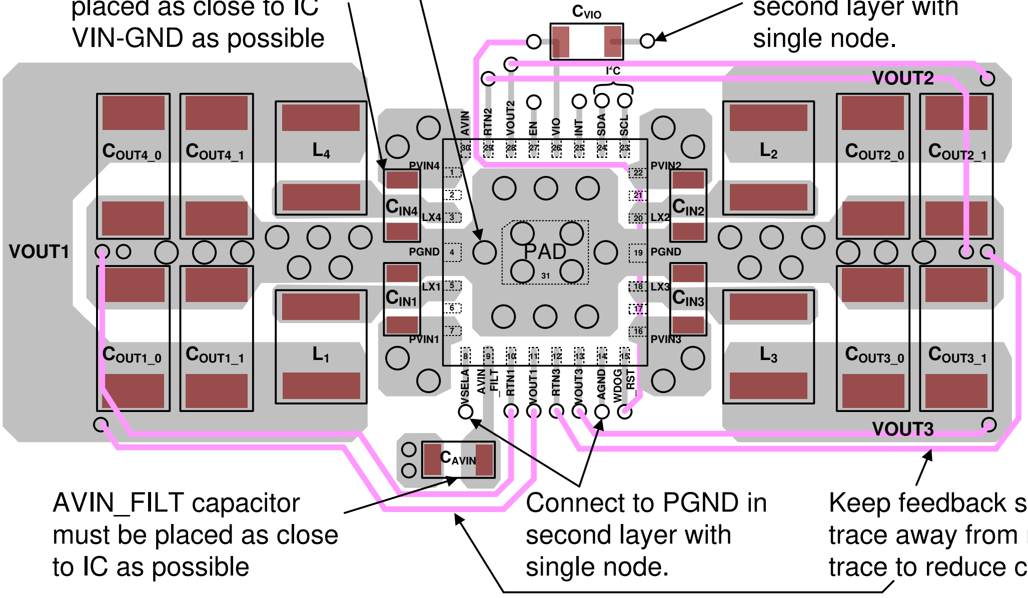
Layout Guidelines

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the RTQ2134 :

- Four-layer or six-layer PCB with maximum ground plane is strongly recommended for good thermal performance.
- Keep the traces of the main current paths wide and short.

- Place high frequency decoupling capacitor as close as possible to the IC to reduce the loop impedance and minimize switch node ringing.
- Place multiple vias under the device near PVIN and PGND and close to input capacitors to reduce parasitic inductance and improve thermal performance. To keep thermal resistance low, extend the ground plane as much as possible, and add twenty thermal vias under and near the RTQ2134 to additional ground planes within the circuit board and on the bottom side.
- The high frequency switching nodes, LX, should be as small as possible. Keep analog components away from the LX node.
- Reduce the area size of the LX exposed copper to reduce the electrically coupling from this voltage.
- Connect the feedback sense network behind via of output capacitor.
- Connect all analog grounds to common node and then connect the common node to the power ground with a single point.

Figure 9 and Figure 10 show the layout example which includes one two phase converter for Core and one single phase converter for Memory application.



Input capacitors must be placed as close to IC VIN-GND as possible

Add vias on exposed pad for thermal dissipation and current carrying capacity

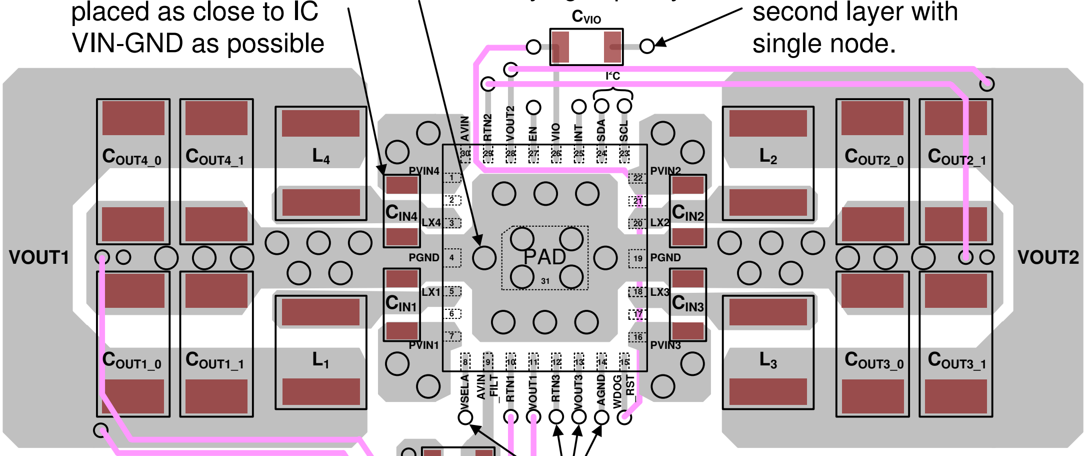
Connect to PGND in second layer with single node.

AVIN_FILT capacitor must be placed as close to IC as possible

Connect to PGND in second layer with single node.

Keep feedback sense trace away from noise trace to reduce coupling.

Figure 9. Layout Guideline for 2 + 1 + 1 Application



Input capacitors must be placed as close to IC VIN-GND as possible

Add vias on exposed pad for thermal dissipation and current carrying capacity

Connect to PGND in second layer with single node.

AVIN_FILT capacitor must be placed as close to IC as possible

Connect to PGND in second layer with single node.

Keep feedback sense trace away from noise trace to reduce coupling.

Figure 10. Layout Guideline for 2 + 2 Application

I^{2}C Interface

The RTQ2134 I^{2}C slave address = 7'b0011000 (Changed by Factory Setting). The RTQ2134 supports fast mode (bit rate up to 400kb/s). The write or read bit stream (N ≥ 1) is shown in Figure 11.

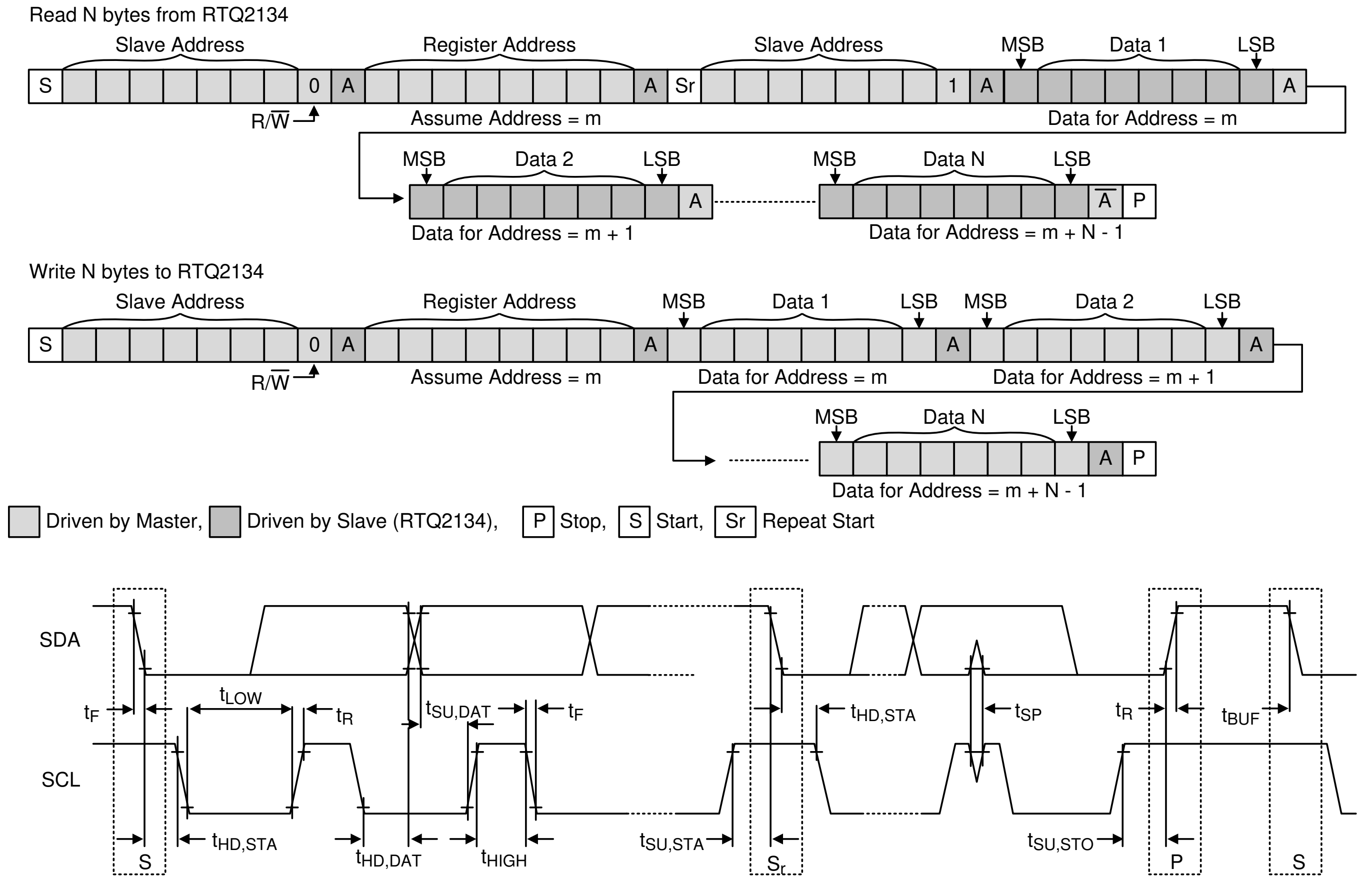


Figure 11. I^{2}C Read and Write Stream and Timing Diagram

The RTQ2134 also supports High-speed mode (bit rate up to 3.4Mb/s) with access code 08H. Figure 12 and Figure 13 show detailed transfer format. Hs-mode can only start after the following conditions (all of which are in F/S-mode) :

- ▶ START condition (S)
- ▶ 8-bit master code (00001xxx)
- ▶ not-acknowledge bit (Ā)

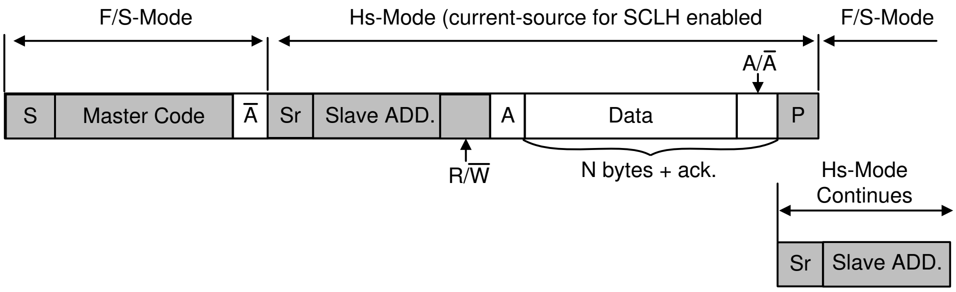


Figure 12. Data Transfer Format in Hs-mode

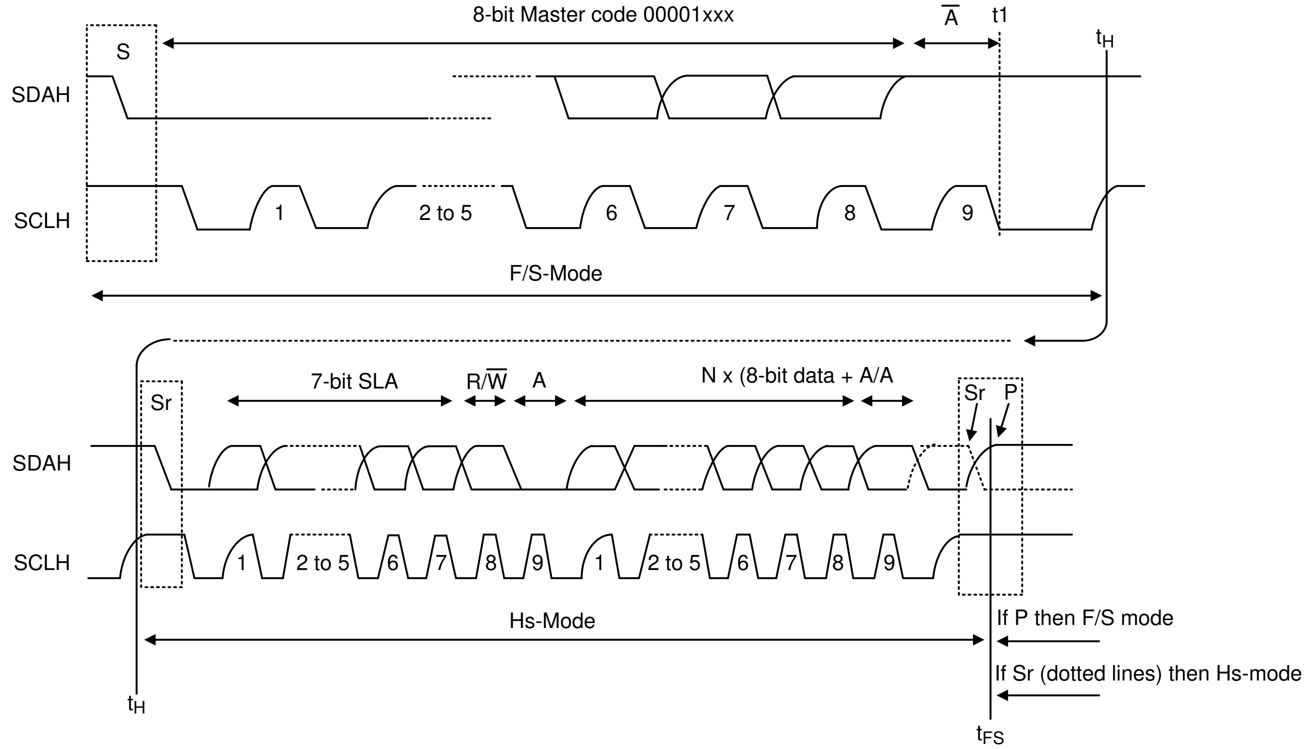


Figure 13. A Complete Hs-mode Transfer

Table 3. I^{2}C Register Summary

Register Address	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default
0x01	IO_CHIPNAME	IO_CHIPNAME								0x01
0x02	IO_CHIPVERSION	IO_CHIPVERSION								0x01
0x0A	IO_DIEID3	IO_DIEID3								0xFE
0x0B	IO_DIEID2	IO_DIEID2								0xDC
0x0C	IO_DIEID1	IO_DIEID1								0xBA
0x0D	IO_DIEID0	IO_DIEID0								0x98
0x0F	IO_SOFTRESET	Reserved							IO_SOFTRESET	0x00
0x13	FLT_RECORDTEMP	FLT_BOOT	Reserved				FLT_HOTDIE	FLT_TEMPSDR	Reserved	0x00
0x14	FLT_RECORDBUCK1	BUCK1_PG	Reserved	FLT_BUCK1_OV	FLT_BUCK1_UV	Reserved				0x00
0x15	FLT_RECORDBUCK2	BUCK2_PG	Reserved	FLT_BUCK2_OV	FLT_BUCK2_UV	Reserved				0x00
0x16	FLT_RECORDBUCK3	BUCK3_PG	Reserved	FLT_BUCK3_OV	FLT_BUCK3_UV	Reserved				0x00
0x22	IO_I2CCFG	Reserved	IO_I2CADDR							0x18
0x25	IO_RSTDVS	Reserved	IO_RSTDVS_CTRL			Reserved	IO_DBNTIME			0x00
0x30	FLT_OT_CTRL	Reserved				FLT_CTRLOT1	Reserved			0x00
0x32	FLT_MASKTEMP	FLT_MASKBOOT	Reserved				FLT_MASKHD	FLT_MASKTSDR	Reserved	0x00
0x33	FLT_MASKBUCK1	FLT_BUCK1MASKPG	BUCK1INTACT	FLT_BUCK1MASKOV	FLT_BUCK1MASKUV	Reserved				0x00
0x34	FLT_MASKBUCK2	FLT_BUCK2MASKPG	BUCK2INTACT	FLT_BUCK2MASKOV	FLT_BUCK2MASKUV	Reserved				0x00
0x35	FLT_MASKBUCK3	FLT_BUCK3MASKPG	BUCK3INTACT	FLT_BUCK3MASKOV	FLT_BUCK3MASKUV	Reserved				0x00
0x37	FLT_BUCK1_CTRL	Reserved				FLT_BUCK1_CTRLUV	Reserved			0x0C

<table>
<tr><th>Register Address</th><th>Register Name</th><th>Bit 7</th><th>Bit 6</th><th>Bit 5</th><th>Bit 4</th><th>Bit 3</th><th>Bit 2</th><th>Bit 1</th><th>Bit 0</th><th>Default</th></tr>
<tr><td>0x38</td><td>FLT_BUCK2_CTRL</td><td colspan="4">Reserved</td><td>FLT_BUCK2_CTRLUV</td><td colspan="3">Reserved</td><td>0x0C</td></tr>
<tr><td>0x39</td><td>FLT_BUCK3_CTRL</td><td colspan="4">Reserved</td><td>FLT_BUCK3_CTRLUV</td><td colspan="3">Reserved</td><td>0x0C</td></tr>
<tr><td>0x3E</td><td>BUCK1_RAMP</td><td>Reserved</td><td>BUCK1_DVS_UP</td><td colspan="3">Reserved</td><td>BUCK1_DVS_DOWN</td><td colspan="2">Reserved</td><td>0x44</td></tr>
<tr><td>0x42</td><td>BUCK1_CFG0</td><td colspan="7">Reserved</td><td>BUCK1_DIS</td><td>0x01</td></tr>
<tr><td>0x48</td><td>BUCK1_DVS0CFG1</td><td colspan="8">BUCK1_DVS0</td><td>0x8C</td></tr>
<tr><td>0x49</td><td>BUCK1_DVS0CFG0</td><td colspan="2">Reserved</td><td>BUCK1_DVS0MODE</td><td colspan="4">Reserved</td><td>BUCK1_ENDVS0</td><td>0x00</td></tr>
<tr><td>0x4A</td><td>BUCK1_DVS1CFG1</td><td colspan="8">BUCK1_DVS1</td><td>0x8C</td></tr>
<tr><td>0x4B</td><td>BUCK1_DVS1CFG0</td><td colspan="2">Reserved</td><td>BUCK1_DVS1MODE</td><td colspan="4">Reserved</td><td>BUCK1_ENDVS1</td><td>0x00</td></tr>
<tr><td>0x52</td><td>BUCK1_DVSCFG</td><td colspan="5">Reserved</td><td>BUCK1_DVSPIN_POL</td><td colspan="2">BUCK1_DVS_CTRL</td><td>0x00</td></tr>
<tr><td>0x54</td><td>BUCK1_RSPCFG</td><td>Reserved</td><td colspan="3">BUCK1_RSPUP</td><td>Reserved</td><td colspan="3">BUCK1_RSPDN</td><td>0x14</td></tr>
<tr><td>0x55</td><td>BUCK1_SLEWCTRL</td><td colspan="2">Reserved</td><td colspan="2">BUCK1_SS_SLEW</td><td colspan="4">Reserved</td><td>0x00</td></tr>
<tr><td>0x5B</td><td>BUCK2_RAMP</td><td>Reserved</td><td>BUCK2_DVS_UP</td><td colspan="3">Reserved</td><td>BUCK2_DVS_DOWN</td><td colspan="2">Reserved</td><td>0x44</td></tr>
<tr><td>0x5F</td><td>BUCK2_CFG0</td><td colspan="7">Reserved</td><td>BUCK2_DIS</td><td>0x01</td></tr>
<tr><td>0x62</td><td>BUCK2_DVS0CFG1</td><td colspan="8">BUCK2_DVS0</td><td>0x8C</td></tr>
<tr><td>0x63</td><td>BUCK2_DVS0CFG0</td><td colspan="2">Reserved</td><td>BUCK2_DVS0MODE</td><td colspan="4">Reserved</td><td>BUCK2_ENDVS0</td><td>0x00</td></tr>
<tr><td>0x64</td><td>BUCK2_DVS1CFG1</td><td colspan="8">BUCK2_DVS1</td><td>0x8C</td></tr>
<tr><td>0x65</td><td>BUCK2_DVS1CFG0</td><td colspan="2">Reserved</td><td>BUCK2_DVS1MODE</td><td colspan="4">Reserved</td><td>BUCK2_ENDVS1</td><td>0x00</td></tr>
<tr><td>0x6C</td><td>BUCK2_DVSCFG</td><td colspan="5">Reserved</td><td>BUCK2_DVSPIN_POL</td><td colspan="2">BUCK2_DVS_CTRL</td><td>0x00</td></tr>
<tr><td>0x6E</td><td>BUCK2_RSPCFG</td><td>Reserved</td><td colspan="3">BUCK2_RSPUP</td><td>Reserved</td><td colspan="3">BUCK2_RSPDN</td><td>0x14</td></tr>
</table>

Register Address	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default
0x6F	BUCK2_SLEWCTRL	Reserved		BUCK2_SS_SLEW		Reserved				0x00
0x75	BUCK3_RAMP	Reserved	BUCK3_DVS_UP	Reserved			BUCK3_DVS_DOWN	Reserved		0x44
0x79	BUCK3_CFG0	Reserved							BUCK3_DIS	0x01
0x7C	BUCK3_DVS0CFG1	BUCK3_DVS0								0x8C
0x7D	BUCK3_DVS0CFG0	Reserved		BUCK3_DVS0MODE	Reserved				BUCK3_ENDVS0	0x00
0x7E	BUCK3_DVS1CFG1	BUCK3_DVS1								0x8C
0x7F	BUCK3_DVS1CFG0	Reserved		BUCK3_DVS1MODE	Reserved				BUCK3_ENDVS1	0x00
0x86	BUCK3_DVSCFG	Reserved					BUCK3_DVSPIN_POL	BUCK3_DVS_CTRL		0x00
0x88	BUCK3_RSPCFG	Reserved	BUCK3_RSPUP			Reserved	BUCK3_RSPDN			0x14
0x89	BUCK3_SLEWCTR	Reserved		BUCK3_SS_SLEW		Reserved				0x00

Table 4. I^2C Register Map

Register Address	0x01		**Register Name**	IO_CHIPNAME				
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0	0	0	0	0	0	0	1
Read/Write	R	R	R	R	R	R	R	R
Bits	**Name**		**Description**					
Bit 7 to Bit 0	IO_CHIPNAME		IO_CHIPNAME					

Register Address	0x02		**Register Name**	IO_CHIPVERSION				
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0	0	0	0	0	0	0	1
Read/Write	R	R	R	R	R	R	R	R
Bits	**Name**		**Description**					
Bit 7 to Bit 0	IO_CHIPVERSION		IO_CHIPVERSION					

Register Address	0x0A		**Register Name**	IO_DIEID3				
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	1	1	1	1	1	1	1	0
Read/Write	R	R	R	R	R	R	R	R
Bits	**Name**		**Description**					
Bit 7 to Bit 0	IO_DIEID3		IO_DIEID3					

Register Address	0x0B		**Register Name**	IO_DIEID2				
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	1	1	0	1	1	1	0	0
Read/Write	R	R	R	R	R	R	R	R
Bits	**Name**		**Description**					
Bit 7 to Bit 0	IO_DIEID2		IO_DIEID2					

Register Address	0x0C		**Register Name**	IO_DIEID1				
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	1	0	1	1	1	0	1	0
Read/Write	R	R	R	R	R	R	R	R
Bits	**Name**		**Description**					
Bit 7 to Bit 0	IO_DIEID1		IO_DIEID1					

Register Address	0x0D		**Register Name**	IO_DIEID0				
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	1	0	0	1	1	0	0	0
Read/Write	R	R	R	R	R	R	R	R
Bits	**Name**		**Description**					
Bit 7 to Bit 0	IO_DIEID0		IO_DIEID0					

Register Address	0x0F		**Register Name**	IO_SOFTRESET				
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0	0	0	0	0	0	0	0
Read/Write	R	R	R	R	R	R	R	RW
Bits	**Name**		**Description**					
Bit 7 to Bit 1	Reserved		Reserved bits					
Bit 0	IO_SOFTRESET		Reset all digital functions to default setting. 0 : Not changed 1 : Reset and bit cleared					

Register Address	0x13		**Register Name**	FLT_RECORDTEMP				
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0	0	0	0	0	0	0	0
Read/Write	RC	R	R	R	R	RC	RC	R

Bits	**Name**	**Description**
Bit 7	FLT_BOOT	Boot interrupt indicator. Read only and automatically cleared. 0 : Boot process doesn't occur. AVIN is less than UVLO rising threshold. 1 : Boot process has occurred. AVIN is greater than UVLO rising threshold or less than UVLO falling threshold.
Bit 6 to Bit 3 Bit 0	Reserved	Reserved bits
Bit 2	FLT_HOTDIE	Hot die interrupt indicator. Read only and automatically cleared. 0 : Temp of die is lower than threshold. 1 : Die hot. Greater than threshold.
Bit 1	FLT_TEMPSDR	OT interrupt indicator. Read only and automatically cleared. 0 : No Fault. Less than threshold. 1 : Fault. Greater than threshold or during fault recovery.

Register Address	0x14		**Register Name**	FLT_RECORDBUCK1				
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0	0	0	0	0	0	0	0
Read/Write	R	R	RC	RC	R	R	R	R

Bits	**Name**	**Description**
Bit 7	BUCK1_PG	Power good status indicator. 0 : VOUT > 110% of setting VOUT or VOUT < 90% of setting VOUT 1 : 110% of setting VOUT > VOUT > 90% of setting VOUT
Bit 6 Bit 3 to Bit 0	Reserved	Reserved bits
Bit 5	FLT_BUCK1_OV	OV interrupt indicator. Read only and automatically cleared. 0 : No Fault. Less than threshold. 1 : Fault. Greater than threshold.
Bit 4	FLT_BUCK1_UV	UV interrupt indicator. Read only and automatically cleared. 0 : No Fault. Greater than threshold. 1 : Fault. Less than threshold or during fault recovery.

Register Address	0x15		**Register Name**	FLT_RECORDBUCK2				
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0	0	0	0	0	0	0	0
Read/Write	R	R	RC	RC	R	R	R	R

Bits	**Name**	**Description**
Bit 7	BUCK2_PG	Power good status indicator. 0 : VOUT > 110% of setting VOUT or VOUT < 90% of setting VOUT 1 : 110% of setting VOUT > VOUT > 90% of setting VOUT
Bit 6 Bit 3 to Bit 0	Reserved	Reserved bits
Bit 5	FLT_BUCK2_OV	OV interrupt indicator. Read only and automatically cleared. 0 : No Fault. Less than threshold. 1 : Fault. Greater than threshold.
Bit 4	FLT_BUCK2_UV	UV interrupt indicator. Read only and automatically cleared. 0 : No Fault. Greater than threshold. 1 : Fault. Less than threshold or during fault recovery.

Register Address	0x16		**Register Name**	FLT_RECORDBUCK3				
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0	0	0	0	0	0	0	0
Read/Write	R	R	RC	RC	R	R	R	R

Bits	**Name**	**Description**
Bit 7	BUCK3_PG	Power good status indicator. 0 : VOUT > 110% of setting VOUT or VOUT < 90% of setting VOUT 1 : 110% of setting VOUT > VOUT > 90% of setting VOUT
Bit 6 Bit 3 to Bit 0	Reserved	Reserved bits
Bit 5	FLT_BUCK3_OV	OV interrupt indicator. Read only and automatically cleared. 0 : No Fault. Less than threshold. 1 : Fault. Greater than threshold.
Bit 4	FLT_BUCK3_UV	UV interrupt indicator. Read only and automatically cleared. 0 : No Fault. Greater than threshold. 1 : Fault. Less than threshold or during fault recovery.

Register Address	0x22		**Register Name**	IO_I2CCFG				
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0	0	0	1	1	0	0	0
Read/Write	R	R	R	R	R	R	R	R

Bits	**Name**	**Description**
Bit 7	Reserved	Reserved bits
Bit 6 to Bit 0	IO_I2CADDR	IO_I2CADDR

Register Address	0x25		**Register Name**	IO_RSTDVS				
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0	0	0	0	0	0	0	0
Read/Write	R	RW	RW	RW	R	RW	RW	RW

Bits	**Name**	**Description**
Bit 7 and Bit 3	Reserved	Reserved bits
Bit 6	IO_RSTDVS	Enable/disable Buck3 watchdog reset function to default voltage when WDOG_RST pin is pulled low. 1 : Enable 0 : Disable
Bit 5		Enable/disable Buck2 watchdog reset function to default voltage when WDOG_RST pin is pulled low. 1 : Enable 0 : Disable
Bit 4		Enable/disable Buck1 watchdog reset function to default voltage when WDOG_RST pin is pulled low. 1 : Enable 0 : Disable
Bit 2 to Bit 0	IO_DBNTIME	Watchdog Debounce Time 000 : 0ms (Default) 100 : 12.5ms 001 : 1.56ms 101 : 9ms 010 : 3.125ms 110 : 15.25ms 011 : 6.25ms 111 : 14.5ms

Register Address	0x30		**Register Name**	FLT_OT_CTRL				
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0	0	0	0	0	0	0	0
Read/Write	R	R	R	R	RW	R	R	R

Bits	**Name**	**Description**
Bit 7 to Bit 4 Bit 2 to Bit 0	Reserved	Reserved bits
Bit 3	FLT_CTRLOT1	When OT is detected, the Buck can be set to shutdown or not shutdown. 0 : Shutdown 1 : Not Shutdown

Register Address	0x32		**Register Name**	FLT_MASKTEMP				
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0	0	0	0	0	0	0	0
Read/Write	RW	R	R	R	R	RW	RW	R

Bits	**Name**	**Description**
Bit 7	FLT_MASKBOOT	Masking the BOOT detection signal. 0 : Pass internal logic output to INT pin. 1 : Mask internal logic output to INT pin.
Bit 6 to Bit 3 Bit 0	Reserved	Reserved bits
Bit 2	FLT_MASKHD	Masking the Hot die detection signal. 0 : Pass internal logic output to INT pin. 1 : Mask internal logic output to INT pin.
Bit 1	FLT_MASKTSDR	Masking the Thermal shutdown detection signal. 0 : Pass internal logic output to INT pin. 1 : Mask internal logic output to INT pin.

Register Address	0x33		**Register Name**	FLT_MASKBUCK1				
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0	0	0	0	0	0	0	0
Read/Write	RW	RW	RW	RW	R	R	R	R
Bits	**Name**		**Description**					
Bit 7	FLT_BUCK1MASKPG		Masking Buck1 power good detection signal. 0 : Pass internal logic output to INT pin. 1 : Mask internal logic output to INT pin.					
Bit 6	BUCK1INTACT		Write this bit to "1" to ensure Buck1 INT function normally. "0" is reserved for Richtek internal use only.					
Bit 5	FLT_BUCK1MASKOV		Masking Buck1 over-voltage detection signal. 0 : Pass internal logic output to INT pin. 1 : Mask internal logic output to INT pin.					
Bit 4	FLT_BUCK1MASKUV		Masking Buck1 under-voltage detection signal. 0 : Pass internal logic output to INT pin. 1 : Mask internal logic output to INT pin.					
Bit 3 to Bit 0	Reserved		Reserved bits					

Register Address	0x34		**Register Name**	FLT_MASKBUCK2				
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0	0	0	0	0	0	0	0
Read/Write	RW	RW	RW	RW	R	R	R	R
Bits	**Name**		**Description**					
Bit 7	FLT_BUCK2MASKPG		Masking Buck2 power good detection signal. 0 : Pass internal logic output to INT pin. 1 : Mask internal logic output to INT pin.					
Bit 6	BUCK2INTACT		Write this bit to "1" to ensure Buck2 INT function normally. "0" is reserved for Richtek internal use only.					
Bit 5	FLT_BUCK2MASKOV		Masking Buck2 over-voltage detection signal. 0 : Pass internal logic output to INT pin. 1 : Mask internal logic output to INT pin.					
Bit 4	FLT_BUCK2MASKUV		Masking Buck2 under-voltage detection signal. 0 : Pass internal logic output to INT pin. 1 : Mask internal logic output to INT pin.					
Bit 3 to Bit 0	Reserved		Reserved bits					

Register Address	0x35		**Register Name**	FLT_MASKBUCK3				
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0	0	0	0	0	0	0	0
Read/Write	RW	RW	RW	RW	R	R	R	R

Bits	**Name**	**Description**
Bit 7	FLT_BUCK3MASKPG	Masking Buck3 power good detection signal. 0 : Pass internal logic output to INT pin. 1 : Mask internal logic output to INT pin.
Bit 6	BUCK3INTACT	Write this bit to "1" to ensure Buck3 INT function normally. "0" is reserved for Richtek internal use only.
Bit 5	FLT_BUCK3MASKOV	Masking Buck3 over-voltage detection signal. 0 : Pass internal logic output to INT pin. 1 : Mask internal logic output to INT pin.
Bit 4	FLT_BUCK3MASKUV	Masking Buck3 under-voltage detection signal. 0 : Pass internal logic output to INT pin. 1 : Mask internal logic output to INT pin.
Bit 3 to Bit 0	Reserved	Reserved bits

Register Address	0x37		**Register Name**	FLT_BUCK1_CTRL				
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0	0	0	0	1	1	0	0
Read/Write	R	R	R	R	RW	R	R	R

Bits	**Name**	**Description**
Bit 7 to Bit 4 Bit 2 to Bit 0	Reserved	Reserved bits
Bit 3	FLT_BUCK1_CTRLUV	Latch or hiccup protection behavior when Buck1 suffers UV detection. 0 : UV Shutdown 1 : UV Hiccup

Register Address	0x38		**Register Name**	FLT_BUCK2_CTRL				
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0	0	0	0	1	1	0	0
Read/Write	R	R	R	R	RW	R	R	R

Bits	**Name**	**Description**
Bit 7 to Bit 4 Bit 2 to Bit 0	Reserved	Reserved bits
Bit 3	FLT_BUCK2_CTRLUV	Latch or hiccup protection behavior when Buck2 suffers UV detection. 0 : UV Shutdown 1 : UV Hiccup

Register Address	0x39		**Register Name**	FLT_BUCK3_CTRL				
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0	0	0	0	1	1	0	0
Read/Write	R	R	R	R	RW	R	R	R
Bits	**Name**		**Description**					
Bit 7 to Bit 4 Bit 2 to Bit 0	Reserved		Reserved bits					
Bit 3	FLT_BUCK3_ CTRLUV		Latch or hiccup protection behavior when Buck3 suffers UV detection. 0 : UV Shutdown 1 : UV Hiccup					

Register Address	0x3E		**Register Name**	BUCK1_RAMP				
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0	1	0	0	0	1	0	0
Read/Write	R	RW	R	R	R	RW	R	R
Bits	**Name**		**Description**					
Bit 7 Bit 5 to Bit 3 Bit 1 to Bit 0	Reserved		Reserved bits					
Bit 6	BUCK1_DVS_UP		The operation mode when Buck1 ramps up. 0 : Auto Mode 1 : FCCM					
Bit 2	BUCK1_DVS_DOWN		The operation mode when Buck1 ramps down. 0 : Decay Mode 1 : FCCM					

Register Address	0x42		**Register Name**	BUCK1_CFG0				
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0	0	0	0	0	0	0	1
Read/Write	R	R	R	R	R	R	R	RW
Bits	**Name**		**Description**					
Bit 7 to Bit 1	Reserved		Reserved bits					
Bit 0	BUCK1_DIS		The output discharge resistor operates when Buck1 is turned off by software or external enable pin. 0 : Disable output discharge resistor. 1 : Enable output discharge resistor.					

Register Address	0x48		**Register Name**	BUCK1_DVS0CFG1				
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	1	0	0	0	1	1	0	0
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW
Bits	**Name**		**Description**					
Bit 7 to Bit 0	BUCK1_DVS0		Buck1 DVS0 output voltage setting SEL[7:0] = 11111111 : V_{OUT} = 1.85V … SEL[7:0] = 11001000 : V_{OUT} = 1.3V … SEL[7:0] = 0000000 : 0.3V For 0.3V to 1.3V, V_{OUT} = 0.3V + SEL[7:0](decimal) x 5mV For 1.3V to 1.85V, V_{OUT} = 1.3V + {SEL[7:0](decimal) - 200} x 10mV					

Register Address	0x49		**Register Name**	BUCK1_DVS0CFG0				
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0	0	0	0	0	0	0	0
Read/Write	R	R	RW	R	R	R	R	RW
Bits	**Name**		**Description**					
Bit 7 to Bit 6 Bit 4 to Bit 1	Reserved		Reserved bits					
Bit 5	BUCK1_DVS0MODE		Buck1 DVS0 operation mode setting 0 : Auto Mode 1 : FCCM Note : Please enable all the set outputs before setting into the FCCM.					
Bit 0	BUCK1_ENDVS0		Enable or disable Buck1 DVS0 0 : Disable 1 : Enable					

Register Address	0x4A		**Register Name**	BUCK1_DVS1CFG1				
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	1	0	0	0	1	1	0	0
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW
Bits	**Name**		**Description**					
Bit 7 to Bit 0	BUCK1_DVS1		Buck1 DVS1 output voltage setting SEL[7:0] = 11111111 : V_{OUT} = 1.85V … SEL[7:0] = 11001000 : V_{OUT} = 1.3V … SEL[7:0] = 0000000 : 0.3V For 0.3V to 1.3V, V_{OUT} = 0.3V + SEL[7:0](decimal) x 5mV For 1.3V to 1.85V, V_{OUT} = 1.3V + {SEL[7:0](decimal) - 200} x 10mV					

Register Address	0x4B		**Register Name**	BUCK1_DVS1CFG0				
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0	0	0	0	0	0	0	0
Read/Write	R	R	RW	R	R	R	R	RW
Bits	**Name**		**Description**					
Bit 7 to Bit 6 Bit 4 to Bit 1	Reserved		Reserved bits					
Bit 5	BUCK1_DVS1MODE		Buck1 DVS1 operation mode setting 0 : Auto Mode 1 : FCCM Note : Please enable all the set outputs before setting into the FCCM.					
Bit 0	BUCK1_ENDVS1		Enable or disable Buck1 DVS1 0 : Disable 1 : Enable					

Register Address	0x52		**Register Name**	BUCK1_DVSCFG				
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0	0	0	0	0	0	0	0
Read/Write	R	R	R	R	R	RW	RW	RW
Bits	**Name**		**Description**					
Bit 7 to Bit 3	Reserved		Reserved bits					
Bit 2	BUCK1_DVSPIN_POL		When Buck1 DVS up and down operations are controlled by using external VSELA pin, this bit can define the polarity for VSELA. 0 : VSELA = 1 → use DVS0 setting VSELA = 0 → use DVS1 setting 1 : VSELA = 1 → use DVS1 setting VSELA = 0 → use DVS0 setting					
Bit 1 to Bit 0	BUCK1_DVS_CTRL		Buck1 DVS up and down operations are controlled by software or external pin. 00 : Use DVS0 setting 01 : Use DVS1 setting 10 : Controlled by VSELA pin					

Register Address	0x54		**Register Name**	BUCK1_RSPCFG				
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0	0	0	1	0	1	0	0
Read/Write	R	RW	RW	RW	R	RW	RW	RW
Bits	**Name**		**Description**					
Bit 7, Bit 3	Reserved		Reserved bits					
Bit 6 to Bit 4	BUCK1_RSPUP		Buck1 DVS slew rate setting for DVS UP 001 = 16mV/μs 101 = 2mV/μs 011 = 8mV/μs 110 = 1mV/μs 100 = 4mV/μs 111 = 0.5mV/μs					
Bit 2 to Bit 0	BUCK1_RSPDN		Buck1 DVS slew rate setting for DVS Down 001 = 16mV/μs 101 = 2mV/μs 011 = 8mV/μs 110 = 1mV/μs 100 = 4mV/μs 111 = 0.5mV/μs					

Register Address	0x55		**Register Name**	BUCK1_SLEWCTRL				
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0	0	0	0	0	0	0	0
Read/Write	R	R	RW	RW	R	R	R	R
Bits	**Name**		**Description**					
Bit 7 to Bit 6 Bit 3 to Bit 0	Reserved		Reserved bits					
Bit 5 to Bit 4	BUCK1_SS_SLEW		Set the soft-start slew rate when Buck1 is turned on by software or external enable pin. 00 = 10mV/μs 10 = 2.5mV/μs 01 = 5mV/μs 11 = 1.25mV/μs					

Register Address	0x5B		**Register Name**	BUCK2_RAMP				
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0	1	0	0	0	1	0	0
Read/Write	R	RW	R	R	R	RW	R	R
Bits	**Name**		**Description**					
Bit 7 Bit 5 to Bit 3 Bit 1 to Bit 0	Reserved		Reserved bits					
Bit 6	BUCK2_DVS_UP		The operation mode when Buck2 ramps up. 0 : Auto Mode 1 : FCCM					
Bit 2	BUCK2_DVS_DOWN		The operation mode when Buck2 ramps down. 0 : Decay Mode 1 : FCCM					

Register Address	0x5F		**Register Name**	BUCK2_CFG0				
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0	0	0	0	0	0	0	1
Read/Write	R	R	R	R	R	R	R	RW
Bits	**Name**		**Description**					
Bit 7 to Bit 1	Reserved		Reserved bits					
Bit 0	BUCK2_DIS		The output discharge resistor operation when Buck2 is turned off by software or external enable pin. 0 : Disable output discharge resistor. 1 : Enable output discharge resistor.					

Register Address	0x62		**Register Name**	BUCK2_DVS0CFG1				
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	1	0	0	0	1	1	0	0
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW
Bits	**Name**		**Description**					
Bit 7 to Bit 0	BUCK2_DVS0		Buck2 DVS0 output voltage setting SEL[7:0] = 11111111 : V_{OUT} = 1.85V … SEL[7:0] = 11001000 : V_{OUT} = 1.3V … SEL[7:0] = 0000000 : 0.3V For 0.3V to 1.3V, V_{OUT} = 0.3V + SEL[7:0](decimal) x 5mV For 1.3V to 1.85V, V_{OUT} = 1.3V + {SEL[7:0](decimal) - 200} x 10mV					

Register Address	0x63		**Register Name**	BUCK2_DVS0CFG0				
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0	0	0	0	0	0	0	0
Read/Write	R	R	RW	R	R	R	R	RW
Bits	**Name**		**Description**					
Bit 7 to Bit 6 Bit 4 to Bit 1	Reserved		Reserved bits					
Bit 5	BUCK2_DVS0MODE		Buck2 DVS0 operation mode setting 0 : Auto Mode 1 : FCCM Note : Please enable all the set outputs before setting into the FCCM.					
Bit 0	BUCK2_ENDVS0		Enable or disable Buck2 DVS0 0 : Disable 1 : Enable					

Register Address	0x64		**Register Name**	BUCK2_DVS1CFG1				
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	1	0	0	0	1	1	0	0
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW
Bits	**Name**		**Description**					
Bit 7 to Bit 0	BUCK2_DVS1		Buck2 DVS1 output voltage setting SEL[7:0] = 11111111 : V_{OUT} = 1.85V … SEL[7:0] = 11001000 : V_{OUT} = 1.3V … SEL[7:0] = 0000000 : 0.3V For 0.3V to 1.3V, V_{OUT} = 0.3V + SEL[7:0](decimal) x 5mV For 1.3V to 1.85V, V_{OUT} = 1.3V + {SEL[7:0](decimal) - 200} x 10mV					

Register Address	0x65		**Register Name**	BUCK2_DVS1CFG0				
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0	0	0	0	0	0	0	0
Read/Write	R	R	RW	R	R	R	R	RW
Bits	**Name**		**Description**					
Bit 7 to Bit 6 Bit 4 to Bit 1	Reserved		Reserved bits					
Bit 5	BUCK2_DVS1MODE		Buck2 DVS1 operation mode setting 0 : Auto Mode 1 : FCCM Note : Please enable all the set outputs before setting into the FCCM.					
Bit 0	BUCK2_ENDVS1		Enable or disable Buck2 DVS1 0 : Disable 1 : Enable					

Register Address	0x6C		**Register Name**	BUCK2_DVSCFG			
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0	0	0	0	0	0	0	0
Read/Write	R	R	R	R	R	RW	RW	RW

Bits	**Name**	**Description**
Bit 7 to Bit 3	Reserved	Reserved bits
Bit 2	BUCK2_DVSPIN_POL	When Buck2 DVS up and down operations are controlled by using external VSELA pin, this bit can define the polarity for VSELA. 0 : VSELA = 1 → use DVS0 setting VSELA = 0 → use DVS1 setting 1 : VSELA = 1 → use DVS1 setting VSELA = 0 → use DVS0 setting
Bit 1 to Bit 0	BUCK2_DVS_CTRL	Buck2 DVS up and down operations are controlled by software or external pin. 00 : Use DVS0 setting 01 : Use DVS1 setting 10 : Controlled by VSELA pin

Register Address	0x6E		**Register Name**	BUCK2_RSPCFG				
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0	0	0	1	0	1	0	0
Read/Write	R	RW	RW	RW	R	RW	RW	RW

Bits	**Name**	**Description**
Bit 7, Bit 3	Reserved	Reserved bits
Bit 6 to Bit 4	BUCK2_RSPUP	Buck2 DVS slew rate setting for DVS UP 001 = 16mV/μs 101 = 2mV/μs 011 = 8mV/μs 110 = 1mV/μs 100 = 4mV/μs 111 = 0.5mV/μs
Bit 2 to Bit 0	BUCK2_RSPDN	Buck2 DVS slew rate setting for DVS Down 001 = 16mV/μs 101 = 2mV/μs 011 = 8mV/μs 110 = 1mV/μs 100 = 4mV/μs 111 = 0.5mV/μs

Register Address	0x6F		**Register Name**	BUCK2_SLEWCTRL				
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0	0	0	0	0	0	0	0
Read/Write	R	R	RW	RW	R	R	R	R
Bits	**Name**		**Description**					
Bit 7 to Bit 6 Bit 3 to Bit 0	Reserved		Reserved bits					
Bit 5 to Bit 4	BUCK2_SS_SLEW		Set the soft-start slew rate when Buck2 is turned on by software or external enable pin. 00 = 10mV/μs 10 = 2.5mV/μs 01 = 5mV/μs 11 = 1.25mV/μs					

Register Address	0x75		**Register Name**	BUCK3_RAMP				
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0	1	0	0	0	1	0	0
Read/Write	R	RW	R	R	R	RW	R	R
Bits	**Name**		**Description**					
Bit 7 Bit 5 to Bit 3 Bit 1 to Bit 0	Reserved		Reserved bits					
Bit 6	BUCK3_DVS_UP		The operation mode when Buck3 ramps up. 0 : Auto Mode 1 : FCCM					
Bit 2	BUCK3_DVS_DOWN		The operation mode when Buck3 ramps down. 0 : Decay Mode 1 : FCCM					

Register Address	0x79		**Register Name**	BUCK3_CFG0				
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0	0	0	0	0	0	0	1
Read/Write	R	R	R	R	R	R	R	RW
Bits	**Name**		**Description**					
Bit 7 to Bit 1	Reserved		Reserved bits					
Bit 0	BUCK3_DIS		The output discharge resistor operation when Buck3 is turned off by software or external enable pin. 0 : Disable output discharge resistor. 1 : Enable output discharge resistor.					

Register Address	0x7C		**Register Name**	BUCK3_DVS0CFG1			
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	1	0	0	0	1	1	0	0
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW

Bits	**Name**	**Description**
Bit 7 to Bit 0	BUCK3_DVS0	Buck3 DVS0 output voltage setting SEL[7:0] = 11111111 : V_{OUT} = 1.85V … SEL[7:0] = 11001000 : V_{OUT} = 1.3V … SEL[7:0] = 0000000 : 0.3V For 0.3V to 1.3V, V_{OUT} = 0.3V + SEL[7:0](decimal) x 5mV For 1.3V to 1.85V, V_{OUT} = 1.3V + {SEL[7:0](decimal) - 200} x 10mV

Register Address	0x7D		**Register Name**	BUCK3_DVS0CFG0				
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0	0	0	0	0	0	0	0
Read/Write	R	R	RW	R	R	R	R	RW

Bits	**Name**	**Description**
Bit 7 to Bit 6 Bit 4 to Bit 1	Reserved	Reserved bits
Bit 5	BUCK3_DVS0MODE	Buck3 DVS0 operation mode setting 0 : Auto Mode 1 : FCCM Note : Please enable all the set outputs before setting into the FCCM.
Bit 0	BUCK3_ENDVS0	Enable or disable Buck3 DVS0 0 : Disable 1 : Enable

Register Address	0x7E		**Register Name**	BUCK3_DVS1CFG1				
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	1	0	0	0	1	1	0	0
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW

Bits	**Name**	**Description**
Bit 7 to Bit 0	BUCK3_DVS1	Buck3 DVS1 output voltage setting SEL[7:0] = 11111111 : V_{OUT} = 1.85V … SEL[7:0] = 11001000 : V_{OUT} = 1.3V … SEL[7:0] = 0000000 : 0.3V For 0.3V to 1.3V, V_{OUT} = 0.3V + SEL[7:0](decimal) x 5mV For 1.3V to 1.85V, V_{OUT} = 1.3V + {SEL[7:0](decimal) - 200} x 10mV

Register Address	0x7F		**Register Name**	BUCK3_DVS1CFG0				
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0	0	0	0	0	0	0	0
Read/Write	R	R	RW	R	R	R	R	RW

Bits	**Name**	**Description**
Bit 7 to Bit 6 Bit 4 to Bit 1	Reserved	Reserved bits
Bit 5	BUCK3_DVS1MODE	Buck3 DVS1 operation mode setting 0 : Auto Mode 1 : FCCM Note : Please enable all the set outputs before setting into the FCCM.
Bit 0	BUCK3_ENDVS1	Enable or disable Buck3 DVS1 0 : Disable 1 : Enable

Register Address	0x86		**Register Name**	BUCK3_DVSCFG				
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0	0	0	0	0	0	0	0
Read/Write	R	R	R	R	R	RW	RW	RW

Bits	**Name**	**Description**
Bit 7 to Bit 3	Reserved	Reserved bits
Bit 2	BUCK3_DVSPIN_POL	When Buck3 DVS up and down operations are controlled by using external VSELA pin, this bit can define the polarity for VSELA. 0 : VSELA = 1 → use DVS0 setting VSELA = 0 → use DVS1 setting 1 : VSELA = 1 → use DVS1 setting VSELA = 0 → use DVS0 setting
Bit 1 to Bit 0	BUCK3_DVS_CTRL	Buck3 DVS up and down operations are controlled by software or external pin. 00 : Use DVS0 setting 01 : Use DVS1 setting 10 : Controlled by VSELA pin

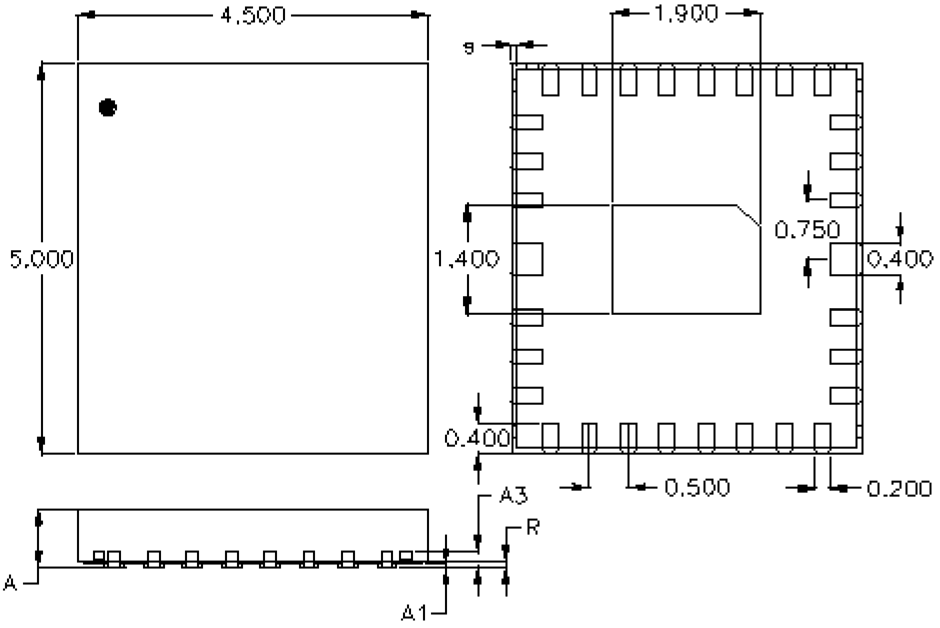
Register Address	0x88		**Register Name**	BUCK3_RSPCFG			
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0	0	0	1	0	1	0	0
Read/Write	R	RW	RW	RW	R	RW	RW	RW

Bits	**Name**	**Description**
Bit 7, Bit 3	Reserved	Reserved bits
Bit 6 to Bit 4	BUCK3_RSPUP	Buck3 DVS slew rate setting for DVS UP 001 = 16mV/μs 101 = 2mV/μs 011 = 8mV/μs 110 = 1mV/μs 100 = 4mV/μs 111 = 0.5mV/μs
Bit 2 to Bit 0	BUCK3_RSPDN	Buck3 DVS slew rate setting for DVS Down 001 = 16mV/μs 101 = 2mV/μs 011 = 8mV/μs 110 = 1mV/μs 100 = 4mV/μs 111 = 0.5mV/μs

Register Address	0x89		**Register Name**	BUCK3_SLEWCTRL				
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0	0	0	0	0	0	0	0
Read/Write	R	R	RW	RW	R	R	R	R

Bits	**Name**	**Description**
Bit 7 to Bit 6 Bit 3 to Bit 0	Reserved	Reserved bits
Bit 5 to Bit 4	BUCK3_SS_SLEW	Set the soft-start slew rate when Buck3 is turned on by software or external enable pin. 00 = 10mV/μs 10 = 2.5mV/μs 01 = 5mV/μs 11 = 1.25mV/μs

Outline Dimension

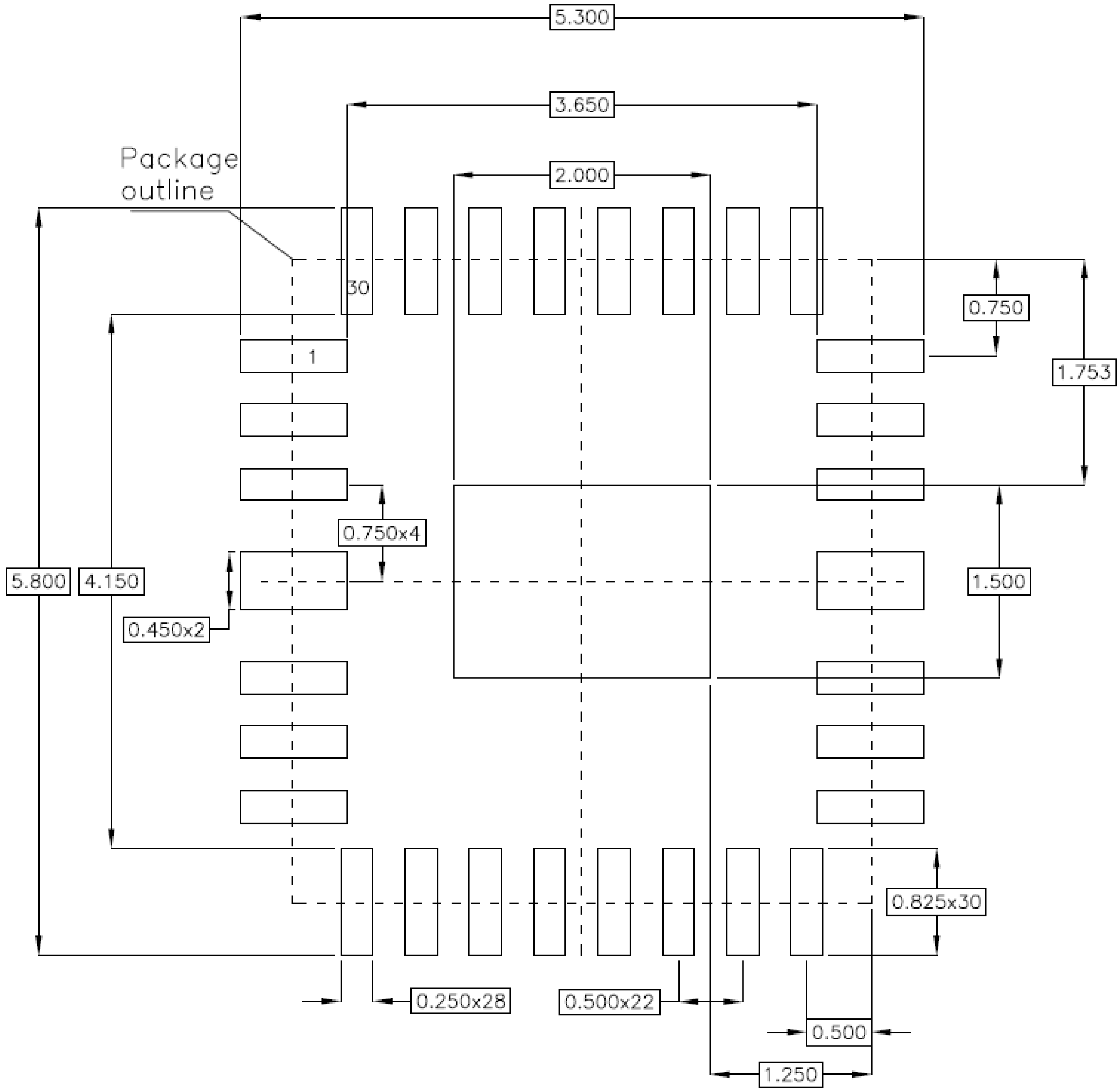


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
R	0.050	0.150	0.002	0.006
S	0.001	0.090	0.000	0.004

Tolerance
±0.050

WET W-Type 30L QFN 4.5x5 (FC) Package

Footprint Information



Package	Number of Pin	Tolerance
WET-V/W/U/XQFN4.5x5-30(FC)	30	±0.05

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