8 K Channel Digital Switch with High Jitter Tolerance, Single Rate (32 Mbps), and 16 Inputs and 16 Outputs

Data Sheet

December 2003

Features

- 8,192 channel x 8,192 channel non-blocking unidirectional switching. The Backplane and Local inputs and outputs can be combined to form a non-blocking switching matrix with 16 input streams and 16 output streams
- 4,096 channel x 4,096 channel non-blocking Backplane input to Local output stream switch
- 4,096 channel x 4,096 channel non-blocking Local input to Backplane output stream switch
- 4,096 channel x 4,096 channel non-blocking Backplane input to Backplane output switch
- 4,096 channel x 4,096 channel non-blocking Local input to Local output stream switch
- Backplane port accepts 8 input and 8 output ST-BUS streams with data rate of 32.768 Mbps
- Local port accepts 8 input and 8 output ST-BUS streams with data rate of 32.768 Mbps
- Exceptional input clock jitter tolerance (14 ns)
- Per-stream bit delay for Local and Backplane input streams
- Per-stream advancement for Local and Backplane output streams

Ordering Information

ZL50052GAC 196 ball PBGA

-40°C to +85°C

- Constant 2-frame throughput delay for frame integrity
- Per-channel high impedance output control for Local and Backplane streams
- Per-channel driven-high output control for Local and Backplane streams
- Per-channel message mode for Local and Backplane output streams
- Connection memory block programming for fast device initialization
- Automatic selection between ST-BUS and GCI-Bus operation
- Non-multiplexed Motorola microprocessor interface

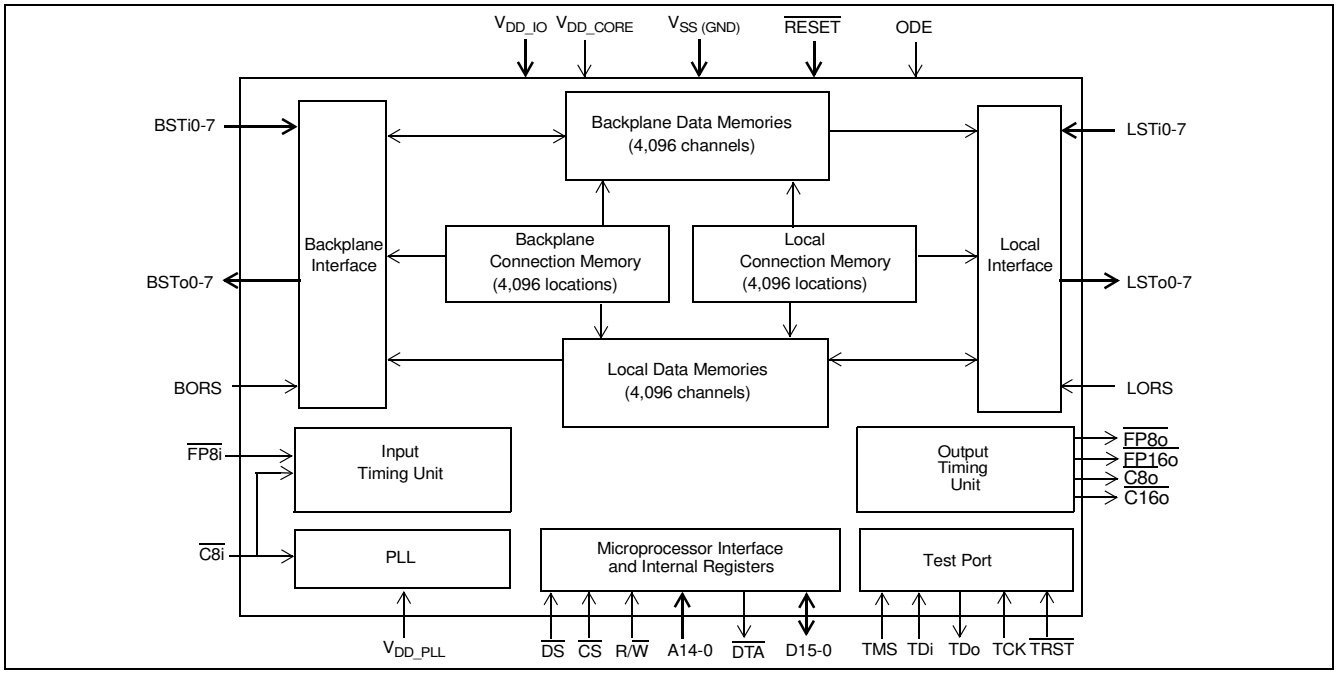

Figure 1 - ZL50052 Functional Block Diagram

- Conforms to the mandatory requirements of the IEEE-1149.1 (JTAG) standard
- Memory Built-In-Self-Test (BIST), controlled via microprocessor register
- 1.8 V core supply voltage
- 3.3 V I/O supply voltage
- 5 V tolerant inputs, outputs and I/Os

Applications

- Central Office Switches (Class 5)
- Media Gateways
- Class-Independent Switches
- Access Concentrators
- Scalable TDM-Based Architectures
- Digital Loop Carriers

Device Overview

The ZL50052 has two data ports, the Backplane and the Local port. Both the Backplane and Local ports operate at 32.768 Mbps.

The ZL50052 contains two data memory blocks (Backplane and Local) to provide the following switching path configurations:

- Input-to-Output Unidirectional, supporting 8 K x 8 K switching
- Backplane-to-Local Bi-directional, supporting 4 K x 4 K data switching
- Local-to-Backplane Bi-directional, supporting 4 K x 4 K data switching
- Backplane-to-Backplane Bi-directional, supporting 4 K x 4 K data switching
- Local-to-Local Bi-directional, supporting 4 K x 4 K data switching

The device contains two connection memory blocks, one for the Backplane output and one for the Local output. Data to be output on the serial streams may come from either of the data memories (Connection Mode) or directly from the connection memory contents (Message Mode).

In Connection Mode, the contents of the connection memory define, for each output stream and channel, the source stream and channel, (stored in data memory), to be switched.

In Message Mode, microprocessor data can be written to the connection memory for broadcast on the output streams on a per-channel basis. This feature is useful for transferring control and status information to external circuits or other ST-BUS devices.

The device uses a master frame pulse ($\overline{\text{FP8i}}$) and master clock ($\overline{\text{C8i}}$) to define the input frame boundary and timing for both the Backplane port and the Local port. The device will automatically detect whether an ST-BUS or a GCI-Bus style frame pulse is being used. There is a two-frame delay from the time $\overline{\text{RESET}}$ is de-asserted to the establishment of full switch functionality. During this period, the input frame pulse format is determined before switching begins.

The device provides $\overline{\text{FP8o}}$, $\overline{\text{FP16o}}$, $\overline{\text{C8o}}$ and $\overline{\text{C16o}}$ outputs to support external devices connected to the outputs of the Backplane and Local ports.

A non-multiplexed Motorola microprocessor port allows programming of the various device operation modes and switching configurations. The microprocessor port provides access for Register read/write, Connection Memory read/write and Data Memory read-only operations. The port has a 15-bit address bus, 16-bit data bus and four control signals. The microprocessor may monitor channel data in the Backplane and Local data memories.

The mandatory requirements of the IEEE-1149.1 (JTAG) standard are fully supported via a dedicated test port.

The ZL50052 is available in one package:

- a 15 mm x 15 mm body, 1 mm ball-pitch, 196-PBGA

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Pinout Diagram: (as viewed through top of package)

A1 corner identified by metallized marking, mold indent, ink dot, or right-angled corner.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	BSTo1	BSTo2	A4	A5	A8	A9	A12	A13	R/$\overline{W}$	$\overline{CS}$	TMS	TDo	IC_ OPEN	$\overline{TRST}$
B	A0	BSTo5	BSTo0	A1	A2	A7	A11	A14	ODE	TDi	TCK	IC_ OPEN	LSTo0	LSTo1
C	IC_GND	BSTo7	IC_ OPEN	BSTo3	BSTo4	A6	A10	$\overline{DS}$	$\overline{RESET}$	IC_ OPEN	IC_GND	IC_ OPEN	IC_GND	LSTo3
D	IC_GND	BSTo6	IC_ OPEN	GND	A3	VDD_IO	VDD_IO	VDD_IO	$\overline{DTA}$	VDD_IO	GND	LSTo4	LSTo6	LSTo2
E	IC_ OPEN	IC_ OPEN	IC_ OPEN	VDD_IO	GND	VDD_ CORE	VDD_ CORE	VDD_ CORE	VDD_ CORE	GND	VDD_IO	IC_ OPEN	LSTo7	LSTo5
F	IC_ OPEN	IC_ OPEN	IC_ OPEN	VDD_IO	VDD_ CORE	GND	GND	GND	GND	VDD_ CORE	VDD_IO	IC_ OPEN	IC_ OPEN	IC_ OPEN
G	BSTi0	BORS	VDD_ CORE	VDD_IO	VDD_ CORE	GND	GND	GND	GND	VDD_ CORE	VDD_IO	IC_ OPEN	IC_ OPEN	IC_ OPEN
H	BSTi1	BSTi2	BSTi3	VDD_IO	VDD_ CORE	GND	GND	GND	GND	VDD_ CORE	VDD_IO	VDD_ CORE	LORS	IC_ OPEN
J	BSTi4	BSTi5	BSTi7	VDD_IO	VDD_ CORE	GND	GND	GND	GND	VDD_ CORE	VDD_IO	LSTi5	LSTi1	LSTi2
K	BSTi6	IC_ OPEN	IC_ OPEN	VDD_IO	GND	VDD_ CORE	VDD_ CORE	VDD_ CORE	VDD_ CORE	GND	VDD_IO	IC_ OPEN	LSTi3	LSTi0
L	IC_ OPEN	IC_ OPEN	IC_ OPEN	GND	VDD_IO	VDD_IO	VDD_IO	VDD_IO	VDD_IO	VDD_IO	GND	IC_ OPEN	IC_ OPEN	LSTi6
M	IC_ OPEN	IC_ OPEN	D15	D14	D12	D5	IC_GND	IC_GND	$\overline{C16o}$	$\overline{FP8i}$	IC_ OPEN	IC_ OPEN	LSTi7	LSTi4
N	IC_ OPEN	D13	D10	D11	D7	D3	D0	IC_GND	VDD_ PLL	$\overline{C8o}$	$\overline{FP8o}$	IC_ OPEN	IC_ OPEN	IC_ OPEN
P	GND	D9	D8	D6	D4	D2	D1	IC_GND	IC_ OPEN	$\overline{C8i}$	IC_ OPEN	$\overline{FP16o}$	GND	GND

Figure 2 - ZL50052 PBGA Connections (196 PBGA, 15 mm x 15 mm) Pin Diagram
(as viewed through top of package)

Pin Description

Pin Name	ZL50052 Package Coordinates (196 ball PBGA)	Description
Device Timing		
$\overline{C8i}$	P10	**Master Clock (5 V Tolerant Schmitt-Triggered Input)** This pin accepts an 8.192 MHz clock. The internal frame boundary is aligned with the clock falling or rising edge, as controlled by the C8IPOL bit in the Control Register. Input data on both the Backplane and Local sides (BSTi0-7 and LSTi0-7) must be aligned to this clock and the accompanying input frame pulse, $\overline{FP8i}$.
$\overline{FP8i}$	M10	**Frame Pulse Input (5 V Tolerant Schmitt-Triggered Input)** When the Frame Pulse Width bit (FPW) of the Control Register is LOW (default), this pin accepts a 122 ns-wide frame pulse. When the FPW bit is HIGH, this pin accepts a 244 ns-wide frame pulse. The device will automatically detect whether an ST-BUS or GCI-Bus style frame pulse is applied. Input data on both the Backplane and Local sides (BSTi0-7 and LSTi0-7) must be aligned to this frame pulse and the accompanying input clock, $\overline{C8i}$.
$\overline{C8o}$	N10	**$\overline{C8o}$ Output Clock (5 V Tolerant Three-state Output)** This pin outputs an 8.192 MHz clock generated within the device. The clock falling edge or rising edge is aligned with the output frame boundary presented on $\overline{FP8o}$; this edge polarity alignment is controlled by the COPOL bit of the Control Register. Output data on both the Backplane and Local sides (BSTo0-7 and LSTo0-7) will be aligned to this clock and the accompanying output frame pulse, $\overline{FP8o}$.
$\overline{FP8o}$	N11	**Frame Pulse Output (5 V Tolerant Three-state Output)** When the Frame Pulse Width bit (FPW) of the Control Register is LOW (default), this pin outputs a 122 ns-wide frame pulse. When the FPW bit is HIGH, this pin outputs a 244 ns-wide frame pulse. The frame pulse, running at 8 kHz rate, will have the same format (ST-BUS or GCI-Bus) as the input frame pulse ($\overline{FP8i}$). Output data on both the Backplane and Local sides (BSTo0-7 and LSTo0-7) will be aligned to this frame pulse and the accompanying output clock, $\overline{C8o}$.
$\overline{C16o}$	M9	**$\overline{C16o}$ Output Clock (5 V Tolerant Three-state Output)** This pin outputs a 16.384 MHz clock generated within the device. The clock falling edge or rising edge is aligned with the output frame boundary presented on $\overline{FP16o}$; this edge polarity alignment is controlled by the COPOL bit of the Control Register. Output data on both the Backplane and Local sides (BSTo0-7 and LSTo0-7) will be aligned to this clock and the accompanying output frame pulse, $\overline{FP16o}$.

Pin Description (continued)

Pin Name	ZL50052 Package Coordinates (196 ball PBGA)	Description
$\overline{\text{FP16o}}$	P12	**Frame Pulse Output (5 V Tolerant Three-state Output)** When the Frame Pulse Width bit (FPW) of the Control Register is LOW (default), this pin outputs a 61 ns-wide frame pulse. When the FPW bit is HIGH, this pin outputs a 122 ns-wide frame pulse. The frame pulse, running at 8 kHz rate, will have the same format (ST-BUS or GCI-Bus) as the input frame pulse ($\overline{\text{FP8i}}$). Output data on both the Backplane and Local sides (BSTo0-7 and LSTo0-7) will be aligned to this frame pulse and the accompanying output clock, $\overline{\text{C16o}}$.
Backplane and Local Inputs		
BSTi0-7	G1, H1, H2, H3, J1, J2, K1, J3	**Backplane Serial Input Streams 0 to 7 (5 V Tolerant Inputs with Internal Pull-downs)** These pins accept serial TDM data streams at a fixed data rate of 32.768 Mbps (with 512 channels per stream).
LSTi0-7	K14, J13, J14, K13, M14, J12, L14, M13	**Local Serial Input Streams 0 to 7 (5 V Tolerant Inputs with Internal Pull-downs)** These pins accept serial TDM data streams at a fixed data rate of 32.768 Mbps (with 512 channels per stream).
Backplane and Local Outputs and Control		
ODE	B9	**Output Drive Enable (5 V Tolerant Input with Internal Pull-up)** An asynchronous input providing Output Enable control to the BSTo0-7 and LSTo0-7 outputs. When LOW, the BSTo0-7 and LSTo0-7 outputs are driven HIGH or high impedance (dependent on the **BORS** and **LORS** pin settings respectively). When HIGH, the outputs BSTo0-7 and LSTo0-7 are enabled.
BORS	G2	**Backplane Output Reset State (5 V Tolerant Input with Internal Pull-down)** When this input is LOW, the device will initialize with the BSTo0-7 outputs driven high. Following initialization, the Backplane stream outputs are always active. When this input is HIGH, the device will initialize with the BSTo0-7 outputs at high impedance. Following initialization, the Backplane stream outputs may be set active or high impedance using the **ODE** pin or on a per-channel basis with the **BE** bit in the Backplane Connection Memory.
BSTo0-7	B3, A1, A2, C4, C5, B2, D2, C2	**Backplane Serial Output Streams 0 to 7 (5 V Tolerant, Three-state Outputs with Slew-Rate Control)** These pins output serial TDM data streams at a fixed data rate of 32.768 Mbps (with 512 channels per stream). Refer to the descriptions of the **BORS** and **ODE** pins for control of the output HIGH or high impedance state.

Pin Description (continued)

Pin Name	ZL50052 Package Coordinates (196 ball PBGA)	Description
LORS	H13	**Local Output Reset State (5 V Tolerant Input with Internal Pull-down)** When this input is LOW, the device will initialize with the LSTo0-7 outputs driven high. Following initialization, the Local stream outputs are always active. When this input is HIGH, the device will initialize with the LSTo0-7 outputs at high impedance. Following initialization, the Local stream outputs may be set active or high impedance using the **ODE** pin or on a per-channel basis with the **LE** bit in the Local Connection Memory.
LSTo0-7	B13, B14, D14, C14, D12, E14, D13, E13	**Local Serial Output Streams 0 to 7 (5 V Tolerant Three-state Outputs with Slew-Rate Control)** These pins output serial TDM data streams at a fixed data rate of 32.768 Mbps (with 512 channels per stream). Refer to the descriptions of the **LORS** and **ODE** pins for control of the output HIGH or high impedance state.
Microprocessor Port Signals		
A0 - A14	B1, B4, B5, D5, A3, A4, C6, B6, A5, A6, C7, B7, A7, A8, B8	**Address 0 - 14 (5 V Tolerant Inputs)** These pins form the 15-bit address bus to the internal memories and registers. A0 = LSB
D0 - D15	N7, P7, P6, N6, P5, M6, P4, N5, P3, P2, N3, N4, M5, N2, M4, M3	**Data Bus 0 - 15 (5 V Tolerant Inputs/Outputs with Slew-Rate Control)** These pins form the 16-bit data bus of the microprocessor port. D0 = LSB
$\overline{CS}$	A10	**Chip Select (5 V Tolerant Input)** Active LOW input used by the microprocessor to enable the microprocessor port access **Note that a minimum of 30 ns must separate the de-assertion of $\overline{DTA}$ (to high) and the assertion of $\overline{CS}$ and/or $\overline{DS}$ to initiate the next access.**
$\overline{DS}$	C8	**Data Strobe (5 V Tolerant Input)** This active LOW input works in conjunction with $\overline{CS}$ to enable the microprocessor port read and write operations. **Note that a minimum of 30 ns must separate the de-assertion of $\overline{DTA}$ (to high) and the assertion of CS and/or DS to initiate the next access.**
R/$\overline{W}$	A9	**Read/$\overline{Write}$ (5 V Tolerant Input)** This input controls the direction of the data bus lines (D0-D15) during a microprocessor access.
$\overline{DTA}$	D9	**Data Transfer Acknowledgment (5 V Tolerant Three-state Output)** This active LOW output indicates that a data bus transfer is complete. A pull-up resistor is required to hold a HIGH level. **Note that a minimum of 30 ns must separate the de-assertion of $\overline{DTA}$ (to high) and the assertion of CS and/or DS to initiate the next access.**

Pin Description (continued)

Pin Name	ZL50052 Package Coordinates (196 ball PBGA)	Description
$\overline{\text{RESET}}$	C9	**Device Reset (5 V Tolerant Input with Internal Pull-up)** This input (active LOW) asynchronously applies reset and synchronously releases reset to the device. In the reset state, the outputs LSTo0-7 and BSTo0-7 are set to a HIGH or high impedance state, depending on the state of the LORS and BORS external control pins, respectively. The assertion of this pin also clears the device registers and internal counters. **Refer to Section 7.3 on page 24 for the timing requirements regarding this reset signal**.
JTAG Control Signals		
TCK	B11	**Test Clock (5 V Tolerant Input)** Provides the clock to the JTAG test logic.
TMS	A11	**Test Mode Select (5 V Tolerant Input with Internal Pull-up)** JTAG signal that controls the state transitions of the TAP controller.
TDi	B10	**Test Serial Data In (5 V Tolerant Input with Internal Pull-up)** JTAG serial test instructions and data are shifted in on this pin.
TDo	A12	**Test Serial Data Out (5 V Tolerant Three-state Output)** JTAG serial data is output on this pin on the falling edge of TCK. This pin is held in a high impedance state when JTAG is not enabled.
$\overline{\text{TRST}}$	A14	**Test Reset (5 V Tolerant Input with Internal Pull-up)** Asynchronously initializes the JTAG TAP controller to the Test-Logic-Reset state. This pin must be pulsed LOW during power-up for JTAG testing. This pin must be held LOW for normal functional operation of the device.
Power and Ground Pins		
V_{DD_IO}	D6, D7, D8, D10, E4, E11, F4, F11, G4, G11, H4, H11, J4, J11, K4, K11, L5, L6, L7, L8, L9, L10	**Power Supply for Periphery Circuits:** +3.3 V
V_{DD_CORE}	E6, E7, E8, E9, F5, F10, G3, G5, G10, H5, H10, H12, J5, J10, K6, K7, K8, K9	**Power Supply for Core Circuits:** +1.8 V
V_{DD_PLL}	N9	**Power Supply for Analog PLL:** +1.8 V

Pin Description (continued)

Pin Name	ZL50052 Package Coordinates (196 ball PBGA)	Description
V_{SS} (GND)	D4, D11, E5, E10, F6, F7, F8, F9, G6, G7, G8, G9, H6, H7, H8, H9, J6, J7, J8, J9, K5, K10, L4, L11, P1, P13, P14	**Ground**
Unused Pins		
IC_OPEN	A13, B12, C3, C10, C12, D3, E1, E2, E3, E12, F1, F2, F3, F12, F13, F14, G12, G13, G14, H14, K2, K3, K12, L1, L2, L3, L12, L13, M1, M2, M11, M12, N1, N12, N13, N14, P9, P11	**Internal Connections - OPEN** These pins must be left unconnected.
IC_GND	C1, C11, C13, D1, M7, M8, N8, P8	**Internal Connections - GND** These pins must be tied LOW.

1.0 Unidirectional and Bi-directional Switching Applications

The ZL50052 has a maximum capacity of 8,192 input channels and 8,192 output channels. This is calculated from the number of streams and channels: 16 input streams (8 Backplane, 8 Local) at 32.768 Mbps and 16 output streams (8 Backplane, 8 Local) at 32.768 Mbps, with each stream providing 512 channels.

A typical mode of operation is to separate the input and output streams to form a unidirectional switch, as shown in Figure 3 below.

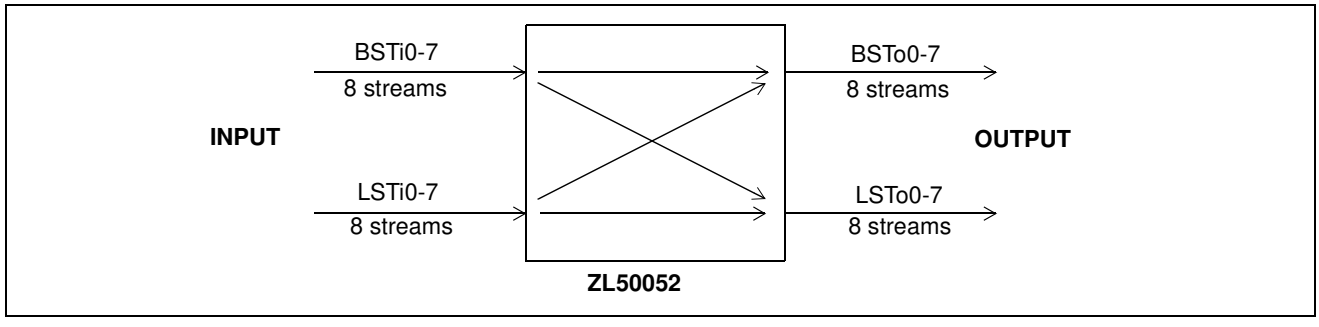


Figure 3 - 8,192 x 8,192 Channels (32 Mbps), Unidirectional Switching

In this system, the Backplane and Local input streams are combined, and the Backplane and Local output streams are combined, so that the switch appears as a 16 input stream by 16 output stream switch. This gives the maximum 8,192 x 8,192 channel capacity.

Often a system design needs to differentiate between a Backplane and a Local side, or it needs to put the switch in a bi-directional configuration. In this case, the ZL50052 can be used as shown in Figure 4 to give 4,096 x 4,096 channel bi-directional capacity.

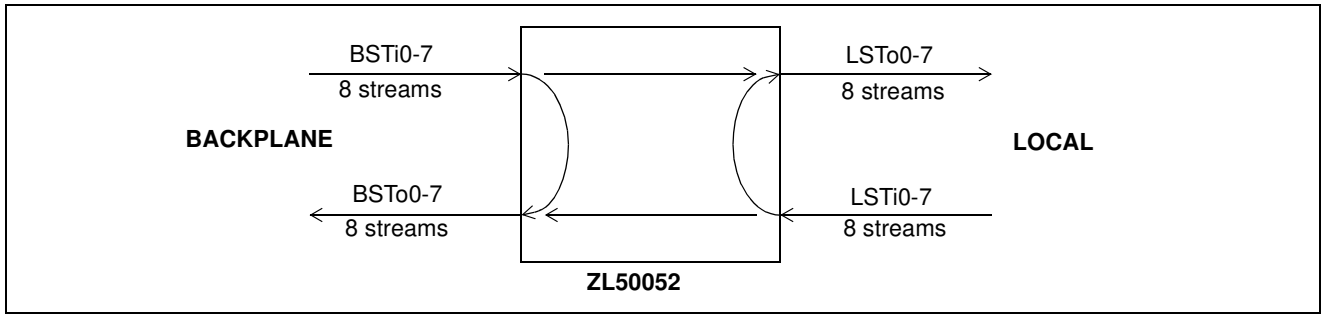


Figure 4 - 4,096 x 4,096 Channels (32 Mbps), Bi-directional Switching

In this system setup, the chip has a capacity of 4,096 input channels and 4,096 output channels on the Backplane side, as well as 4,096 input channels and 4,096 output channels on the Local side. Note that some or all of the output channels on one side can come from the other side, e.g., Backplane input to Local output switching.

1.1 Flexible Configuration

The ZL50052 can be configured as an 8 K by 8 K non-blocking unidirectional digital switch, a 4 K by 4 K non-blocking bi-directional digital switch, or as a blocking switch with various switching capacities.

1.1.1 Non-Blocking Unidirectional Configuration (Typical System Configuration)

Because the input and output drivers are synchronous, the user can combine input Backplane streams and input Local streams as well as output Backplane streams and output Local streams to increase the total number of input and output streams of the switch in a unidirectional configuration, as shown in Figure 3.

- 8,192 channel x 8,192 channel non-blocking switching from input to output streams

1.1.2 Non-Blocking Bi-directional Configuration

Another typical application is to configure the ZL50052 as a non-blocking 4 K by 4 K bi-directional switch, as shown in Figure 4:

- 4,096 channel x 4,096 channel non-blocking switching from Backplane input to Local output streams
- 4,096 channel x 4,096 channel non-blocking switching from Local input to Backplane output streams
- 4,096 channel x 4,096 channel non-blocking switching from Backplane input to Backplane output streams
- 4,096 channel x 4,096 channel non-blocking switching from Local input to Local output streams

1.1.3 Blocking Bi-directional Configuration

The ZL50052 can be configured as a blocking bi-directional switch if it is an application requirement. For example, it can be configured as a 6 K by 2 K bi-directional blocking switch, as shown in Figure 5:

- 6,144 channel x 2,048 channel blocking switching from Backplane input to Local output streams
- 2,048 channel x 6,144 channel blocking switching from Local input to Backplane output streams
- 6,144 channel x 6,144 channel non-blocking switching from Backplane input to Backplane output streams
- 2,048 channel x 2,048 channel non-blocking switching from Local input to Local output streams

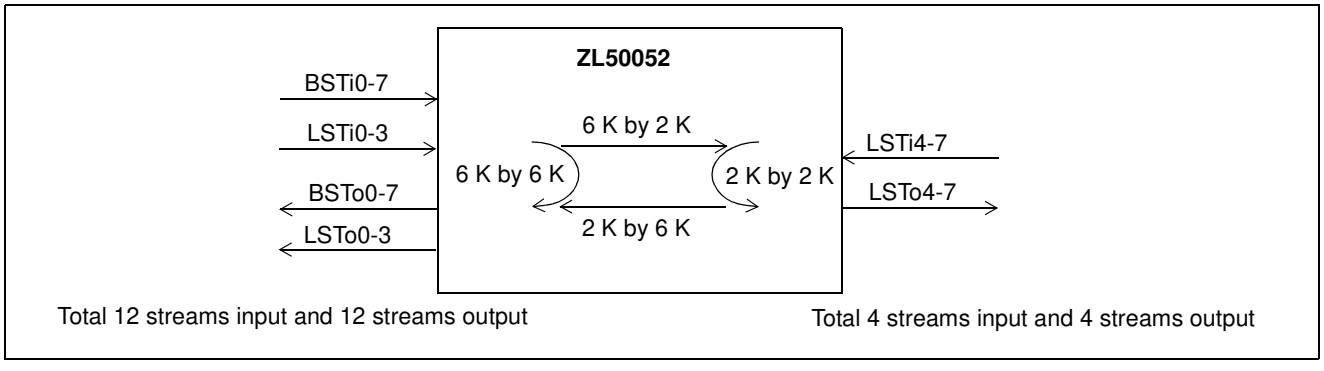


Figure 5 - 6,144 x 2,048 Channels Blocking Bi-directional Configuration

2.0 Functional Description

2.1 Switching Configuration

The device supports five switching configurations:

1. Unidirectional switch
2. Backplane-to-Local
3. Local-to-Backplane
4. Backplane-to-Backplane
5. Local-to-Local

The following sections describe the switching paths in detail. Configurations (2) - (5) enable a non-blocking bi-directional switch with 4,096 Backplane input/output channels at Backplane stream data rates of 32.768 Mbps, and 4,096 Local input/output channels at Local stream data rates of 32.768 Mbps. The switching paths of configurations (2) to (5) may be operated simultaneously.

2.1.1 Unidirectional Switch

The device can be configured as a 8,192 x 8,192 unidirectional switch by grouping together all input streams and all output streams. All streams operate at a data rate of 32.768 Mbps.

2.1.2 Backplane-to-Local Path

The device can provide data switching between the Backplane input port and the Local output port. The Local Connection Memory determines the switching configurations.

2.1.3 Local-to-Backplane Path

The device can provide data switching between the Local input port and the Backplane output port. The Backplane Connection Memory determines the switching configurations.

2.1.4 Backplane-to-Backplane Path

The device can provide data switching between the Backplane input and output ports. The Backplane Connection Memory determines the switching configurations.

2.1.5 Local-to-Local Path

The device can provide data switching between the Local input and output ports. The Local Connection Memory determines the switching configurations.

2.1.6 Port Operation

The Local port has 8 input (LSTi0-7) and 8 output (LSTo0-7) data streams. Similarly, the Backplane port has 8 input (BSTi0-7) and 8 output (BSTo0-7) data streams. All the streams operate at 32.768 Mbps. The timing of the input and output clocks and frame pulses is shown in Figure 7, “Input and Output (Generated) Frame Pulse Alignment” on page 17. The input traffic are aligned based on the $\overline{\text{FP8i}}$ and C8i input timing signals, while the output traffic are aligned based on the $\overline{\text{FP8o}}$ and C8o output timing signals.

2.1.6.1 Local Output Port

Operation of stream data in Connection Mode or Message Mode is determined by the state of the LMM bit of the Local Connection Memory. The channel high impedance state is controlled by the LE bit of the Local Connection Memory. The data source (e.g., from the Local or Backplane Data Memory) is determined by the LSRC bit of the Local Connection Memory. Refer to Section 8.1, Local Connection Memory, and Section 11.3, Local Connection Memory Bit Definition for more details.

2.1.6.2 Backplane Output Port

Operation of stream data in Connection Mode or Message Mode is determined by the state of the BMM bit of the Backplane Connection Memory and the channel high impedance state is controlled by the BE bit of the Backplane Connection Memory. The data source (e.g., from the Local or Backplane Data Memory) is determined by the BSRC bit of the Backplane Connection Memory. Refer to Section 8.2, Backplane Connection Memory and Section 11.4, Backplane Connection Memory Bit Definition for more details.

2.2 Frame Pulse Input and Master Input Clock Timing

The input frame pulse ($\overline{\text{FP8i}}$) is an 8 kHz input signal active for 122 ns or 244 ns at the frame boundary. The FPW bit in the Control Register must be set according to the applied pulse width. See Pin Description and Table 11, “Control Register Bits” on page 32 for details.

The active state and timing of $\overline{\text{FP8i}}$ can conform either to the ST-BUS or to the GCI-Bus as shown in Figure 6, “ST-BUS and GCI-Bus Input Timing Diagram”. The ZL50052 device will automatically detect whether an ST-BUS or a GCI-Bus style frame pulse is being used for the master frame pulse ($\overline{\text{FP8i}}$). The output frame pulses ($\overline{\text{FP8o}}$ and $\overline{\text{FP16o}}$) are always of the same style (ST-BUS or GCI-Bus) as the input frame pulse. The active edge of the input clock (C8i) shall be selected by the state of the Control Register bit C8IPOL.

Note that the active edge of ST-BUS is falling edge, which is the default mode of the device, while GCI-Bus uses rising edge as the active edge. Although GCI frame pulse will be automatically detected, to fully conform to GCI-Bus operation, the device should be set to use C8i rising edge as the active edge (by setting bit C8IPOL HIGH) when GCI-Bus is used.

For the purposes of describing the device operation, the remaining part of this document assumes the ST-BUS frame pulse format with a single width frame pulse of 122ns and a falling active clock-edge, unless explicitly stated otherwise.

In addition, the device provides FP8o, FP16o, C8o and C16o outputs to support external devices which connect to the output ports. The generated frame pulses (FP8o, FP16o) will be provided in the same format as the master frame pulse (FP8i). The polarity of C8o and C16o, at the frame boundary, can be controlled by the Control Register bit, COPOL. An analog phase lock loop (APLL) is used to multiply the input clock frequency on C8i to generate an internal clock signal operating at 131.072 MHz.

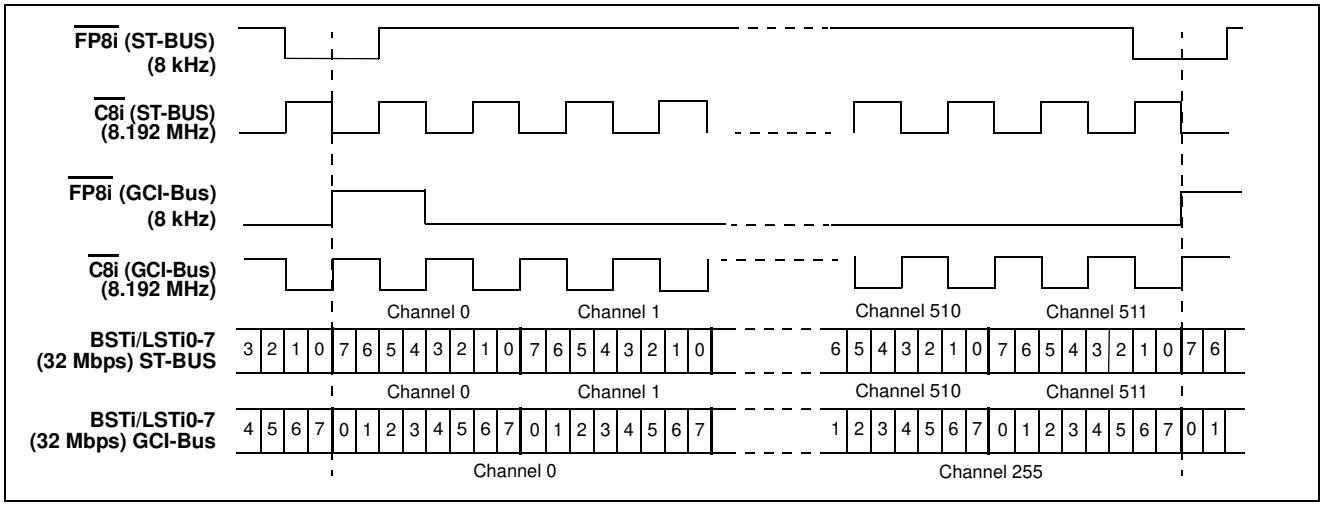


Figure 6 - ST-BUS and GCI-Bus Input Timing Diagram

2.3 Input Frame Pulse and Generated Frame Pulse Alignment

The ZL50052 accepts a frame pulse (FP8i) and generates two frame pulse outputs, FP8o and FP16o, which are aligned to the master frame pulse. There is a constant throughput delay for data being switched from the input to the output of the device such that data which is input during Frame N is output during Frame N+2.

For further details of frame pulse conditions and options, see Section 13.1, Control Register (CR), Figure 15, “Frame Boundary Conditions, ST-BUS Operation”, and Figure 16, “Frame Boundary Conditions, GCI-Bus Operation”.

Figure 7 - Input and Output (Generated) Frame Pulse Alignment

Figure 7 illustrates the input and output frame pulse alignment. The t_{FBOS} is the offset between the input frame pulse, FP8i, and the generated output frame pulse, FP8o. Refer to the “AC Electrical Characteristics”, on page 47. Note that although this figure shows the traditional setups of the frame pulses and clocks for both ST-BUS and

GCI-Bus configurations, the devices can be configured to accept/generate double-width frame pulses (if the FPW bit in the Control Register is set) as well as to use the opposite clock edge for frame-boundary determination (using the C8IPOL and COPOL bits in the Control Register). See the timing diagrams in “AC Electrical Characteristics”, on page 47 for all of the available configurations.

2.4 Jitter Tolerance Improvement Circuit - Frame Boundary Discriminator

To improve the jitter tolerance of the ZL50052, a Frame Boundary Discriminator (FBD) circuit was added to the device. This circuit is enabled by setting the Control Register bit FBDEN to HIGH. By default the FBD is disabled.

The FBD can operate in two modes, as controlled by the FBD_MODE[2:0] bits of the Control Register. When bits FBD_MODE[2:0] are set to 000_B, the FBD is set to handle lower frequency jitter only (<8 kHz). When bits FBD_MODE[2:0] are set to 111_B, the FBD can handle both low frequency and high frequency jitter. All other values are reserved. These bits are ignored when bit FBDEN is LOW. It is strongly recommended that if bit FBDEN is set HIGH, bits FBD_MODE[2:0] should be set to 111_B to improve the high frequency jitter handling capability.

To achieve the best jitter tolerance performance, it is also recommended that the input data sampling point be optimized. In most applications, the optimum sampling point is 1/2 instead of the default 3/4 (it can be changed by programming all the LIDR and BIDR registers). This will give more allowance for sampling point variations caused by jitter. There are, however, some cases where data experiences more delay than the timing signals. A common example occurs when multiple data lines are tied together to form bi-directional buses. The large bus loading may cause data to be delayed. If this is the case, the optimum sampling point may be 3/4 or 4/4 instead of 1/2. The optimum sampling point is dependent on the application. The user should optimize the sampling point to achieve the best jitter tolerance performance.

2.5 Input Clock Jitter Tolerance

Jitter tolerance can not be accurately represented by just one number. Jitter of the same amplitude but different frequency spectrum can have different effect on the operation of a device. For example, a device that can tolerate 20 ns of jitter of 10 kHz frequency may only be able to tolerate 10ns of jitter of 1 MHz frequency. Therefore, jitter tolerance should be represented as a spectrum over frequency. The highest possible jitter frequency is half of the carrier frequency. In the case of the ZL50052, the input clock is 8.192 MHz, and the jitter associated with this clock can have the highest frequency component at 4.096 MHz.

Tolerance of jitter of different frequencies are shown in the “AC Electrical Characteristics” section, table “Input Clock Jitter Tolerance” on page 54. The Jitter Tolerance Improvement Circuit was enabled (Control Register, bit FBDEN set HIGH, and bits FBD_MODE[2:0] set to 111_B), and the sampling point was optimized.

3.0 Input and Output Offset Programming

Various registers are used to control the input sampling point (delay) and the output advancement for the Local and Backplane streams. The following sections explain the details of these offset programming features.

3.1 Input Offsets

Control of the Input Bit Delay allows each input stream to have a different frame boundary with respect to the master frame pulse, $\overline{FP8i}$. Each input stream can be individually delayed by up to 7 3/4 bits with a resolution of 1/4 bit of the bit period.

3.1.1 Input Bit Delay Programming (Backplane and Local Input Streams)

Input Bit Delay Registers LIDR0 - 7 and BIDR0 - 7 work in conjunction with the SMPL_MODE bit in the Control Register to allow users to control input bit fractional delay as well as input bit sample point selection for greater flexibility when designing switch matrices for high speed operation.

When SMPL_MODE = LOW (input bit fractional delay mode) , bits LID[4:0] and BID[4:0] in the LIDR0 - 7 and BIDR0 - 7 registers respectively define the input bit fractional delay of the corresponding Local and Backplane stream. The total delay can be up to 7 3/4 bits with a resolution of 1/4 bit at the selected data rate. When SMPL_MODE = HIGH (sampling point select mode), bits LID[1:0] and BID[1:0] define the input bit sampling point of the stream. The sampling point can be programmed at the 3/4, 4/4, 1/4 or 2/4 bit location to allow better tolerance for input jitter. Bits LID[4:2] and BID[4:2] define the integer input bit delay, with a maximum value of 7 bits at a resolution of 1 bit.

Refer to Figure 8 for Input Bit Delay Timing at 32 Mbps data rates.

Refer to Figure 9 for Input Sampling Point Selection Timing at 32 Mbps data rates.

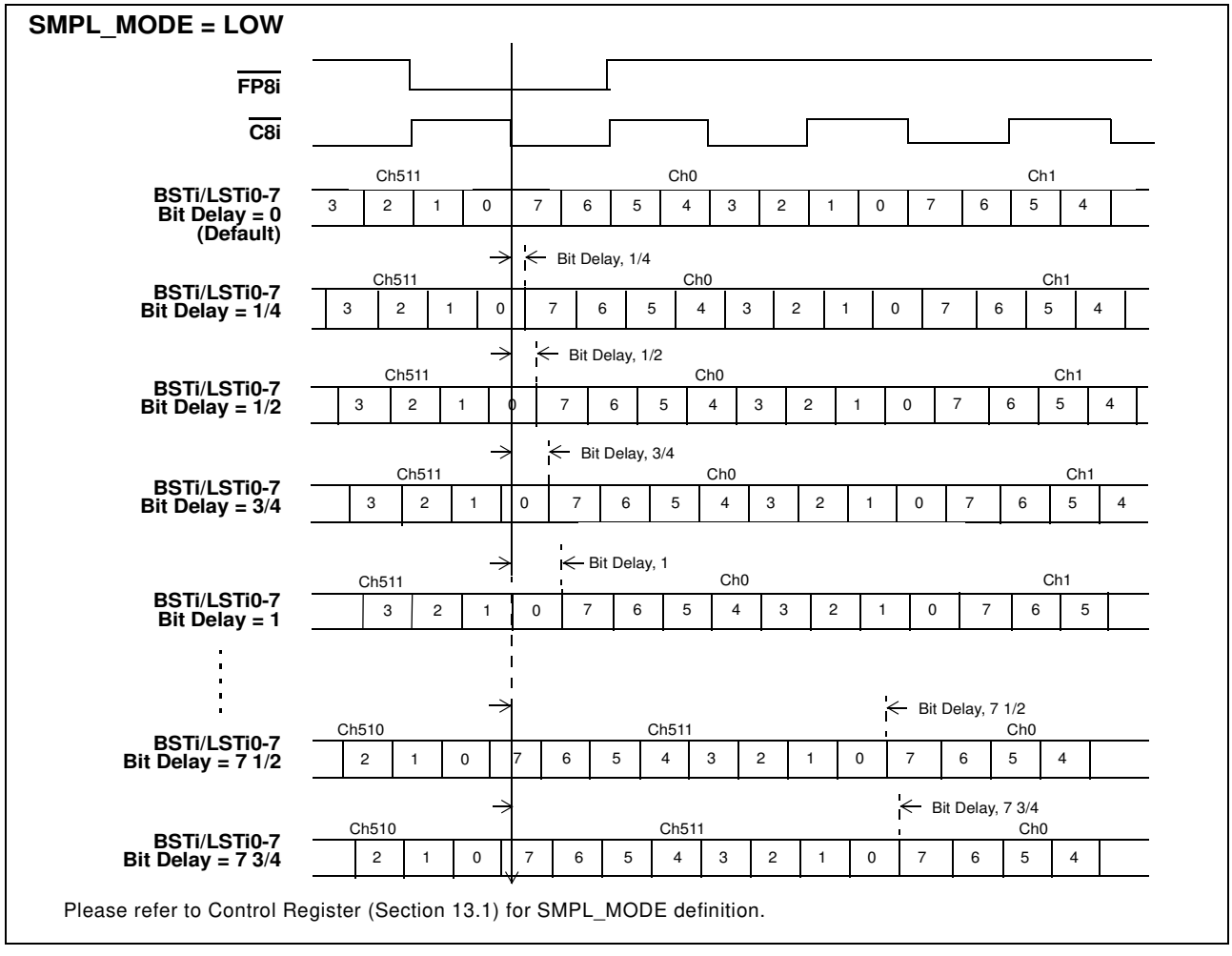


Figure 8 - Backplane and Local Input Bit Delay Timing Diagram for Data Rate of 32 Mbps

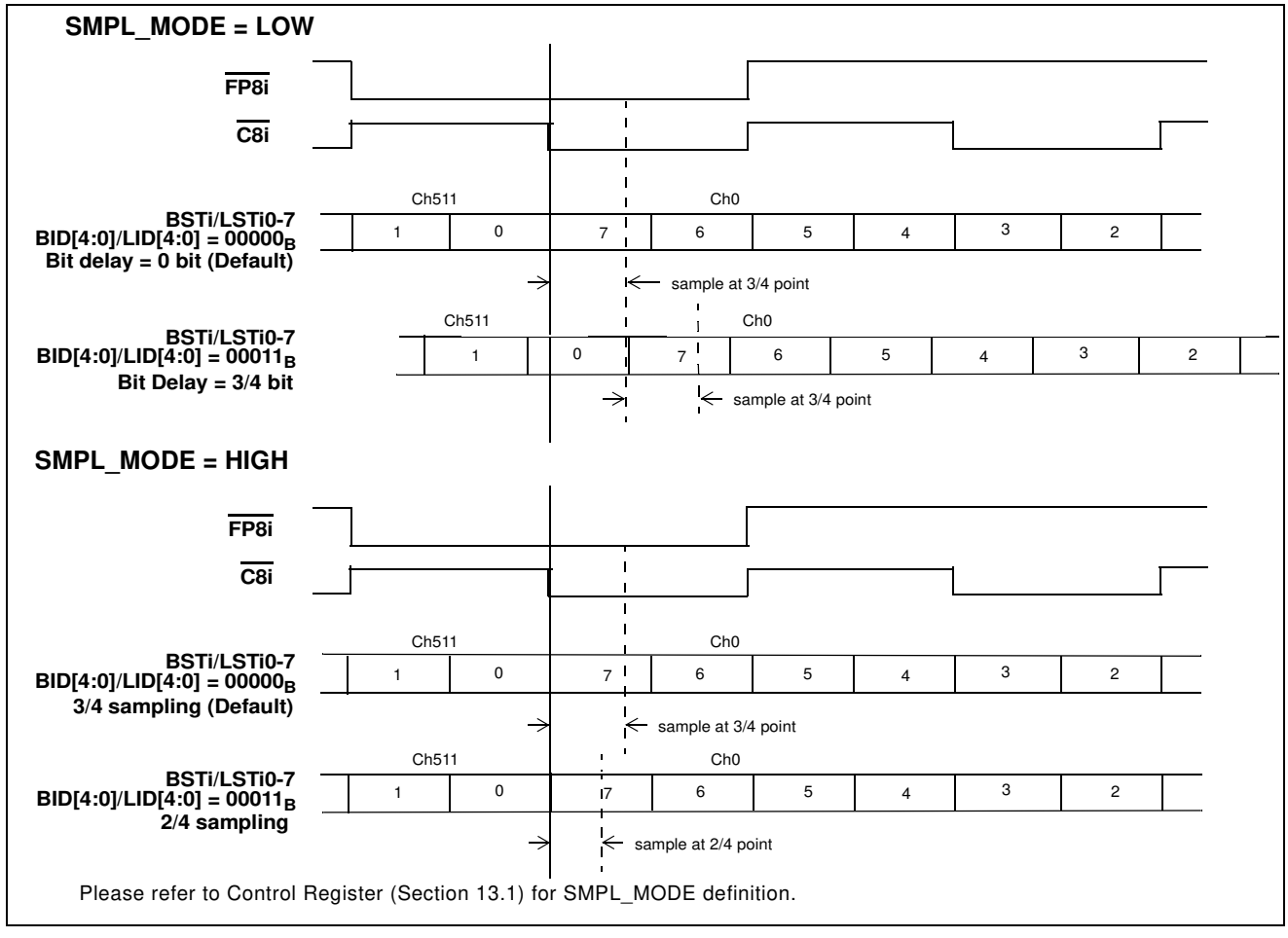


Figure 9 - Backplane and Local Input Bit Delay or Sampling Point Selection Timing Diagram for Data Rate of 32 Mbps

3.2 Output Advancement Programming (Backplane and Local Output Streams)

This feature is used to advance the output channel alignment of individual Local or Backplane output streams with respect to the frame boundary $\overline{FP8o}$. Each output stream has its own advancement value that can be programmed by the Output Advancement Registers. The output advancement selection is useful in compensating for various parasitic loading on the serial data output pins.

The Local and Backplane Output Advancement Registers, LOAR0 - LOAR7 and BOAR0 - BOAR7, are used to control the Local and Backplane output advancement respectively. The advancement is determined with reference to the internal system clock rate (131.072 MHz). The advancement can be 0, -1 cycle, -2 cycles or -3 cycles, which converts to approximately 0 ns, -7.6 ns, -15 ns or -23 ns as shown in Figure 10.

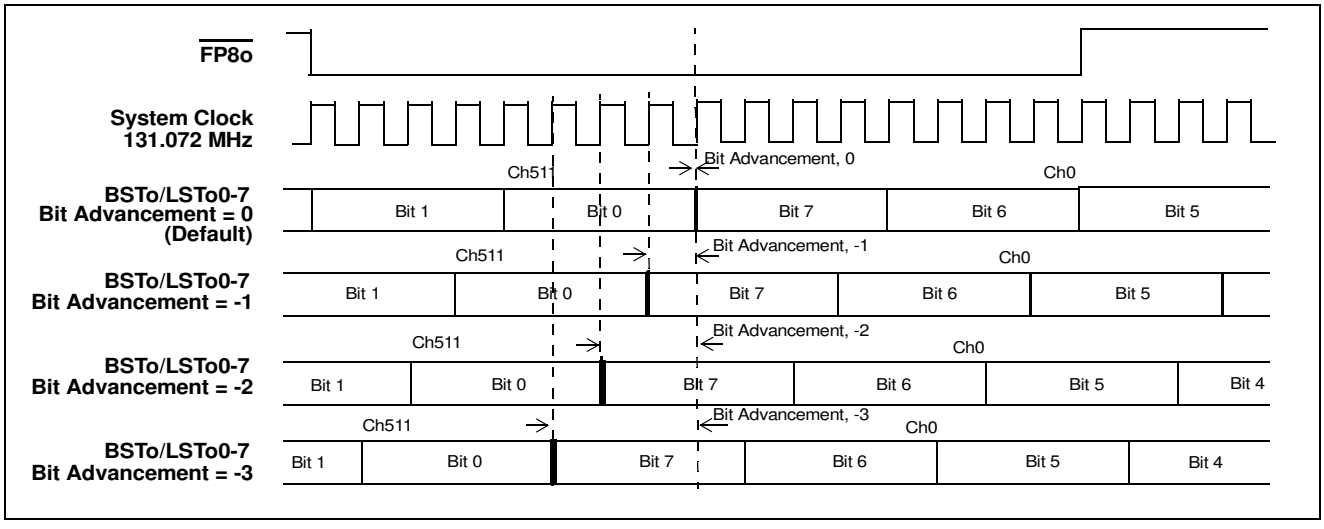


Figure 10 - Local and Backplane Output Advancement Timing Diagram for Data Rate of 32 Mbps

4.0 Port High-Impedance Control

The input pins, **LORS** and **BORS**, select whether the Local (**LSTo0-7**) and Backplane (**BSTo0-7**) output streams, respectively, are set to high impedance at the output of the device itself, or are always driven (active HIGH or active LOW).

Setting **LORS**/**BORS** to a LOW state will configure the output streams, **LSTo0-7**/**BSTo0-7,** to transmit bi-state channel data.

Setting **LORS**/**BORS** to a HIGH state will configure the output streams, **LSTo0-7**/**BSTo0-7,** of the device to invoke a high impedance output on a per-channel basis. The Local/Backplane Output Enable Bit (**LE**/**BE**) of the Local/Backplane Connection Memory has direct per-channel control on the high impedance state of the Local/Backplane output streams, **L**/**BSTo0-7**. Programming a LOW state in the connection memory LE/BE bit will set the stream output of the device to high impedance for the duration of the channel period. See “Local Connection Memory Bit Definition”, on page 29 and “Backplane Connection Memory Bit Definition”, on page 30 for programming details.

The state of the **LORS**/**BORS** pin is detected and the device configured accordingly during a **$\overline{\text{RESET}}$** operation, e.g., following power-up. The **LORS**/**BORS** pin is an asynchronous input and is expected to be hard-wired for a particular system application, although it may be driven under logic control if preferred.

The Local/Backplane output enable control in order of highest priority is: $\overline{\text{RESET}}$, ODE, OSB, LE/BE.

$\overline{\text{RESET}}$ (input pin)	**ODE (input pin)**	**OSB (Control Register bit)**	**LE/BE (Local / Backplane Connection Memory bit)**	**LORS/BORS (input pin)**	**LSTo0-7/ BSTo0-7**
0	X	X	X	0	HIGH
0	X	X	X	1	HI-Z
1	0	X	X	0	HIGH
1	0	X	X	1	HI-Z
1	1	0	X	0	HIGH

Table 1 - Local and Backplane Output Enable Control Priority

$\overline{\text{RESET}}$ (input pin)	ODE (input pin)	OSB (Control Register bit)	LE/BE (Local / Backplane Connection Memory bit)	LORS/BORS (input pin)	LSTo0-7/ BSTo0-7
1	1	0	X	1	HI-Z
1	1	1	0	0	HIGH
1	1	1	0	1	HI-Z
1	1	1	1	X	ACTIVE (HIGH or LOW)

Table 1 - Local and Backplane Output Enable Control Priority (continued)

5.0 Data Delay Through the Switching Paths

Serial data which goes into the device is converted into parallel format and written to consecutive locations in the data memory. Each data memory location corresponds to the input stream and channel number. Channels written to any of the buffers during Frame N will be read out during Frame N+2. The input bit delay and output bit advancement have no impact on the overall data throughput delay.

In the following paragraphs, the data throughput delay (**T**) is represented as a function of ST-BUS frames, input channel number, (**m**), and output channel number (**n**). For 32.768 Mbps data rate, there are 512 channels on each stream. The input channel number (**m**) and output channel number (**n**) can therefore have a range of 0 to 511. The data throughput delay under various input channel and output channel conditions can be summarized as:

T = 2 frames + (n - m)

The data throughput delay (**T**) is: **T = 2 frames + (n - m)**. Assuming that **m** (input channel) and **n** (output channel) are equal, we have the figure below, in which the delay between the input data being written and the output data being read is exactly 2 frames.

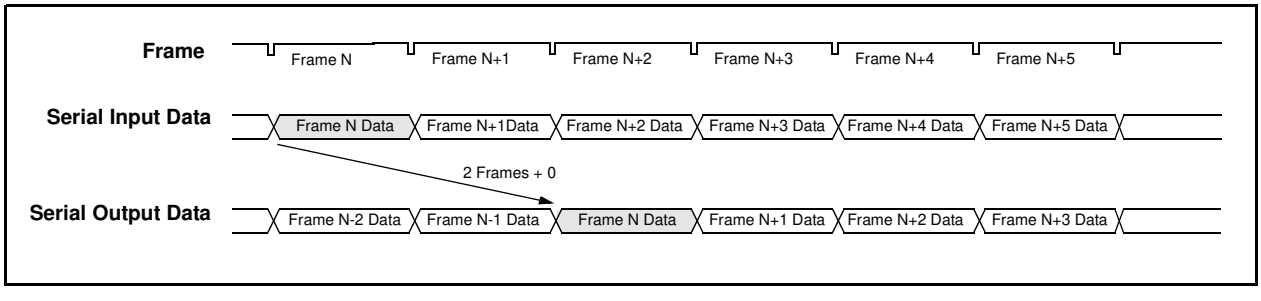


Figure 11 - Data Throughput Delay with Input Ch0 Switched to Output Ch0

Assuming that **n** (output channel) is greater than **m** (input channel), we have the figure below, in which the delay time between the input channel being written and the output channel being read exceeds 2 frames.

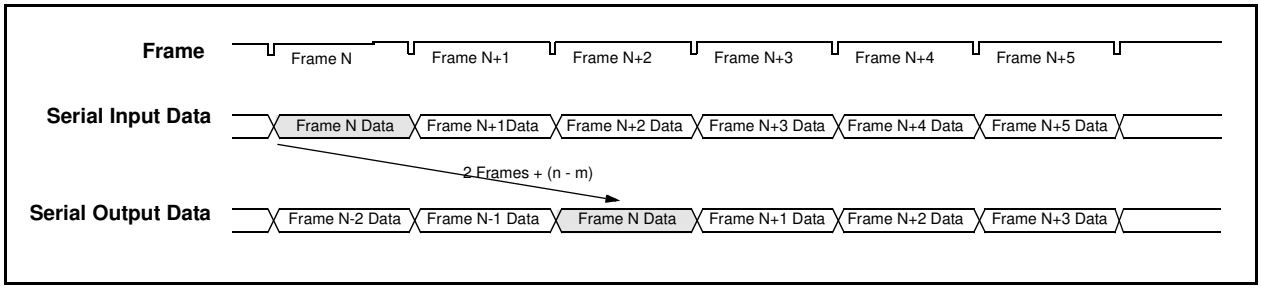


Figure 12 - Data Throughput Delay with Input Ch0 Switched to Output Ch13

Assuming that **n** (output channel) is less than **m** (input channel), we have the figure below, in which the delay time between the input channel being written and the output channel being read is less than 2 frames.

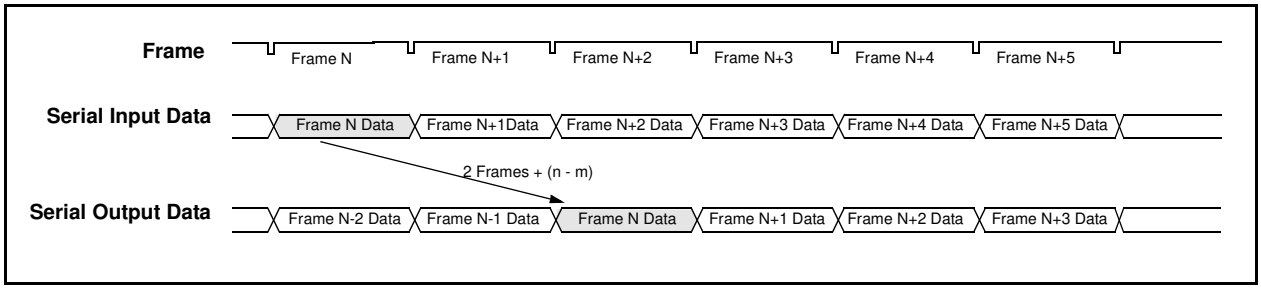


Figure 13 - Data Throughput Delay with Input Ch13 Switched to Output Ch0

6.0 Microprocessor Port

The 8 K switch family supports non-multiplexed Motorola type microprocessor buses. The microprocessor port consists of a 16-bit parallel data bus (**D0-15**), a 15-bit address bus (**A0-14**) and four control signals (**CS, DS, R/W** and **DTA**). The data bus provides access to the internal registers, the Backplane Connection and Data Memories, and the Local Connection and Data Memories. Each memory has 4,096 locations. See Table 5, Address Map for Data and Connection Memory Locations (A14 = 1), for the address mapping.

Each Connection Memory can be read or written via the 16-bit microprocessor port. The Data Memories can only be read (but not written) from the microprocessor port.

To prevent the bus 'hanging', in the event of the switch not receiving a master clock, the microprocessor port shall complete the $\overline{\text{DTA}}$ handshake when accessed, but any data read from the bus will be invalid.

7.0 Device Power-Up, Initialization and Reset

7.1 Power-Up Sequence

The recommended power-up sequence is for the V_{DD_IO} supply (nominally +3.3 V) to be established before the power-up of the V_{DD_PLL} and V_{DD_CORE} supplies (nominally +1.8 V). The V_{DD_PLL} and V_{DD_CORE} supplies may be powered-up simultaneously, but neither should 'lead' the V_{DD_IO} supply by more than 0.3 V.

All supplies may be powered-down simultaneously.

7.2 Initialization

Upon power-up, the device should be initialized by applying the following sequence:

1 Ensure the **TRST** pin is permanently LOW to disable the JTAG TAP controller.

2 Set **ODE** pin to LOW. This sets the **LSTo0-7** outputs to HIGH or high impedance, dependent on the **LORS** input value, and sets the **BSTo0-7** outputs to HIGH or high impedance, dependent on **BORS** input value. Refer to Pin Description for details of the **LORS** and **BORS** pins.

3 Reset the device by asserting the **RESET** pin to zero for at least two cycles of the input clock, **C8i**. A delay of an additional 250 µs must also be applied before the first microprocessor access is performed following the de-assertion of the **RESET** pin; this delay is required for determination of the input frame pulse format.

4 Use the Block Programming Mode to initialize the Local and the Backplane Connection Memories. Refer to Section 8.3, Connection Memory Block Programming.

5 Set **ODE** pin to HIGH after the connection memories are programmed to ensure that bus contention will not occur at the serial stream outputs.

7.3 Reset

The **RESET** pin is used to reset the device. When set LOW, an asynchronous reset is applied to the device. It is then synchronized to the internal clock. During the reset period, depending on the state of input pins **LORS** and **BORS**, the output streams **LSTo0-7** and **BSTo0-7** are set to HIGH or high impedance, and all internal registers and counters are reset to the default state.

The **RESET** pin must remain LOW for two input clock cycles (**C8i**) to guarantee a synchronized reset release. A delay of an additional 250 µs must also be waited before the first microprocessor access is performed following the de-assertion of the **RESET** pin; this delay is required for determination of the frame pulse format.

In addition, the reset signal must be de-asserted less than 12 µs after the frame boundary or more than 13µs after the frame boundary, as illustrated in Figure 14. This can be achieved, for example, by synchronizing the de-assertion of the reset signal with the input frame pulse **FP8i**.

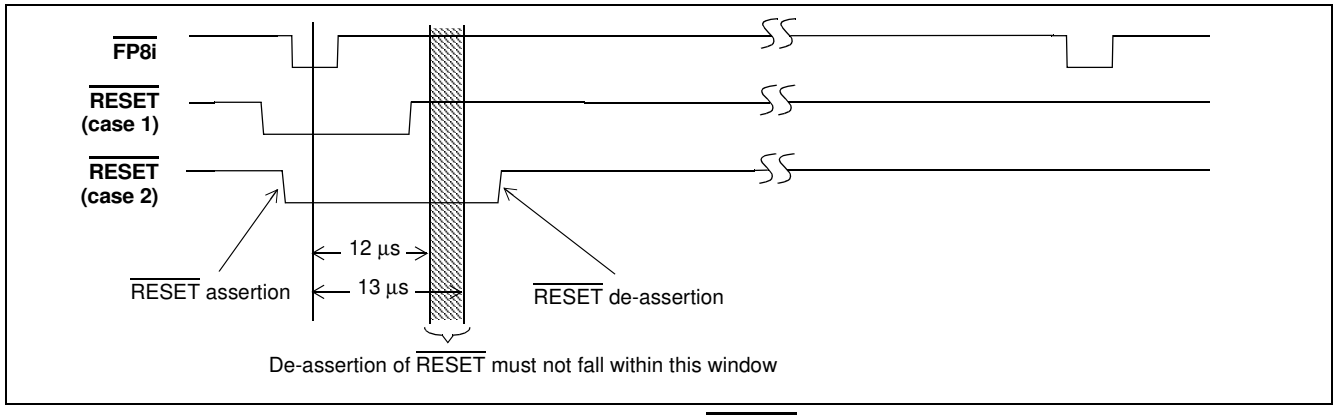


Figure 14 - Hardware RESET De-assertion

8.0 Connection Memory

The device includes two connection memories, the Local Connection Memory and the Backplane Connection Memory.

8.1 Local Connection Memory

The Local Connection Memory (LCM) is a 16-bit wide memory with 4,096 memory locations to support the Local output port. The most significant bit of each word, bit[15], selects the source stream from either the Backplane (LSRC = LOW) or the Local (LSRC = HIGH) port and determines the Backplane-to-Local or Local-to-Local data routing. Bits[14:13] select the control modes of the Local output streams, the per-channel Message Mode and the per-channel high impedance output control modes. In Connection Mode (bit[14] = LOW), bits[12:0] select the source stream and channel number as detailed in Table 2. In Message Mode (bit[14] = HIGH), bits[12:8] are unused and bits[7:0] contain the message byte to be transmitted. Bit[13] must be HIGH for Message Mode to ensure that the output channel is not tri-stated.

8.2 Backplane Connection Memory

The Backplane Connection Memory (BCM) is a 16-bit wide memory with 4,096 memory locations to support the Backplane output port. The most significant bit of each word, bit[15], selects the source stream from either the Backplane (BSRC = HIGH) or the Local (BSRC = LOW) port and determines the Local-to-Backplane or Backplane-to-Backplane data routing. Bit[14:13] select the control modes of the Backplane output streams, namely the per-channel Message Mode and the per-channel high impedance output control mode. In Connection Mode (bit[14] = LOW), bits[12:0] select the source stream and channel number as detailed in Table 2. In Message Mode (bit[14] = HIGH), bits[12:8] are unused and bits[7:0] contain the message byte to be transmitted. Bit[13] must be HIGH for Message Mode to ensure that the output channel is not tri-stated.

The Control Register bits MS[2:0] must be set to 000 to select the Local Connection Memory for the write and read operations via the microprocessor port. The Control Register bits MS[2:0] must be set to 001 to select the Backplane Connection Memory for the write and read operations via the microprocessor port. See Section 6.0, Microprocessor Port, and Section 13.1, Control Register (CR) for details on microprocessor port access.

Source Stream Bit Rate	Source Stream No.	Source Channel No.
32 Mbps	Bits[12:9] legal values 0:7	Bits[8:0] legal values 0:511

Table 2 - Local and Backplane Connection Memory Configuration

8.3 Connection Memory Block Programming

This feature allows fast, simultaneous, initialization of the Local and Backplane Connection Memories after power-up. When the Memory Block Programming mode is enabled, the contents of the Block Programming Register (BPR) will be loaded into the connection memories. See Table 11 and Table 12 for details of the Control Register and Block Programming Register values, respectively.

8.3.1 Memory Block Programming Procedure

- Set the **MBP** bit in the Control Register from LOW to HIGH.
- Set the **BPE** bit to HIGH in the Block Programming Register (BPR). The Local Block Programming data bits, **LBPD[2:0]**, of the Block Programming Register, will be loaded into bits[15:13] of the Local Connection Memory. The remaining bit positions are loaded with zeros as shown in Table 3.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LBPD2	LBPD1	LBPD0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 3 - Local Connection Memory in Block Programming Mode

The Backplane Block Programming data bits, **BBPD[2:0]**, of the Block Programming Register, will be loaded into bits[15:13] respectively, of the Backplane Connection Memory. The remaining bit positions are loaded with zeros as shown in Table 4.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BBPD2	BBPD1	BBPD0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4 - Backplane Connection Memory in Block Programming Mode

The Block Programming Register bit, **BPE** will be automatically reset LOW within 125 µs, to indicate completion of memory programming.

The Block Programming Mode can be terminated at any time prior to completion by clearing the **BPE** bit of the Block Programming Register or the **MBP** bit of the Control Register.

Note that the default values (LOW) of **LBPD[2:0]** and **BBPD[2:0]** of the Block Programming Register, following a device reset, can be used.

During reset, all output channels go HIGH or high impedance, depending on the value of the LORS and BORS pins, irrespective of the values in bits[14:13] of the connection memory.

9.0 Memory Built-In-Self-Test (BIST) Mode

As operation of the memory BIST will corrupt existing data, this test must only be instigated when the device is placed “out-of-service” or isolated from live traffic.

The memory BIST mode is enabled through the microprocessor port (**Section 13.7, Memory BIST Register**). Internal BIST memory controllers generate the memory test pattern (S-march) and control the memory test. The memory test result is monitored through the Memory BIST Register.

10.0 JTAG Port

The ZL50052 JTAG interface conforms to the IEEE 1149.1 standard. The operation of the boundary-scan circuit shall be controlled by an external Test Access Port (TAP) Controller.

10.1 Test Access Port (TAP)

The Test Access Port (TAP) consists of four input pins and one output pin described as follows:

- **Test Clock Input (TCK)**
  TCK provides the clock for the TAP Controller and is independent of any on-chip clock. **TCK** permits the shifting of test data into or out of the Boundary-Scan register cells under the control of the TAP Controller in Boundary-Scan Mode.
- **Test Mode Select Input (TMS)**
  The TAP controller uses the logic signals applied to the **TMS** input to control test operations. The TMS signals are sampled at the rising edge of the **TCK** pulse. This pin in internally pulled to V_{DD_IO} when not driven from an external source.
- **Test Data Input (TDi)**
  Depending on the previously applied data to the **TMS** input, the serial input data applied to the **TDi** port is connected either to the Instruction Register or to a Test Data Register. Both registers are described in Section 10.2, TAP Registers. The applied input data is sampled at the rising edge of **TCK** pulses. This pin is internally pulled to V_{DD_IO} when not driven from an external source.
- **Test Data Output (TDo)**
  Depending on the previously applied sequence to the **TMS** input, the contents of either the instruction register or data register are serially shifted out towards the **TDo**. The data out of the **TDo** is clocked on the falling edge of the **TCK** pulses. When no data is shifted through the boundary scan cells, the **TDo** output is set to a high impedance state.
- **Test Reset ($\overline{\text{TRST}}$)**
  TRST provides an asynchronous Reset to the JTAG scan structure. This pin is internally pulled high when not driven from an external source. This pin MUST be pulled low for normal operation.

10.2 TAP Registers

The ZL50052 implements the public instructions defined in the IEEE-1149.1 standard with the provision of an Instruction Register and three Test Data Registers.

10.2.1 Test Instruction Register

The JTAG interface contains a 4-bit instruction register. Instructions are serially loaded into the Instruction Register from the **TDi** pin when the TAP Controller is in the shift-IR state. Instructions are subsequently decoded to achieve two basic functions: to select the Test Data Register to operate while the instruction is current, and to define the serial Test Data Register path to shift data between **TDi** and **TDo** during data register scanning. Please refer to Figure 24 for JTAG test port timing.

10.2.2 Test Data Registers

10.2.2.1 The Boundary-Scan Register

The Boundary-Scan register consists of a series of Boundary-Scan cells arranged to form a scan path around the boundary of the ZL50052 core logic.

10.2.2.2 The Bypass Register

The Bypass register is a single stage shift register to provide a 1-bit path from **TDi** to **TDo**.

10.2.2.3 The Device Identification Register

The JTAG device ID for the ZL50052 is $0C38414B_H$.

Version, Bits <31:28>: 0000

Part No., Bits <27:12>: 1100 0011 1000 0100

Manufacturer ID, Bits <11:1>: 0001 0100 101

Header, Bit <0> (LSB): 1

10.3 Boundary Scan Description Language (BSDL) File

A Boundary Scan Description Language (BSDL) file is available from Zarlink Semiconductor to aid in the use of the IEEE 1149.1 test interface.

11.0 Memory Address Mappings

When the most significant bit, A14, of the address bus is set to '1', the microprocessor performs an access to one of the device's internal memories. The Control Register bits MS[2:0] indicate which memory (Local Connection, Local Data, Backplane Connection, or Backplane Data) is being accessed. Address bits A0-A13 indicate which location within the particular memory is being accessed.

Address Bit	Description
A14	**Selects memory or register access (0 = register, 1 = memory)** Note that which memory (Local Connection, Local Data, Backplane Connection, Backplane Data) is accessed depends on the **MS[2:0] bits in the Control Register**.
A13-A9	**Stream address (0 - 7)** Streams 0 to 7 are used
A8-A0	**Channel address (0 - 511)** Channels 0 to 511 are used when serial stream is at 32.768 Mbps

Table 5 - Address Map for Data and Connection Memory Locations (A14 = 1)

The device contains two data memory blocks, one for received Backplane data and one for received Local data. For all data rates, the received data is converted to parallel format by internal serial-to-parallel converters and stored sequentially in the relevant data memory.

11.1 Local Data Memory Bit Definition

The 8-bit Local Data Memory (LDM) has 4,096 positions. The locations are associated with the Local input streams and channels. As explained in the section above, address bits A13-A0 of the microprocessor define the addresses of the streams and the channels. The LDM is read-only and configured as follows:

Bit	Name	Description
15:8	Reserved	Set to a default value of 8'h00.
7:0	LDM	**Local Data Memory - Local Input Channel Data** The LDM[7:0] bits contain the timeslot data from the Local side input TDM stream. LDM[7] corresponds to the first bit received, e.g., bit 7 in ST-BUS mode, bit 0 in GCI-Bus mode. See Figure 6, "ST-BUS and GCI-Bus Input Timing Diagram" for the arrival order of the bits.

Table 6 - Local Data Memory (LDM) Bits

Note that the Local Data Memory is actually an 8-bit wide memory. The most significant 8 bits expressed in the table above are presented to provide 16-bit microprocessor read accesses.

11.2 Backplane Data Memory Bit Definition

The 8-bit Backplane Data Memory (BDM) has 4,096 positions. The locations are associated with the Backplane input streams and channels. As explained previously, address bits A13-A0 of the microprocessor define the addresses of the streams and the channels. The BDM is read-only and configured as follows:

Bit	Name	Description
15:8	Reserved	Set to a default value of 8'h00.
7:0	BDM	**Backplane Data Memory - Backplane Input Channel Data.** The BDM[7:0] bits contain the timeslot data from the Backplane side input TDM stream. BDM[7] corresponds to the first bit received, i.e. bit 7 in ST-BUS mode, bit 0 in GCI-Bus mode. See Figure 6, "ST-BUS and GCI-Bus Input Timing Diagram" for the arrival order of the bits.

Table 7 - Backplane Data Memory (BDM) Bits

Note that the Backplane Data Memory is actually an 8-bit wide memory. The most significant 8 bits expressed in the table above are presented to provide 16-bit microprocessor read accesses.

11.3 Local Connection Memory Bit Definition

The Local Connection Memory (LCM) has 4,096 addresses of 16-bit words. Each address, accessed through bits A13-A0 of the microprocessor port, is allocated to an individual Local output stream and channel. The bit definition for each 16-bit word is presented in Table 8 for Source-to-Local connections.

The most-significant bit in the memory location, LSRC, selects the switch configuration for Backplane-to-Local or Local-to-Local. When the per-channel Message Mode is selected (LMM memory bit = HIGH), the lower byte of the LCM word (LCAB[7:0]) will be transmitted as data on the output stream (LSTo0-7) in place of data defined by the Source Control, Stream and Channel Address bits.

Bit	Name	Description
15	LSRC	**Local Source Control Bit** When LOW, the source is from the Backplane input port (Backplane Data Memory). When HIGH, the source is from the Local input port (Local Data Memory). Ignored when LMM is set HIGH.
14	LMM	**Local Message Mode Bit** When LOW, the channel is in Connection Mode (data to be output on channel originated in Local or Backplane Data Memory). When HIGH, the channel is in Message Mode (data to be output on channel originated in Local Connection Memory).
13	LE	**Local Output Enable Bit** When LOW, the channel may be high impedance, either at the device output, or set by an external buffer dependent upon the LORS pin. When HIGH, the channel is active.
12:9	LSAB[3:0]	**Source Stream Address Bits** The binary value of these 4 bits represents the input stream number. Ignored when LMM is set HIGH.
8:0	LCAB[8:0]	**Source Channel Address Bits / Message Mode Data** The binary value of these 9 bits represents the input channel number, when LMM is LOW. Bits LCAB[7:0] transmitted as data when LMM is set HIGH. Note: When LMM is set HIGH, in both ST-BUS and GCI-Bus modes, the LCAB[7:0] bits are output sequentially to the timeslot with LCAB[7] being output first.

Table 8 - LCM Bits for Source-to-Local Switching

11.4 Backplane Connection Memory Bit Definition

The Backplane Connection Memory (BCM) has 4,096 addresses of 16-bit words. Each address, accessed through bits A13-A0 of the microprocessor port, is allocated to an individual Backplane output stream and channel. The bit definition for each 16-bit word is presented in Table 9 for Source-to-Backplane connections.

The most-significant bit in the memory location, BSRC, selects the switch configuration for Local-to-Backplane or Backplane-to-Backplane. When the per-channel Message Mode is selected (BMM memory bit = HIGH), the lower byte of the BCM word (BCAB[7:0]) will be transmitted as data on the output stream (BSTo0-7) in place of data defined by the Source Control, Stream and Channel Address bits.

Bit	Name	Description
15	BSRC	**Backplane Source Control Bit** When LOW, the source is from the Local input port (Local Data Memory). When HIGH, the source is from the Backplane input port (Backplane Data Memory). Ignored when BMM is set HIGH.
14	BMM	**Backplane Message Mode Bit** When LOW, the channel is in Connection Mode (data to be output on channel originated in Backplane or Local Data Memory). When HIGH, the channel is in Message Mode (data to be output on channel originated in Backplane Connection Memory).

Bit	Name	Description
13	BE	**Backplane Output Enable Bit** When LOW, the channel may be high impedance, either at the device output, or set by an external buffer dependent upon the BORS pin. When HIGH, the channel is active.
12:9	BSAB[3:0]	**Source Stream Address Bits** The binary value of these 4 bits represents the input stream number. Ignored when BMM is set HIGH.
8:0	BCAB[8:0]	**Source Channel Address Bits / Message Mode Data** The binary value of these 9 bits represents the input channel number, when BMM is LOW. Bits BCAB[7:0] transmitted as data when BMM is set HIGH. Note: When BMM is set HIGH, in both ST-BUS and GCI-Bus modes, the BCAB[7:0] bits are output sequentially to the timeslot with BCAB[7] being output first.

Table 9 - BCM Bits for Source-to-Backplane Switching

12.0 Internal Register Mappings

When the most significant bit, A14, of the address bus is set to '0', the microprocessor is performing an access to one of the device's internal registers. Address bits A13-A0 indicate which particular register is being accessed.

A14-A0	Register
0000_H	Control Register, CR
0001_H	Block Programming Register, BPR
0023_H - $002A_H$	Local Input Bit Delay Register 0 - 7, LIDR0 - 7
0063_H - $006A_H$	Backplane Input Bit Delay Register 0 - 7, BIDR0 - 7
0083_H - $008A_H$	Local Output Advancement Register 0 - 7, LOAR0 - 7
$00A3_H$ - $00AA_H$	Backplane Output Advancement Register 0 - 7, BOAR0 - 7
$014D_H$	Memory BIST Register, MBISTR
$3FFF_H$	Device Identification Register, DIR

Table 10 - Address Map for Registers (A14 = 0)

13.0 Detailed Register Descriptions

This section describes the registers that are used in the device.

13.1 Control Register (CR)

Address 0000_H.

The Control Register defines which memory is to be accessed. It initiates the memory block programming mode and selects the Backplane and Local data rate modes. The Control Register (**CR**) is configured as follows:

Bit	Name	Reset Value	Description
15:13	FBD_ MODE[2:0]	0	**Frame Boundary Discriminator Mode** When set to 111_B, the Frame Boundary Discriminator can handle both low frequency and high frequency jitter. When set to 000_B, the Frame Boundary Discriminator is set to handle lower frequency jitter only. All other values are reserved. These bits are ignored when FBDEN bit is LOW.
12	SMPL_ MODE	0	**Sample Point Mode** When LOW the input bit sampling point is always at the 3/4 bit location. The input bit fractional delay is programmed in 1/4 bit increments from 0 to 7 3/4 as per the value of the LIDR0 to LIDR7 and BIDR0 to BIDR7 registers. When HIGH, the input bit sampling point is programmed to the 3/4, 4/4, 1/4, 2/4 bit location as per the value of the LIDR0 to LIDR7 and BIDR0 to BIDR7 registers. In addition the incoming data can be delayed by 0 to 7 bits in 1 bit increments. See Table 13, Table 14, Table 15 and Table 16 for details.
11	Reserved	0	**Reserved** Must be set to 0 for normal operation
10	FBDEN	0	**Frame Boundary Discriminator Enable** When LOW, the frame boundary discriminator function is disabled. When HIGH, enables frame boundary discriminator function which allows the device to tolerate inconsistent frame boundaries, hence improving the tolerance to cycle-to-cycle variation on the input clock.
9	Reserved	0	**Reserved** Must be set to 0 for normal operation
8	FPW	0	**Frame Pulse Width** When LOW, the user must apply a 122 ns frame pulse on $\overline{\text{FP8i}}$; the $\overline{\text{FP8o}}$ pin will output a 122 ns wide frame pulse; $\overline{\text{FP16o}}$ will output a 61 ns wide frame pulse. When HIGH, the user must apply a 244 ns frame pulse on $\overline{\text{FP8i}}$; the $\overline{\text{FP8o}}$ pin will output a 244 ns wide frame pulse; $\overline{\text{FP16o}}$ will output a 122 ns wide frame pulse.
7	Reserved	0	**Reserved** Must be set to 0 for normal operation
6	C8IPOL	0	**8 MHz Input Clock Polarity** The frame boundary is aligned to the falling or rising edge of the input clock. When LOW, the frame boundary is aligned to the clock falling edge. When HIGH, the frame boundary is aligned to the clock rising edge.
5	COPOL	0	**Output Clock Polarity** When LOW, the output clock has the same polarity as the input clock. When HIGH, the output clock is inverted. This applies to both the 8 MHz ($\overline{\text{C8o}}$) and 16 MHz ($\overline{\text{C16o}}$) output clocks.

Table 11 - Control Register Bits

<table>
<tr><th>Bit</th><th>Name</th><th>Reset Value</th><th>Description</th></tr>
<tr><td>4</td><td>MBP</td><td>0</td><td>Memory Block Programming
When LOW, the memory block programming mode is disabled.
When HIGH, the connection memory block programming mode is ready to program the Local Connection Memory (LCM) and the Backplane Connection Memory (BCM).</td></tr>
<tr><td>3</td><td>OSB</td><td>0</td><td>Output Stand By
This bit enables the BSTo0-7 and LSTo0-7 serial outputs.
<table><tr><th>ODE Pin</th><th>OSB bit</th><th>BSTo0-7, LSTo0-7</th></tr><tr><td>0</td><td>X</td><td>Disabled</td></tr><tr><td>1</td><td>0</td><td>Disabled</td></tr><tr><td>1</td><td>1</td><td>Enabled</td></tr></table>Output Control with ODE pin and OSB bit
When LOW, BSTo0-7 and LSTo0-7 are driven HIGH or high impedance, dependent on the BORS and LORS pin settings respectively.
When HIGH, BSTo0-7 and LSTo0-7 are enabled.</td></tr>
<tr><td>2</td><td>Reserved</td><td>0</td><td>Reserved
Must be set to 0 for normal operation</td></tr>
<tr><td>1:0</td><td>MS[1:0]</td><td>0</td><td>Memory Select Bits
These three bits select the connection or data memory for subsequent microport memory access operations:
00 selects Local Connection Memory (LCM) for read or write operations.
01 selects Backplane Connection Memory (BCM) for read or write operations.
10 selects Local Data Memory (LDM) for read-only operation.
11 selects Backplane Data Memory (BDM) for read-only operation.</td></tr>
</table>

Table 11 - Control Register Bits (continued)

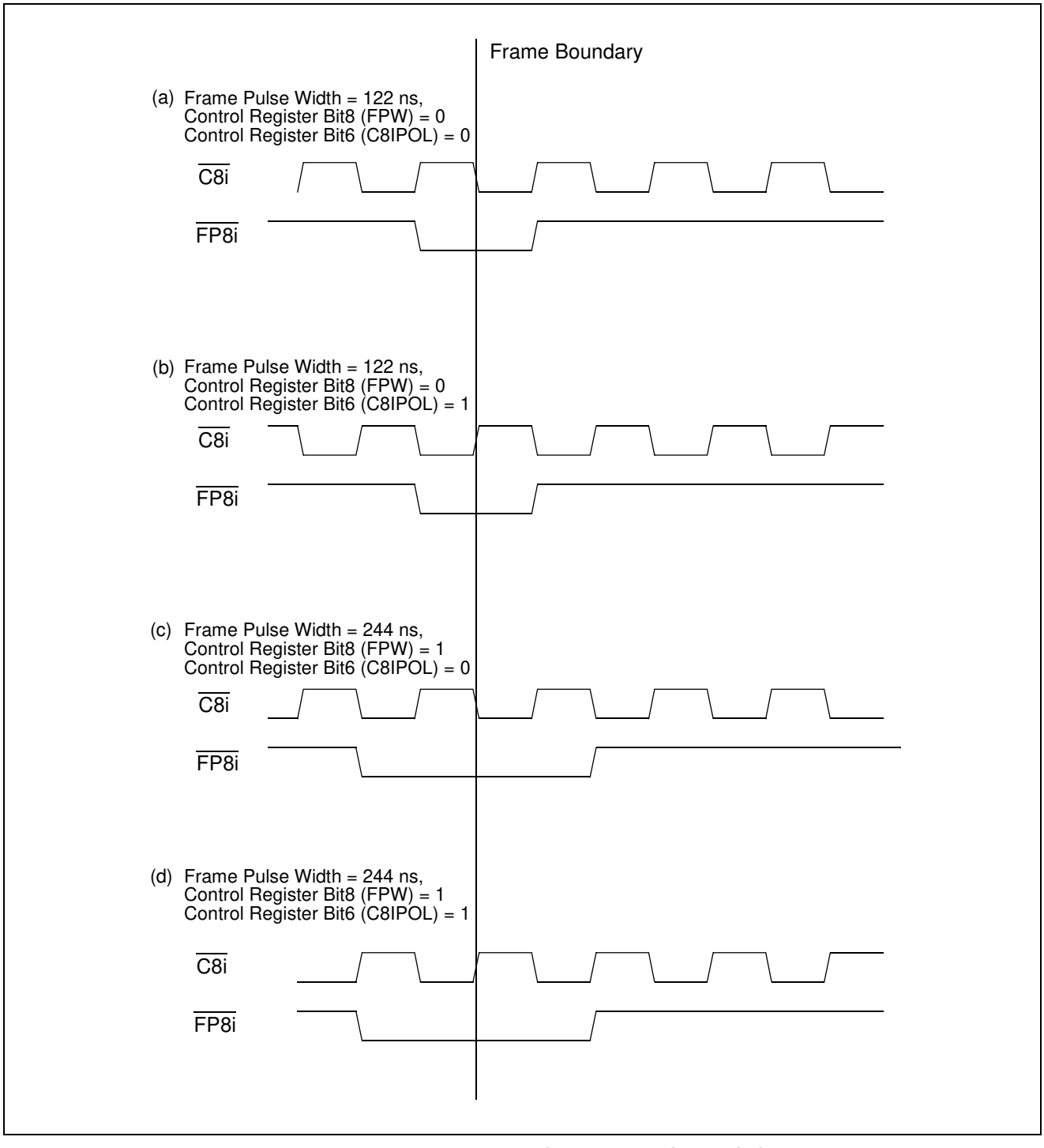


Figure 15 - Frame Boundary Conditions, ST-BUS Operation

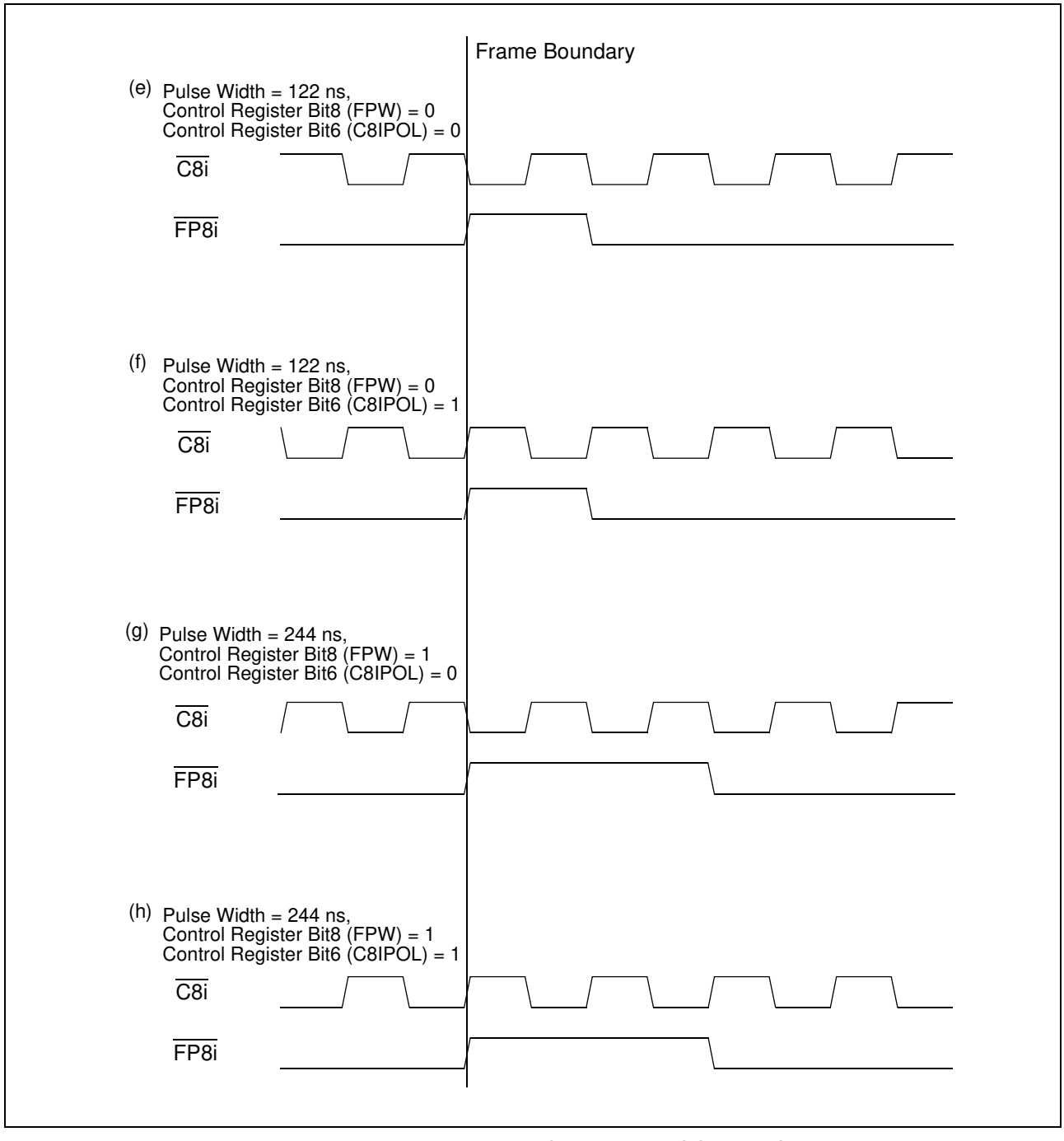


Figure 16 - Frame Boundary Conditions, GCI-Bus Operation

13.2 Block Programming Register (BPR)

Address 0001_H.

The Block Programming Register stores the bit patterns to be loaded into the connection memories when the Memory Block Programming feature is enabled. The BPE, LBPD[2:0] and BBPD[2:0] bits in the BPR register must be defined in the same write operation.

The BPE bit is set HIGH to commence the block programming operation. Programming is completed in one frame period and may be initiated at any time within a frame. The BPE bit returns to LOW to indicate that the block programming function has completed.

When BPE is HIGH, no other bits of the BPR register may be changed for at least a single frame period, except to abort the programming operation. The programming operation may be aborted by setting either BPE to LOW, or the Control Register bit, MBP, to LOW.

The **BPR** register is configured as follows.

Bit	Name	Reset Value	Description
15:7	Reserved	0	**Reserved** Must be set to 0 for normal operation
6:4	BBPD[2:0]	0	**Backplane Block Programming Data** These bits refer to the value loaded into the Backplane Connection Memory (BCM) when the Memory Block Programming feature is activated. When the MBP bit in the Control Register (CR) is set HIGH and BPE (in this register) is set HIGH, the contents of bits BBPD[2:0] are loaded into bits 15-13, respectively, of the BCM. Bits 12-0 of the BCM are set LOW.
3:1	LBPD[2:0]	0	**Local Block Programming Data** These bits refer to the value loaded into the Local Connection Memory (LCM), when the Memory Block Programming feature is activated. When the MBP bit in the Control Register is set HIGH and BPE (in this register) is set HIGH, the contents of bits LBPD[2:0] are loaded into bits 15-13, respectively, of the LCM. Bits 12-0 of the LCM are set LOW.
0	BPE	0	**Block Programming Enable** A LOW to HIGH transition of this bit enables the Memory Block Programming function. A LOW will be returned after 125 µs, upon completion of programming. Set LOW to abort the programming operation.

Table 12 - Block Programming Register Bits

13.3 Local Input Bit Delay Registers (LIDR0 to LIDR7)

Addresses 0023_H to $002A_H$.

There are 8 Local Input Delay Registers (LIDR0 to LIDR7).

When the SMPL_MODE bit in the Control Register is LOW, the input data sampling point defaults to the 3/4 bit location and LIDR0 to LIDR7 define the input bit and fractional bit delay of each Local stream. The possible bit delay adjustment is up to 7 3/4 bits, in steps of 1/4 bit.

When the SMPL_MODE bit is HIGH, LIDR0 to LIDR7 define the input bit sampling point as well as the integer bit delay of each Local stream. The input bit sampling point can be adjusted in 1/4 bit increments. The bit delay can be adjusted in 1-bit increments from 0 to 7 bits.

The **LIDR0 to LIDR7** registers are configured as follows:

LIDRn Bit (where n = 0 to 7)	**Name**	**Reset Value**	**Description**
15:5	Reserved	0	**Reserved** Must be set to 0 for normal operation
4:0	LID[4:0]	0	**Local Input Bit Delay Register** When SMPL_MODE = LOW, the binary value of these bits refers to the input bit and fractional bit delay value (0 to 7 3/4). When SMPL_MODE = HIGH, the binary value of LID[1:0] refers to the input bit sampling point (1/4 to 4/4). LID[4:2] refers to the integer bit delay value (0 to 7 bits).

Table 13 - Local Input Bit Delay Register (LIDRn) Bits

13.3.1 Local Input Delay Bits 4-0 (LID[4:0])

When SMPL_MODE = LOW, these five bits define the amount of input bit delay adjustment that the receiver uses to sample each input. Input bit delay adjustment can range up to 7 3/4 bit periods forward, with resolution of 1/4 bit period. The default sampling point is at the 3/4 bit location.

This can be described as: **no. of bits delay = LID[4:0] / 4**
For example, if LID[4:0] is set to 10011 (19), the input bit delay = $19 * {}^1/_4 = 4{}^3/_4$.

When SMPL_MODE = HIGH, the binary value of LID[1:0] refers to the input bit sampling point (1/4 to 4/4). LID[4:2] refers to the integer bit delay value (0 to 7 bits). This means that bits can be delayed by an integer value of up to 7 and that the sampling point can vary from 1/4 to 4/4 in 1/4 bit increments.

Table 14 illustrates the bit delay and sampling point selection.

LIDn					SMPL_MODE = LOW	SMPL_MODE = HIGH	
LID4	LID3	LID2	LID1	LID0	Input Data Bit Delay	Input Data Bit Delay	Input Data Sampling Point
0	0	0	0	0	0 (Default)	0 (Default)	3/4
0	0	0	0	1	1/4	0	4/4
0	0	0	1	0	1/2	0	1/4
0	0	0	1	1	3/4	0	2/4
0	0	1	0	0	1	1	3/4
0	0	1	0	1	1 1/4	1	4/4
0	0	1	1	0	1 1/2	1	1/4
0	0	1	1	1	1 3/4	1	2/4
0	1	0	0	0	2	2	3/4
0	1	0	0	1	2 1/4	2	4/4
0	1	0	1	0	2 1/2	2	1/4
0	1	0	1	1	2 3/4	2	2/4
0	1	1	0	0	3	3	3/4
0	1	1	0	1	3 1/4	3	4/4
0	1	1	1	0	3 1/2	3	1/4
0	1	1	1	1	3 3/4	3	2/4
1	0	0	0	0	4	4	3/4
1	0	0	0	1	4 1/4	4	4/4
1	0	0	1	0	4 1/2	4	1/4
1	0	0	1	1	4 3/4	4	2/4
1	0	1	0	0	5	5	3/4
1	0	1	0	1	5 1/4	5	4/4
1	0	1	1	0	5 1/2	5	1/4
1	0	1	1	1	5 3/4	5	2/4
1	1	0	0	0	6	6	3/4
1	1	0	0	1	6 1/4	6	4/4
1	1	0	1	0	6 1/2	6	1/4
1	1	0	1	1	6 3/4	6	2/4
1	1	1	0	0	7	7	3/4
1	1	1	0	1	7 1/4	7	4/4
1	1	1	1	0	7 1/2	7	1/4
1	1	1	1	1	7 3/4	7	2/4

Table 14 - Local Input Bit Delay and Sampling Point Programming Table

13.4 Backplane Input Bit Delay Registers (BIDR0 to BIDR7)

Addresses 0063_H to $006A_H$

There are 8 Backplane Input Delay Registers (BIDR0 to BIDR7).

When the SMPL_MODE bit in the Control Register is LOW, the input data sampling point defaults to the 3/4 bit location and BIDR0 to BIDR7 define the input bit and fractional bit delay of each Backplane stream. The possible bit delay adjustment is up to 7 3/4 bits, in steps of 1/4 bit.

When the SMPL_MODE bit is HIGH, BIDR0 to BIDR7 define the input bit sampling point as well as the integer bit delay of each Backplane stream. The input bit sampling point can be adjusted in 1/4 bit increments. The bit delay can be adjusted in 1-bit increments from 0 to 7 bits.

The **BIDR0 to BIDR7** registers are configured as follows:

BIDRn Bit (where n = 0 to 7)	**Name**	**Reset Value**	**Description**
15:5	Reserved	0	**Reserved** Must be set to 0 for normal operation
4:0	BID[4:0]	0	**Backplane Input Bit Delay Register** When SMPL_MODE = LOW, the binary value of these bits refers to the input bit fractional delay value (0 to 7 3/4). When SMPL_MODE = HIGH, the binary value of BID[1:0] refers to the input bit sampling point (1/4 to 4/4). BID[4:2] refers to the integer bit delay value (0 to 7 bits).

Table 15 - Backplane Input Bit Delay Register (BIDRn) Bits

13.4.1 Backplane Input Delay Bits 4-0 (BID[4:0])

When SMPL_MODE = LOW, these five bits define the amount of input bit delay adjustment that the receiver uses to sample each input. Input bit delay adjustment can range up to 7 3/4 bit periods forward, with resolution of 1/4 bit period. The default sampling point is at the 3/4 bit location.

This can be described as: **no. of bits delay = BID[4:0] / 4**

For example, if BID[4:0] is set to 10011 (19), the input bit delay = $19 * {}^{1}/_{4} = 4{}^{3}/_{4}$.

When SMPL_MODE = HIGH, the binary value of BID[1:0] refers to the input bit sampling point (1/4 to 4/4). BID[4:2] refers to the integer bit delay value (0 to 7 bits). This means that bits can be delayed by an integer value of up to 7 and that the sampling point can vary from 1/4 to 4/4 in 1/4 bit increments.

Table 16 illustrates the bit delay and sampling point selection.

BIDn					SMPL_MODE = LOW	SMPL_MODE = HIGH	
BID4	**BID3**	**BID2**	**BID1**	**BID0**	**Input Data Bit Delay**	**Input Data Bit Delay**	**Input Data Sampling Point**
0	0	0	0	0	0 (Default)	0 (Default)	3/4
0	0	0	0	1	1/4	0	4/4
0	0	0	1	0	1/2	0	1/4
0	0	0	1	1	3/4	0	2/4
0	0	1	0	0	1	1	3/4
0	0	1	0	1	1 1/4	1	4/4
0	0	1	1	0	1 1/2	1	1/4
0	0	1	1	1	1 3/4	1	2/4
0	1	0	0	0	2	2	3/4
0	1	0	0	1	2 1/4	2	4/4
0	1	0	1	0	2 1/2	2	1/4
0	1	0	1	1	2 3/4	2	2/4
0	1	1	0	0	3	3	3/4
0	1	1	0	1	3 1/4	3	4/4
0	1	1	1	0	3 1/2	3	1/4
0	1	1	1	1	3 3/4	3	2/4
1	0	0	0	0	4	4	3/4
1	0	0	0	1	4 1/4	4	4/4
1	0	0	1	0	4 1/2	4	1/4
1	0	0	1	1	4 3/4	4	2/4
1	0	1	0	0	5	5	3/4
1	0	1	0	1	5 1/4	5	4/4
1	0	1	1	0	5 1/2	5	1/4
1	0	1	1	1	5 3/4	5	2/4
1	1	0	0	0	6	6	3/4
1	1	0	0	1	6 1/4	6	4/4
1	1	0	1	0	6 1/2	6	1/4
1	1	0	1	1	6 3/4	6	2/4
1	1	1	0	0	7	7	3/4
1	1	1	0	1	7 1/4	7	4/4
1	1	1	1	0	7 1/2	7	1/4
1	1	1	1	1	7 3/4	7	2/4

Table 16 - Backplane Input Bit Delay and Sampling Point Programming Table

13.5 Local Output Advancement Registers (LOAR0 to LOAR7)

Addresses 0083_H to $008A_H$.

8 Local Output Advancement Registers (LOAR0 to LOAR7) allow users to program the output advancement for output data streams LSTo0 to LSTo7. The possible adjustment is -1 (7.6 ns), -2 (15 ns) or -3 (23 ns) cycles of the internal system clock (131.072 MHz).

The **LOAR0** to **LOAR7** registers are configured as follows:

LOARn Bit (where n = 0 to 7)	**Name**	**Reset Value**	**Description**
15:2	Reserved	0	**Reserved** Must be set to 0 for normal operation
1:0	LOA[1:0]	0	**Local Output Advancement Value**

Table 17 - Local Output Advancement Register (LOAR) Bits

13.5.1 Local Output Advancement Bits 1-0 (LOA1-LOA0)

The binary value of these two bits indicates the amount of offset that a particular stream output can be advanced with respect to the output frame boundary. When the advancement is 0, the serial output stream has the normal alignment with the generated frame pulse $\overline{FP8o}$.

Local Output Advancement	**Corresponding Advancement Bits**	
Clock Rate 131.072 MHz	**LOA1**	**LOA0**
0 (Default)	0	0
-1 cycle (~7.6 ns)	0	1
-2 cycles (~15 ns)	1	0
-3 cycles (~23 ns)	1	1

Table 18 - Local Output Advancement (LOAR) Programming Table

13.6 Backplane Output Advancement Registers (BOAR0 - BOAR7)

Addresses $00A3_H$ to $00AA_H$

8 Backplane Output Advancement Registers (BOAR0 to BOAR7) allow users to program the output advancement for output data streams BSTo0 to BSTo7. The possible adjustment is -1 (7.6 ns), -2 (15 ns) or -3 (23 ns) cycles of the internal system clock (131.072 MHz).

The **BOAR0** to **BOAR7** registers are configured as follows:

BOARn Bit (where n = 0 to 7)	**Name**	**Reset Value**	**Description**
15:2	Reserved	0	**Reserved** Must be set to 0 for normal operation
1:0	BOA[1:0]	0	**Backplane Output Advancement Value**

Table 19 - Backplane Output Advancement Register (BOAR) Bits

13.6.1 Backplane Output Advancement Bits 1-0 (BOA1-BOA0)

The binary value of these two bits indicates the amount of offset that a particular stream output can be advanced with respect to the output frame boundary. When the advancement is 0, the serial output stream has the normal alignment with the generated frame pulse $\overline{FP8o}$.

Backplane Output Advancement	**Corresponding Advancement Bits**	
Clock Rate 131.072 MHz	**BOA1**	**BOA0**
0 (Default)	0	0
-1 cycle (~7.6 ns)	0	1
-2 cycles (~15 ns)	1	0
-3 cycles (~23 ns)	1	1

Table 20 - Backplane Output Advancement (BOAR) Programming Table

13.7 Memory BIST Register

Address $014D_H$.

The Memory BIST Register enables the self-test of chip memory. Two consecutive write operations are required to start MBIST: the first with only bit 12 (LV_TM) set HIGH (i.e. 1000h); the second with bit 12 maintained HIGH but with the required start bit(s) also set HIGH.

The **MBISTR** register is configured as follows:

Bit	Name	Reset Value	Description
15:13	Reserved	0	**Reserved** Must be set to 0 for normal operation
12	LV_TM	0	**MBIST Test Enable** Set HIGH to enable MBIST mode. Set LOW for normal operation.
11	BISTSDB	0	**Backplane Data Memory Start BIST Sequence** Sequence enabled on LOW to HIGH transition.
10	BISTCDB	0	**Backplane Data Memory BIST Sequence Completed (Read-only)** This bit must be polled - when HIGH, indicates completion of Backplane Data Memory BIST sequence.
9	BISTPDB	0	**Backplane Data Memory Pass/Fail Bit (Read-only)** This bit indicates the Pass/Fail status following completion of the Backplane Data Memory BIST sequence (indicated by assertion of BISTCDB). A HIGH indicates Pass, a LOW indicates Fail.
8	BISTSDL	0	**Local Data Memory Start BIST Sequence** Sequence enabled on LOW to HIGH transition.
7	BISTCDL	0	**Local Data Memory BIST Sequence Completed (Read-only)** This bit must be polled - when HIGH, indicates completion of Local Data Memory BIST sequence.
6	BISTPDL	0	**Local Data Memory Pass/Fail Bit (Read-only)** This bit indicates the Pass/Fail status following completion of the Local Data Memory BIST sequence (indicated by assertion of BISTCDL). A HIGH indicates Pass, a LOW indicates Fail.
5	BISTSCB	0	**Backplane Connection Memory Start BIST Sequence** Sequence enabled on LOW to HIGH transition.
4	BISTCCB	0	**Backplane Connection Memory BIST Sequence Completed (Read-only)** This bit must be polled - when HIGH, indicates completion of Backplane Connection Memory BIST sequence.
3	BISTPCB	0	**Backplane Connection Memory Pass/Fail Bit (Read-only)** This bit indicates the Pass/Fail status following completion of the Backplane Connection Memory BIST sequence (indicated by assertion of BISTCCB). A HIGH indicates Pass, a LOW indicates Fail.

Table 21 - Memory BIST Register (MBISTR) Bits

Bit	Name	Reset Value	Description
2	BISTSCL	0	**Local Connection Memory Start BIST Sequence** Sequence enabled on LOW to HIGH transition.
1	BISTCCL	0	**Local Connection Memory BIST Sequence Completed (Read-only)** This bit must be polled - when HIGH, indicates completion of Local Connection Memory BIST sequence.
0	BISTPCL	0	**Local Connection Memory Pass/Fail Bit (Read-only)** This bit indicates the Pass/Fail status following completion of the Local Connection Memory BIST sequence (indicated by assertion of BISTCCL). A HIGH indicates Pass, a LOW indicates Fail.

Table 21 - Memory BIST Register (MBISTR) Bits (continued)

13.8 Device Identification Register

Address $3FFF_H$.

The Device Identification Register stores the binary value of the silicon revision number and the Device ID. This register is read-only. The **DIR** register is configured as follows:

Bit	Name	Reset Value	Description
15:8	Reserved	0	**Reserved** Will be set to 0 in normal operation
7:4	RC[3:0]	0000	**Revision Control Bits**
3	Reserved	0	**Reserved** Will be set to 0 in normal operation
2:0	DID[2:0]	101	**Device ID**

Table 22 - Device Identification Register (DIR) Bits

14.0 DC Electrical Characteristics

Absolute Maximum Ratings*

	Parameter	Symbol	Min.	Max.	Units
1	Core Supply Voltage	V_{DD_CORE}	-0.5	2.5	V
2	I/O Supply Voltage	V_{DD_IO}	-0.5	5.0	V
3	PLL Supply Voltage	V_{DD_PLL}	-0.5	2.5	V
4	Input Voltage (non-5 V tolerant inputs)	V_I	-0.5	V_{DD_IO} +0.5	V
5	Input Voltage (5 V tolerant inputs)	V_{I_5V}	-0.5	7.0	V
6	Continuous Current at digital outputs	I_o		15	mA
7	Package power dissipation	P_D		1.5	W
8	Storage temperature	T_S	- 55	+125	°C

* Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions

	Characteristics	Sym.	Min.	Typ.	Max.	Units
1	Operating Temperature	T_{OP}	-40	25	+85	°C
2	Positive Supply	V_{DD_IO}	3.0	3.3	3.6	V
3	Positive Supply	V_{DD_CORE}	1.71	1.8	1.89	V
4	Positive Supply	V_{DD_PLL}	1.71	1.8	1.89	V
5	Input Voltage	V_I	0		V_{DD_IO}	V
6	Input Voltage on 5 V Tolerant Inputs	V_{I_5V}	0		5.5	V

Voltages are with respect to ground (V_{SS}) unless otherwise stated.

DC Electrical Parameters

		Characteristics	Sym.	Min.	Typ.	Max.	Units.	Test Conditions
1a	I N P U T S	Supply Current	I_{DD_Core}			4	mA	Static I_{DD_Core} and PLL current
1b		Supply Current	I_{DD_Core}		240	290	mA	Applied clock C8i = 8.192 MHz
1c		Supply Current	I_{DD_IO}			100	µA	Static I_{DD_IO}
1d		Supply Current	I_{DD_IO}		14	18	mA	I_{AV} with all output streams at max. data rate unloaded
2		Input High Voltage	V_{IH}	2.0			V	
3		Input Low Voltage	V_{IL}			0.8	V	
4		Input Leakage (input pins) Input Leakage (bi-directional pins)	I_{IL} I_{BL}			5 5	µA µA	$0 < V < V_{DD\_IO}$ Note 1
		Weak Pullup Current	I_{PU}			200	µA	Input at 0 V
5		Weak Pulldown Current	I_{PD}			200	µA	Input at V_{DD_IO}
6		Input Pin Capacitance	C_I			5	pF	
7	O U T P U T S	Output High Voltage	V_{OH}	2.4			V	I_{OH} = 8 mA
8		Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 8 mA
9		High-Impedance Leakage	I_{OZ}			5	µA	$0 \le V_0 \le V_{DD\_IO}$ Note 1
10		Output Pin Capacitance	C_O			5	pF	

Voltages are with respect to ground (V_{ss}) unless otherwise stated.
Note 1: Maximum leakage on pins (output or I/O pins in high impedance state) is over an applied voltage (V).

15.0 AC Electrical Characteristics

AC Electrical Characteristics Timing Parameter Measurement: Voltage Levels

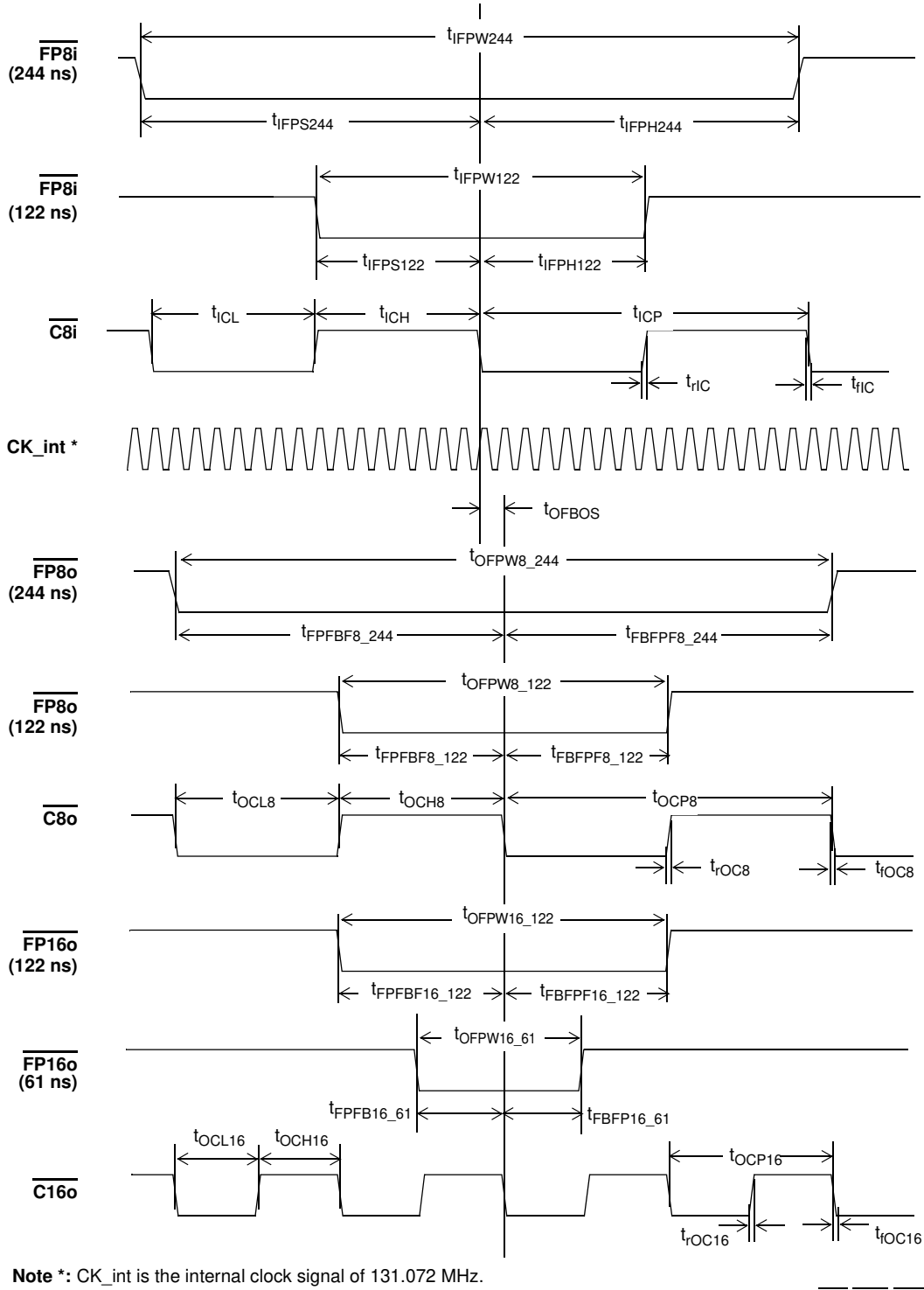
	Characteristics	Sym.	Level	Units	Conditions
1	CMOS Threshold	V_{CT}	0.5 V_{DD_IO}	V	3.0 V ≤ V_{DD_IO} ≤ 3.6 V
2	Rise/Fall Threshold Voltage High	V_{HM}	0.7 V_{DD_IO}	V	3.0 V ≤ V_{DD_IO} ≤ 3.6 V
3	Rise/Fall Threshold Voltage Low	V_{LM}	0.3 V_{DD_IO}	V	3.0 V ≤ V_{DD_IO} ≤ 3.6 V

Input and Output Clock Timing

	Characteristic	Sym.	Min.	Typ.	Max.	Units	Notes
1	$\overline{FP8i}$, Input Frame Pulse Width	$t_{IFPW244}$ $t_{IFPW122}$	210 10	244 122	350 220	ns	
2	Input Frame Pulse Setup Time (before $\overline{C8i}$ clock falling/rising edge)	$t_{IFPS244}$ $t_{IfPS122}$	5 5		110 60	ns	
3	Input Frame Pulse Hold Time (from $\overline{C8i}$ clock falling/rising edge)	$t_{IFPH244}$ $t_{IFPH122}$	0 0		110 60	ns	
4	$\overline{C8i}$ Clock Period (Average value, does not consider the effects of jitter)	t_{ICP}	120	122	124	ns	
5	$\overline{C8i}$ Clock Pulse Width High	t_{ICH}	50	61	70	ns	
6	$\overline{C8i}$ Clock Pulse Width Low	t_{ICL}	50	61	70	ns	
7	$\overline{C8i}$ Clock Rise/Fall Time	t_{rIC}, t_{fIC}	0	2	3	ns	
8	$\overline{C8i}$ Cycle to Cycle Variation (This values is with respect to the typical $\overline{C8i}$ Clock Period, and using mid-bit sampling)	t_{CCVIC}	-7.0		7.0	ns	
9	Output Frame Boundary Offset	t_{OFBOS}		7	9.5	ns	
10	$\overline{FP8o}$ Frame Pulse Width	t_{OFPW8_244} t_{OFPW8_122}	224 117	244 122	264 127	ns	FPW = 1 FPW = 0 C_L = 60 pF
11	$\overline{FP8o}$ Output Delay (from frame pulse edge to output frame boundary)	t_{FPFBF8_244} t_{FPFBF8_122}	117 58	122 61	127 64	ns	FPW = 1 FPW = 0 C_L = 60 pF
12	$\overline{FP8o}$ Output Delay (from output frame boundary to frame pulse edge)	t_{FBFPF8_244} t_{FBFPF8_122}	117 58	122 61	127 64	ns	FPW = 1 FPW = 0 C_L = 60 pF
13	$\overline{C8o}$ Clock Period	t_{OCP8}	117	122	127	ns	C_L = 60 pF
14	$\overline{C8o}$ Clock Pulse Width High	t_{OCH8}	58	61	64	ns	
15	$\overline{C8o}$ Clock Pulse Width Low	t_{OCL8}	58	61	64	ns	
16	$\overline{C8o}$ Clock Rise/Fall Time	t_{rOC8}, t_{fOC8}	3		7	ns	

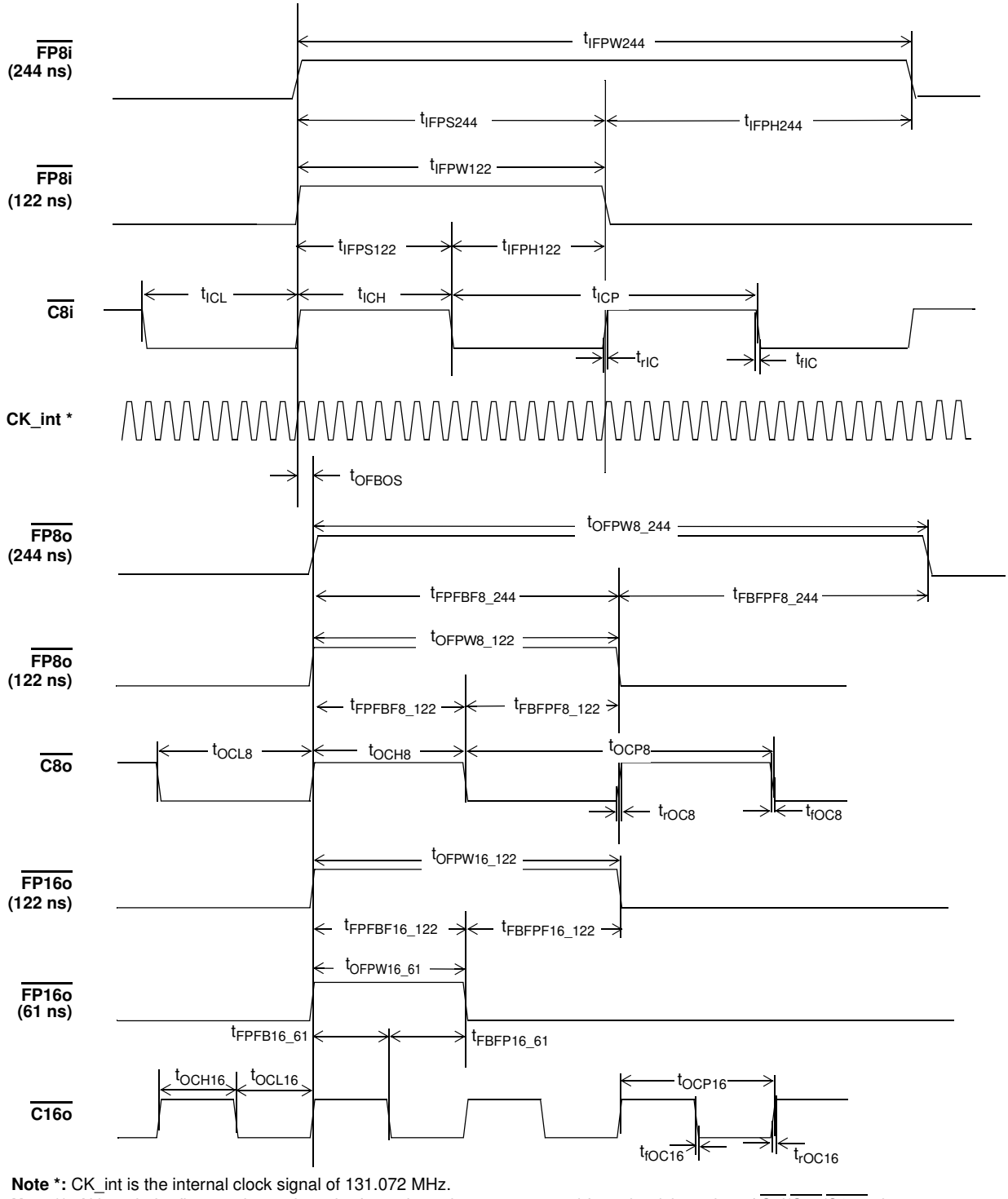
Input and Output Clock Timing (continued)

	Characteristic	Sym.	Min.	Typ.	Max.	Units	Notes
17	$\overline{\text{FP16o}}$ Frame Pulse Width	t_{OFPW16_122} t_{OFPW16_61}	117 58	122 61	127 64	ns	FPW = 1 FPW = 0 C_L = 60 pF
18	$\overline{\text{FP16o}}$ Output Delay (from frame pulse edge to output frame boundary)	$t_{FPFBF16\_122}$ $t_{FPFBF16\_61}$	58 29	61 31	64 33	ns	FPW = 1 FPW = 0
19	$\overline{\text{FP16o}}$ Output Delay (from output frame boundary to frame pulse edge)	$t_{FBFPF16\_122}$ $t_{FBFPF16\_61}$	58 29	61 31	64 33	ns	FPW = 1 FPW = 0
20	$\overline{\text{C16o}}$ Clock Period	t_{OCP16}	58	61	64	ns	C_L= 60 pF
21	$\overline{\text{C16o}}$ Clock Pulse Width High	t_{OCH16}	29	31	33	ns	
22	$\overline{\text{C16o}}$ Clock Pulse Width Low	t_{OCL16}	29	31	33	ns	
23	$\overline{\text{C16o}}$ Clock Rise/Fall Time	t_{rOC16}, t_{fOC16}	3		7	ns	



Note *: CK_int is the internal clock signal of 131.072 MHz.
Note **: Although the figures above show the frame boundary as measured from the falling edge of $\overline{C8i}$/$\overline{C8o}$/$\overline{C16o}$, the frame-controlling edge of $\overline{C8i}$/$\overline{C8o}$/$\overline{C16o}$ may be the rising edge, as configured via the C8iPOL and COPOL bits of the Control Register.

Figure 17 - Input and Output Clock Timing Diagram for ST-BUS

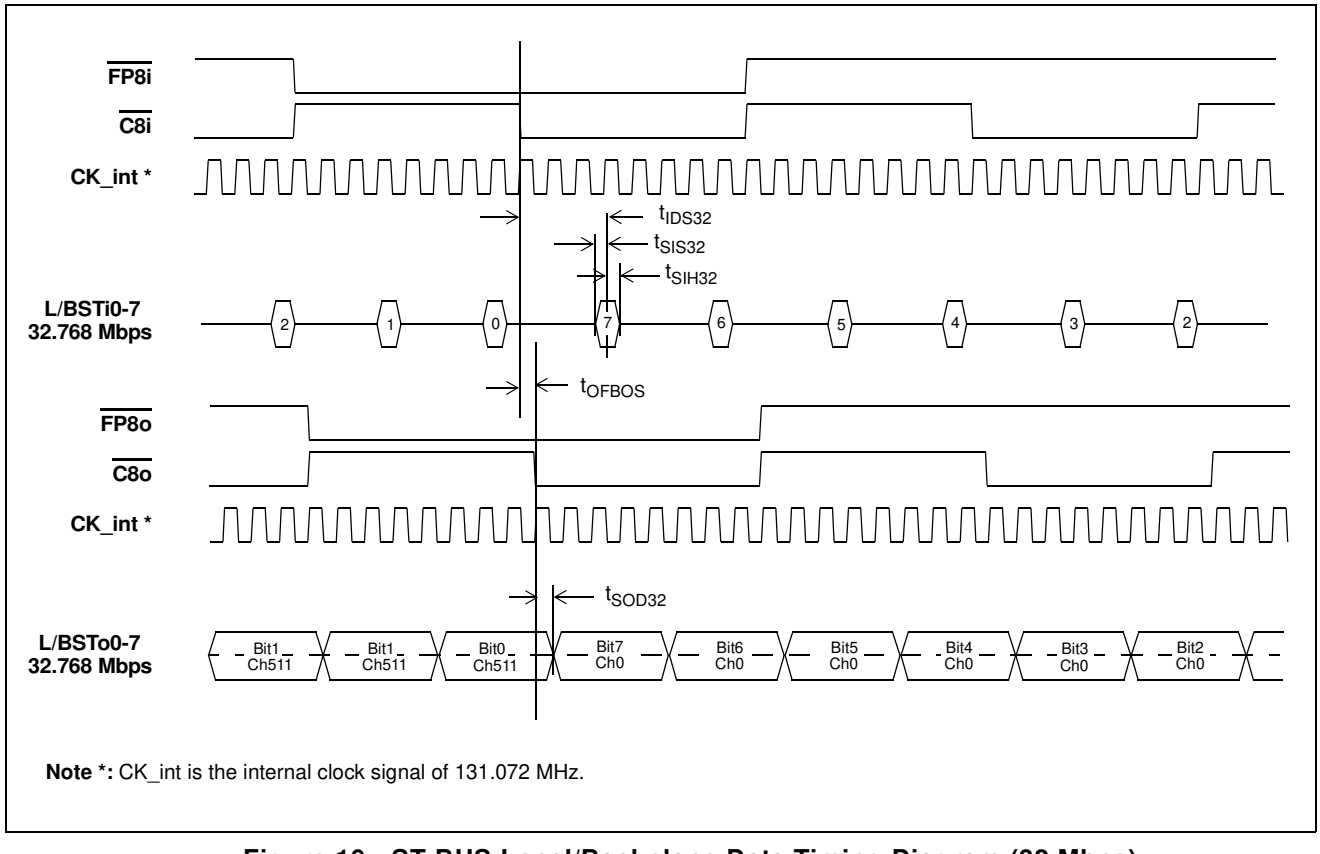


Note *: CK_int is the internal clock signal of 131.072 MHz.
Note **: Although the figures above show the frame boundary as measured from the rising edge of $\overline{C8i}$/$\overline{C8o}$/$\overline{C16o}$, the frame-controlling edge of $\overline{C8i}$/$\overline{C8o}$/$\overline{C16o}$ may be the rising edge, as configured via the C8iPOL and COPOL bits of the Control Register.

Figure 18 - Input and Output Clock Timing Diagram for GCI-Bus

Local and Backplane Data Timing

	Characteristic	Sym.	Min.	Typ.	Max.	Units	Notes
1	Local/Backplane Input Data Sampling Point	t_{IDS32}	20	23	26	ns	With SMPL_MODE = 0 (3/4-bit sampling) and zero offset.
2	Local/Backplane Serial Input Set-up Time	t_{SIS32}	2			ns	With respect to **Min**. Input Data Sampling Point
3	Local/Backplane Serial Input Hold Time	t_{SIH32}	2			ns	With respect to **Max**. Input Data Sampling Point
4	Output Frame Boundary Offset	t_{OFBOS}		7	9.5	ns	
5	Local/Backplane Serial Output Delay	t_{SOD32}			4.5	ns	C_L= 50 pF These numbers are referencing output frame boundary.



Note *: CK_int is the internal clock signal of 131.072 MHz.

Figure 19 - ST-BUS Local/Backplane Data Timing Diagram (32 Mbps)

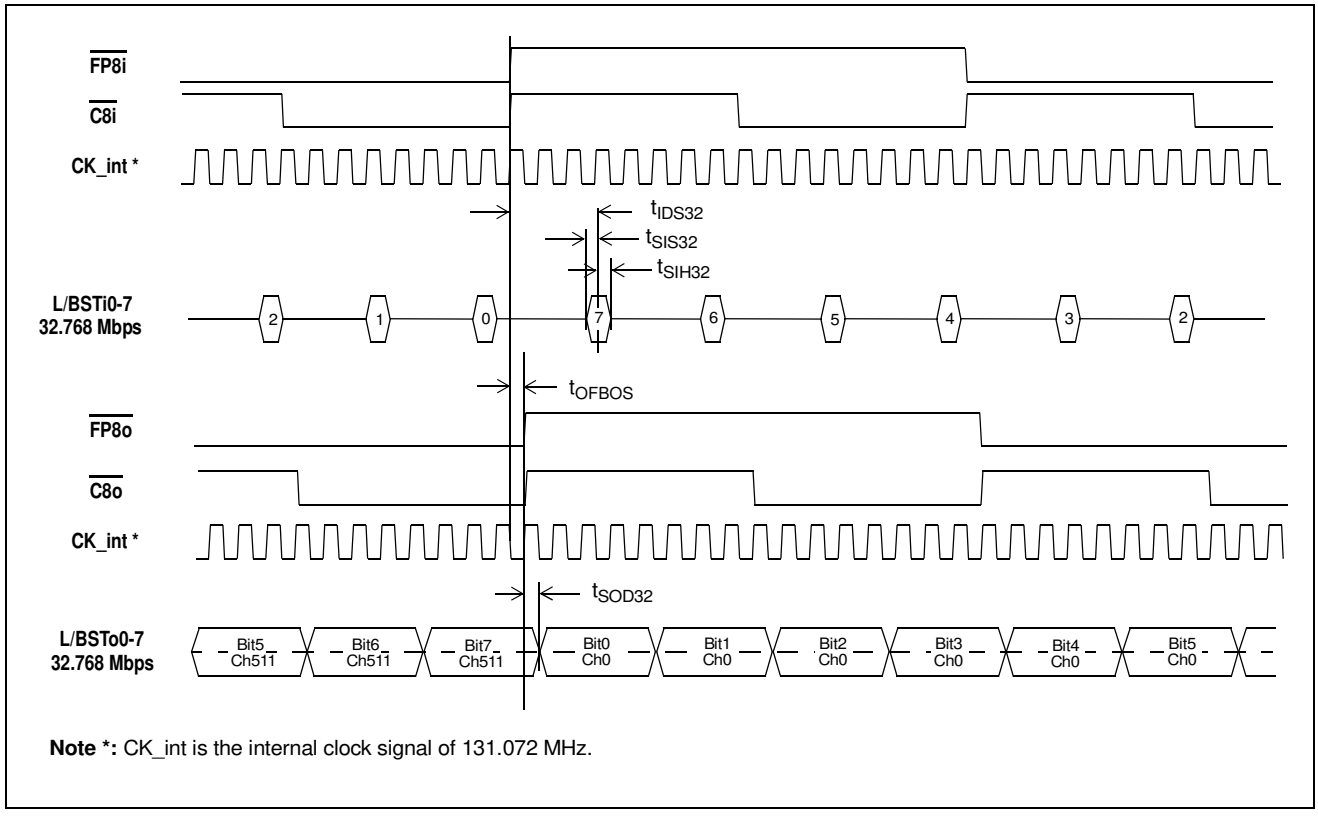


Figure 20 - GCI-Bus Local/Backplane Data Timing Diagram (32 Mbps)

Local and Backplane Output High-Impedance Timing

	Characteristic	Sym.	Min.	Typ.	Max.	Units	Test Conditions
1	STo delay - Active to High-Z - High-Z to Active	t_{DZ} t_{ZD}		4 4	6 6	ns ns	R_L = 1k, C_L = 50 pF, See Note 1
2	Output Driver Enable (ODE) Delay to Active Data Output Driver Enable (ODE) Delay to High-Impedance	t_{ODE} t_{ODZ}			14 14	ns ns	R_L = 1 k, C_L = 50 pF, See Note 1 R_L 1 k, C_L = 50 pF, See Note 1

Note 1: High Impedance is measured by pulling to the appropriate rail with R_L, with timing corrected to cancel time taken to discharge C_L.

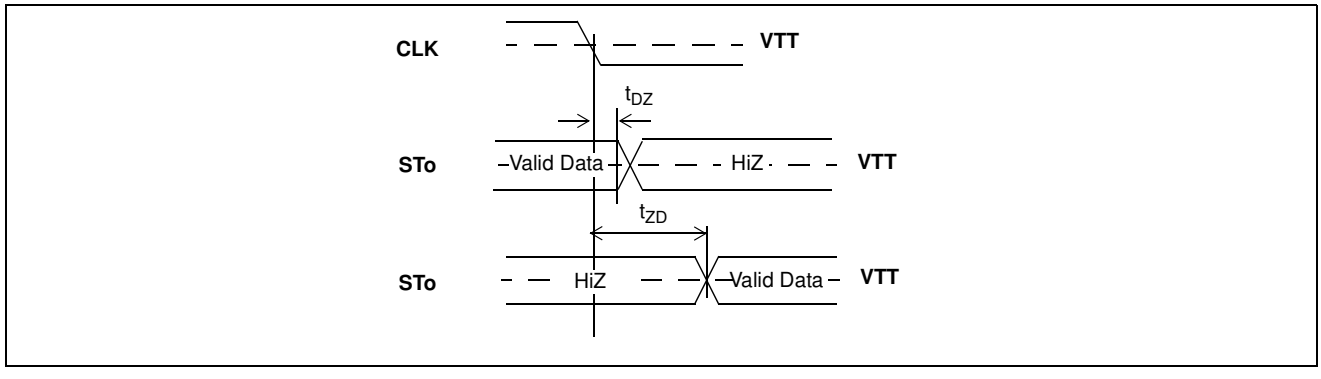


Figure 21 - Serial Output and External Control

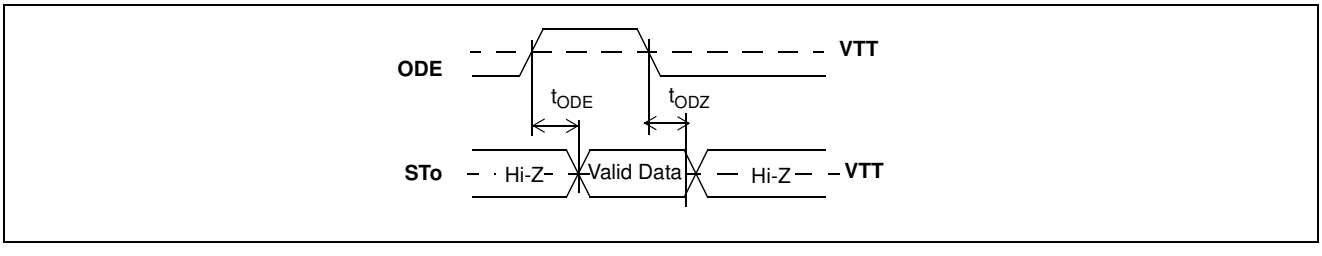


Figure 22 - Output Driver Enable (ODE)

Input Clock Jitter Tolerance

	Jitter Frequency	32.768 Mbps Data Rate Jitter Tolerance	Units
1	1 kHz	600	ns
2	10 kHz	600	ns
3	50 kHz	80	ns
4	66 kHz	50	ns
5	83 kHz	35	ns
6	95 kHz	30	ns
7	100 kHz	20	ns
8	200 kHz	14	ns
9	300 kHz	14	ns
10	400 kHz	14	ns
11	500 kHz	14	ns
12	1 MHz	14	ns
13	2 MHz	14	ns
14	4 MHz	14	ns

Non-Multiplexed Microprocessor Port Timing

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Test Conditions
1	$\overline{CS}$ setup from $\overline{DS}$ falling	t_{CSS}	0			ns	
2	R/$\overline{W}$ setup from $\overline{DS}$ falling	t_{RWS}	9			ns	
3	Address setup from $\overline{DS}$ falling	t_{ADS}	9			ns	
4	$\overline{CS}$ hold after $\overline{DS}$ rising	t_{CSH}	0			ns	
5	R/$\overline{W}$ hold after $\overline{DS}$ rising	t_{RWH}	9			ns	
6	Address hold after $\overline{DS}$ rising	t_{ADH}	9			ns	
7	Data setup from $\overline{DTA}$ Low on Read	t_{RDS}	5 12			ns ns	Memory Read Register Read C_L = 60 pF
8	Data hold on read	t_{RDH}			4.5	ns	C_L = 60 pF, R_L = 1 k Note 1
9	Data setup on write	t_{WDS}	9			ns	
10	Data hold on write	t_{WDH}	9			ns	
11	Acknowledgment Delay: Reading/Writing Registers Reading/Writing Memory	t_{AKD}			 88 80	 ns ns	 C_L = 60 pF C_L = 60 pF
12	Acknowledgment Hold Time	t_{AKH}			11	ns	C_L= 60 pF, R_L = 1 k, Note 1

Note 1: High Impedance is measured by pulling to the appropriate rail with R_L, with timing corrected to cancel time taken to discharge C_L.

Note 2: There must be a minimum of 30 ns between CPU accesses, to allow the device to recognize the accesses as separate (i.e., a minimum of 30 ns must separate the de-assertion of $\overline{DTA}$ (to high) and the assertion of $\overline{CS}$ and/or $\overline{DS}$ to initiate the next access).

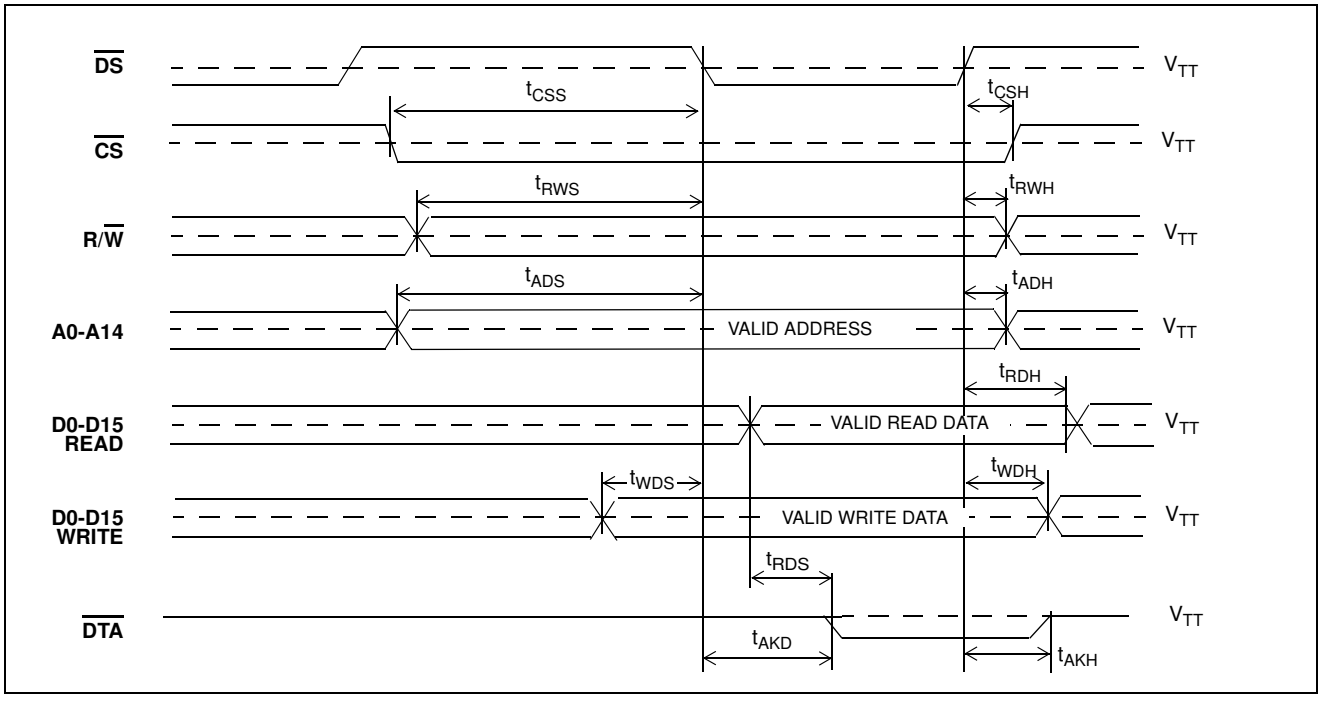


Figure 23 - Motorola Non-Multiplexed Bus Timing

AC Electrical Characteristics† - JTAG Test Port Timing

	Characteristic	Sym.	Min.	Typ.	Max.	Units	Notes
1	TCK Clock Period	t_{TCKP}	100			ns	
2	TCK Clock Pulse Width High	t_{TCKH}	80			ns	
3	TCK Clock Pulse Width Low	t_{TCKL}	80			ns	
4	TMS Set-up Time	t_{TMSS}	10			ns	
5	TMS Hold Time	t_{TMSH}	10			ns	
6	TDi Input Set-up Time	t_{TDIS}	20			ns	
7	TDi Input Hold Time	t_{TDIH}	60			ns	
8	TDo Output Delay	t_{TDOD}			30	ns	C_L = 30 pF
9	$\overline{\text{TRST}}$ pulse width	t_{TRSTW}	200			ns	

† Characteristics are over recommended operating conditions unless otherwise stated.

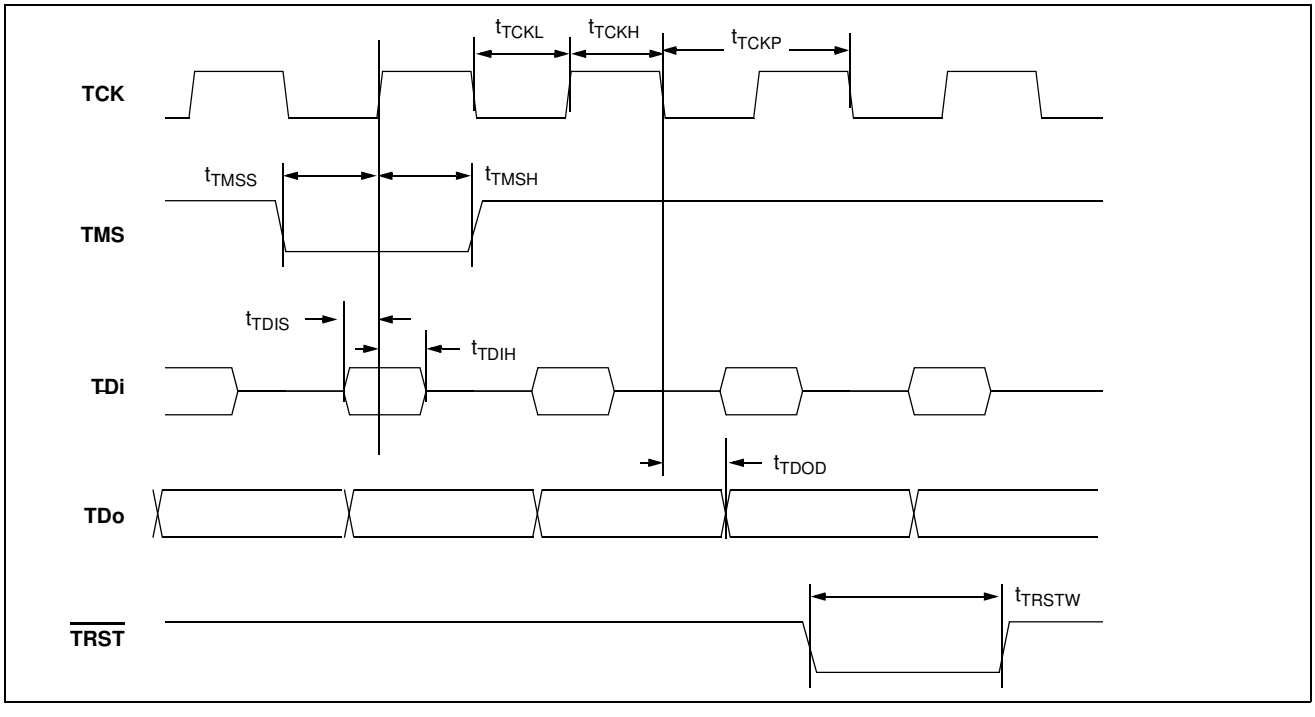
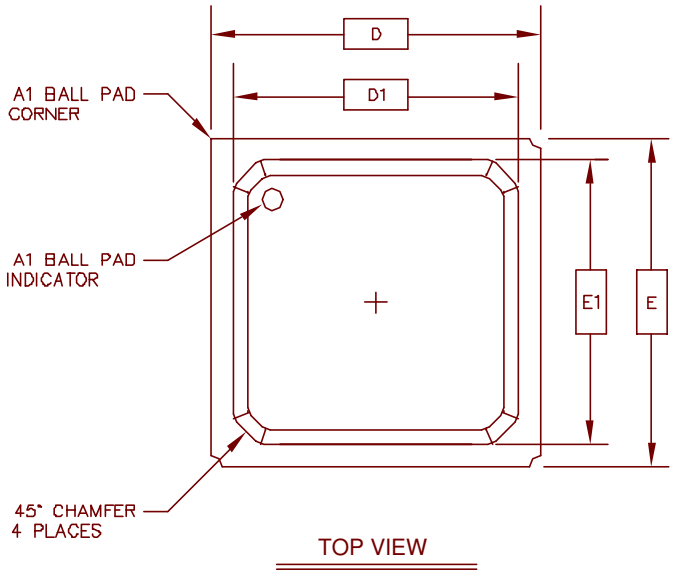
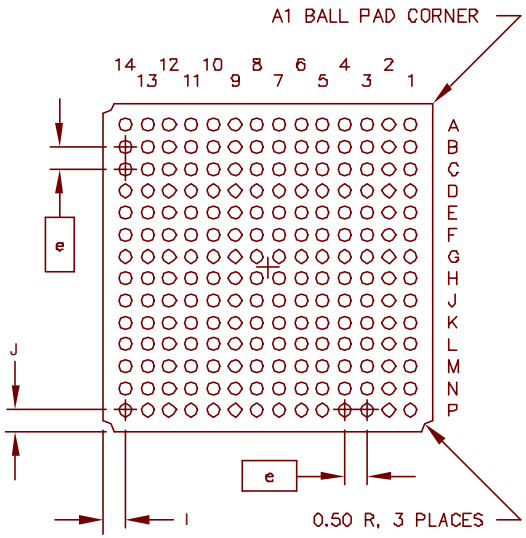


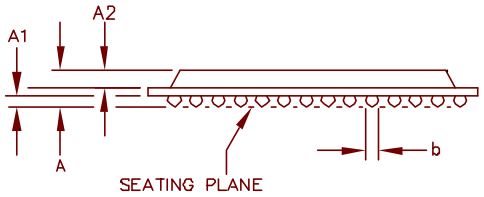
Figure 24 - JTAG Test Port Timing Diagram



TOP VIEW



BOTTOM VIEW



SIDE VIEW

DIMENSION	MIN	MAX
A	1.35 (1.55)	1.75 (1.97)
A1	0.30	0.50
A2	0.75	0.85
D	15.00 BSC	
D1	12.95	13.70
E	15.00 BSC	
E1	12.95	13.70
I	1.0 REF.	
J	1.0 REF.	
b	0.40	0.60
e	1.00 BSC	
N	196	
2 LAYERS (4 LAYERS)		

Conforms to JEDEC MS - 034
Except dimensions 'A1' and 'b'.

NOTES:-
1. Controlling dimensions are in MM.
2. Seating plane is defined by the spherical crown of the solder balls.
3. Not to scale.
4. Ball arrangement: 14 x 14 array

ISSUE	1	2		
ACN	211873	213916		
DATE	26Nov01	13Jan03		
APPRD.				

ZARLINK SEMICONDUCTOR

Previous package codes: BP / G

Package Code GA

Package Outline for 196 Ball PBGA (15 x 15mm)

GPD00779

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