



ON Semiconductor®

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DATA SHEET**2SA1740 / 2SC4548**PNP Epitaxial Planar Silicon Transistor
NPN Triple Diffused Planar Silicon Transistor**High-Voltage Driver Applications****Features**

- High breakdown voltage.
- Adoption of MBIT process.
- Excellent hFE linearity.

Specifications () : 2SA1740**Absolute Maximum Ratings** at Ta=25°C

Parameter	Symbol	Conditions	Ratings	Unit
Collector-to-Base Voltage	VCBO		(-)400	V
Collector-to-Emitter Voltage	VCEO		(-)400	V
Emitter-to-Base Voltage	VEBO		(-)5	V
Collector Current	IC		(-)200	mA
Collector Current (Pulse)	ICP		(-)400	mA
Collector Dissipation	PC	Mounted on a ceramic board (250mm²×0.8mm)	1.3	W
Junction Temperature	Tj		150	°C
Storage Temperature	Tstg		-55 to +150	°C

Electrical Characteristics at Ta=25°C

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Collector Cutoff Current	ICBO	VCB=(-)300V, IE=0A			(-)0.1	μA
Emitter Cutoff Current	IEBO	VEB=(-)4V, IC=0A			(-)0.1	μA
DC Current Gain	hFE	VCE=(-)10V, IC=(-)50mA	60*		200*	

Marking 2SA1740 : AK

2SC4548 : CN

Continued on next page.

*: The 2SA1740 / 2SC4548 are classified by 50mA hFE as follows:

Rank	D	E
hFE	60 to 120	100 to 200

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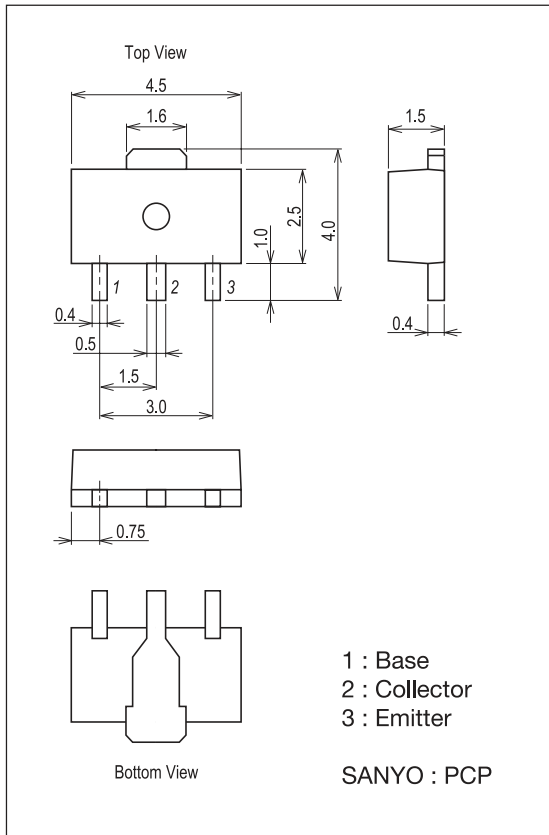
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Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Gain-Bandwidth Product	f_T	$V_{CE}=(-)30V, I_C=(-)10mA$		70		MHz
Output Capacitance	C_{ob}	$V_{CB}=(-)30V, f=1MHz$		(5)4		pF
Reverse Transfer Capacitance	C_{re}	$V_{CB}=(-)30V, f=1MHz$		(4)3		pF
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$	$I_C=(-)50mA, I_B=(-)5mA$			(-0.8)0.6	V
Base-to-Emitter Saturation Voltage	$V_{BE}(sat)$	$I_C=(-)50mA, I_B=(-)5mA$			(-1.0)	V
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	$I_C=(-)10\mu A, I_E=0A$	(-)400			V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	$I_C=(-)1mA, R_{BE}=\infty$	(-)400			V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	$I_E=(-)10\mu A, I_C=0A$	(-)			V
Turn-ON Time	t_{on}	See specified Test Circuit.		0.25		μs
Turn-OFF Time	t_{off}	See specified Test Circuit.		5.0		μs

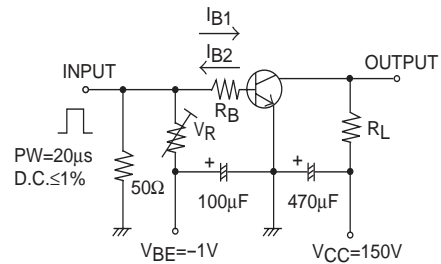
Package Dimensions

unit : mm (typ)

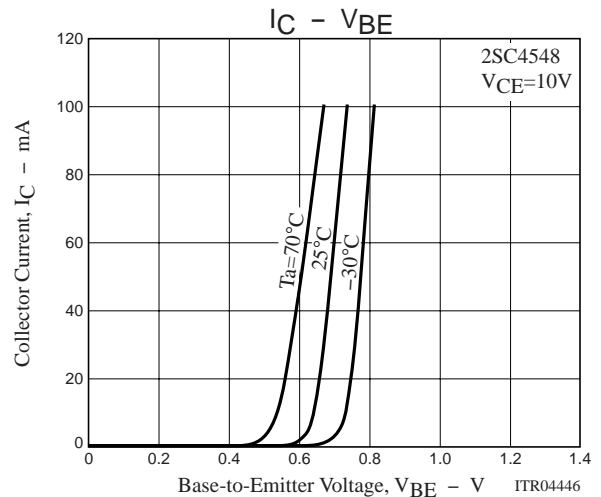
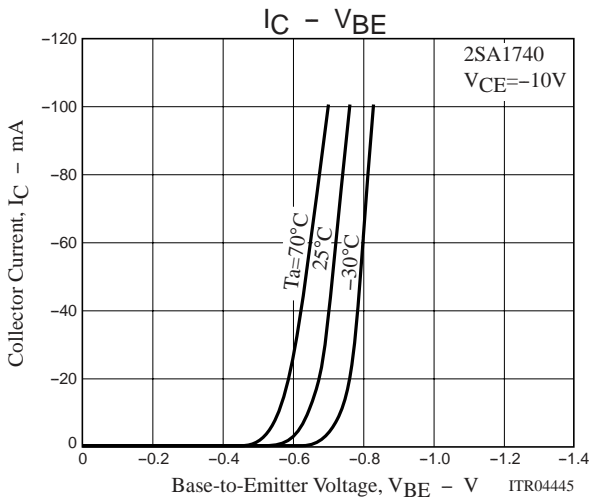
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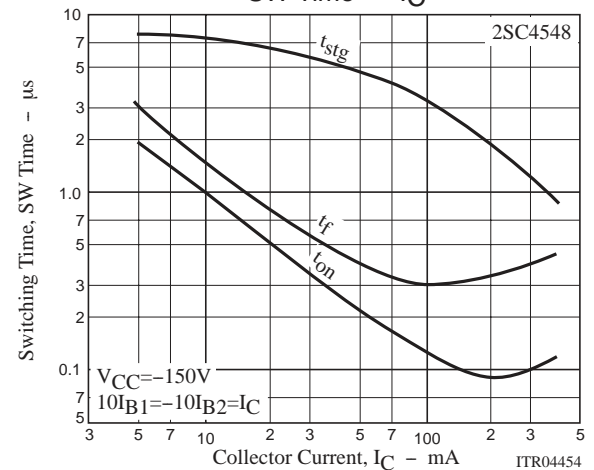
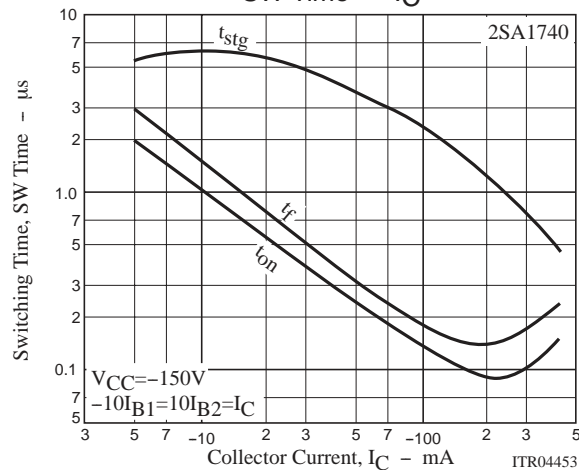
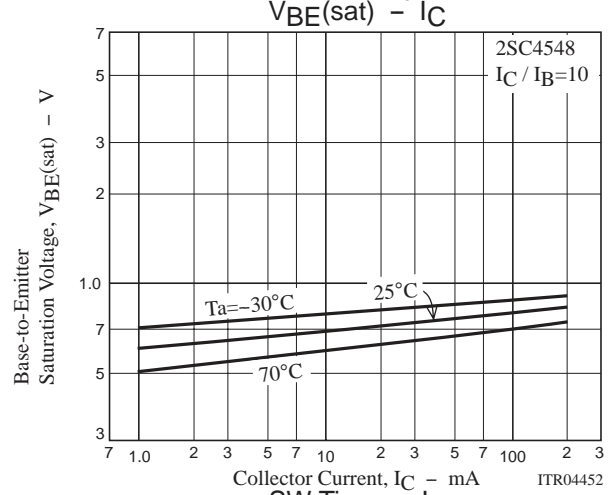
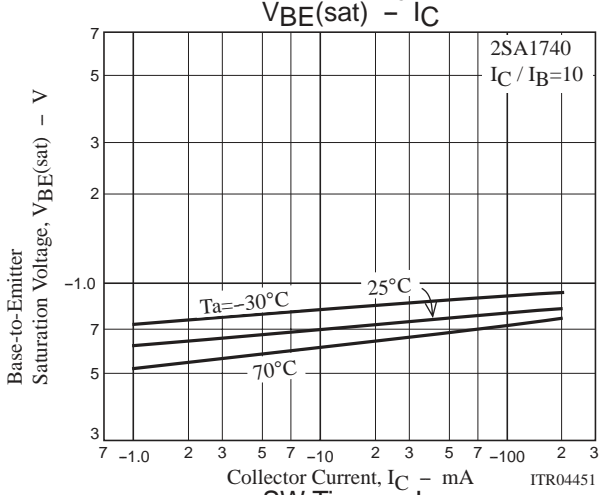
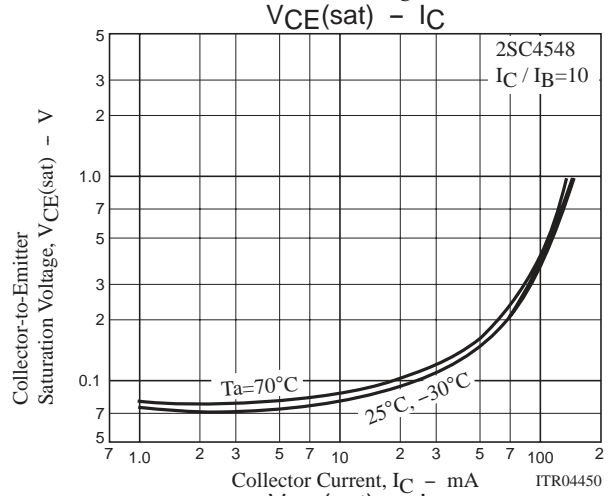
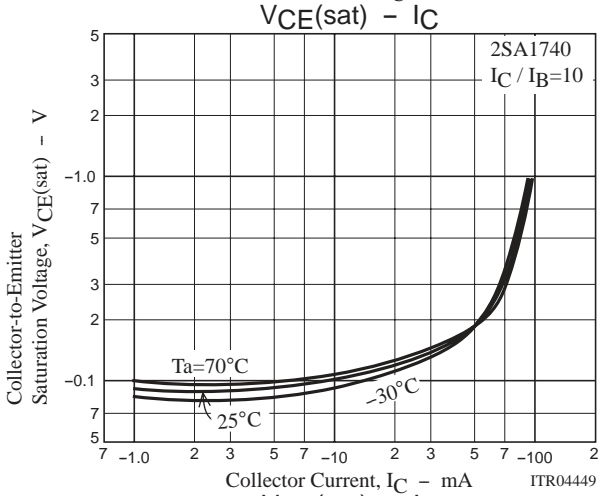
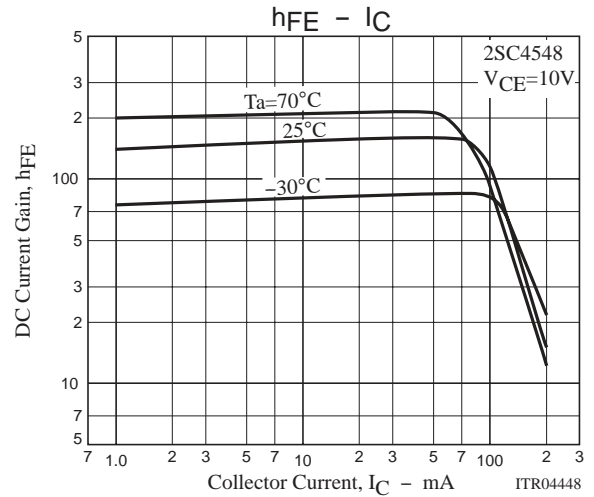
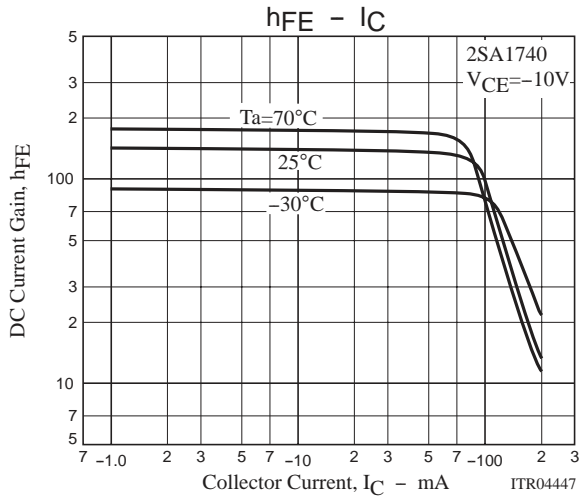
Switching Time Test Circuit



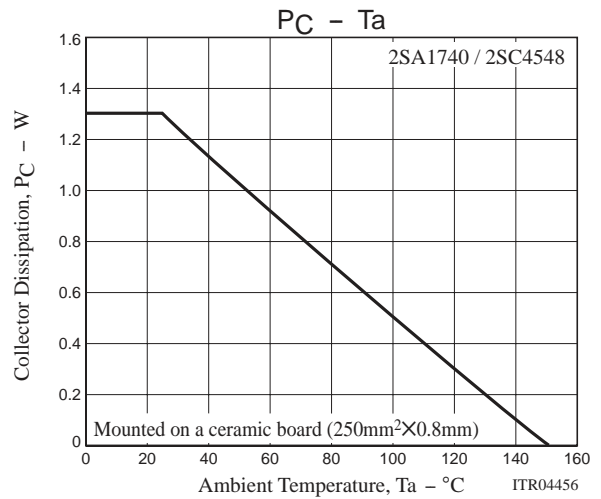
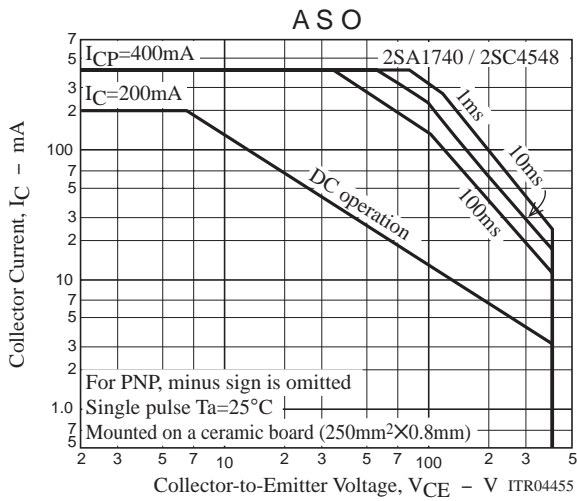
$I_C=10I_B1 = -10I_B2=50mA$
 $R_L=3k\Omega, R_B=200\Omega$ at $I_C=50mA$
 For PNP, the polarity is reversed



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