Texas Instruments

PGA2500EVM

Evaluation Module

User's Guide

December 2003

SBOU023

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the specified input and output ranges described in the EVM User's Guide.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 60°C. The EVM is designed to operate properly with certain components above 60°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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Preface

Read This First

About This Manual

This document provides the information needed to set up and operate the PGA2500EVM evaluation module (EVM) and accompanying software. For a detailed description of the PGA2500 product, please refer to the product data sheet available from the Texas Instruments web site at http://www.ti.com. Additional support documents are listed in the section of this guide entitled *Related Documentation* from Texas Instruments.

How to Use This Manual

Throughout this document, the abbreviation EVM and the term *evaluation module* are synonymous with the PGA2500EVM.

Chapter 1 provides an overview for the PGA2500 digitally-controlled microphone preamplifier. The PGA2500EVM block diagram and primary features are also discussed.

Chapter 2 provides general information regarding EVM handling and unpacking, as well as the absolute operating conditions for the EVM.

Chapter 3 provides descriptions of the primary hardware functions, as well as hardware configuration details for the EVM.

Chapter 4 includes the EVM electrical schematic, PCB layout, and the Bill of Materials.

Chapter 5 provides the information required to install and operate the PGA2500EVM applications software using a personal computer running the Microsoft Windows 9x, 2000, or XP operating systems.

Information About Cautions and Warnings

This book contains cautions and warnings.

This is an example of a caution statement.

A caution statement describes a situation that could potentially damage your software or equipment.

This is an example of a warning statement.

A warning statement describes a situation that could potentially cause harm to you.

The information in a caution or a warning is provided for your protection. Please read each caution and warning carefully.

Related Documentation From Texas Instruments

The following documents provide information regarding Texas Instruments integrated circuits used in the assembly of the PGA2500EVM. These documents are available from the TI web site. The last character of the literature number corresponds to the document revision, which is current at the time of the writing of this User's Guide. Newer revisions may be available from the TI web site at http://www.ti.com/ or call the Texas Instruments Literature Response Center at (800) 477−8924 or the Product Information Center at (972) 644−5580. When ordering, identify the document(s) by both title and literature number.

Document	Literature number
PGA2500 Data Sheet	SBOS289A
SN74AHCT541 Data Sheet	SCLS269O

If You Need Assistance

If you have questions regarding either the use of this evaluation module or the information contained in the accompanying documentation, please contact the Texas Instruments Product Information Center at (972) 644−5580 or visit the TI Semiconductor Online Technical Support pages at www.ti.com.

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Contents

Figures

Tables

Notes, Cautions, and Warnings

Chapter 1

Introduction

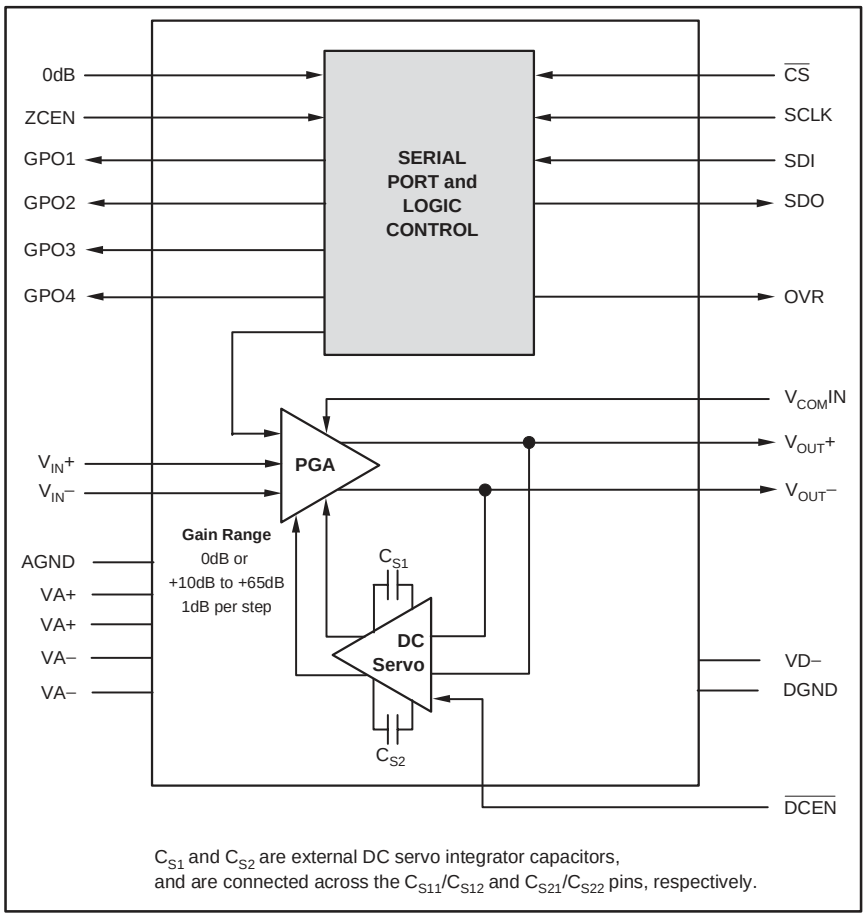
This chapter provides a brief technical overview for the PGA2500 digitally-controlled microphone preamplifier, as well as a general description and feature list for the PGA2500EVM.

Topic **Page**

1.1 PGA2500 Product Overview

The PGA2500 is a digitally-controlled, microphone preamplifier integrated circuit designed for amplifying the output of dynamic and condenser microphones and driving high-performance audio analog-to-digital (A/D) converters. A functional block diagram of the PGA2500 is shown in Figure 1−1.

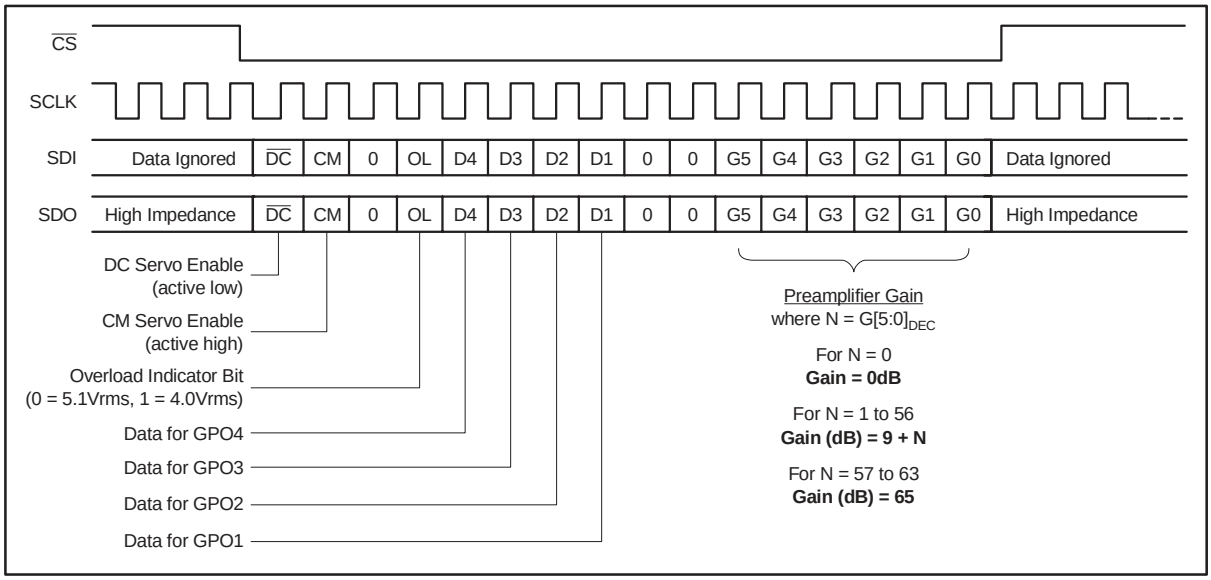
Figure 1−1. PGA2500 Functional Block Diagram



The analog input to the preamplifier is provided differentially at the $V_{IN}+$ and $V_{IN}-$ inputs (pins 27 and 26, respectively). The programmable gain amplifier can be programmed to either pass through the signal at unity gain, or apply 10dB to 65dB of gain to the input signal. The gain of the amplifier is adjustable over the full 10dB to 65dB range in 1dB steps. The differential output of the PGA2500 is made available at $V_{OUT}+$ and $V_{OUT}-$ (pins 17 and 16, respectively). Gain is controlled using a serial port interface.

The 4-wire serial port interface is used to program the PGA2500 gain and support functions. A 16-bit control word is utilized to program these functions; see Figure 1−2. A serial data output pin provides support for daisy-chaining multiple PGA2500 devices on a single serial interface bus.

Figure 1−2. PGA2500 Serial Port Protocol



The differential analog output of the PGA2500 is constantly monitored by a DC servo amplifier loop. The purpose of the servo loop is to minimize the DC offset voltage present at the analog outputs by feeding back an error signal to the input stage of the programmable gain amplifier. The error signal is then used to correct the offset. The DC servo may be disabled by driving the $\overline{\text{DCEN}}$ input (pin 7) high or setting the $\overline{\text{DC}}$ bit in the serial control word to 1. Normally, the $\overline{\text{DCEN}}$ pin is connected to DGND and the $\overline{\text{DC}}$ bit is set to 0 to enable the DC servo.

Two external capacitors are required for the DC servo function, with one capacitor connected between C_{S11} and C_{S12} (pins 24 and 23), and the second capacitor connected between C_{S21} and C_{S22} (pins 22 and 21). Capacitor values up to 4.7µF may be utilized. However, larger valued capacitors will result in longer settling times for the DC servo loop. A value of 1µF is recommended for use in most microphone preamplifier applications.

The PGA2500 includes a common-mode servo function. This function is enabled and disabled using the CM bit in the serial control word, as shown in Figure 1−2. When enabled, the servo provides common-mode negative feedback at the input differential pair, resulting in very low common-mode input impedance. The differential input impedance is not affected by this feedback. This function is useful when the source is floating, or has a high common-mode output impedance. In this case, the only connection between the source and the ground will be through the PGA2500 preamplifier input resistance.

In this case, input common-mode parasitic current is determined by high output impedance of the source, not by input impedance of the amplifier. Therefore, input common-mode interference can be reduced by lowering the common-mode input impedance while not increasing the input common-mode current. Increasing common-mode current degrades common-mode rejection. Using the common-mode servo, overall common-mode rejection can be improved by suppressing low and medium frequency common-mode interference.

The common-mode servo function is designed to operate with a total common-mode input capacitance (including the microphone cable capacitance) of up to 10nF. Beyond this limit, stable servo operation is not ensured.

The common-mode voltage control input, named V_{COM}IN (pin 25), allows the PGA2500 output and input to be DC biased to a common-mode voltage between 0V and +2.5V. This allows for a DC-coupled interface between the PGA2500 preamplifier output and the inputs of common single-supply audio A/D converters.

A dedicated 0dB input (pin 8) is provided so that the gain of the PGA2500 may be forced to unity without using the serial port interface. The 0dB input overrides gain settings made through the serial port. While the 0dB input is active (forced high), the serial port register may be updated or data may be passed through the serial interface to other PGA2500 devices in daisy-chain configuration. However, any changes in gain will not take effect until the 0dB input is driven low.

The zero-crossing control input, named ZCEN (pin 9), is provided for enabling and disabling the internal zero-crossing detector function. Forcing the ZCEN input high enables the function. Zero-crossing detection is used to force gain changes on zero crossings of the analog input signal. This limits the glitch energy associated with the switched gain network, thereby minimizing audible artifacts at the preamplifier output. Since zero-crossing detection can add some delay when performing gain changes (up to 16ms maximum for a detector timeout event), there may be cases where the user may wish to disable the function. Forcing the ZCEN input low disables zero-crossing detection, with gain changes occurring immediately when programmed.

An overflow indicator output, OVR, is provided at pin 5. The OVR pin is an active high, CMOS-logic-level output. The overflow output is forced high when the preamplifier output voltage exceeds one of two preset thresholds. The threshold is programmed through the serial port interface using the OL bit. If OL = 0, then the threshold is set to 5.1Vrms differential, which is approximately −1dB below the specified output voltage range. If OL = 1, then the threshold is set to 4.0Vrms differential, which is approximately −3dB below the specified output voltage range.

The PGA2500 includes four general-purpose programmable digital outputs, named GPO1 through GPO4 (pins 1 through 4, respectively), which are controlled via the serial port interface. All four pins are CMOS-logic-level outputs. These pins may be used to control relay drivers or switches used for external preamplifier functions, including input pads, filtering, polarity reversal, or phantom power.

1.2 PGA2500EVM Features

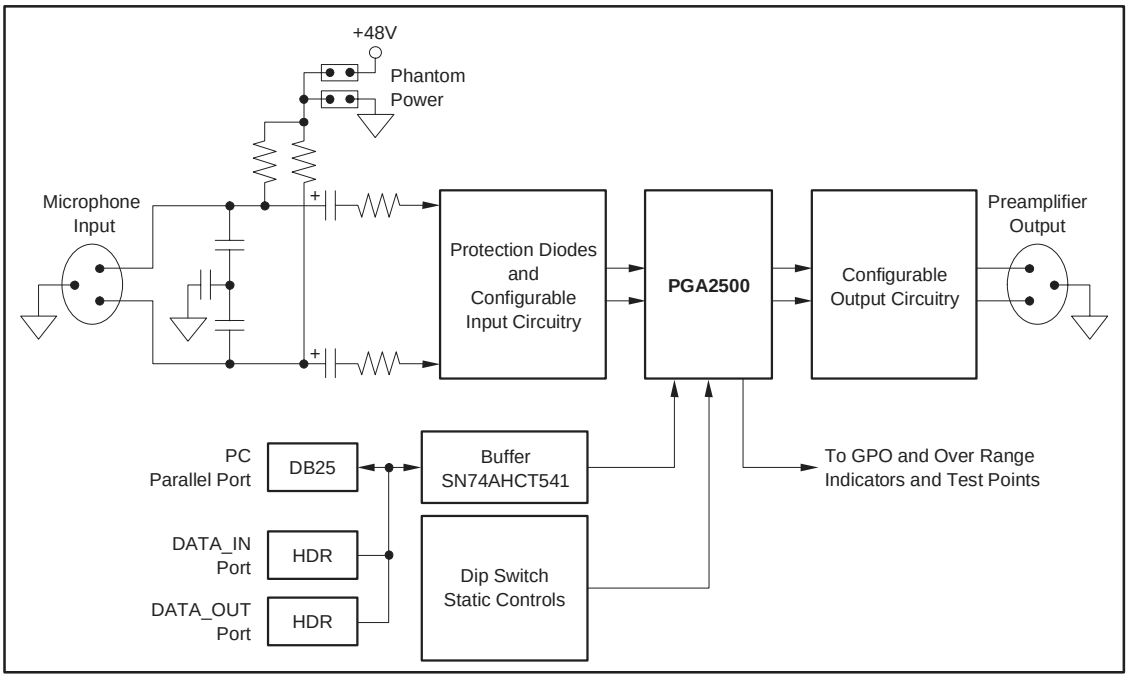
The PGA2500EVM provides a convenient platform for evaluating the performance and features of the PGA2500 product. Key EVM features include the following:

- ❑ Accepts either XLR or TRS balanced input connections
- ❑ Configurable front-end circuit options for prototyping pads and filters
- ❑ XLR balanced output with flexible output loading options
- ❑ Buffered PC parallel and DATA_IN ports provide host interface connections
- ❑ DATA_OUT port allows daisy-chaining of multiple PGA2500EVM boards
- ❑ Register readback function supports host interface diagnostic capability
- ❑ LED indicators for GPOs and the over range output
- ❑ Common-mode voltage input (V_{COM}IN) terminal
- ❑ Includes applications software which is compatible with most personal computers that have a built-in parallel port and run the Microsoft Windows 9x, 2000, or XP operating systems
- ❑ Requires +5V and −5V analog supplies, as well as a +5V digital supply

1.3 PGA2500EVM Block Diagram

The main functions of the PGA2500EVM are shown in Figure 1−3. Configurable input and output circuitry provide convenient prototype options, while the buffered host interface supports the supplied applications software and alternate host configurations.

Figure 1−3. Functional Block Diagram for the PGA2500EVM



Chapter 2

Getting Started

This chapter provides information regarding PGA2500EVM handling and unpacking, as well as the absolute operating conditions.

Topic **Page**

2.1 Electrostatic Discharge Warning

Many of the components on the PGA2500EVM are susceptible to damage by electrostatic discharge (ESD). Customers are advised to observe proper ESD handling precautions when unpacking and handling the EVM. Failure to observe ESD handling procedures may result in damage to the EVM components.

Caution: Failure to observe ESD handling procedures may result in damage to the EVM.

2.2 Unpacking the EVM

Upon opening the PGA2500EVM package, please check to verify that the following items are included:

- ❑ One PGA2500EVM evaluation module
- ❑ One CD-ROM, containing the applications software and support documents
- ❑ One straight-through cable, DB25 male to DB25 female, for PC parallel port interface
- ❑ One printed PGA2500EVM Evaluation Module User's Guide (TI literature number SBOU023)
- ❑ One printed PGA2500 data sheet (TI literature number SBOS289A)

If any of these items are missing, please contact the Texas Instruments Product Information Center at (972) 644−5580 to inquire about replacements

2.3 Absolute Operating Conditions Warning

Caution: Exceeding the absolute operating conditions may result in damage to the EVM and/or the equipment attached to it.

The user should be aware of the absolute maximum operating conditions for the evaluation module. Table 2−1 summarizes the critical data points.

Table 2−1. Absolute Operating Conditions

Parameter	Maximum Condition
Power-Supply Voltages(1)	
VA+	+5.5V DC Maximum
VA−	−5.5V DC Maximum
VCOM	−0.3V DC Minimum to (VA+) + 0.3V DC Maximum
VCC	+5.5V DC Maximum
Phantom Power	+50V DC Maximum
Microphone Input (J1), XLR, or TRS(2)	
Maximum Input Voltage, Differential	$20.0V_{PP}$ (or 7.0Vrms) Maximum
Preamplifier Output (J3)(2)	
Maximum Output Voltage, Differential	$17.5V_{PP}$ (or 6.2Vrms) Maximum
Digital Input Voltage(2)	
Parallel Port (J5), DATA_IN (J6), and DATA_OUT (J7)	−0.3V Minimum to +5.5V Maximum
Digital Output Voltage(2)	
Parallel Port (J5), DATA_IN (J6), and DATA_OUT (J7)	+5.5V Maximum

1) Referenced to the GND terminal of connector J4.
2) Assumes VA+ = +5.0V DC and VA− = −5.0V DC.

Chapter 3

Setup Guide

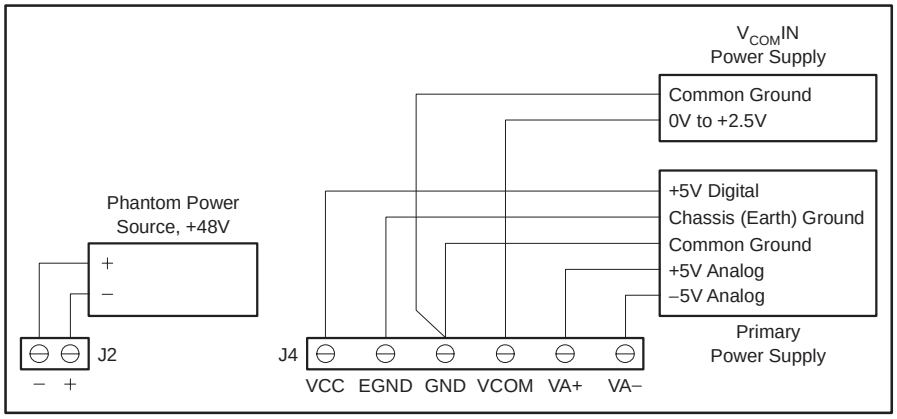
This chapter provides descriptions of the hardware components that make up the PGA2500EVM. In addition, configuration information for power supplies, analog input and output connections, switches, and jumpers are provided.

Topic **Page**

3.1 Analog and Digital Power Supplies

All analog and digital power supplies are connected through terminal block J4. Recommended power-supply connections are shown in Figure 3−1.

Figure 3−1. Recommended Power-Supply Connections



The PGA2500EVM requires two analog supplies and one digital power supply. The analog supplies are VA+ and VA−, respectively. VA+ is typically set to +5.0V DC, while VA− is typically set to −5.0V DC. The analog supplies power the PGA2500 microphone preamplifier integrated circuit. The digital power supply, VCC, is typically set to +5.0V DC. The VCC supply powers the SN74AHCT541 buffer IC (U2) and the associated pull-up resistors for the digital section of the board.

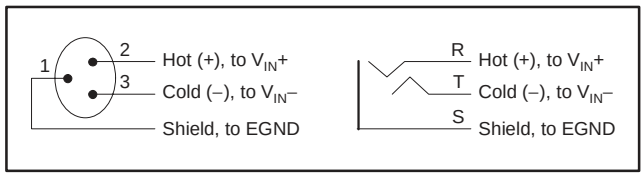
An optional third analog power supply may be utilized for the PGA2500 common-mode DC voltage input, V_{COM}IN (pin 25). The common-mode input can be connected to analog ground by shorting pins 3 and 4 of Jumper JMP3. Alternatively, the common-mode input can be connected to the VCOM supply terminal of connector J4 by shorting pins 1 and 2 of Jumper JMP3. The VCOM supply will typically be set to a DC voltage within the 0V to +2.5V DC range (with respect to GND). The common-mode voltage biases both the output and input terminals of the PGA2500, with the output pins being biased to the V_{COM}IN voltage level and the input pins being biased to approximately V_{COM}IN − 0.65V.

The GND terminal of connector J4 serves as the common ground connection for both the analog and digital sections of the PGA2500EVM. The EGND (earth ground) terminal should be connected to the earth or chassis ground of the power supply. The common ground (GND) and earth ground (EGND) are connected to one another using a 0.1µF capacitor (C3).

3.2 Microphone Input

Dynamic and condenser microphones or audio test equipment are connected to the PGA2500EVM input through combo connector J1. The combo connector combines both a 3-pin female XLR and a 1/4-inch TRS jack for connecting to microphones and test signal sources. Both the XLR and TRS jacks are wired for a balanced input. Figure 3−2 illustrates the combo connector pin configuration for the PGA2500EVM.

Figure 3−2. Microphone Input Connector Configuration



The microphone input includes 1000pF capacitors configured as an EMI filter to help suppress electromagnetic interference present at the preamplifier input. Additional filtering may be required in the customer's end application circuit, depending on the operating environment.

3.3 Phantom Power Connections

The PGA2500EVM supports connection of a phantom power source across the inputs of the preamplifier using terminal block J2. The voltage source is connected to the hot (+) and cold (−) sides of the preamplifier input through 6.81kΩ resistors. Phantom power may be operated at voltages up to +50V DC.

Phantom power is required for condenser microphones, but should not be applied when using dynamic microphones, as they may be subject to damage if phantom voltage is applied. When using a dynamic microphone, terminals 3 and 4 of jumper JMP1 should be shorted, while terminals 1 and 2 remain open. When using a condenser microphone requiring a phantom power source, terminals 1 and 2 of jumper JMP1 should be shorted, while terminals 3 and 4 remain open.

3.4 DC Blocking Capacitors

Capacitors C_{19} and C_{20} are utilized as DC blocking capacitors. They provide AC-coupling to the microphone input, as well as blocking the phantom voltage from reaching the PGA2500 input terminals when using a condenser microphone. The blocking capacitors are selected in order to not degrade the dynamic performance of the PGA2500. The surface-mount aluminum electrolytic capacitors shown in the Bill of Materials (see Table 4−1) are installed by default at the factory. The PGA2500EVM also supports the use of through-hole capacitors for C_{19} and C_{20}. If using an alternative capacitor, use components rated for 50WV minimum, with 63WV or higher recommended for long-term reliability.

3.5 Protection Network

Resistors R_7 and R_8, along with Schottky diodes D6 through D9, provide input protection for the PGA2500 preamplifier when using phantom power, or when the input voltage exceeds the VA+ or VA− power supplies by more than 350mV (the approximate turn-on voltage of the Schottky diodes).

A common fault condition is for either the hot (+) or cold (−) input of the preamplifier to be shorted to ground. With phantom voltage applied, this will cause the blocking capacitors to discharge, with a large surge current presented at the PGA2500 input pins. Without the protection network, the PGA2500 would be permanently damaged by the surge current, which can reach several amperes in peak magnitude. The Schottky diodes are forced into conduction during this fault condition, steering most of the charge away from the PGA2500 device and towards the power supplies. The series resistors can be set to a value that will help limit the input current, although care must taken to avoid adding too much resistance, since the added noise can degrade the overall performance of the preamplifier.

The Schottky diodes add a nonlinear capacitance to the input circuit, which can result in additional distortion. However, with the relatively small input voltage swing present when the preamplifier is set to gains between 10dB and 65dB, the effect on the THD+N of the PGA2500 is small or negligible. For unity-gain applications, where the voltage swing may become large enough in magnitude to transition over a greater portion of the diodes nonlinear capacitance, the THD+N ratio may degrade by as much as 3dB from the published typical performance specifications.

3.6 Configurable Input Circuitry

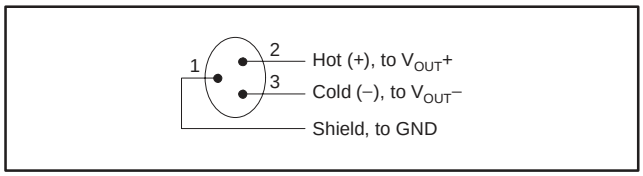
The configurable portion of the input circuit includes R_5, R_6, R_{10}, R_{11}, R_{14}, R_{15}, C_C1, C_C2, and jumper JMP2. These components support prototyping of additional circuitry, such as pads and filters. During assembly at the factory, resistors R_5 and R_6 are not installed, while R_{10}, R_{11}, R_{14}, R_{15}, C_C1, and C_C2 are replaced by wire shunts.

3.7 Configurable Output Circuitry and Preamp Output Connector

The configurable portion of the output circuit includes R_1, R_2, R_3, R_{12}, R_{13}, C_{23}, C_{24}, and C_{25}. These components support prototyping of additional circuitry, such as pads and filters, as well as emulation of various loading conditions. During assembly at the factory, resistors R_{12} and R_{13} are replaced by wire shunts. Resistors R_1 through R_3, as well as capacitors C_{23} through C_{25}, are not installed.

The differential preamplifier output is provided at connector J3, which is a 3-pin male XLR connector. Figure 3−3 illustrates the pin connections for connector J3.

Figure 3−3. Preamp Output Connector Configuration



3.8 Host Interface

The PGA2500EVM supports an external host interface to the PGA2500 serial port utilizing connectors J5 through J7. A PC parallel port may be connected to connector J5, using the straight through cable supplied with the EVM package. The PC parallel port is used as the communications interface for the applications software provided with the EVM. Chapter 5 provides details for installing and using the applications software.

The DATA_IN header (J6) may be used as an alternative host interface connection, and is designed primarily for interfacing to microprocessors, digital signal processors, or other host devices in either end equipment or hardware development platforms.

The DATA_OUT header (J7) is designed primarily for cascading multiple PGA2500EVM boards in a daisy-chain fashion. Daisy-chaining is described in more detail in the PGA2500 datasheet.

3.9 Switch and Jumper Quick Reference

Table 3−1 and Table 3−2 provide a quick configuration reference of the switch and jumper settings for the PGA2500EVM. Factory default settings are also indicated.

Table 3−1. Switch Configuration Quick Reference

Switch	Setting	Function
$\overline{\text{DCEN}}$	LO (default)	DC Servo Enabled(1)(2)
	HI	DC Servo Disabled
0dB	LO (default)	Unity (odB) Gain Disabled, Gain Programmed Through Serial Port(2)
	HI	Unity (0dB) Gain Enabled, Overrides Gain Set Through Serial Port
ZCEN	LO	Zero-Crossing Detection Disabled(2)
	HI (default)	Zero-Crossing Detection Enabled

1) When $\overline{\text{DCEN}}$ = LO, the $\overline{\text{DC}}$ bit in the serial control word may be used to disable and enable the DC servo under software control.
2) A switch is set to LO when in the ON position (labeled ON C & K TDA04 on the switch itself). A switch is set to HI when in the numbered position (labeled 1, 2, 3, or 4 on the switch itself).

Table 3−2. Jumper Configuration Quick Reference

Jumper Configuration		
Jumper JMP1: Phantom Power	Pins 1 to 2	Pins 3 to 4
Phantom Power Disabled, Connected to GND (default)	Open	Short
Phantom Power Enabled, Connected to J2 Terminal Block	Short	Open
Jumper JMP3: V_{COM}IN Input Connection	Pins 1 to 2	Pins 3 to 4
V_{COM}IN (pin 25) Connected to GND (default)	Open	Short
V_{COM}IN (pin 25) Connected to the VCOM Terminal of J4	Short	Open
Jumper J9: Register Read Back	Pins 1 to 2	
Register Read Back Function Disabled	Open	
Register Read Back Function Enabled (default)	Short	

Jumpers JMP4 through JMP8, as well as JMP10, are shorted on the PCB layout. They may be cut and replaced by jumpers if desired.

Jumper JMP2 is provided in order to add flexibility for the configurable input circuitry. This jumper is left open by default.

Chapter 4

Schematic, PCB Layout and Bill of Materials

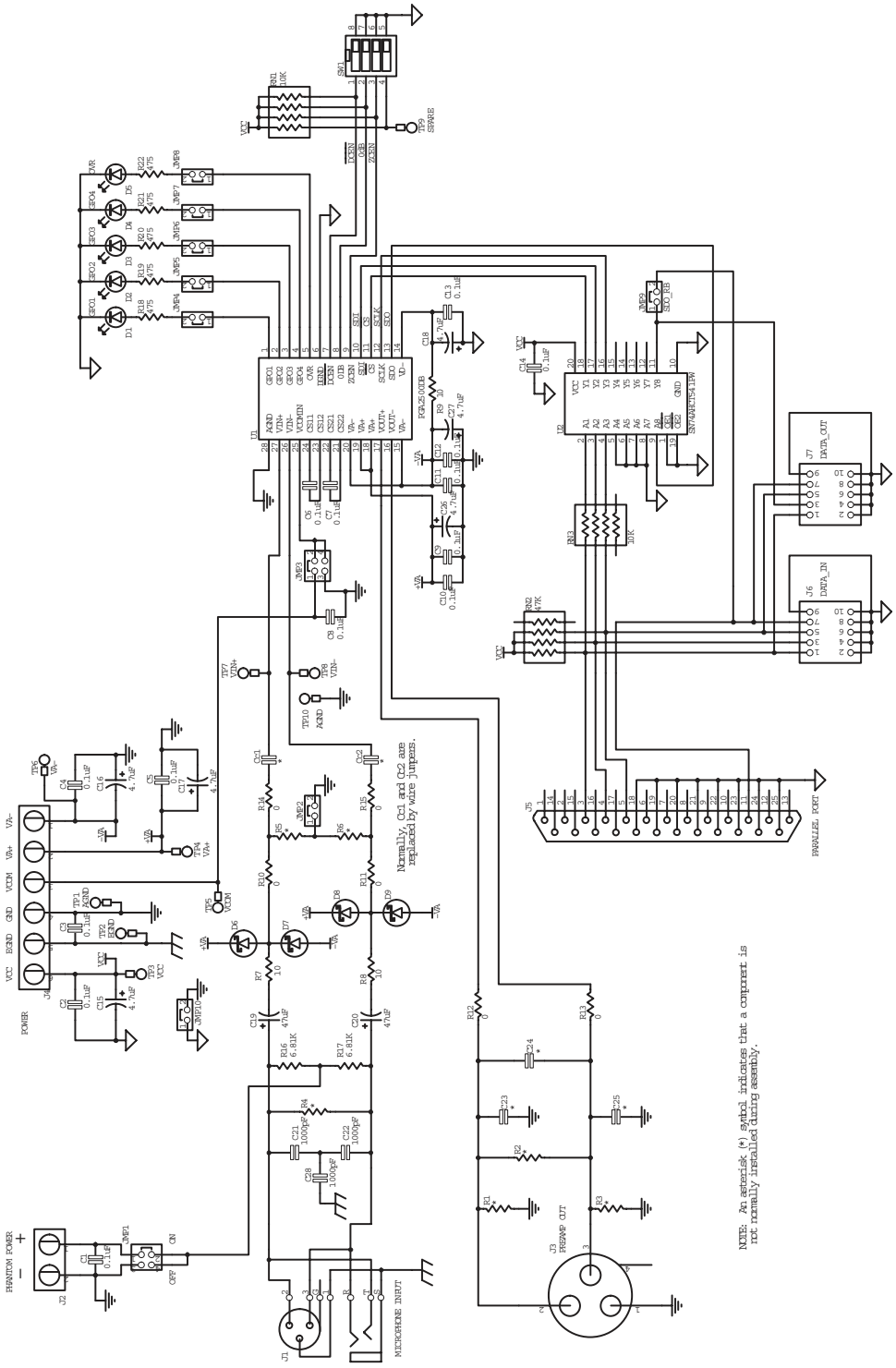
This chapter provides the electrical schematic and physical PCB layout information for the PGA2500EVM. The Bill of Materials is included for component reference.

Topic **Page**

4.1 Schematic

The complete electrical schematic for the PGA2500EVM is shown in Figure 4−1. Refer to the Bill of Materials in Table 4−1 for descriptions of components shown in the schematic.

Figure 4−1. Schematic



4.2 PCB Layout

The PGA2500EVM is a two-layer printed circuit board using both through-hole and surface-mount components. The silkscreen, top, and bottom layer plots are shown in Figure 4−2 through Figure 4−4, respectively.

Figure 4−2. PGA2500EVM PCB Silkscreen

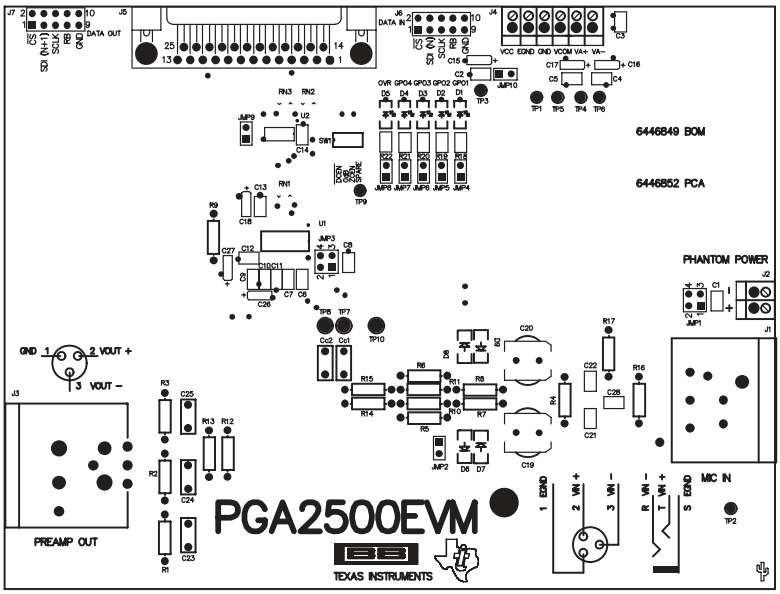


Figure 4−3. PGA2500EVM PCB Top Layer (Component Side)

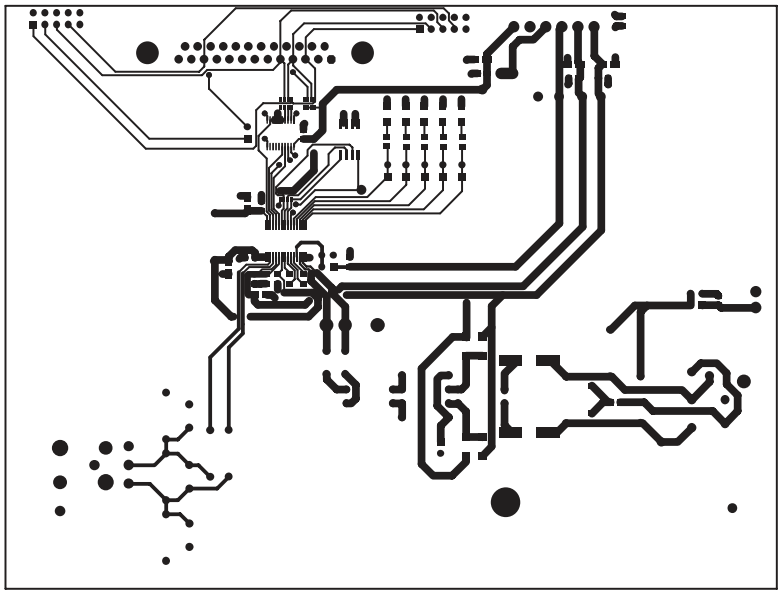
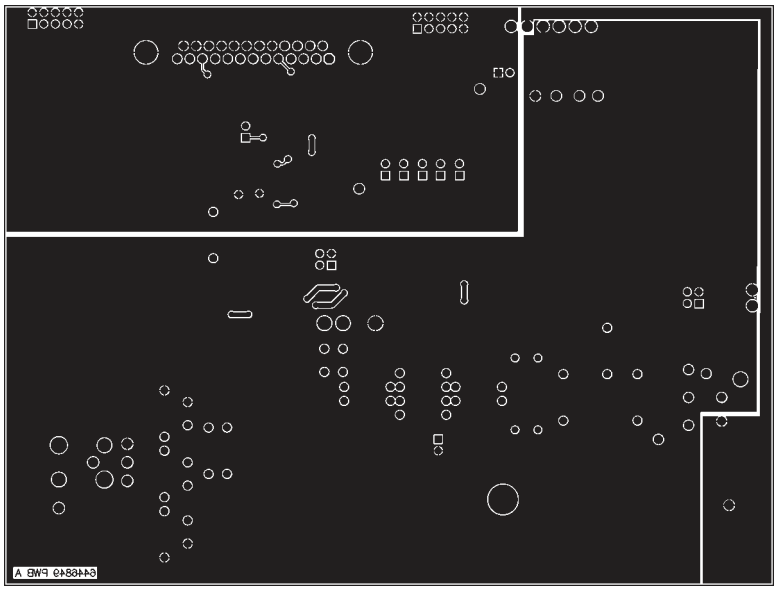


Figure 4−4. PGA2500EVM PCB Bottom Layer (Solder Side)



4.3 Bill of Materials

The complete bill of materials for the PGA2500EVM is shown in Table 4−1. Data for each component is available from the corresponding manufacturer's web site.

Table 4−1. Bill of Materials

Item	Value	Reference Designator	Qty Per Bd	Manufacturer	Mfg Part Number	Description
1	1000pF	C21, C22, C28	3	Kemet	C0805C102J5GACTU	Capacitor, Ceramic C0G/NPO, SMT, 1000pF ± 5%, 50WV, Size = 0805
2	0.1µF	C1-C5, C8-C14	12	Kemet	C0805C104K5RACTU	Capacitor, Ceramic X7R, SMT, 1µF ±10%, 50WV, Size = 0805
3	1µF	C6, C7	2	Kemet	C0805C105K4RACTU	Capacitor, Ceramic X7R, SMT, 1µF ±10%, 16WV, Size = 0805
4	4.7µF	C15-C18, C26, C27	6	Kemet	T494A475K016AS	Capacitor, Low ESR Tantalum, SMT, 4.7µF ±10%, 16WV, Size = A
5	47µF	C19, C20	2	Panasonic	EEV-FK1J470P	Capacitor, Alum Electrolytic, SMT, 47µF ±20%, 63WV
6		D1-D5	5	Lumex	SML-LX1206IC-TR	Red LED, SMT, Size = 1206
7		D6-D9	4	ON Semiconductor	MBRA120LT3	Surface-Mount Schottky Power Rectifier, Size = SMA
8		J1	1	Neutrik	NCJ6FI-H	Combo Connector, Female XLR + TRS Vert PC Mount
9		J2	1	Weidmuller	1699670000	3.5mm PCB Terminal Block, 2 Poles
10		J3	1	Switchcraft or ITT Cannon	PQG3MRA112 XLB-3-32PCV-M01	XLR Connector, Male, 3-Pin Vert PC Mount with PCB Retainers XLR Connector, Male, 3-Pin Vert PC Mount with Ground Lug
11		J4	1	Weidmuller	9967720000	3.5mm PCB Terminal Block, 6 Poles
12		J5	1	AMP	747842-6	DB-25 Connector, Male, Tin-Plated Shell, 0.318in (8.08mm) Mount, Rt Angle PCB w/ Boardlocks, Female Screwlocks
13		J6, J7	2	Samtec	TSW-105-07-G-D	Terminal Strip, 10-Pin (5x2)
14		JMP2, JMP9	2	Samtec	TSW-102-07-G-S	Terminal Strip, 2-Pin (2x1)

(continued on next page)

Table 4−1. Bill of Materials (continued)

Item	Value	Reference Designator	Qty Per Bd	Manufacturer	Mfg Part Number	Description
15		JMP1, JMP3	2	Samtec	TSW-102-07-G-D	Terminal Strip, 4-Pin (2x2)
16	10	R7-R9	3	Vishay Dale or Equivalent	CMF-55 10R0BT-9	Resistor, Metal Film, Axial Lead, 10Ω, ± 0.1%, 1/4W
17	475	R18-R22	5	Panasonic or equivalent	ERJ-6ENF4750V	Resistor, Thick Film SMT, 475Ω, ± 1%, 1/10W, Size = 0805
18	6.81K	R16, R17	2	Vishay Dale or Equivalent	CMF-55 6811BT-9	Resistor, Metal Film, Axial Lead, 6.81kΩ ± 0.1%, 1/4W
19	10K	RN1, RN3	2	CTS	742C083103J	Thick Film Chip Resistor Array, 10kΩ, 8 Terminal, 4 Resistors, Isolated
20	47K	RN2	1	CTS	742C083473J	Thick Film Chip Resistor Array, 47kΩ, 8 Terminal, 4 Resistors, Isolated
21		SW1	1	ITT Industries/C&K	TDA04H0SK1	DIP Switch, 4 Element, Half Pitch Surface-Mount, Tape Sealed
22		TP7, TP8, TP10	3	Keystone Electronics	5006	PCB Test Point, Compact Style, Black
23		U1	1	Texas Instruments	PGA2500IDB	Digitally-Controlled Microphone Preamplifier
24		U2	1	Texas Instruments	SN74AHCT541PW	Octal Buffer/Driver
25			4	3M Bumpon	SJ-5003	Rubber Feet, Adhesive Backed
26			4	Samtec	SNT-100-BK-G-H	Shorting Blocks

Chapter 5

Software Installation and Operation

This chapter provides instructions for installing the PGA2500EVM application software and using the software to control the PGA2500 gain and support functions.

Topic **Page**

5.1 Applications Software Overview

The applications software supplied with the PGA2500EVM allows the user to control the board via a PC equipped with a parallel printer port running the Microsoft Windows 9x, 2000, or XP operating systems. The software is supplied on the accompanying CD-ROM, while a straight-through cable (DB25 male to DB25 female) is provided for interfacing between the EVM and the PC parallel port. The applications software provides a simple graphical user interface with which the user can program the PGA2500 16-bit control word. All programmable functions are supported.

5.2 Software Installation

The applications software is provided on the accompanying CD-ROM. The following steps are required to install the applications software:

1) Insert the accompanying CD-ROM disc into the PC CD-ROM drive.
2) Locate the directory named *Apps Software* on the CD-ROM disc.
3) Copy the *Apps Software* folder to your hard disk.
4) Once copied, open the *Apps Software* folder on your hard disk. There will be two files in the folder:
    a) **PGA2500EVM.exe**, the executable program file.
    b) **inpout32.dll**, the driver file required for parallel port operation on Windows 9x, 2000, and XP.
5) Using your pointing device, click on and hold the PGA2500EVM.exe file icon and drag it to the desktop to create a shortcut to the program file. Once the shortcut has been made, you can rename the shortcut if desired, but it is recommended to include *PGA2500* in the shortcut name.

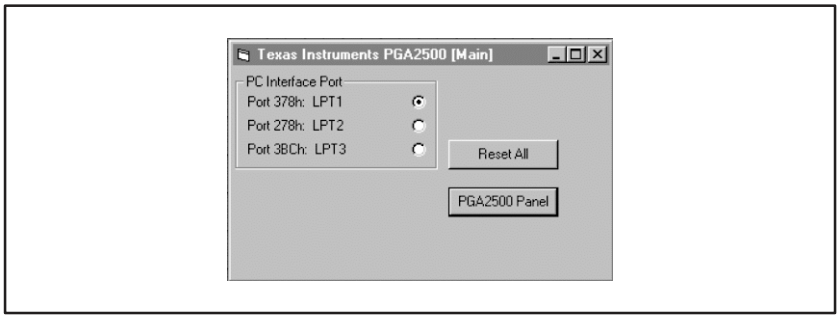
This completes the installation of the PGA2500EVM applications software.

5.3 Using the Applications Software

The program is executed by double-clicking on the desktop shortcut created during the installation process. The Main panel, shown in Figure 5−1, will appear on the screen. The Main panel allows the user to select the parallel port address to be used for communications with the PGA2500EVM. The Main panel also includes a Reset button, which is utilized to set the PGA2500 16-bit control word to the reset default conditions. The default conditions are:

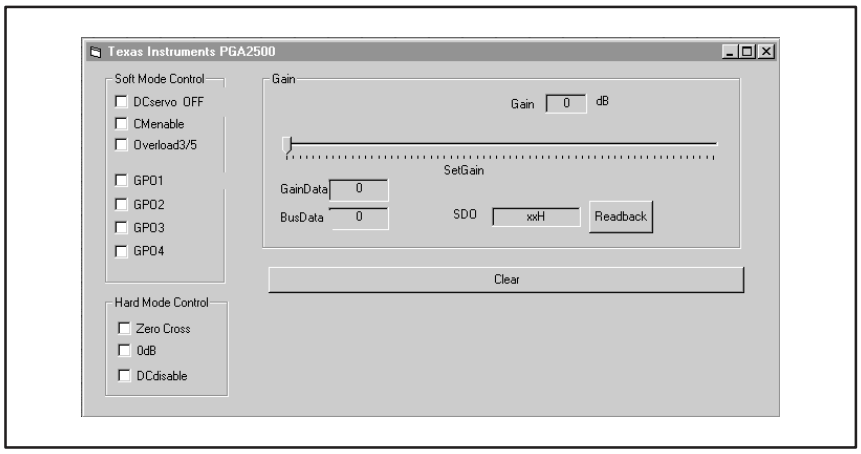
- ❑ DC Servo Enabled ($\overline{DC}$ bit set to 0).
- ❑ Common-Mode Servo Disabled (CM bit set to 0).
- ❑ Overload level set to 5.1Vrms (OL bit set to 0)
- ❑ General-purpose digital output bits GPO1 through GPO4 are all set to 0.
- ❑ Gain set to 0dB (gain bits G0 through G5 are all set to 0).

Figure 5−1. Applications Software Main Panel



Clicking on the PGA2500 Panel button within the Main panel brings up a second window, which is referred to as the Device panel. The Device panel includes groups of objects, which are utilized to control various bits within the PGA2500 control word. Figure 5−2 shows the PGA2500 Device Panel.

Figure 5−2. Applications Software Device Panel



The Soft Mode Control group includes checkboxes for toggling the state of the DC servo ($\overline{DC}$), common-mode servo (CM), overload (OL), and GPO1 through GPO4 control bits. An empty checkbox sets the state of the corresponding bit to 0. Clicking on the checkbox will set the corresponding control bit to 1. Clicking on the checkbox again will clear the control bit, setting it to 0.

The Hard Mode Control group is not utilized for the PGA2500EVM. Instead, these controls are configured using switch SW1 on the PGA2500EVM.

The Gain group includes a slider for setting the gain of the PGA2500. Simple text displays are provided for the programmed gain in dB, as well as the gain and bus data shown in hexadecimal data format. A Readback button is provided with a corresponding text display, and may be used to read and display the control word value in hexadecimal data format. The Readback function is provided mainly as a software and hardware diagnostic function, because it allows the user to determine if the PGA2500 control word is being programmed correctly. This function can be used to debug hardware and cable connection problems, or to help identify possible software compatibility issues.

Finally, a Clear button is provided, which sets all of the data bits in the PGA2500 control word to 0.