19-3683; Rev 0; 5/05

Multiple-Output Clock Generator with Spread Spectrum

General Description

The MAX9492 frequency synthesizer is designed to generate multiple clocks for clock distribution in network routers or switches. The device provides a total of six buffered clock outputs (CLK1 to CLK6). CLK1 is the buffered output of the reference clock. CLK2 through CLK6 are independently programmable to generate eight different frequencies based on a 25MHz input crystal: 133, 125, 83, 66, 62.5, 50, 33, and 25MHz. All the outputs are LVCMOS single-ended signals. Either a 25MHz crystal or an external clock can serve as the input reference clock. The MAX9492 incorporates two phase-locked loops (PLLs) with two internal loop filters.

Select the MAX9492's output clock frequency by programming on-chip registers through the MAX9492's I²C interface. The device also features spread-spectrum capability to reduce electromagnetic interference (EMI). This technique allows spreading the fundamental energy over a wider frequency range, hence reducing the respective energy amplitude. The output frequency spectrum is downspread by -1.25% or -2.5%.

The MAX9492 operates from a 3.3V supply and is guaranteed over the extended temperature range (-40°C to +85°C). The device is available in a space-saving, 20-pin, TQFN, 5mm x 5mm package.

Applications

Network Routers

Telecom/Networking Equipment

Storage Area Networks/Network Attached Storage

Typical Operating Circuit and Pin Configuration appear at end of data sheet.

Features

- **Five LVCMOS Outputs with Independent Frequency Selections**
- **One Buffered Reference Clock Output**
- **Eight Selectable Frequencies: 133, 125, 83, 66, 62.5, 50, 33, and 25MHz**
- **Crystal or an Input-Clock-Based Clock Reference**
- **Output Frequency Programmed Through I²C Interface**
- **0, -1.25%, or -2.5% Selectable Downspreading Rate**
- **Low Output Period Jitter (Without Spread Spectrum) < $10ps_{RMS}$**
- **<220ps Output-to-Output Skew**
- **Available in 20-Lead, 5mm x 5mm, TQFN Package**
- **+3.3V Supply**
- **-40°C to +85°C Extended Temperature Range**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX9492ETP	-40°C to +85°C	20 Thin QFN-EP** 5mm x 5mm x 0.8mm	T2055-3

***EP = Exposed pad.*

Multiple-Output Clock Generator with Spread Spectrum

ABSOLUTE MAXIMUM RATINGS

$V_{DD\_}$ to GND .....-0.3V to +4.0V
All Other Pins to GND.....-0.3V to (V_{DD} + 1.0V)
Short-Circuit Duration (all LVCMOS outputs).....Continuous
ESD Protection (Human Body Model)..... ±2kV
Continuous Power Dissipation (T_A = +70°C)
20-Pin TQFN (derate 20.8mW/°C above +70°C) 1667mW
Storage Temperature Range .....-65°C to +165°C
Maximum Junction Temperature .....+150°C
Operating Temperature Range .....-40°C to +85°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{DD} = V_{DDA} = +3.0V to +3.6V, T_A = -40°C to +85°C, unless otherwise noted. Typical values at V_{DD} = V_{DDA} = +3.3V, T_A = +25°C, with CLK1 at 25MHz, and all other CLK_ outputs at 133MHz.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CLOCK INPUT (X1)						
Input High Level	V_{IH1}		2.0			V
Input Low Level	V_{IL1}				0.8	V
Input Current	I_{IL1}, I_{IH1}	$V_{X\_}$ = 0 to V_{DD}	-20		+20	µA
CLOCK OUTPUTS (CLK_)						
Output High Level	V_{OH}	I_{OH} = -100µA	V_{DD} - 0.2			V
		I_{OH} = -4mA	2.4			
Output Low Level	V_{OL}	I_{OL} = 100µA			0.2	V
		I_{OL} = 4mA			0.4	
Output Short-Circuit Current	I_{OS}	CLK_ = V_{DD} or GND	-60		+69	mA
Output Capacitance	C_O	(Note 2)			5	pF
THREE-LEVEL INPUTS (SSC, SA0, SA1)						
Input High Level	V_{IH2}		2.5			V
Input Low Level	V_{IL2}				0.8	V
Input Open Level	V_{IO2}		1.35		1.90	V
Input Current	I_{IL2}, I_{IH2}	V_{IL2} = 0 or V_{IH2} = V_{DD}	-15		+15	µA
SERIAL INTERFACE (SCL, SDA) (Note 3)						
Input High Level	V_{IH}		0.7 x V_{DD}			V
Input Low Level	V_{IL}				0.3 x V_{DD}	V
Input Leakage Current	I_{IH}, I_{IL}		-1		+1	µA
Low-Level Output	V_{OL}	I_{SINK} = 4mA			0.4	V
Input Capacitance	Ci	(Note 2)			10	pF
POWER SUPPLIES						
Digital Power-Supply Voltage	V_{DD}		3.0		3.6	V
Analog Power-Supply Voltage	V_{DDA}		3.0		3.6	V
Total Supply Current	I_{DC}	C_L = 10pF		60	76	mA
Output Disabled Supply Current	I_{OD}	All clock registers = 0x0F		18	24	mA

AC ELECTRICAL CHARACTERISTICS

(V_{DD} = V_{DDA} = +3.0V to +3.6V, C_L = 10pF, unless otherwise noted. Typical values at V_{DD} = V_{DDA} = +3.3V, T_A = +25°C, with CLK1 at 25MHz and all other CLK_ outputs at 133MHz.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
OUTPUTS (CLK_)						
Crystal Frequency			10		35	MHz
Input Frequency Range		External clock	15		35	MHz
Crystal Frequency Tolerance	Δf_A		-50		+50	ppm
Output-to-Output Skew	t_{SKO}	Any two CLK_ outputs			220	ps
Rise Time	t_{R1}	20% V_{DD} to 80% V_{DD}		1.9	2.5	ns
Fall Time	t_{F1}	80% V_{DD} to 20% V_{DD}		1.3	2.5	ns
Duty Cycle			40		60	%
Output Period Jitter	J_P	RMS (SSC = 0), CLK1 is disabled to high impedance		10	15	ps
Power-Up Time	t_{PO}	V_{DD} > 2.8V to PLL lock		2		ms
Frequency Spread		SSC = high		-2.5		%
		SSC = floating		-1.25		

SERIAL INTERFACE TIMING

(V_{DD} = V_{DDA} = +3.3V, T_A = -40°C to +85°C.) (Note 1, Figure 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Serial Clock	f_{SCL}				400	kHz
Bus Free Time Between STOP and START Conditions	t_{BUF}		1.3			µs
Hold Time, Repeated START Condition	$t_{HD,STA}$		0.6			µs
Repeated START Condition Setup Time	$t_{SU,STA}$		0.6			µs
STOP Condition Setup Time	$t_{SU,STO}$		0.6			µs
Data Hold Time	$t_{HD,DAT}$	(Note 4)	15		900	ns
Data Hold Time Slave	$t_{HD,DAT}$	(Note 4)	15		900	ns
Data Setup Time	$t_{SU,DAT}$		100			ns
SCL Clock Low Period	t_{LOW}		1.3			µs
SCL Clock High Period	t_{HIGH}		0.7			µs
Rise Time of SDA and SCL, Receiving	t_R	(Notes 2, 5)	20 + 0.1C_B		300	ns
Fall Time of SDA and SCL, Receiving	t_F	(Notes 2, 5)	20 + 0.1C_B		300	ns

Multiple-Output Clock Generator with Spread Spectrum

SERIAL INTERFACE TIMING (continued)

(V_{DD} = V_{DDA} = +3.3V, T_A = -40°C to +85°C.) (Note 1, Figure 1)

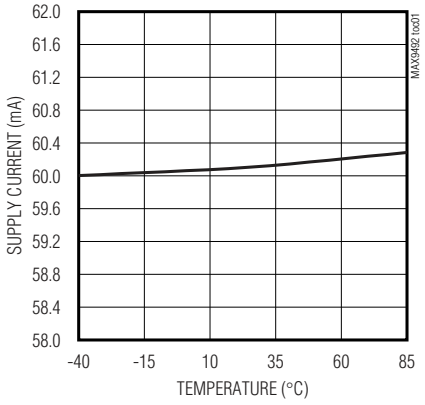
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Fall Time of SDA, Transmitting	$t_{F,TX}$	(Notes 2, 6)	20 + 0.1C_B		250	ns
Pulse Width of Spike Suppressed	t_{SP}	(Notes 2, 7)	0		50	ns
Capacitive Load for Each Bus Line	C_B	(Note 2)			400	pF

Note 1: All DC parameters tested at T_A = +25°C. Specifications over temperature are guaranteed by design.
Note 2: Guaranteed by design.
Note 3: No high output level is specified but only the output resistance to the bus. For I²C, the high-level voltage is provided by pullup resistors on the bus.
Note 4: The device provides a hold time of at least 300ns for the SDA signal (referred to V_{IL} of the SCL signal) to bridge the undefined region of SCL's falling edge.
Note 5: C_B = total capacitance of one bus line in pF. t_R and t_F measured between 0.3 x V_{DD} and 0.7 x V_{DD}.
Note 6: Bus sink current is less than 6mA. C_B is the total capacitance of one bus line in pF. t_R and t_F are measured between 0.3 x V_{DD} and 0.7 x V_{DD}.
Note 7: Input filters on the SDA and SCL inputs suppress noise spikes less than 50ns.

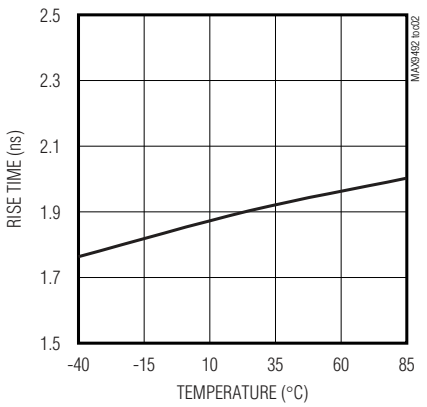
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

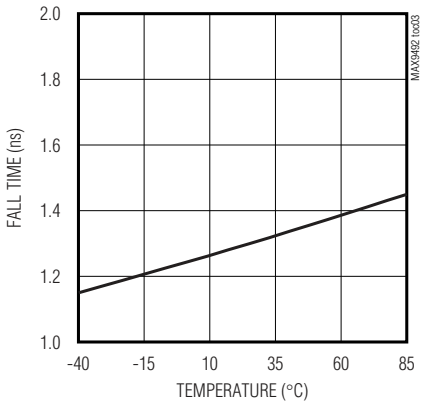
SUPPLY CURRENT vs. TEMPERATURE (ALL OUTPUTS SET TO 133MHz)



RISE TIME vs. TEMPERATURE (ALL OUTPUTS SET TO 133MHz)



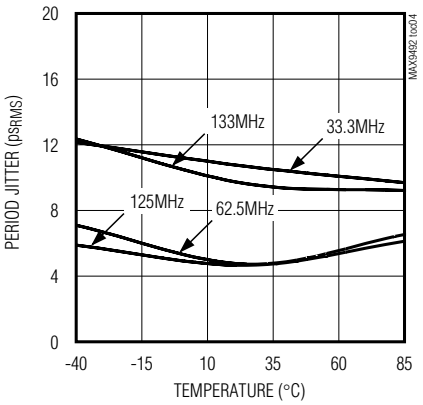
FALL TIME vs. TEMPERATURE (ALL OUTPUTS SET TO 133MHz)



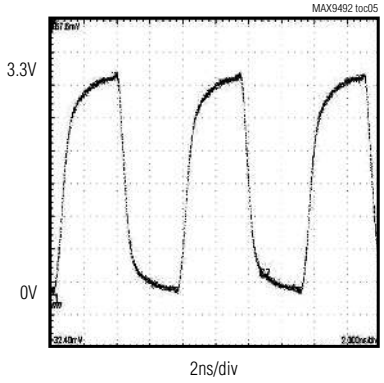
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

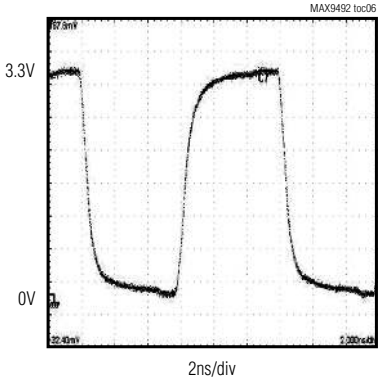
PERIOD JITTER vs. TEMPERATURE



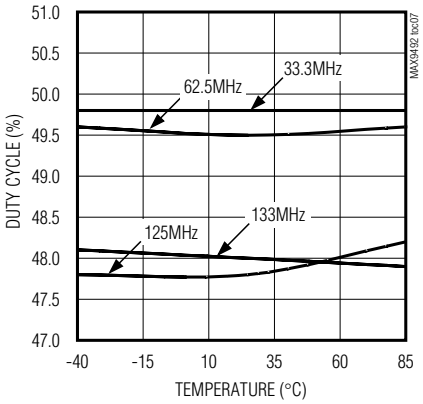
133MHz OUTPUT WAVEFORM



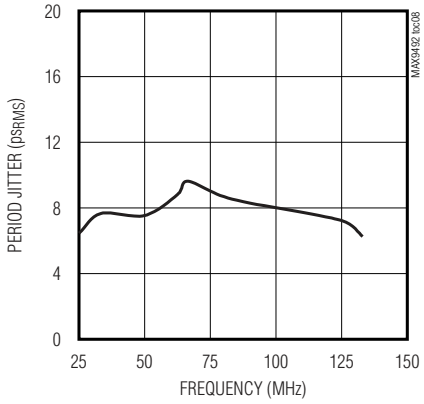
83MHz OUTPUT WAVEFORM



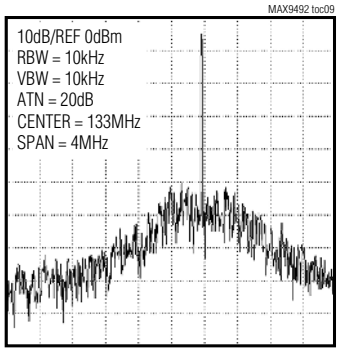
DUTY CYCLE vs. TEMPERATURE



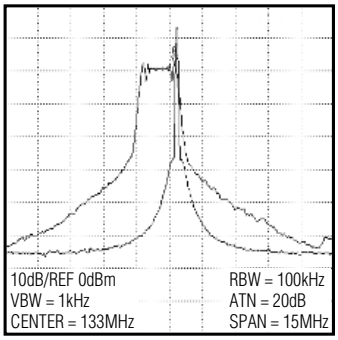
PERIOD JITTER vs. FREQUENCY



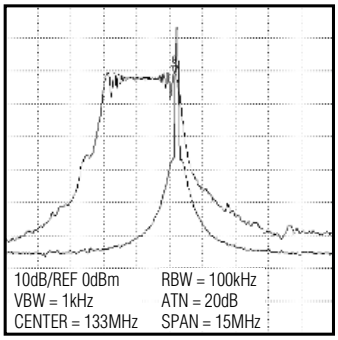
133MHz OUTPUT 0% DOWNSPREADING



133MHz OUTPUT WITH 0% AND 1.25% DOWNSPREADING



133MHz OUTPUT WITH 0% AND 2.5% DOWNSPREADING

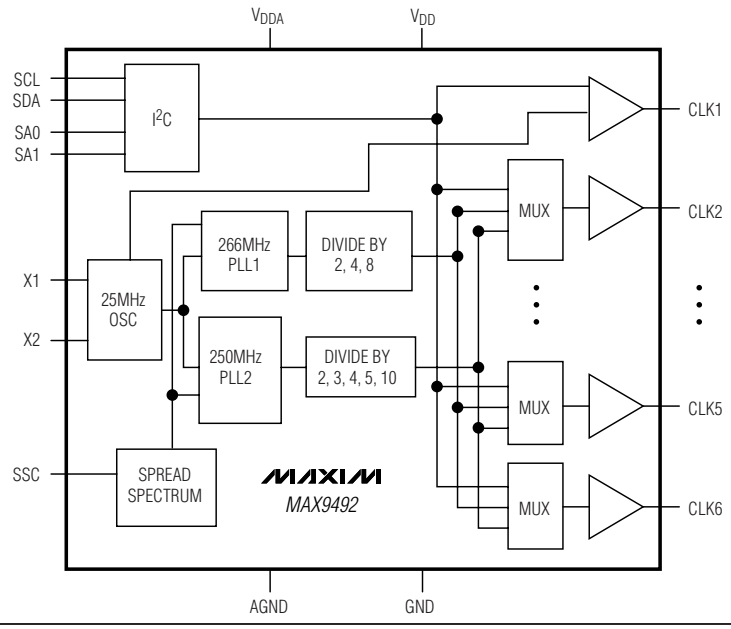


Multiple-Output Clock Generator with Spread Spectrum

Pin Description

PIN	NAME	FUNCTION
1	GNDA	Analog Ground
2	X1	Crystal Connection or Clock Input. If using a 25MHz crystal, connect it to X1 and X2. If using a reference clock, connect the clock signal to X1 and leave X2 floating. See the *Typical Operating Circuit*.
3	X2	
4	V_{DDA}	Power-Supply Input for Analog Circuits. Bypass to GNDA with a 0.1µF capacitor.
5, 13, 16	V_{DD}	Power-Supply Input for Digital Circuits. Bypass to GND with a 0.1µF capacitor.
6	SCL	Serial Clock Input. Serial interface clock.
7	SDA	Serial Data I/O. Data I/O of serial interface.
8, 20	GND	Digital Ground
9	CLK1	Clock 1 Output. Buffered reference clock output.
10	CLK2	Clock 2 Output. Frequency-selectable clock output.
11	CLK3	Clock 3 Output. Frequency-selectable clock output.
12	CLK4	Clock 4 Output. Frequency-selectable clock output.
14	CLK5	Clock 5 Output. Frequency-selectable clock output.
15	CLK6	Clock 6 Output. Frequency-selectable clock output.
17	SSC	Spread-Spectrum-Select Input. Selects the spectrum-spread percentage. When SSC is low, spread spectrum is disabled. When SSC is floating, spread spectrum is set to -1.25%. When SSC is high, spread spectrum is set to -2.5%.
18	SA1	Address-Select Inputs for Serial Interface. SA0 and SA1 select the serial interface address, as shown in Table 1. SA0 and SA1 are three-level inputs, making nine possible address combinations.
19	SA0	
EP	GND	Exposed pad. Connect to GND.

Block Diagram



Detailed Description

The MAX9492 frequency synthesizer is designed to generate multiple clocks for clock distribution in network routers or switches. The device provides a total of six buffered clock outputs (CLK1 to CLK6). CLK1 is the buffered output of the reference clock. CLK2 through CLK6 are independently programmable to generate eight different frequencies based on a 25MHz input crystal: 133, 125, 83, 66, 62.5, 50, 33, and 25MHz. All the outputs are LVCMOS single-ended signals.

Select the MAX9492's output frequency by programming on-chip registers through the I²C interface. The MAX9492 also features spread-spectrum capability to reduce EMI. Output frequency spectrum can be downspread by -2.5% or -1.25%. The 25MHz reference comes from either a crystal or an external clock. The MAX9492 incorporates two PLLs with two internal loop filters. The MAX9492 operates from a 3.3V supply.

Reference Frequency Input

The MAX9492 requires a reference frequency. The reference can be a 25MHz crystal or an external clock signal. If using a 25MHz crystal, connect it across X1 and X2, and connect loading capacitors from X1 and X2 to GND (refer to the crystal manufacturer's specification). If using an external clock, connect the signal to X1 and leave X2 floating.

Power-Up State

At power-up, the CLK1 output is enabled and free running, the CLK2 to CLK4 outputs are set at 33.3MHz, and the other CLK outputs are disabled at logic-low. The output states can be overridden by writing to the registers through the I²C interface.

Serial Interface

The MAX9492 is programmed through its I²C serial interface. This interface has a clock, SCL, and a bidirectional data line, SDA. In an I²C system, a master, typically a microcontroller, initiates all data transfers to and from slave devices, and generates the clock to synchronize the data transfers.

The MAX9492 operates as a slave device. The timing of the SDA and SCL signals is detailed in Figure 1. SDA operates as both an input and an open-drain output. A pullup resistor, typically 4.7kΩ, is required on SDA. SCL operates only as an input. A pullup resistor, typically 4.7kΩ, is required on SCL.

START and STOP Conditions

A master signals the beginning of a transmission with a START condition by transitioning SDA from high to low while SCL is high (Figure 2). When communication is complete, a master issues a STOP condition by transitioning SDA from low to high while SCL is high. The bus is then free for another transmission.

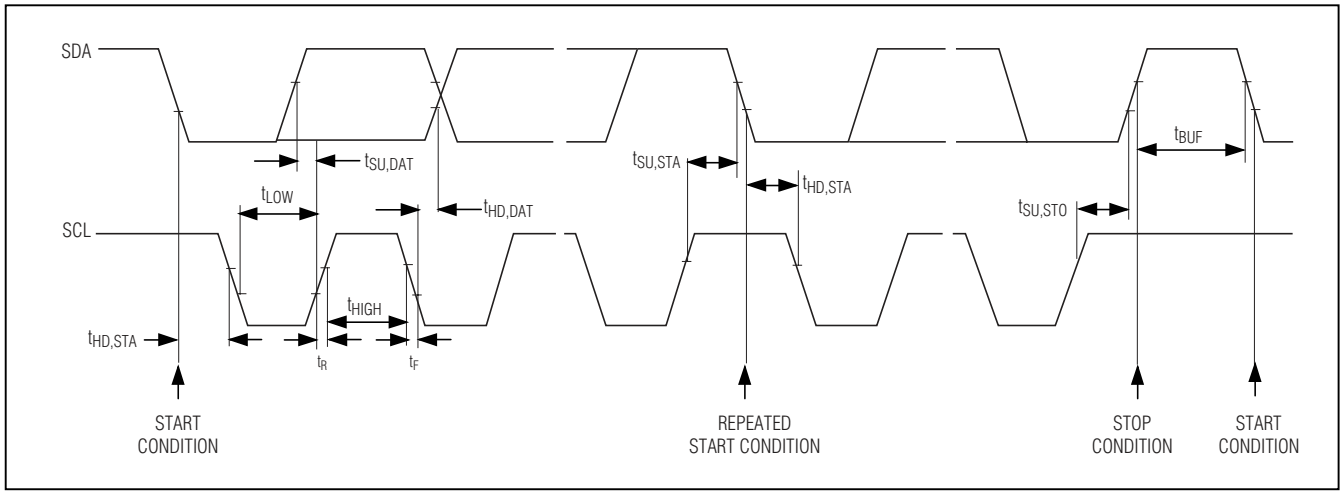


Figure 1. Serial-Interface Timing Diagram

Multiple-Output Clock Generator with Spread Spectrum

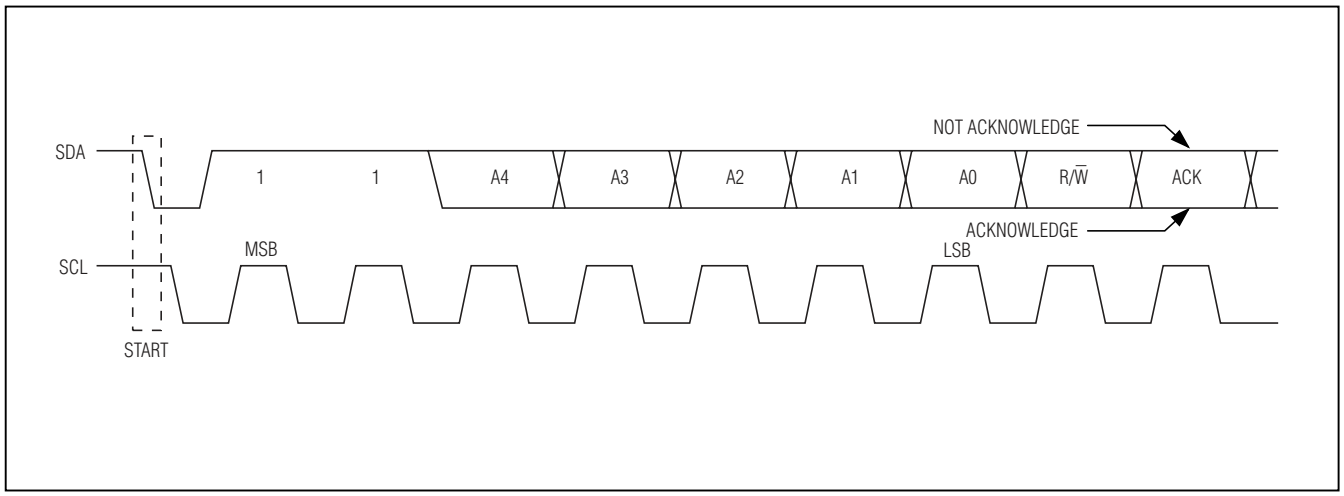


Figure 2. I²C Address and Acknowledge

Bit Transfer

One data bit is transferred during each SCL clock cycle. SDA must remain stable during the high period of SCL, as changes in SDA while SCL is high are START and STOP control signals. Idle the interface by pulling both SDA and SCL high.

After 8 bits are transferred, the receiving device generates an acknowledge signal by pulling SDA low for the entire duration of the 9th clock pulse. If the receiving device does not pull SDA low, a not acknowledge is indicated (Figure 2).

Table 1. Device I²C Address Selection

SA0	SA1	DEVICE ADDRESS
Open	Open	110 1000
Low	Open	110 0100
High	Open	110 0010
Open	Low	110 1100
Low	Low	110 1001
High	Low	111 0000
Open	High	111 0001
Low	High	111 0010
High	High	111 0100

Device Address

The MAX9492 features a 7-bit device address, configured by the two three-level address inputs, SA1 and SA0. To select the device address, connect SA1 and SA0 to V_{DD}, GND, or leave floating, as indicated in Table 1. The MAX9492 has nine possible addresses, allowing up to nine MAX9492 devices to share the same interface bus.

Writing to the MAX9492

Writing to the MAX9492 begins with a START condition (Figure 3). Following the START condition, each pulse on SCL transfers 1 bit of data. The first 7 bits comprise the device address (see the *Device Address* section). The 8th bit is low to indicate a write operation. An acknowledge bit is then generated by the MAX9492, signaling that it recognizes its address. The next 8 bits form the register address byte (Table 2) and determine which control register receives the following data byte. The MAX9492 then generates another acknowledge bit. The data byte is then written into the addressed register of the MAX9492. An acknowledge bit by the MAX9492 followed by a required STOP condition by the master completes the communication. To write to the device again, the entire write procedure is repeated; I²C burst-write mode is not supported by the MAX9492.

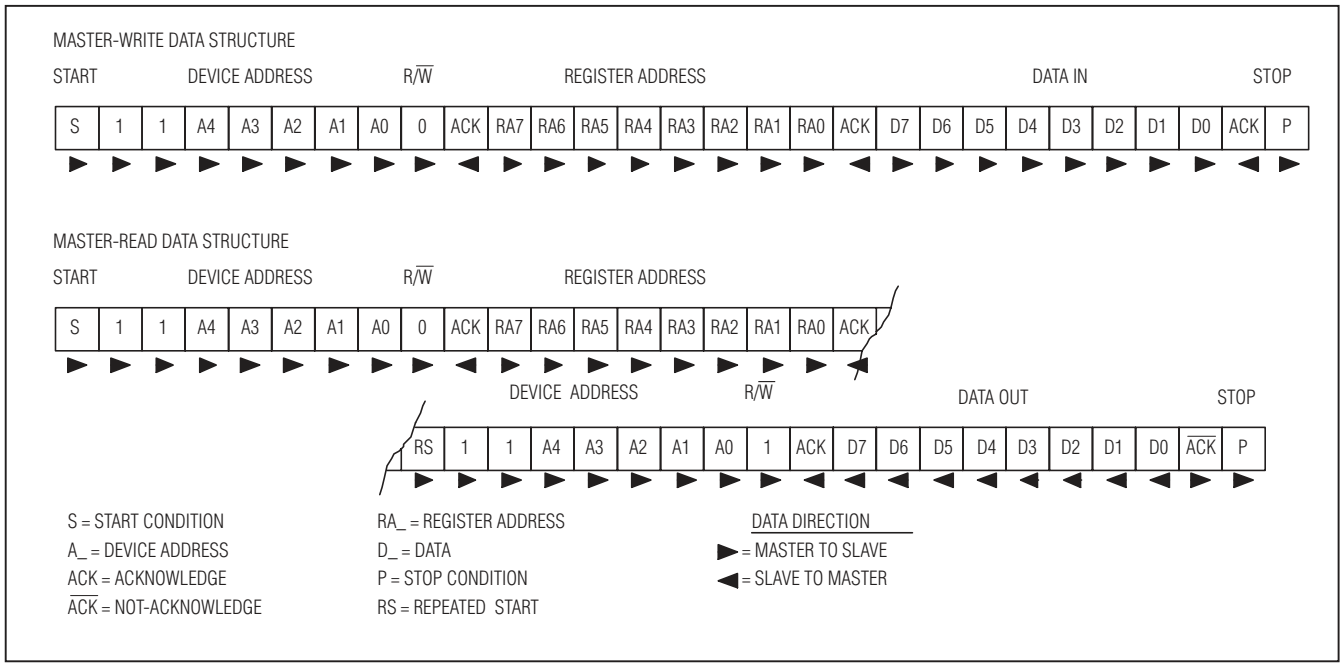


Figure 3. I²C Interface Data Structure

Reading from the MAX9492

Reading from the MAX9492 registers begins with a START condition and a device address with the write bit set low, then the register address that is to be read, followed by a repeated START condition and a device address with the write bit set high, and finally the data are shifted out (Figure 3). Following a START condition, the first 7 bits comprise the device address. The 8th bit is low to indicate a write operation (to write in the following register address). An acknowledge bit is then generated by the MAX9492, signaling that it recognizes its address. The next 8 bits form the register address, indicating the location of the data to be read, followed by another acknowledge, again generated by the MAX9492. The master then produces a repeated START condition and readdresess the device, with the R/$\overline{W}$ bit high to indicate a read operation (Figure 3). The MAX9492 generates an acknowledge bit, signaling that it recognizes its address. The data byte is then clocked out of the MAX9492. A final not-acknowledge bit, generated by the master (not required), and a STOP condition, also generated by the master, complete the communication. To read from the device again, the entire read procedure is repeated; I²C burst-read mode is not supported by the MAX9492.

Device Control Registers

The MAX9492 has eight control registers. The register addresses and functions are shown in Table 2. The first seven registers are used to set the six outputs, with register 0x00 controlling all outputs simultaneously, and the rest are mapped to individual outputs. All other addresses are reserved and are not to be used.

Table 2. Register Address Mapping

REGISTER ADDRESS	OUTPUT PORT
00	Broadcast to all CLK registers
01	CLK1
02	CLK2
03	CLK3
04	CLK4
05	CLK5
06	CLK6
All others	Reserved

Multiple-Output Clock Generator with Spread Spectrum

Setting the Clock Frequencies

Each CLK_ output has an associated control register. The contents of the registers determine the frequencies of their associated outputs. Table 3 provides the frequency mapping for the registers. CLK1 only responds to the 25MHz and high-impedance settings in Table 3. For example, writing 03h to the CLK1 control register does not change CLK1's output frequency to 133.3MHz. The CLK1 output continues to output a buffered reference clock signal.

Table 3. Output Frequency Selection for CLK1–CLK6

BITS IN CLKn REGISTERS	OUTPUT FREQUENCY (MHz)
00	Logic-Low
01	133.3
02	125
03	83.3
04	66.6
05	62.5
06	50
07	33.3
08	25
0F	High Impedance

Spread-Spectrum Control

The MAX9492 features spread-spectrum output structures to spread radiated emissions over the frequency band. A programmable triangle-wave generator injects an offset element into the master oscillator to dither its output by -1.25% or -2.5%. The dither is controlled by the SSC input. When SSC is low, spread spectrum is disabled. When SSC is floating, spread spectrum is set to -1.25%. When SSC is high, spread spectrum is set to -2.5%.

Power Supply

The MAX9492 uses a 3.0V to 3.6V power supply connected to V_{DD}, and 3.0V to 3.6V connected to V_{DDA}. Bypass V_{DDA} and V_{DD} at the device with a 0.1µF capacitor. Additionally, use bulk bypass capacitors of 10µF where power enters the circuit board.

Applications Information

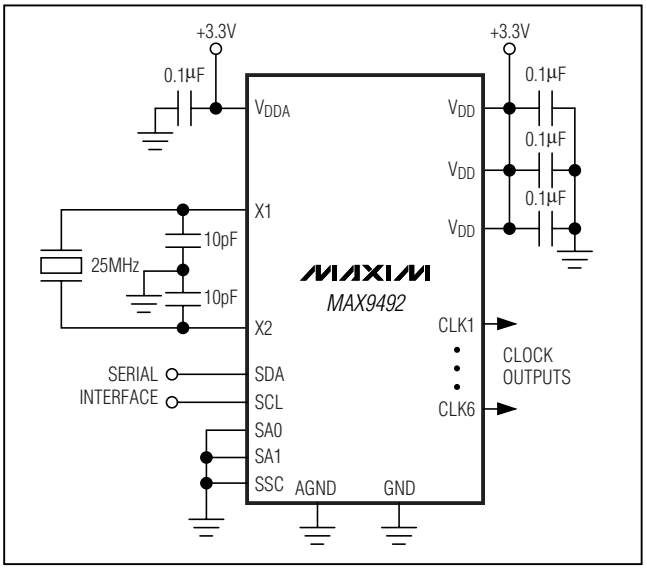
Board Layout Considerations

As with all high-frequency devices, board layout is critical to proper operation. Place the crystal as close as possible to X1 and X2, and minimize parasitic capacitance around the crystal leads. Ensure that the exposed pad makes good contact with GND.

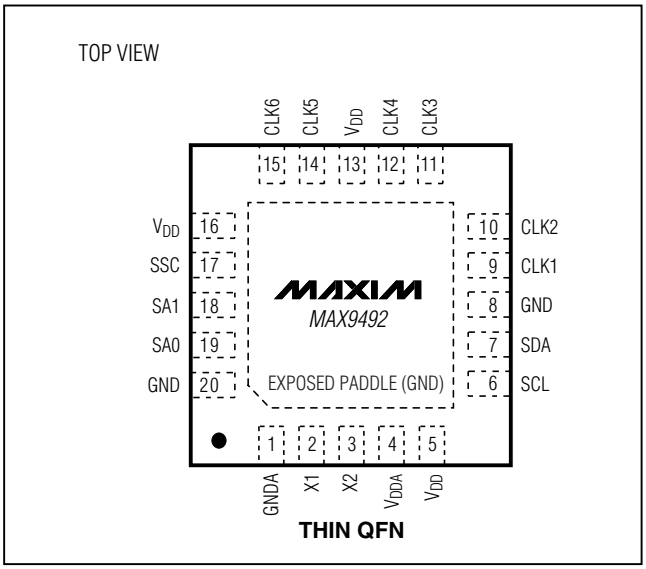
Chip Information

PROCESS: BiCMOS

Typical Operating Circuit

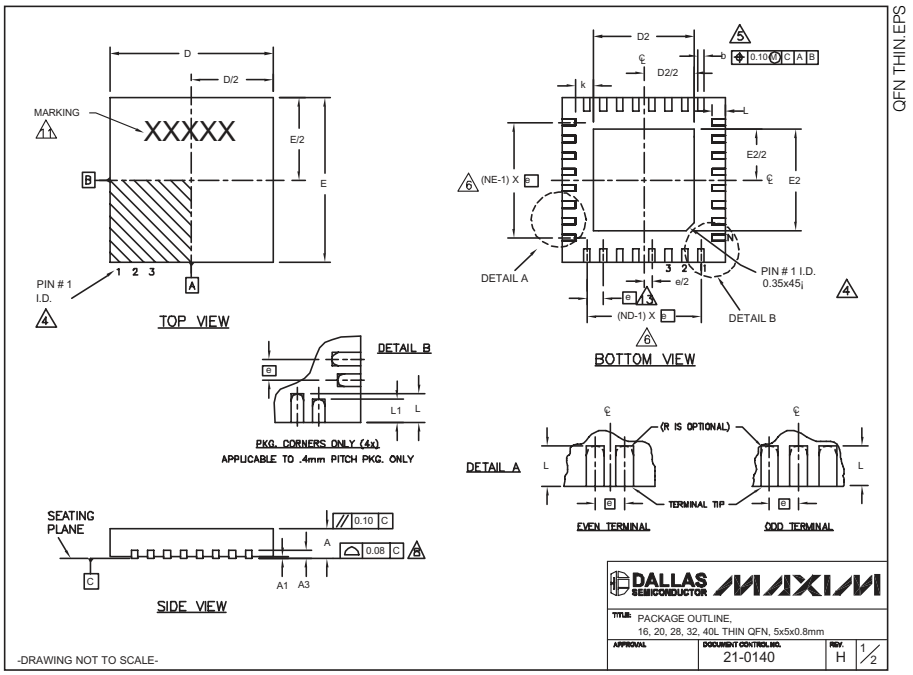


Pin Configuration



Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



COMMON DIMENSIONS

PKG.	16L 5x5			20L 5x5			28L 5x5			32L 5x5			40L 5x5		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05
A3	0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.		
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.20	0.25	0.30	0.15	0.20	0.25
D	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
E	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.			0.40 BSC.		
k	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-	0.25	0.35	0.45
L	0.30	0.40	0.50	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50	0.40	0.50	0.60
L1	-	-	-	-	-	-	-	-	-	-	-	-	0.30	0.40	0.50
N	16			20			28			32			40		
ND	4			5			7			8			10		
NE	4			5			7			8			10		
JEDEC	WHHB			WHHC			WHHD-1			WHHD-2			-----		

EXPOSED PAD VARIATIONS

PKG. CODES	D2			E2			L	DOWN BONDS ALLOWED
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	-0.15	
T1655-1	3.00	3.10	3.20	3.00	3.10	3.20	**	NO
T1655-2	3.00	3.10	3.20	3.00	3.10	3.20	**	YES
T1655N-1	3.00	3.10	3.20	3.00	3.10	3.20	**	NO
T2055-2	3.00	3.10	3.20	3.00	3.10	3.20	**	NO
T2055-3	3.00	3.10	3.20	3.00	3.10	3.20	**	YES
T2055-4	3.00	3.10	3.20	3.00	3.10	3.20	**	NO
T2055-5	3.15	3.25	3.35	3.15	3.25	3.35	0.40	YES
T2855-1	3.15	3.25	3.35	3.15	3.25	3.35	**	NO
T2855-2	2.60	2.70	2.80	2.60	2.70	2.80	**	NO
T2855-3	3.15	3.25	3.35	3.15	3.25	3.35	**	YES
T2855-4	2.60	2.70	2.80	2.60	2.70	2.80	**	YES
T2855-5	2.60	2.70	2.80	2.60	2.70	2.80	**	NO
T2855-6	3.15	3.25	3.35	3.15	3.25	3.35	**	NO
T2855-7	2.60	2.70	2.80	2.60	2.70	2.80	**	YES
T2855-8	3.15	3.25	3.35	3.15	3.25	3.35	0.40	YES
T2855N-1	3.15	3.25	3.35	3.15	3.25	3.35	**	NO
T3255-2	3.00	3.10	3.20	3.00	3.10	3.20	**	NO
T3255-3	3.00	3.10	3.20	3.00	3.10	3.20	**	YES
T3255-4	3.00	3.10	3.20	3.00	3.10	3.20	**	NO
T3255N-1	3.00	3.10	3.20	3.00	3.10	3.20	**	NO
T4055-1	3.20	3.30	3.40	3.20	3.30	3.40	**	YES

** SEE COMMON DIMENSIONS TABLE

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT EXPOSED PAD DIMENSION FOR T2855-1, T2855-3, AND T2855-6.
10. WARPAGE SHALL NOT EXCEED 0.10 mm.
11. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
12. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
13. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION "e", –0.05.

DALLAS SEMICONDUCTOR MAXIM
PACKAGE OUTLINE, 16, 20, 28, 32, 40L THIN QFN, 5x5x0.8mm
21-0140
H
2/2
-DRAWING NOT TO SCALE-