

MN54F175-X REV 1A0

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QUAD D FLIP-FLOP

General Description

The F175 is a high-speed quad D flip-flop. The device is useful for general flip-flop requirements where clock and clear inputs are common. The information on the D inputs is stored during the LOW-to-HIGH clock transition. Both true and complemented outputs of each flip-flop are provided. A Master Reset input resets all flip-flops, independent of the Clock or D inputs, when LOW.

Industry Part Number

54F175

NS Part Numbers

54F175DMQB
 54F175FMQB
 54F175LMQB

Prime Die

M175

Processing

MIL-STD-883, Method 5004

Quality Conformance Inspection

MIL-STD-883, Method 5005

| Subgrp | Description | Temp (°C) |
|--------|---------------------|------------|
| 1 | Static tests at | +25 |
| 2 | Static tests at | +125 |
| 3 | Static tests at | -55 |
| 4 | Dynamic tests at | +25 |
| 5 | Dynamic tests at | +125 |
| 6 | Dynamic tests at | -55 |
| 7 | Functional tests at | +25 |
| 8A | Functional tests at | +125 |
| 8B | Functional tests at | -55 |
| 9 | Switching tests at | +25 |
| 10 | Switching tests at | +125 |
| 11 | Switching tests at | -55 |

Features

- Edge-Triggered D-Type Inputs
- Buffered Positive Edge- Triggered Clock
- Asynchronous Common Reset
- True and Complement Output

(Absolute Maximum Ratings)

(Note 1)

| | |
|---|-------------------------|
| Storage Temperature | -65 C to +150 C |
| Ambient Temperature under Bias | -55 C to +125 C |
| Junction Temperature under Bias | -55 C to +175 C |
| Vcc Pin Potential to Ground Pin | -0.5V to +7.0V |
| Input Voltage (Note 2) | -0.5V to +7.0V |
| Input Current (Note 2) | -30 mA to +5.0mA |
| Voltage Applied to Output in HIGH State (with Vcc=0V) | |
| Standard Output | -0.5V to Vcc |
| TRI-STATE Output | -0.5V to +5.5V |
| Current Applied to Output in LOW State (Max) | twice the rated Iol(mA) |

Note 1: Absolute Maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

| | |
|------------------------------|-----------------|
| Free Air Ambient Temperature | |
| Commercial | 0 C to +70 C |
| Military | -55 C to +125 C |
| Supply Voltage | |
| Military | +4.5V to +5.5V |
| Commercial | +4.5V to +5.5V |

Electrical Characteristics

DC PARAMETER

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: VCC 4.5V to 5.5V, Temp range: -55C to 125C

| SYMBOL | PARAMETER | CONDITIONS | NOTES | PIN-NAME | MIN | MAX | UNIT | SUB-GROUPS |
|--------|-----------------------------|--|-------|----------|-----|------|------|------------|
| IIH | Input High Current | VCC=5.5V, VM=2.7V, VINH=5.5V | 1, 3 | INPUTS | | 20 | uA | 1, 2, 3 |
| IBVI | Input High Current | VCC=5.5V, VM=7.0V, VINH=5.5V | 1, 3 | INPUTS | | 100 | uA | 1, 2, 3 |
| IIL | Input LOW Current | VCC=5.5V, VM=0.5V | 1, 3 | INPUTS | | -0.6 | mA | 1, 2, 3 |
| VOL | Output LOW Voltage | VCC=4.5V, VIL=0.8V, IOL=20mA, VINH=5.5V, VINL=0.0V, VIH=2.0V | 1, 3 | OUTPUTS | | 0.5 | V | 1, 2, 3 |
| VOH | Output HIGH Voltage | VCC=4.5V, VIH=2.0V, IOH=-1.0mA, VIL=0.8V, VINL=0.0V | 1, 3 | OUTPUTS | 2.5 | | V | 1, 2, 3 |
| IOS | Short Circuit Current | VCC=5.5V, VINH=5.5V, VM=0.0V, VINL=0.0V | 1, 3 | OUTPUTS | -60 | -150 | mA | 1, 2, 3 |
| VCD | Input Clamp Diode Voltage | VCC=4.5V, IM=-18mA, VINH=5.5V | 1, 3 | INPUTS | | -1.2 | V | 1, 2, 3 |
| ICC | Supply Current | VCC=5.5V, VINH=5.5V | 1, 3 | VCC | | 34 | mA | 1, 2, 3 |
| ICEX | Output HIGH Leakage Current | VCC=5.5V, VINH=5.5V, VINL=0.0V, VM=5.5V | 1, 3 | OUTPUTS | | 250 | uA | 1, 2, 3 |

Electrical Characteristics

AC PARAMETER

(The following conditions apply to all the following parameters, unless otherwise specified.)
 AC: CL=50pf, RL=500 OHMS, TR=2.5ns, TF=2.5ns SEE AC FIGS

| SYMBOL | PARAMETER | CONDITIONS | NOTES | PIN-NAME | MIN | MAX | UNIT | SUB-GROUPS |
|---------|-------------------------|--|-------|----------------|-----|------|------|------------|
| tpLH(1) | Propagation Delay | VCC=5.0V @25C, VCC=4.5V & 5.5V @-55/125C | 2, 4 | CP to Qn or Qn | 4.0 | 6.5 | ns | 9 |
| | | | 2, 4 | CP to Qn or Qn | 3.5 | 8.5 | ns | 10, 11 |
| tpHL(1) | Propagation Delay | VCC= 5.0V @25C, VCC=4.5V & 5.5V @-55/125C | 2, 4 | CP to Qn or Qn | 4.0 | 8.5 | ns | 9 |
| | | | 2, 4 | CP to Qn or Qn | 4.0 | 10.5 | ns | 10, 11 |
| tpLH(2) | Propagation Delay | VCC= 5.0V @25C, VCC=4.5V & 5.5V @-55/125C | 2, 4 | MR to Qn | 4.0 | 8.0 | ns | 9 |
| | | | 2, 4 | MR to Qn | 4.0 | 10.0 | ns | 10, 11 |
| tpHL(2) | Propagation Delay | VCC= 5.0V @25C, VCC=4.5V & 5.5V @-55/125C | 2, 4 | MR to Qn | 4.5 | 11.5 | ns | 9 |
| | | | 2, 4 | MR to Qn | 4.5 | 15.0 | ns | 10, 11 |
| ts(H/L) | Setup Time | VCC= 5.0V @25C, VCC=4.5V & 5.5V @-55/125C | 5 | Dn to CP | 3.0 | | ns | 9, 10, 11 |
| th(H) | Hold Time | VCC=5.0V @25C, VCC=4.5V & 5.5V @-55/125C | 5 | Dn to CP | 1.0 | | ns | 9, 10, 11 |
| th(L) | Hold Time | VCC=5.0V @25C, VCC=4.5V & 5.5V @-55/125C | 5 | Dn to CP | 2.0 | | ns | 9, 10, 11 |
| tw(H) | Pulse Width | VCC=5.0V @25C, VCC=4.5V & 5.5V @-55/125C TR/TF=1.0ns | 5 | CP | 4.0 | | ns | 9, 10, 11 |
| tw(L) | Pulse Width | VCC=5.0V @25C, VCC=4.5V & 5.5V @-55/125C TR/TF=1.0ns | 5 | CP | 5.0 | | ns | 9, 10, 11 |
| tw (L) | Pulse Width | VCC=5.0V @25C, VCC=4.5V & 5.5V @-55/125C TR/TF=1.0ns | 5 | MR | 5.0 | | ns | 9, 10, 11 |
| tREC | Recovery Time | VCC=5.0V @25C, VCC=4.5V & 5.5V @-55/125C | 5 | MR to CP | 5.0 | | ns | 9, 10, 11 |
| fMAX | Maximum Count Frequency | VCC=5.0V @25C, VCC=4.5V & 5.5V @-55/125C TR/TF=1.0ns | 5 | | 100 | | MHZ | 9 |
| | | | 5 | | 80 | | MHZ | 10, 11 |

Note 1: Screen tested 100% on each device at +25C, +125C & -55C temperature, subgroups A1, 2, 3, 7 & 8.

Note 2: Screen tested 100% on each device at +25C temperature only, subgroup A9.

Note 3: Sample tested (Method 5005, Table 1) on each MFG. lot at +25C, +125C & -55C temperature, subgroups A1, 2, 3, 7 & 8.

Note 4: Sample tested (Method 5005, Table 1) on each MFG. lot at +25C subgroup A9, and periodically at +125C & -55C temperature, subgroups 10 & 11.

Note 5: GUARANTEED BUT NOT TESTED. (Design Characterization Data)