XIO2001

Evaluation Module (EVM)

User's Guide

TEXAS INSTRUMENTS

![Texas Instruments]

Contents

XIO2001 Evaluation Module (EVM)

Read This First

About This Manual

This manual describes the operation of the XIO2001 evaluation module (EVM) from Texas Instruments.

How to Use This Manual

This document contains the following sections:

- Overview
- EVM Features
- FAQ/Troubleshooting
- Schematics
- Bill of Materials

Information About Cautions and Warnings

This manual may contain cautions and warnings.

CAUTION

This is an example of a caution statement.

A caution statement describes a situation that could potentially damage your software or equipment.

WARNING

This is an example of a warning statement.

A warning statement describes a situation that could potentially cause harm to you.

Related Documentation from Texas Instruments

Related TI Documentation contains a list of data manuals that have detailed descriptions of the integrated circuits used in the design of the TAS3208EVM-LC. The data manuals can be obtained at www.ti.com.

Related TI Documentation

DOCUMENT	LITERATURE NUMBER
XIO2001 Implementation Guide	SCPA045
XIO2001 Data Manual	SCPS212

1 Overview

The XIO2001 evaluation board (EVM) implements a peripheral component interconnect (PCI) express to PCI bridge circuit using the Texas Instruments XIO2001 PCI Express to PCI Bus Translation Bridge. Designed as an ×1 add-in card, it is routed on FR4 as a 8-layer (4 signals, 2 power, and 2 ground) board with a 100-Ω differential impedance (50-Ω single-ended) using standard routing guidelines and requirements. [(1)]

Power for the XIO2001 EVM and any PCI add-in card connected to the EVM is provided or derived from the standard voltages provided on the PCI Express connector. Power for the 3.3-V rail is provided directly from the add-in connector, 5-V and 12-V is provided from the IDE power connector, while regulators are present to derive 1.5-V for the XIO2001 and -12-V for the PCI connectors.

Upon request, gerber files for the EVM can be provided that illustrate techniques that achieve fan-out of the μ*BGA, use of split power planes, placement of filters and other critical components, and methods used to match lengths on PCI and PCI Express signals on a standard 8-layer board.

Schematics and a Bill of Materials are provided to illustrate the design of this EVM.

> **NOTE:** Observe proper ESD procedures when handling the EVM. Failure to observe proper procedures may result in damage either to the EVM or the XIO2001 silicon which may cause the board to malfunction.

2 EVM Features

2.1 PCI Express Connector

The EVM is designed as a half-width PCI Express add-in card. The card fits into any standard ×1, ×2, ×4, ×8, or ×16 add-in connector that is compliant with the *PCI Express Electromechanical Specification*, Revision 2.0 or earlier. In addition to the standard transmit-and-receive pairs, the connector must supply 3.3 V, 12 V, $\overline{\text{PERST}}$, a 100-MHz differential clock, and V_{AUX}. The $\overline{\text{WAKE}}$ signal is also supported by the EVM although, as an optional pin, the system is not required to support this signal.

The height of the board is nonstandard due to the presence of PCI slots. Inserting PCI add-in cards into the EVM will, in most cases, prohibit the EVM from being placed in a case. If possible, provide some mechanical support to the EVM. Otherwise, the weight of PCI add-in cards can strain the board in the PCI Express add-in slot and may result in the board making poor contact with the connector. Poor connector contact can lead to signal integrity issues.

2.2 PCI Add-In Slots

The XIO2001 EVM provides three standard PCI add-in slots. While reversible, these slots, as shipped, are keyed as 5-V slots and provide a 5-V V_{IO} clamping voltage that provides accessibility to any 5-V or universally keyed PCI add-in cards. All standard voltages (3.3 V, 5 V, 12 V, and –12 V) are provided through the PCI connectors, enabling standard PCI add-in cards to function without requiring external power.

Cards placed into the PCI add-in slots must be inserted into the slots in accordance with labeling on the EVM. Referencing the component side of the EVM as front and the PCI express edge connector as down, boards must be inserted with the component side of the board down and the mounting bracket to the left of the EVM.

WARNING

Inserting either a 3.3-V card or a universally keyed card into the EVM backwards will damage the EVM and possibly the add-in card as well.

[(1)] As specified in *PCI Express Electromechanical Specification*, Revision 1.0a and *PCI Local Bus Specification*, Revision 2.3

The PCI bus operates at 66 MHz only when 66-MHz-capable PCI add-in cards are placed in the socket. If a 33-MHz card is inserted into the socket, then the XIO2001 detects the presence of the lower speed device and automatically sets the bus speed to 33 MHz. If 66-MHz operation is desired, place no more than two add-in cards into board slots. (This limitation is due to bus loading issues inherent to the PCI specification.) If a third 66-MHz device is added to the bus, signal integrity may still permit proper functioning of the interface, but such functionality cannot be assured and is beyond the scope of this document.

Two of the reserved pins on the PCI add-in connectors are used to route $\overline{PME}$ and V_{AUX} to any add-in cards. These assignments, while not part of the *PCI Local Bus Specification*, are used by many in the industry as de facto standards and must not interfere with any add-in cards. If cards are used that use these terminals for other purposes, the following modifications may be made to the EVM to isolate the signals from the PCI add-in connectors:

- $\overline{PME}$ (routed to reserved terminal A19 on each connector). Remove resistors R55, R53, and R54 (for slots 0, 1, and 2, respectively).

- V_{AUX} (routed to reserved terminal A14 on each connector). Remove resistors R50, R51, and R52 (for slots 0, 1, and 2, respectively).

2.3 EEPROM Interface

Each XIO2001 EVM provides an on-board EEPROM. As shipped, each EEPROM is programmed with values that will allow the EVM to function in most systems. The EEPROM interface is left as programmable (not write-protected) so that EEPROM contents may be modified for testing other optional settings. TI recommends that you do not change the EEPROM values. To change EEPROM contents, use the EEPROM access registers as detailed in the XIO2001 data manual or request the WinROM access tool.

2.4 Test Header

Each XIO2001 EVM provides accessibility to the GPIO pins on the XIO2001. From header J1, all five GPIOs have external visibility and can be used in any manner consistent with their functionality as detailed in the XIO2001 data manual. All GPIO signals are labeled on the header and are terminated with an on-board pullup resistor.

By default, GPIO3 and GPIO4 are configured as the EEPROM interface which was detailed in the previous section. The EEPROM interface can be removed from the XIO2001 by removing resistors R28 and R29. This allows these GPIO pins to be used for another purpose, although any configuration done by the EEPROM will then have to be done in some other fashion. While removing R28 and R29 will physically disconnect the EEPROM from GPIO3/GPIO4, in order to release the pins from this functionality, GPIO4 (SCL) must be held low at the deassertion of PERST. As no pulldown is available for this purpose, the pin must be externally shorted at boot time (deassertion of reset) by shorting J1 pin 5 to J1 pin 11. Once the system has booted, this short may be removed and GPIO3 and GPIO4 will be available for other uses.

Pin 9 on the J1 header is a global reset (GRST) for the XIO2001. Driving this pin low will cause all registers and state machines within the XIO2001 to return to a default power-up state. This pin generally must remain disconnected.

Pin 10 is an access point for the PME signal and may be used to externally wire this signal to any PCI add-in card that has the signal available but does not route the signal to pin A19 on the PCI expansion connector.

Pin 8 on header J1 is $\overline{CLKREQ}$ for the XIO2001. Driving this pin low will allow the REFCLK to stop when the XIO2001 is in PCI PM L1. The $\overline{CLKREQ}$ protocol as described in the PCI Express Base Specification and Express Card standard is supported.

Pin 7 on header J1 is $\overline{PERST}$ for the XIO2001. When asserted, this signal generates an internal PCI Express reset, clears all non-sticky bit registers and is deasserted when system power is stable.

Pin 12 on header J1 is PCLK66_SEL for the XIO2001 controlling the PCI clock frequency. When this signal is pulled high, the PCI clock will operate at 33 or 66 Mz depending on the state of M66EN. When this signal is low, the PCI clock will operate at 25 MHz or 50 MHz, depending on the state of M66EN. Most applications will pull this pin high.

Pin 2 on the connector is a 3.3-V test point and pin 11 is a ground test point. These signals may be used to externally toggle GPIOs for any required testing.

2.5 Clock Run ($\overline{CLKRUN}$)

The $\overline{CLKRUN}$ signal is a power-saving mechanism (defined in the *PCI Mobile Design Guide*) that stops the PCI bus clock when the bus is idle. Because devices that do not support this protocol are unable to restart the system clock, this feature is disabled by default on the XIO2001 EVM. This feature may be enabled to function with PCI add-in cards that also support this feature.

Enabling $\overline{CLKRUN}$ requires that resistor R24 be populated with a 0805 form factor 10-kΩ resistor. When this option is populated at the de-assertion of the reset pin, GPIO0 will internally map to $\overline{CLKRUN}$. When this happens, GPIO0 will be unavailable for other purposes. An external wire must then be connected from GPIO0/$\overline{CLKRUN}$ (available on J1 pin 1) to all add-in cards being tested with this functionality.

2.6 JTAG Header

Each XIO2001 EVM provides access to JTAG interface pins for boundary scan testing on test header JP1. The JTAG interface for the XIO2001 complies with IEEE standard 1149 using the standard 5 pin interface (TCK, TDI, TDO, TMS and $\overline{TRST}$). If boundary scan testing is not needed, TCK (JP1 pin 10) and $\overline{TRST}$ (JP1 pin 2) should be connected to GND (JP1 pins 1, 3, 5, 7 or 9). The remainder of the JTAG signals can be left unconnected. By default the EVM is configured with 0 Ω option resistors R40 and R77 that connect $\overline{TRST}$ and TCK to ground.

If boundary scan testing is needed, TI can provide the appropriate BDSL file upon request.

2.7 LEDs

The XIO2001 EVM has LEDs onboard to indicate availability of power and status of certain control signals. The onboard LEDs are as follows:

*   LED1: 5 V power indicator
*   LED2: 3.3 V power indicator
*   LED4: 12 V power indicator
*   LED5: –12 V power indicator

3   FAQ/Troubleshooting

To use the EVM

- Plug the PCI add-in cards into the EVM, oriented as indicated on the board
- Place the EVM into a PCI express add-in slot
- Turn the system on

From the operating system perspective, the XIO2001 appears to be a standard PCI-to-PCI bridge (PCI header type 1) and the OS will configure the bridge and any devices behind the bridge accordingly using legacy PCI configuration transactions. Following sections of this chapter describe issues that may impair use of the bridge in a system.

3.1   BIOS Fails to Assign Memory Window to Bridge

Microsoft operating systems generally attempt to respect the resource allocations made by system BIOS. The XIO2001 requires a memory window in order to access some registers used by the device. If the Microsoft OS determines that the BIOS failed to assign a memory window to the XIO2001, it will assume that one cannot be assigned and that the device is nonfunctional. The OS will then assume the bridge is not functional and will not enumerate devices behind the bus. Consequently, these devices will never be configured or assigned resources.

This failure can be determined by examining device manager in the OS. If failure has occurred, the bridge will appear "banged out" and if the bridge properties are examined the OS will reveal this device cannot find enough free resources that it can use. (Code 12) If you want to use this device, you will need to disable one of the other devices on this system.

3.2   ×16 Slots Only Support $\overline{INTA}$

As the x16 PCI express add-in slots are designed as a graphics expansion port, many only support a single interrupt (INTA), as this is the only interrupt that will be required by a graphics card. The XIO2001 EVM supports all interrupts and balances interrupt loading by rotating the interrupts to each add-in slot as required by the *PCI Local Bus Specification*. Accordingly, any PCI add-in card behind the bridge that asserts an interrupt other than INTA will not be serviced as the interrupt is not supported by the chipset. Consequently, the add-in card will fail. Any devices that do not require interrupts or that only assert INTA (as routed to the specific slot they are placed in) will still function normally.

3.3   System Turns On When PCI Card Is Inserted Into EVM Or When EVM Is Plugged Into Slot

As mentioned previously, PME is routed on the EVM to the various PCI slots through a reserved pin that many PCI add-in cards use for this purpose. On occasion, when a PCI card is inserted into the EVM (while the EVM is plugged into a board), the add-in card may be inserted in such a way as to pull the $\overline{PME}$ line low on the EVM. When this happens, the XIO2001 sees a PCI device trying to wake the system and will appropriately assert $\overline{WAKE}$, which may cause the system to turn on.

Similarly, when the EVM is inserted into the slot, V_{AUX} from the connector may not have had enough time to pull the $\overline{PME}$ line high (as the on-board pullup resistors dictate), yet V_{AUX} may have powered the XIO2001 which now samples $\overline{PME}$ as low and again wakes the system. This is a limitation of the inability to appropriately power the pullup resistors before the XIO2001 is powered. If this occurs, turn power to the system off and reboot to ensure the EVM receives a clean reset from the system.

3.4 *What To Do If EVM Is Not Working*

3.4.1 Check EVM Power

Diodes LED1, LED2, LED4 and LED5 show the status of the 5-V, 3.3-V, 12-V, and –12-V rails, respectively. 1.5 V may be probed on the top pad of C44 (directly next to U3), and –12 V may be probed from C100. A ground reference is available at J1 pin 11 and JP1 pins 2, 4, 6, 8 and 10. If any of these voltages fail, a problem is likely to occur with EVM functionality. The XIO2001 requires 3.3 V and 1.5 V; other voltages are supplied for use by PCI add-in cards, and PCI V_{IO} is by default 5 V (which will cause the entire PCI bus to be clamped to 0.7 V if this voltage is not present). If any of these voltages fail, it is likely that the EVM won't function because:

- XIO2001 will not be powered
- The add-in card will not be powered
- Neither the XIO2001 or the add-in card will be powered

All voltages have resettable fuses to prevent overcurrent conditions, so if a particular power rail fails:

- Detach all devices from the EVM
- Remove the EVM from the system
- Wait for 30 minutes before trying again

3.4.2 Check If Bridge Is Link Training

If the system does not boot, remove all PCI add-in cards from EVM and try again. If the system hangs before the OS loads, then probably the system and the EVM are having difficulty completing link training (probably an issue with signal integrity on the differential pairs). If a PCI Express analyzer is unavailable, then try a different express slot or a different system if possible. Re-check the 1.5-V rail and examine the differential clock on an oscilloscope to ensure it is clean.

If link training successfully completes, the system will boot and the XIO2001 will appear in the device manager. If the bridge does not appear in the device manager, then the system may not have detected the presence of the bridge, perform the previous checks again.

Also, if the PCI add-in cards have enough weight and there is no mechanical support, the EVM may flex and some components may crack or become disconnected. Check the coupling capacitors on the EVM transmit lines (C102 and C103). These 0.1-µF 0402 components have a tendency to crack if enough weight is put on the board; they will need to be replaced if they are damaged.

3.4.3 Check If Bridge Has Been Configured

Once the bridge is communicating with the system, the BIOS and/or the OS are expected to configure the bridge for proper operation. As the bridge appears to software to be a standard PCI-to-PCI bridge, most existing BIOS and OS software must be capable of configuring the bridge with no special considerations for PCI Express. In addition to the memory window the bridge requests for internal resources, the following items are required for bridge operation:

- Command register – PCI offset 0×4 : The bus master enable (bit 2), memory enable (bit 1), and I/O enable (bit 0) must be set to enable the bridge to send upstream transactions.
- Cache line size register – PCI offset 0×C : Must be set to the cache line size for the system. Failure to set this bit will not cause the bridge to fail but will cause the bridge to limit all upstream transactions to 1 DWord.
- Primary, secondary, and subordinate bus numbers– PCI offsets 0×18, 0×19, and 0×1A : The bridge must have the bus numbers configured so that it can determine which transactions are targeting the bridge, which transactions are targeting devices directly attached to the bridge, and which transactions are farther downstream from the bridge.
- I/O base and limit registers and I/O base upper 16 bits and I/O limit upper 16 bits registers –PCI offsets 0×1C, 0×1D, 0×30 and 0×32: If any devices downstream from the bridge require I/O resources, the bridge must be programmed with a window that contains the I/O resources of all devices downstream. Failure to program these windows will cause the bridge to respond to I/O transactions with a response of Unsupported Request. Any transactions initiated on the secondary side of the bus that fall within this

range will not be claimed by the bridge. The I/O window for the XIO2001 has a minimum size of 4 KBytes and is naturally 4K-aligned. Typically, most systems use only 16-bit addressing for I/O transactions, so the upper base and limit registers remain 0.

- Memory base and memory limit registers – PCI offsets 0×20 and 0×22 : Similar to the I/O base and limit registers, the bridge must be programmed with a memory address window containing the nonprefetchable memory resources of all downstream PCI devices requiring nonprefetchable memory. Memory windows have a minimum size of 1 MByte and are naturally 1M-aligned. The bridge does not claim either a memory transaction initiated from upstream that does not fall within its memory window nor memory transactions initiated downstream that do fall within its memory window.

- Prefetchable memory base, prefetchable memory limit, prefetchable base upper 32-bit, and prefetchable limit upper 32-bit registers – PCI offsets 0x24, 0x26, 0x28, and 0×2C: Identical to the memory base and limit registers but for prefetchable memory resources. The prefetchable base upper 32-bit, and prefetchable limit upper 32-bit registers are only used if 64-bit addressing is in use and in most systems both of these registers will remain all zeroes. If 64-bit addressing is desired and the memory window for devices behind the XIO2001 resides all or in part in 64-bit memory space then the prefetchable base upper 32-bit register will combine with the prefetchable base register and the prefetchable limit upper 32-bit register will combine with the prefetchable limit register to create 64-bit base and limit registers. All memory addresses between the two addresses will be considered to be located behind the bridge.

- For all base and limit registers any case in which the limit register contains a lower address than the base register will be considered invalid. In this situation the bridge will react as if all resources of that type resided upstream of the bridge. The bridge will respond to all downstream transactions of that type with Unsupported Request and will claim and forward upstream any transactions of that type that initiate on the PCI bus.
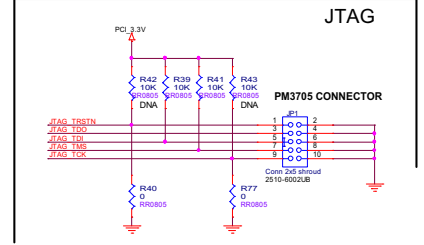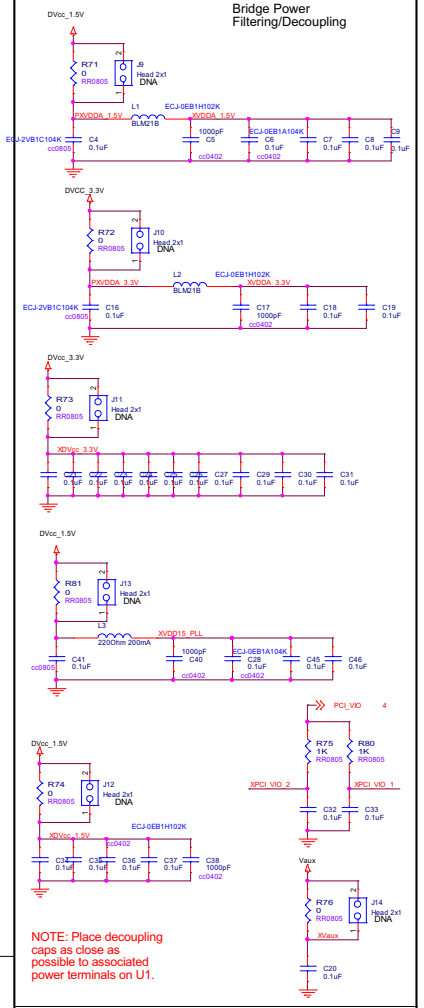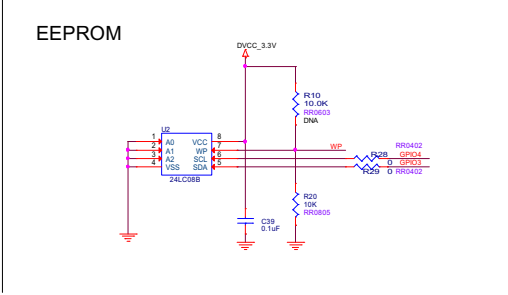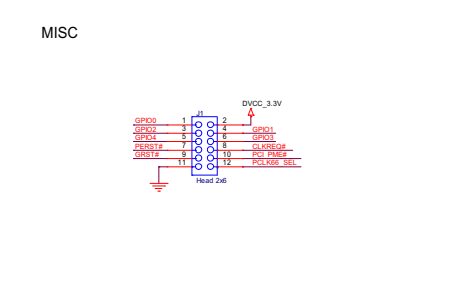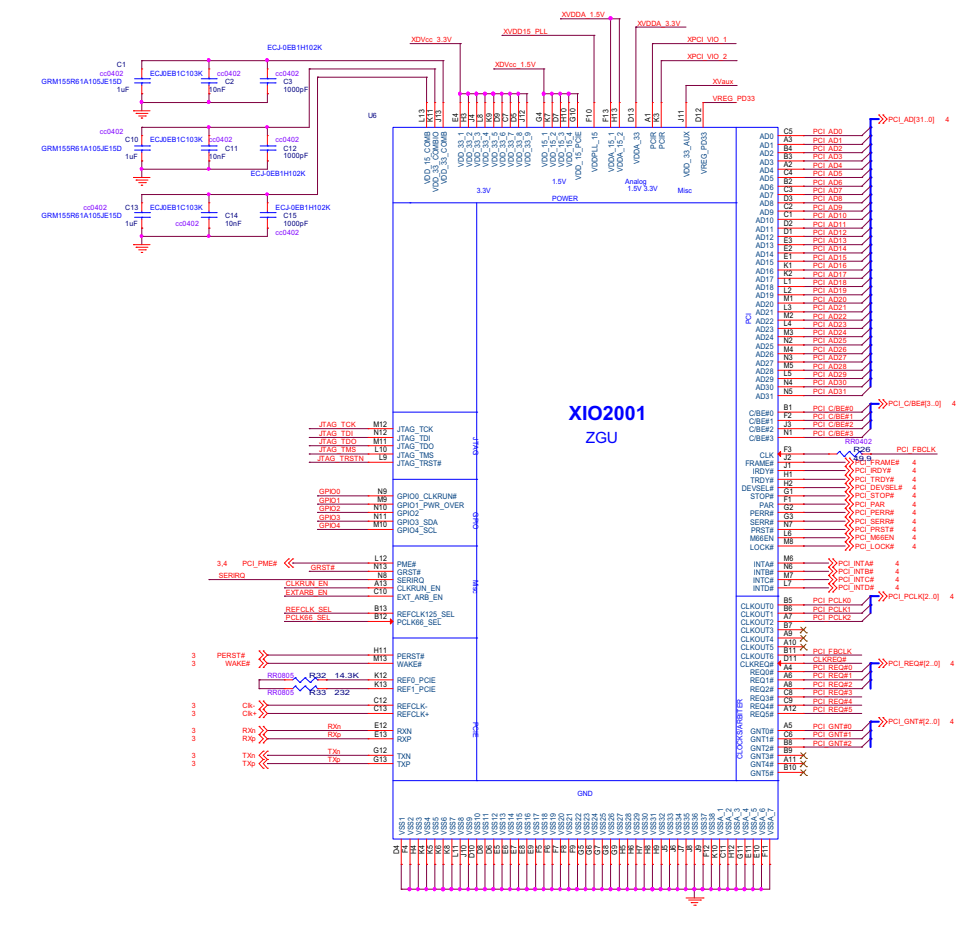
Depending on desired functionality, other PCI registers on the XIO2001 may have to be configured. Consult the *XIO2001 Data Manual* for a description of the previous registers or for any other XIO2001 registers.
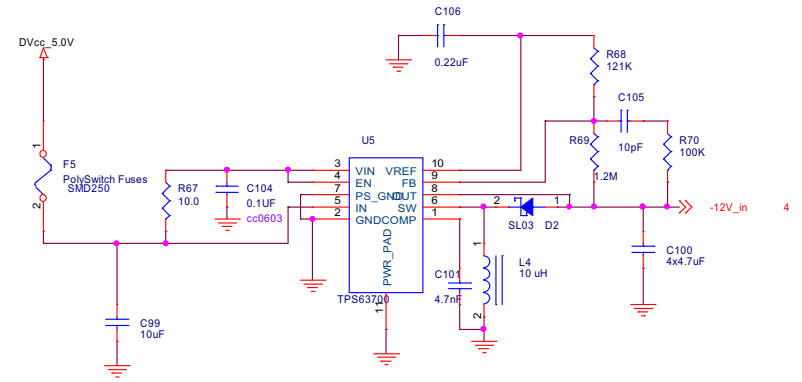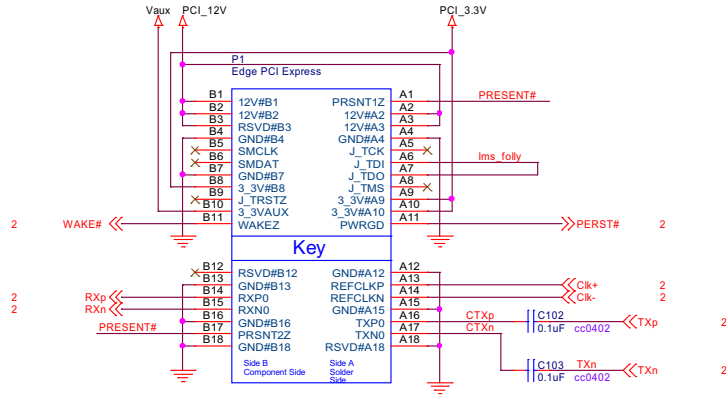
3.4.4   Check Devices Downstream From Bridge

Once the bridge is communicating and is properly configured, check if devices downstream from the bridge have been configured as required. Check the Windows Device Manager to determine if the device drivers have been loaded or if other problems exist with the device. Once you have performed these checks, you can perform PCI transactions on the bus and examine them with any standard PCI analyzer.
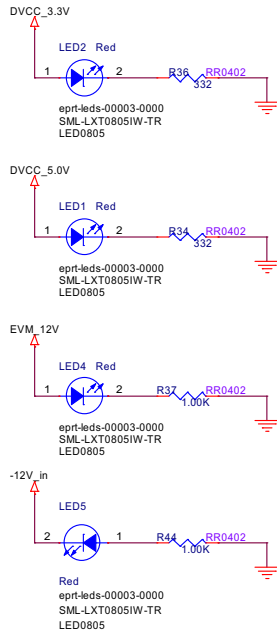
4   Schematics

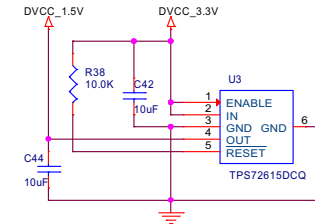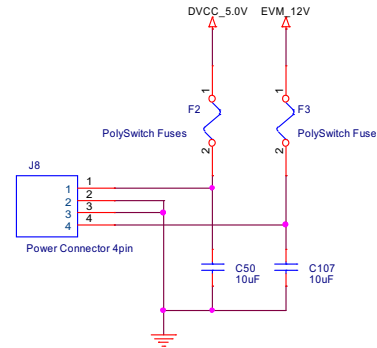Schematics for the XIO2001 EVM are shown on the following pages.

Bridge Power Filtering/Decoupling

Pull Ups/Pull Downs

XIO2001
ZGU

MISC

EEPROM

JTAG

NOTE: Place decoupling caps as close as possible to associated power terminals on U1.
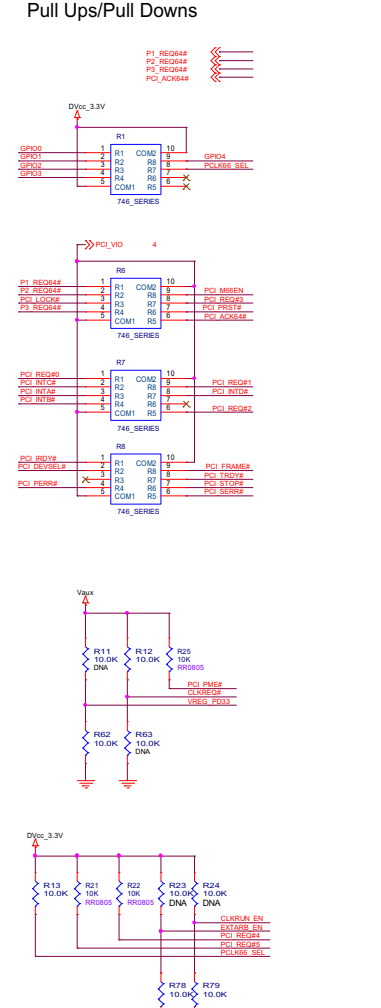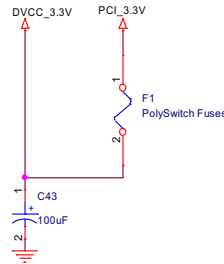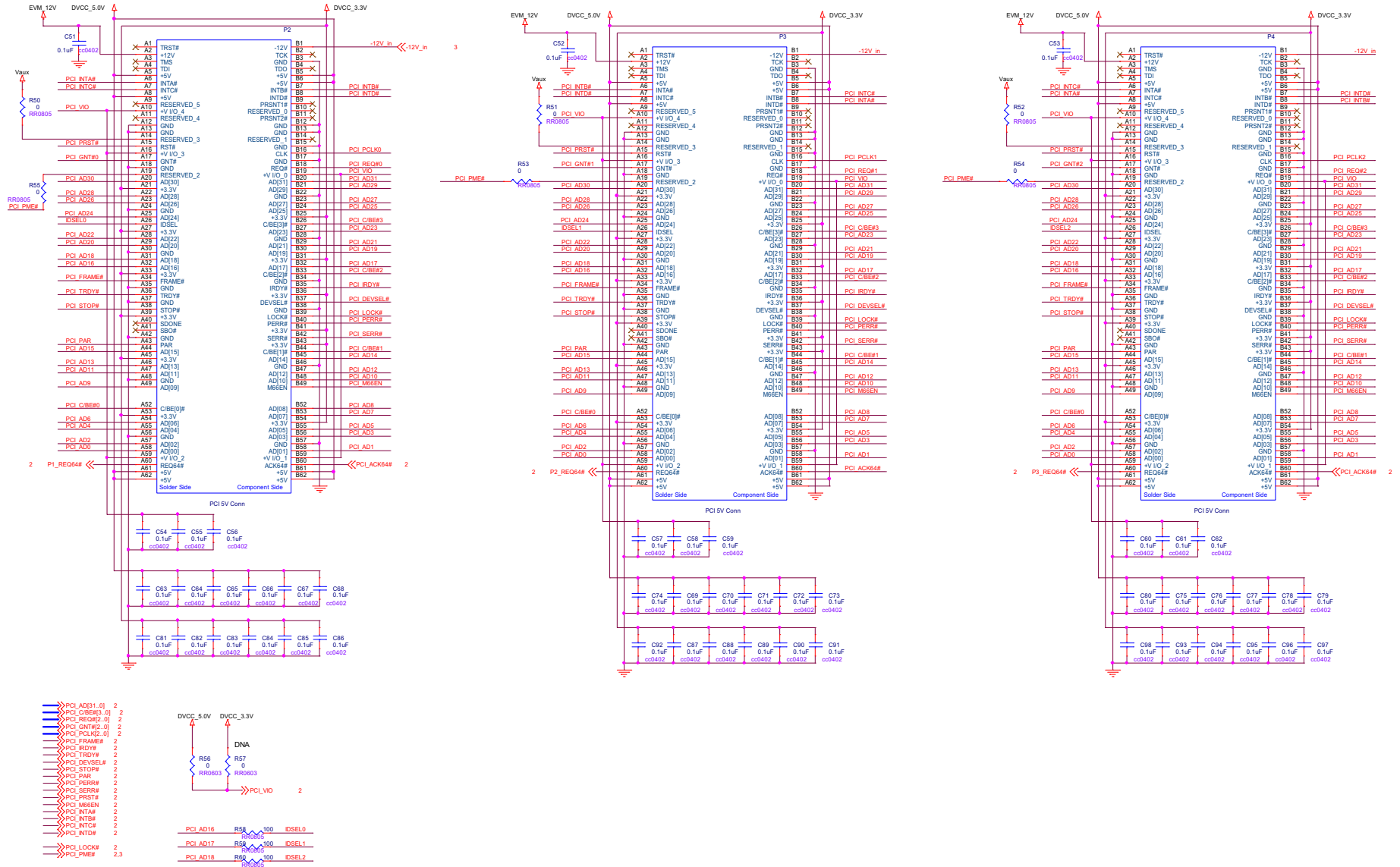
POWER LEDs

Power

5   Bill of Materials

Evaluation board bill of materials as assembled. Unused options (e.g., 3.3-V V_{IO}) are not populated and not listed.

Bill of Materials

ITEM	QTY	REFERENCE	VALUE	MFR	PART NO.	PACKAGE
1	3	C1, C10, C13	1 µF	Murata	GRM155R61A105JE15D	cc0402
2	3	C2, C11, C14	10 nF	Panasonic	ECJ0EB1C103K	cc0402
3	4	C3, C12, C15, C38	1000 pF	Panasonic	ECJ-0EB1H102K	cc0402
4	2	C4, C16	0.1 µF	Panasonic	ECJ-2VB1C104K	cc0805
5	2	C5, C17	0.001 µF	Panasonic	ECH-U1H102JB5	cc0805
6	72	C6, C7, C8, C9, C18, C19, C20, C21, C22, C23, C24, C25, C26, C27, C29, C3, C31, C32, C33, C34, C35, C36, C37, C39, C51, C52, C53, C54, C55, C56, C57, C58, C59, C60, C61, C62, C63, C64, C65, C66, C67, C68, C69, C70, C71 C72, C73, C74 C75, C76, C77, C78, C79, C80 C81, C82, C83, C84, C85, C86, C87, C88, C89, C90 C91, C92, C93, C94 C95, C96, C97, C98	0.1 µF	Panasonic	ECJ-0EB1A104K	cc0402
7	6	C42, C44, C50, C99, C100, C101	10 µF	Panasonic	ECJ-2FB1A106K	cc0805
8	1	C43	100 µF	Panasonic	ECA1EHG101	THCap_2P5MM
9	3	C45, C48, C49	22 µF	AVX	TAJC226K016R	cc6032
10	2	C46, C47	0.047 µF	Panasonic	ECJ1VB1C473K	cc0603
11	3	C102, C103, C104	0.1 µF	Kemet	C0603C104M4RACTU	cc0603
12	1	C105	10 pF	TDK	C1608C0G1H100DB	cc0603
13	1	C106	0.22 µF	Panasonic	ECJ1VB1A224K	cc0603
14	1	D1	MBRD835L	Diodes, Inc.	MBRD835L	DPAK_4
15	1	D2	SL03	Vishay	SL03D0-219AB-GS08	sl03_schottky_diode
16	4	F1, F2, F3, F5	Polyswitch fuses	Tyco Electronics	SMD250	SMD250
17	1	J1	Head 2 × 6	Berg	54102-T32-05	HDR_6X2
18	1	JP1	Conn 2 × 5 shroud	3M	2510-6002UB	eprt-conn-00002-0001
19	2	L1, L2	BLM21B	MuRata	BLM21BB221SN1	cc0805
20	1	L3	10 µH	Coiltronics	UP4B-100-R	IND_UP4B_100_R
21	1	L4	10 µH	Sumida	CDRH5D18NP-100NC	CDRH5D18
22	4	LED1, LED2, LED3, LED4	Red Lumex	Lumex	SML-LXT0805IW-TR	LED0805
23	1	LED5	Green	Lumex	SML-LXT0805GW-TR	LED0805
24	2	LED6, LED7	Yellow	Lumex	SML-LXT0805YW-TR	LED0805
25	1	P1	Edge PCI Express		DNA	eprt-conn- 00023-0000
26	3	P2, P3, P4	PCI 5 V conn	Tyco Electronics	145154-8	Conn_PCI_60_Dual
27	4	R1, R6, R7, R8	746_SERIES	CTS	746X101103JCT-ND?	10Pin_8Res
28	14	R2, R3, R4, R5, R19, R20, R21, R22, R25, R39, R41, R42, R43, R61	10K	Panasonic	ERJ6ENF1002V	RR0805
29	9	R10, R11, R12, R13, R23, R24, R38, R62, R63	10.0K	Panasonic	ERJ3EKF1002V	RR0603
30	2	R26, R35	49.9	Panasonic	ERJ2RKF49R9X	RR0402
31	2	R28, R29	0	Panasonic	ERJ2GE0R00X	RR0402
32	1	R32	14.3K	Panasonic	ERJ6ENF1432V	RR0805
33	1	R33	232	Panasonic	ERJ6ENF2320V	RR0805
34	2	R34,R36	332	Panasonic	ERJ2GEJ3320X	RR0402
35	1	R37	Conn 2 × 5 shroud	Panasonic	ERJ2RKF1001V	RR0402
36	7	R40, R50, R51, R52, R53, R54, R55	0	Panasonic	ERJ6ENF0000V	RR0805
37	1	R45	18.7K	Panasonic	ERJ6ENF1872V	RR0805
38	1	R47	6.19K	Panasonic	ERJ6ENF6191V	RR0805
39	1	R49	2K	Panasonic	ERJ6ENF2001V	RR0805

Bill of Materials (continued)

ITEM	QTY	REFERENCE	VALUE	MFR	PART NO.	PACKAGE
40	2	R56, R57	0	Panasonic	ERJ3GEY0R00V	RR0603
41	3	R58, R59, R60	100	Panasonic	ERJ6ENF1000V	RR0805
42	3	R64, R65, R66	332	Panasonic	ERAV39J3320V	RR0603
43	1	R67	10.0	Panasonic	ERJ2RKF10R0V	RR0402
44	1	R68	121K	Panasonic	ERJ2RKF1213X	RR0402
45	1	R69	1.2M	Vishay	CRCW0603	RR0603
46	1	R70	100K	Panasonic	ERJ2RKF1003V	RR0402
47	1	U2	24LC08B	Microchip	24LC08BIST	TSSOP_8_122X177_ 26
48	1	U3	TPS72615DCQ	Texas Instruments	TPS72615DCQ	TO_263_6_DCQ
49	1	U4	LT1370	Linear Technology	LT1370CR	DDPAK_R_7
50	1	U5	TPS63700	Texas Instruments	TPS63700DRCT	DRC_S_PVSON_N10
51	1	U6	XIO2001_ZAJ	Texas Instruments	XIO2001ZAJ	bga144ZAJ_0p5mm_ socket

Revision History

Changes from A Revision (February 2009) to B Revision   **Page**

ADDITIONAL TERMS AND CONDITIONS, WARNINGS, RESTRICTIONS, AND DISCLAIMERS FOR EVALUATION MODULES

Texas Instruments Incorporated (TI) markets, sells, and loans all evaluation boards, kits, and/or modules (EVMs) pursuant to, and user expressly acknowledges, represents, and agrees, and takes sole responsibility and risk with respect to, the following:

1. User agrees and acknowledges that EVMs are intended to be handled and used for feasibility evaluation only in laboratory and/or development environments. Notwithstanding the foregoing, in certain instances, TI makes certain EVMs available to users that do not handle and use EVMs solely for feasibility evaluation only in laboratory and/or development environments, but may use EVMs in a hobbyist environment. All EVMs made available to hobbyist users are FCC certified, as applicable. Hobbyist users acknowledge, agree, and shall comply with all applicable terms, conditions, warnings, and restrictions in this document and are subject to the disclaimer and indemnity provisions included in this document.

2. Unless otherwise indicated, EVMs are not finished products and not intended for consumer use. EVMs are intended solely for use by technically qualified electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems.

3. User agrees that EVMs shall not be used as, or incorporated into, all or any part of a finished product.

4. User agrees and acknowledges that certain EVMs may not be designed or manufactured by TI.

5. User must read the user's guide and all other documentation accompanying EVMs, including without limitation any warning or restriction notices, prior to handling and/or using EVMs. Such notices contain important safety information related to, for example, temperatures and voltages. For additional information on TI's environmental and/or safety programs, please visit www.ti.com/esh or contact TI.

6. User assumes all responsibility, obligation, and any corresponding liability for proper and safe handling and use of EVMs.

7. Should any EVM not meet the specifications indicated in the user's guide or other documentation accompanying such EVM, the EVM may be returned to TI within 30 days from the date of delivery for a full refund. THE FOREGOING LIMITED WARRANTY IS THE EXCLUSIVE WARRANTY MADE BY TI TO USER AND IS IN LIEU OF ALL OTHER WARRANTIES, EXPRESSED, IMPLIED, OR STATUTORY, INCLUDING ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR ANY PARTICULAR PURPOSE. TI SHALL NOT BE LIABLE TO USER FOR ANY INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES RELATED TO THE HANDLING OR USE OF ANY EVM.

8. No license is granted under any patent right or other intellectual property right of TI covering or relating to any machine, process, or combination in which EVMs might be or are used. TI currently deals with a variety of customers, and therefore TI's arrangement with the user is not exclusive. TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services with respect to the handling or use of EVMs.

9. User assumes sole responsibility to determine whether EVMs may be subject to any applicable federal, state, or local laws and regulatory requirements (including but not limited to U.S. Food and Drug Administration regulations, if applicable) related to its handling and use of EVMs and, if applicable, compliance in all respects with such laws and regulations.

10. User has sole responsibility to ensure the safety of any activities to be conducted by it and its employees, affiliates, contractors or designees, with respect to handling and using EVMs. Further, user is responsible to ensure that any interfaces (electronic and/or mechanical) between EVMs and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard.

11. User shall employ reasonable safeguards to ensure that user's use of EVMs will not result in any property damage, injury or death, even if EVMs should fail to perform as described or expected.

12. User shall be solely responsible for proper disposal and recycling of EVMs consistent with all applicable federal, state, and local requirements.

Certain Instructions. User shall operate EVMs within TI's recommended specifications and environmental considerations per the user's guide, accompanying documentation, and any other applicable requirements. Exceeding the specified ratings (including but not limited to input and output voltage, current, power, and environmental ranges) for EVMs may cause property damage, personal injury or death. If there are questions concerning these ratings, user should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the applicable EVM user's guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, some circuit components may have case temperatures greater than 60°C as long as the input and output are maintained at a normal ambient operating temperature. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors which can be identified using EVMs' schematics located in the applicable EVM user's guide. When placing measurement probes near EVMs during normal operation, please be aware that EVMs may become very warm. As with all electronic evaluation tools, only qualified personnel knowledgeable in electronic measurement and diagnostics normally found in development environments should use EVMs.

Agreement to Defend, Indemnify and Hold Harmless. User agrees to defend, indemnify, and hold TI, its directors, officers, employees, agents, representatives, affiliates, licensors and their representatives harmless from and against any and all claims, damages, losses, expenses, costs and liabilities (collectively, "Claims") arising out of, or in connection with, any handling and/or use of EVMs. User's indemnity shall apply whether Claims arise under law of tort or contract or any other legal theory, and even if EVMs fail to perform as described or expected.

Safety-Critical or Life-Critical Applications. If user intends to use EVMs in evaluations of safety critical applications (such as life support), and a failure of a TI product considered for purchase by user for use in user's product would reasonably be expected to cause severe personal injury or death such as devices which are classified as FDA Class III or similar classification, then user must specifically notify TI of such intent and enter into a separate Assurance and Indemnity Agreement.

RADIO FREQUENCY REGULATORY COMPLIANCE INFORMATION FOR EVALUATION MODULES

Texas Instruments Incorporated (TI) evaluation boards, kits, and/or modules (EVMs) and/or accompanying hardware that is marketed, sold, or loaned to users may or may not be subject to radio frequency regulations in specific countries.

General Statement for EVMs Not Including a Radio

For EVMs not including a radio and not subject to the U.S. Federal Communications Commission (FCC) or Industry Canada (IC) regulations, TI intends EVMs to be used only for engineering development, demonstration, or evaluation purposes. EVMs are not finished products typically fit for general consumer use. EVMs may nonetheless generate, use, or radiate radio frequency energy, but have not been tested for compliance with the limits of computing devices pursuant to part 15 of FCC or the ICES-003 rules. Operation of such EVMs may cause interference with radio communications, in which case the user at his own expense will be required to take whatever measures may be required to correct this interference.

General Statement for EVMs including a radio

User Power/Frequency Use Obligations: For EVMs including a radio, the radio included in such EVMs is intended for development and/or professional use only in legally allocated frequency and power limits. Any use of radio frequencies and/or power availability in such EVMs and their development application(s) must comply with local laws governing radio spectrum allocation and power limits for such EVMs. It is the user's sole responsibility to only operate this radio in legally acceptable frequency space and within legally mandated power limitations. Any exceptions to this are strictly prohibited and unauthorized by TI unless user has obtained appropriate experimental and/or development licenses from local regulatory authorities, which is the sole responsibility of the user, including its acceptable authorization.

U.S. Federal Communications Commission Compliance

For EVMs Annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant

Caution

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation. Changes or modifications could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at its own expense.

FCC Interference Statement for Class B EVM devices

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Industry Canada Compliance (English)

For EVMs Annotated as IC – INDUSTRY CANADA Compliant:

This Class A or B digital apparatus complies with Canadian ICES-003.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

Concerning EVMs Including Radio Transmitters

This device complies with Industry Canada licence-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concerning EVMs Including Detachable Antennas

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication.

This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Canada Industry Canada Compliance (French)

Cet appareil numérique de la classe A ou B est conforme à la norme NMB-003 du Canada

Les changements ou les modifications pas expressément approuvés par la partie responsable de la conformité ont pu vider l'autorité de l'utilisateur pour actionner l'équipement.

Concernant les EVMs avec appareils radio

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes : (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante.

Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur.

Important Notice for Users of EVMs Considered "Radio Frequency Products" in Japan

EVMs entering Japan are NOT certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If user uses EVMs in Japan, user is required by Radio Law of Japan to follow the instructions below with respect to EVMs:

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after user obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after user obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless user gives the same notice above to the transferee. Please note that if user does not follow the instructions above, user will be subject to penalties of Radio Law of Japan.

http://www.tij.co.jp

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