Freescale Semiconductor
Technical Data

Document Number: MRF6S18100N
Rev. 2, 12/2008

RoHS

RF Power Field Effect Transistors

N-Channel Enhancement-Mode Lateral MOSFETs

MRF6S18100NR1
MRF6S18100NBR1

1805-1990 MHz, 100 W, 28 V
GSM/GSM EDGE
LATERAL N-CHANNEL
RF POWER MOSFETs

Designed for GSM and GSM EDGE base station applications with frequencies from 1800 to 2000 MHz. Suitable for TDMA, CDMA and multicarrier amplifier applications.

GSM Application

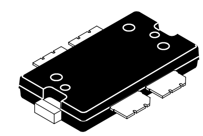
- Typical GSM Performance: V_{DD} = 28 Volts, I_{DQ} = 900 mA, P_{out} = 100 Watts, f = 1990 MHz
  Power Gain — 14.5 dB
  Drain Efficiency — 49%

GSM EDGE Application

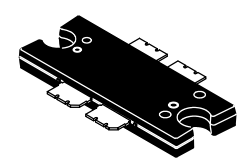
- Typical GSM EDGE Performance: V_{DD} = 28 Volts, I_{DQ} = 700 mA, P_{out} = 40 Watts Avg., Full Frequency Band (1805-1880 MHz or 1930-1990 MHz)
  Power Gain — 15 dB
  Drain Efficiency — 35%
  Spectral Regrowth @ 400 kHz Offset = -63 dBc
  Spectral Regrowth @ 600 kHz Offset = -76 dBc
  EVM — 2% rms
- Capable of Handling 5:1 VSWR, @ 28 Vdc, 1990 MHz, 100 Watts CW Output Power

Features

- Characterized with Series Equivalent Large-Signal Impedance Parameters
- Internally Matched for Ease of Use
- Qualified Up to a Maximum of 32 V_{DD} Operation
- Integrated ESD Protection
- Designed for Lower Memory Effects and Wide Instantaneous Bandwidth Applications
- 225°C Capable Plastic Package
- RoHS Compliant
- In Tape and Reel. R1 Suffix = 500 Units per 44 mm, 13 inch Reel.



CASE 1486-03, STYLE 1
TO-270 WB-4
MRF6S18100NR1



CASE 1484-04, STYLE 1
TO-272 WB-4
MRF6S18100NBR1

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	-0.5, +68	Vdc
Gate-Source Voltage	V_{GS}	-0.5, +12	Vdc
Storage Temperature Range	T_{stg}	- 65 to +150	°C
Case Operating Temperature	T_C	150	°C
Operating Junction Temperature (1,2)	T_J	225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value (2,3)	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$		°C/W
Case Temperature 80°C, 100 CW		0.51	
Case Temperature 77°C, 40 CW		0.62	

1. Continuous use at maximum temperature will affect MTTF.
2. MTTF calculator available at http://www.freescale.com/rf. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.
3. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.freescale.com/rf. Select Documentation/Application Notes - AN1955.

freescale semiconductor

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22-A114)	1B (Minimum)
Machine Model (per EIA/JESD22-A115)	A (Minimum)
Charge Device Model (per JESD22-C101)	IV (Minimum)

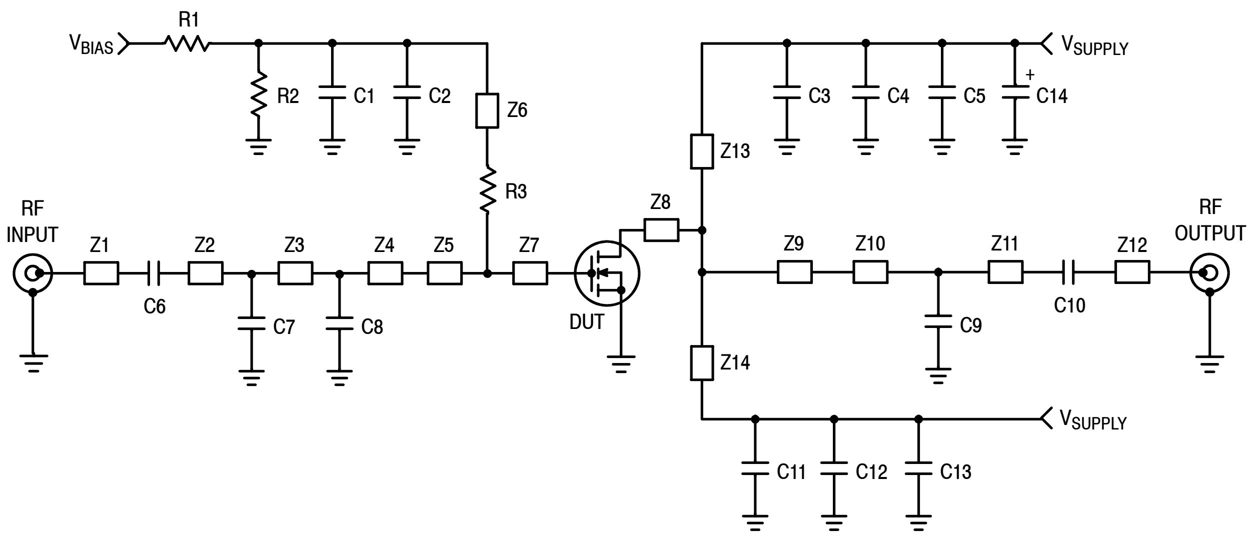
Table 4. Moisture Sensitivity Level

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD22-A113, IPC/JEDEC J-STD-020	3	260	°C

Table 5. Electrical Characteristics (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Off Characteristics					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 68 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 28 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate-Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	500	nAdc
On Characteristics					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 330 μAdc)	$V_{GS(th)}$	1.6	2	3	Vdc
Gate Quiescent Voltage (V_{DD} = 28 Vdc, I_D = 900 mAdc, Measured in Functional Test)	$V_{GS(Q)}$	1.5	2.8	3.5	Vdc
Drain-Source On-Voltage (V_{GS} = 10 Vdc, I_D = 3.3 Adc)	$V_{DS(on)}$	—	0.24	—	Vdc
Dynamic Characteristics(1)					
Reverse Transfer Capacitance (V_{DS} = 28 Vdc ± 30 mV(rms)ac @ 1 MHz, V_{GS} = 0 Vdc)	C_{rss}	—	1.5	—	pF
Functional Tests (In Freescale Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, P_{out} = 100 W, I_{DQ} = 900 mA, f = 1990 MHz					
Power Gain	G_{ps}	13	14.5	16	dB
Drain Efficiency	η_D	47	49	—	%
Input Return Loss	IRL	—	-12	-9	dB
P_{out} @ 1 dB Compression Point	P1dB	100	110	—	W
Typical GSM EDGE Performances (In Freescale GSM EDGE Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ} = 700 mA, P_{out} = 40 W Avg., 1805-1880 MHz or 1930-1990 MHz EDGE Modulation					
Power Gain	G_{ps}	—	15	—	dB
Drain Efficiency	η_D	—	35	—	%
Error Vector Magnitude	EVM	—	2	—	% rms
Spectral Regrowth at 400 kHz Offset	SR1	—	-63	—	dBc
Spectral Regrowth at 600 kHz Offset	SR2	—	-76	—	dBc
Typical CW Performances (In Freescale GSM Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ} = 900 mA, P_{out} = 100 W, 1805-1880 MHz					
Power Gain	G_{ps}	—	14.5	—	dB
Drain Efficiency	η_D	—	49	—	%
Input Return Loss	IRL	—	-12	—	dB
P_{out} @ 1 dB Compression Point	P1dB	—	110	—	W

1. Part internally matched both on input and output.



Z1, Z12	0.250″ x 0.083″ Microstrip	Z9	0.485″ x 1.000″ Microstrip
Z2*	0.450″ x 0.083″ Microstrip	Z10*	0.590″ x 0.083″ Microstrip
Z3*	0.535″ x 0.083″ Microstrip	Z11*	0.805″ x 0.083″ Microstrip
Z4*	0.540″ x 0.083″ Microstrip	Z13, Z14	0.870″ x 0.080″ Microstrip
Z5	0.365″ x 1.000″ Microstrip	PCB	Taconic TLX8-0300, 0.030″, ε_r = 2.55
Z6	1.190″ x 0.080″ Microstrip	*Variable for tuning.	
Z7, Z8	0.115″ x 1.000″ Microstrip		

Figure 1. MRF6S18100NR1(NBR1) Test Circuit Schematic — 1930-1990 MHz

Table 6. MRF6S18100NR1(NBR1) Test Circuit Component Designations and Values — 1930-1990 MHz

Part	Description	Part Number	Manufacturer
C1	100 nF Chip Capacitor	12065C104KAT	AVX
C2, C3, C6, C10, C11	6.8 pF Chip Capacitors	ATC100B6R8BT500XT	ATC
C4, C5, C12, C13	4.7 μF Chip Capacitors	C4532X5R1H475MT	TDK
C7	0.3 pF Chip Capacitor	ATC700B0R3BT500XT	ATC
C8	1.3 pF Chip Capacitor	ATC100B1R3BT500XT	ATC
C9	0.5 pF Chip Capacitor	ATC100B0R5BT500XT	ATC
C14	470 μF, 63 V Electrolytic Capacitor, Radial	EKME630ELL471MK25S	Multicomp
R1, R2	10 kΩ, 1/4 W Chip Resistors	CRCW12061002FKEA	Vishay
R3	10 Ω, 1/4 W Chip Resistor	CRCW120610R0FKEA	Vishay

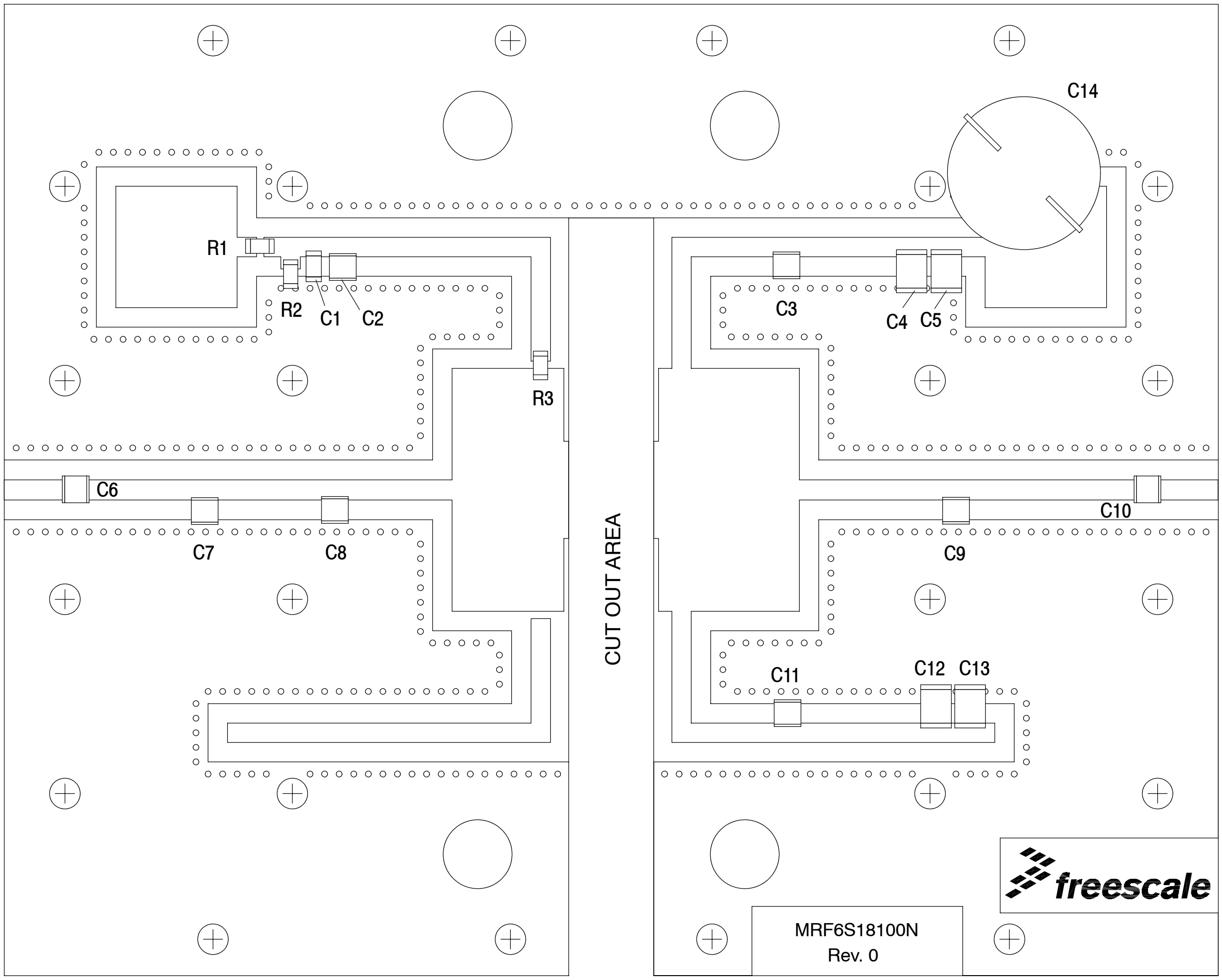


Figure 2. MRF6S18100NR1(NBR1) Test Circuit Component Layout — 1930-1990 MHz

TYPICAL CHARACTERISTICS — 1930-1990 MHz

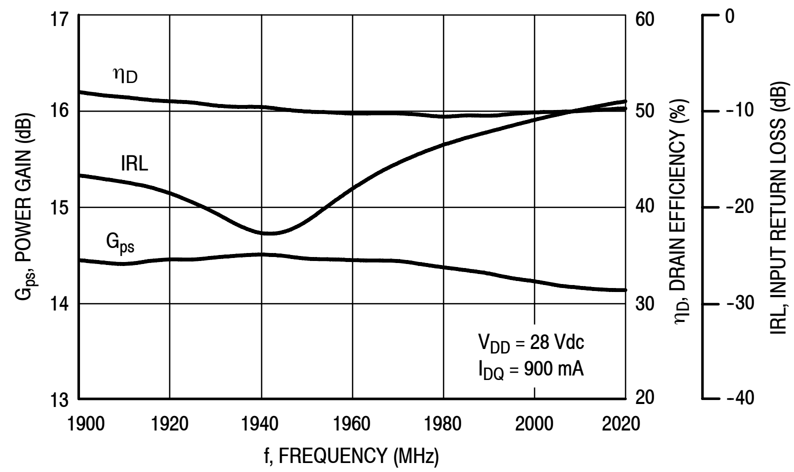


Figure 3. Power Gain, Input Return Loss and Drain Efficiency versus Frequency @ P_{out} = 100 Watts

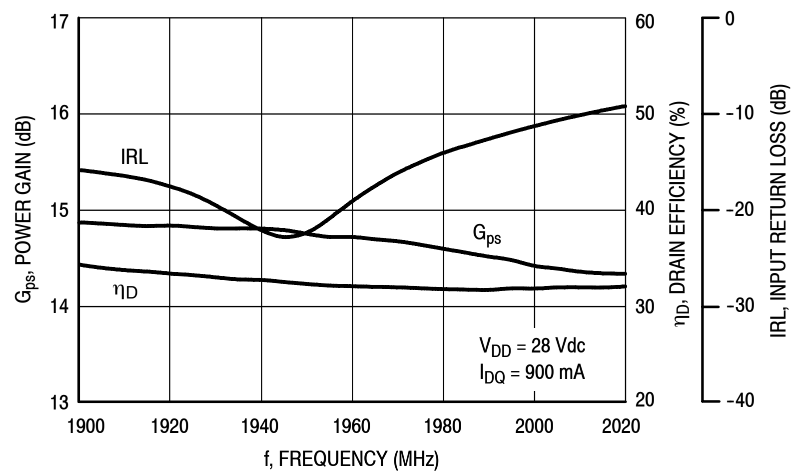


Figure 4. Power Gain, Input Return Loss and Drain Efficiency versus Frequency @ P_{out} = 40 Watts

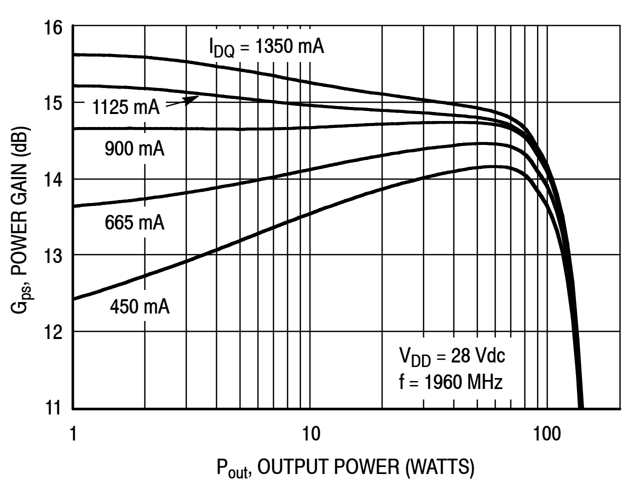


Figure 5. Power Gain versus Output Power

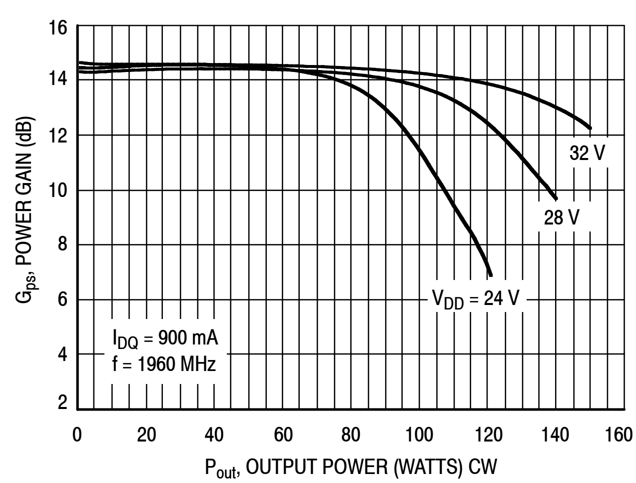


Figure 6. Power Gain versus Output Power

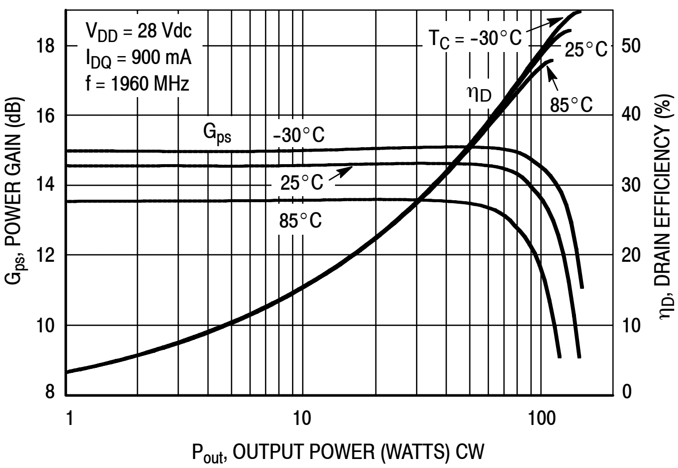


Figure 7. Power Gain and Drain Efficiency versus CW Output Power

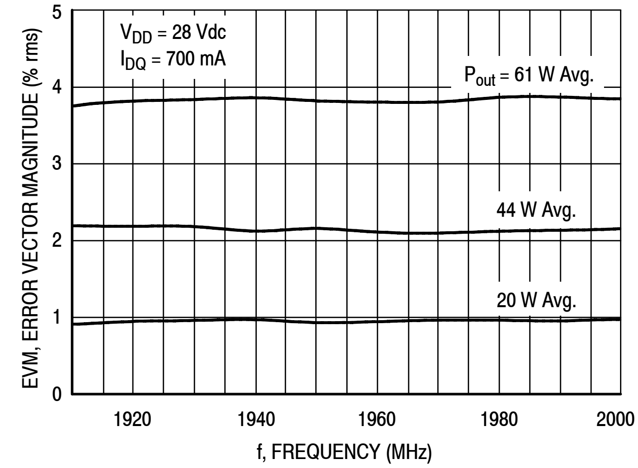


Figure 8. EVM versus Frequency

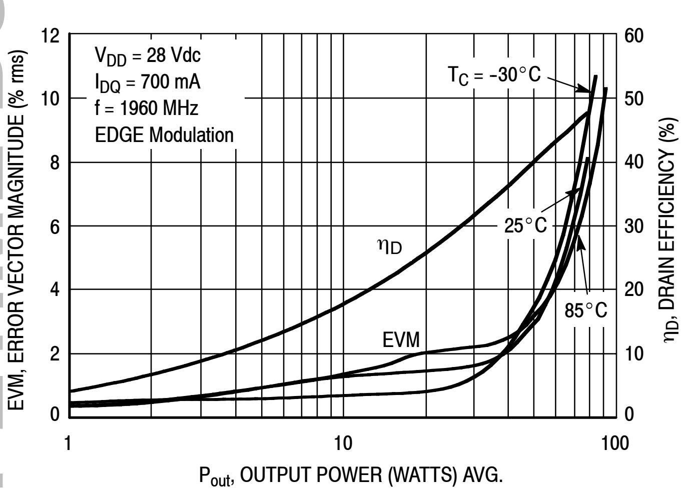


Figure 9. EVM and Drain Efficiency versus Output Power

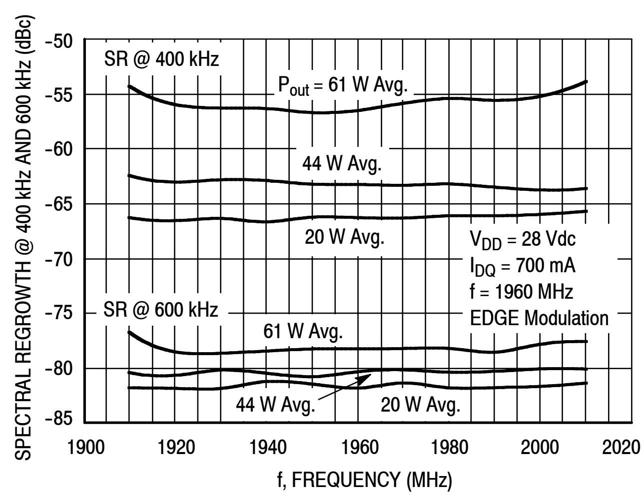


Figure 10. Spectral Regrowth at 400 kHz and 600 kHz versus Frequency

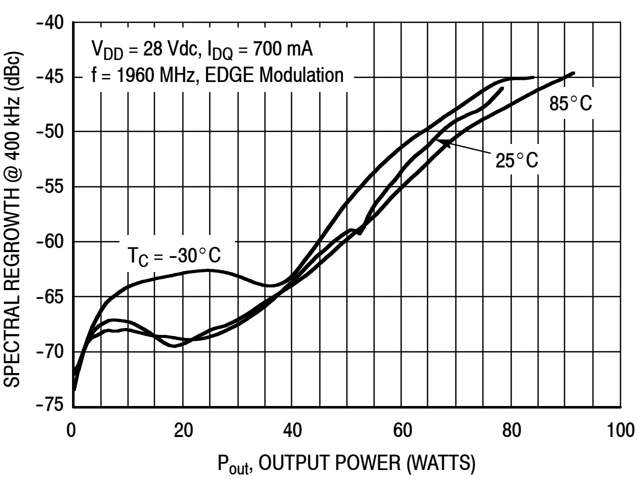


Figure 11. Spectral Regrowth at 400 kHz versus Output Power

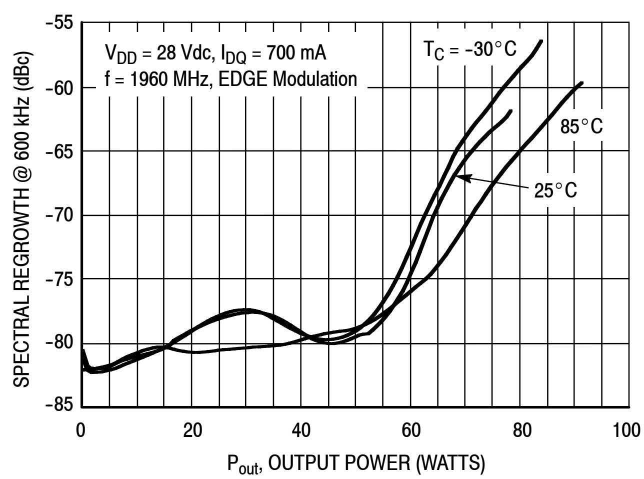
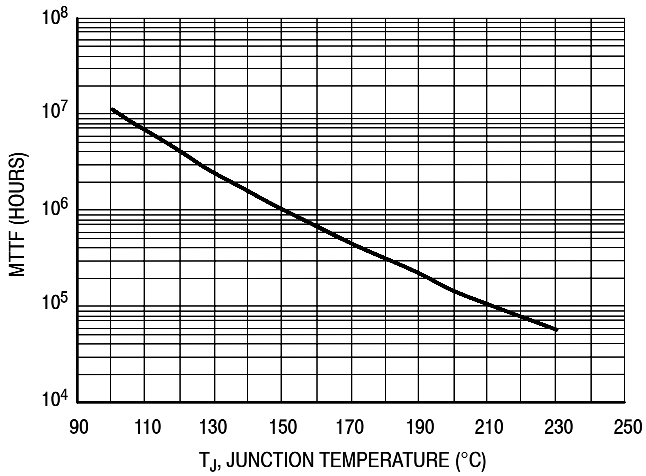


Figure 12. Spectral Regrowth at 600 kHz versus Output Power

TYPICAL CHARACTERISTICS



This above graph displays calculated MTTF in hours when the device is operated at V_{DD} = 28 Vdc, P_{out} = 100 W, and η_D = 49%.

MTTF calculator available at http://www.freescale.com/rf. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.

Figure 13. MTTF versus Junction Temperature

GSM TEST SIGNAL

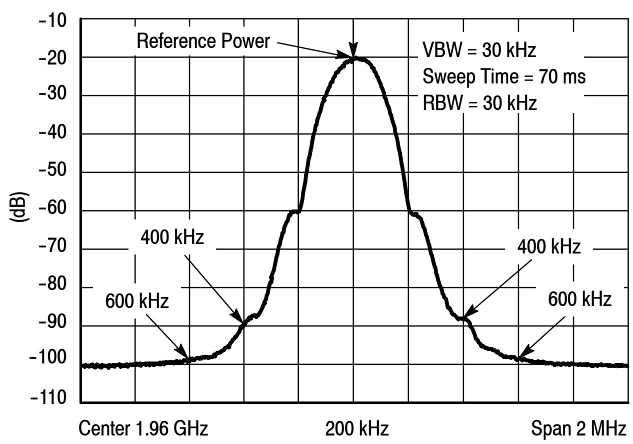
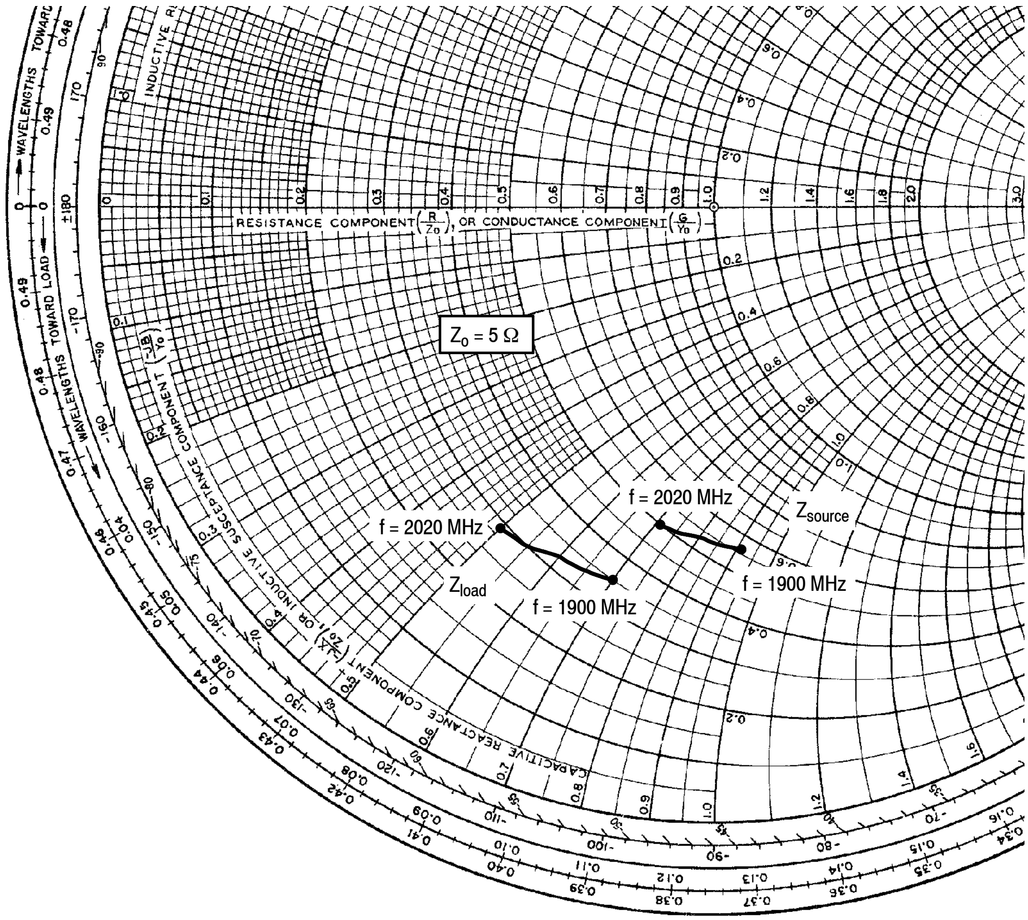


Figure 14. EDGE Spectrum



V_{DD} = 28 Vdc, I_{DQ} = 900 mA, P_{out} = 100 W

f MHz	Z_{source} Ω	Z_{load} Ω
1900	2.80 - j4.53	1.75 - j3.52
1930	2.71 - j4.27	1.67 - j3.25
1960	2.63 - j4.03	1.59 - j2.99
1990	2.56 - j3.79	1.52 - j2.74
2020	2.51 - j3.57	1.47 - j2.51

Z_{source} = Test circuit impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

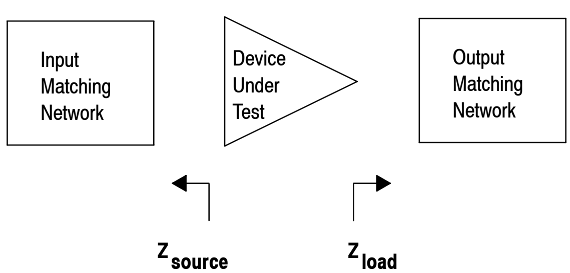
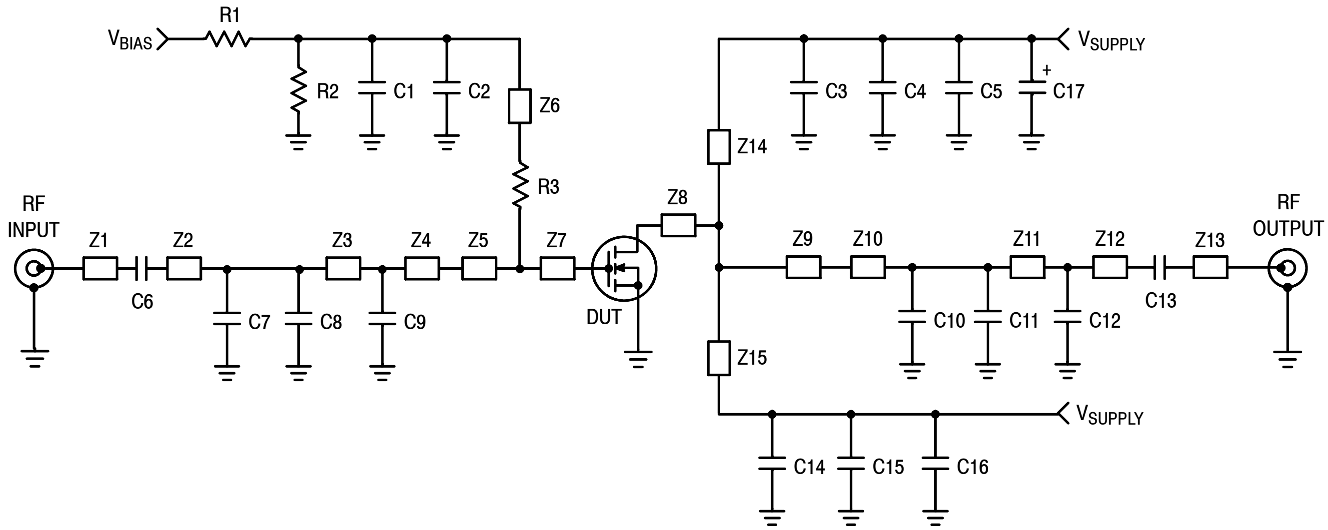


Figure 15. Series Equivalent Source and Load Impedance — 1930-1990 MHz



Z1, Z13	0.250″ x 0.083″ Microstrip	Z9	0.485″ x 1.000″ Microstrip
Z2*	0.620″ x 0.083″ Microstrip	Z10*	0.080″ x 0.083″ Microstrip
Z3*	0.715″ x 0.083″ Microstrip	Z11*	0.340″ x 0.083″ Microstrip
Z4*	0.190″ x 0.083″ Microstrip	Z12*	0.975″ x 0.083″ Microstrip
Z5	0.365″ x 1.000″ Microstrip	Z14, Z15	0.960″ x 0.080″ Microstrip
Z6	1.190″ x 0.080″ Microstrip	PCB	Taconic TLX8-0300, 0.030″, ε_r = 2.55
Z7, Z8	0.115″ x 1.000″ Microstrip		

*Variable for tuning.

Figure 16. MRF6S18100NR1(NBR1) Test Circuit Schematic — 1805-1880 MHz

Table 7. MRF6S18100NR1(NBR1) Test Circuit Component Designations and Values — 1805-1880 MHz

Part	Description	Part Number	Manufacturer
C1	100 nF Chip Capacitor	12065C104KAT	AVX
C2, C3, C6, C13, C14	8.2 pF Chip Capacitors	ATC100B8R2BT500XT	ATC
C4, C5, C15, C16	4.7 μF Chip Capacitors	C4532X5R1H475MT	TDK
C7, C8, C11, C12	0.2 pF Chip Capacitors	ATC700B0R2BT500XT	ATC
C9	1 pF Chip Capacitor	ATC100B1R0BT500XT	ATC
C10	0.5 pF Chip Capacitor	ATC100B0R5BT500XT	ATC
C17	470 μF, 63 V Electrolytic Capacitor, Radial	EKME630ELL471MK25S	Multicomp
R1, R2	10 kΩ, 1/4 W Chip Resistors	CRCW12061002FKEA	Vishay
R3	10 Ω, 1/4 W Chip Resistor	CRCW120610R0FKEA	Vishay

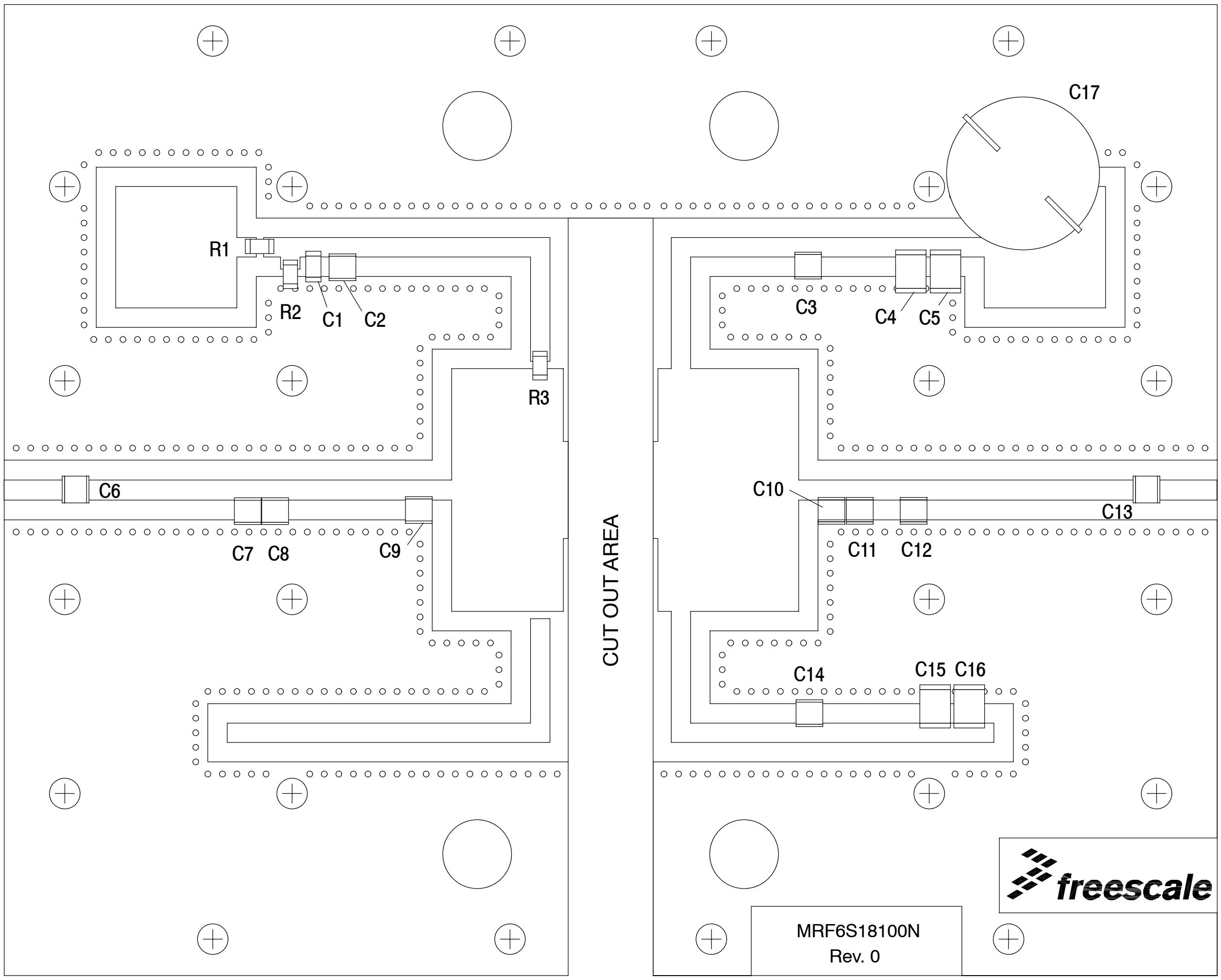


Figure 17. MRF6S18100NR1(NBR1) Test Circuit Component Layout — 1805-1880 MHz

TYPICAL CHARACTERISTICS — 1805-1880 MHz

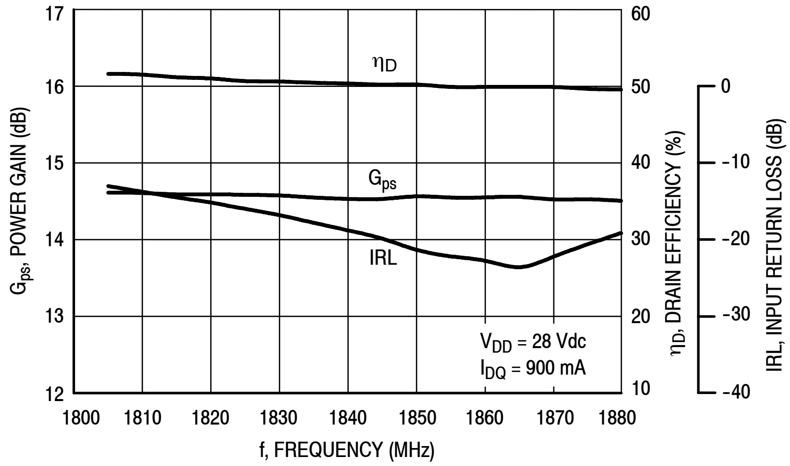


Figure 18. Power Gain, Input Return Loss and Drain Efficiency versus Frequency @ P_{out} = 100 Watts

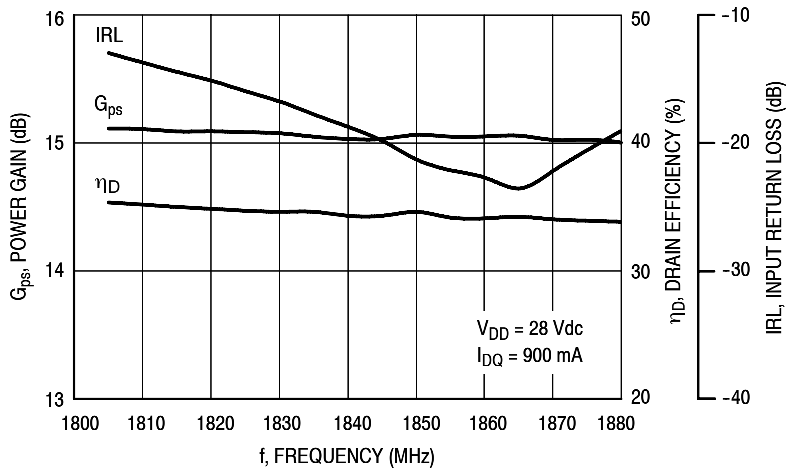


Figure 19. Power Gain, Input Return Loss and Drain Efficiency versus Frequency @ P_{out} = 40 Watts

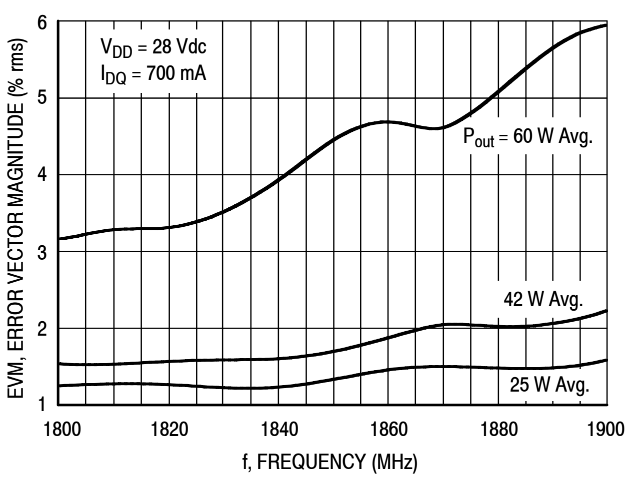


Figure 20. EVM versus Frequency

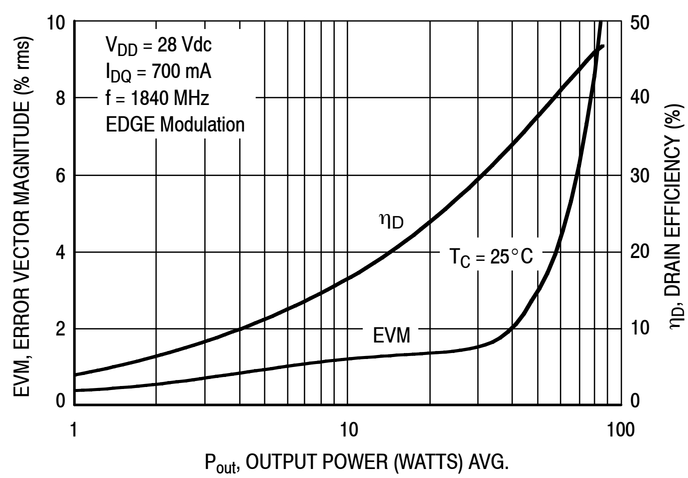


Figure 21. EVM and Drain Efficiency versus Output Power

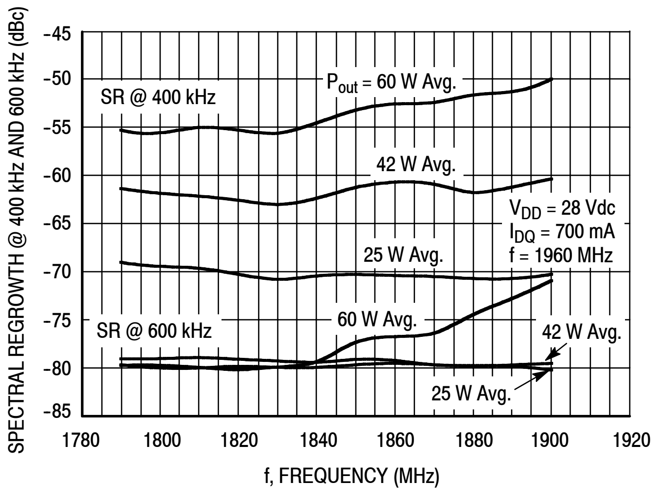


Figure 22. Spectral Regrowth at 400 kHz and 600 kHz versus Frequency

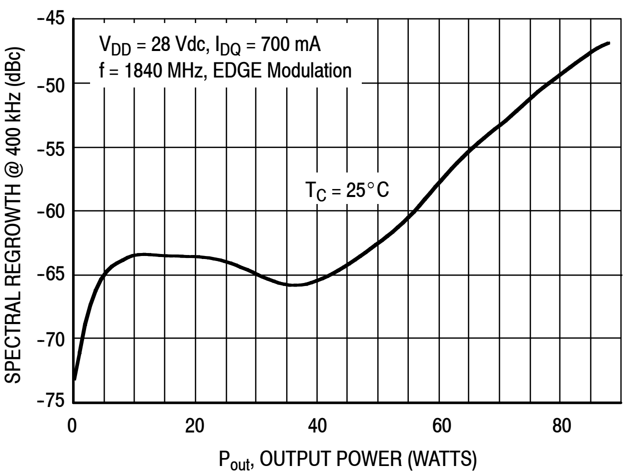


Figure 23. Spectral Regrowth at 400 kHz versus Output Power

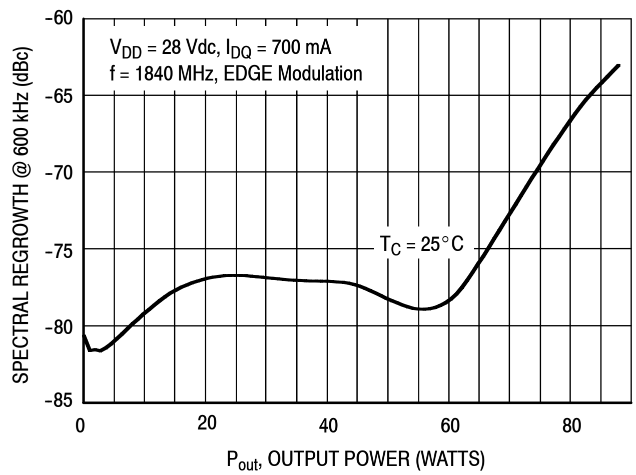
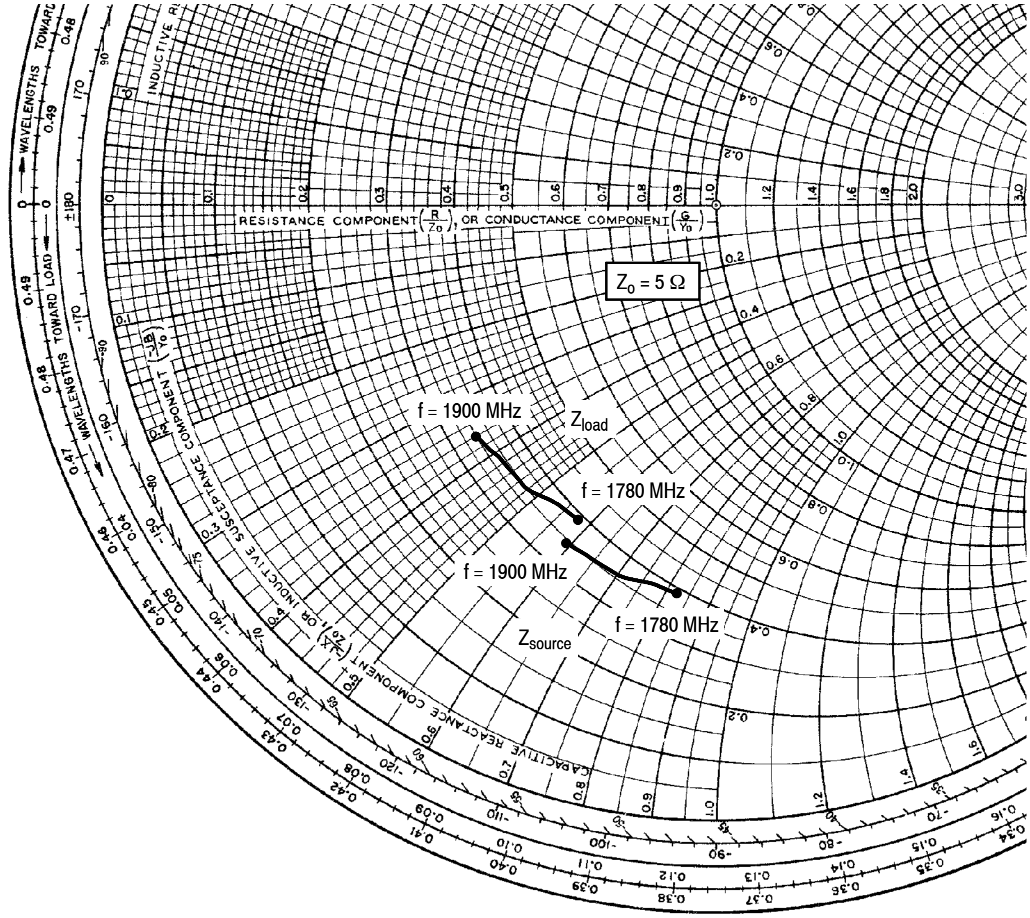


Figure 24. Spectral Regrowth at 600 kHz versus Output Power



$V_{DD} = 28$ Vdc, $I_{DQ} = 900$ mA, $P_{out} = 100$ W

f MHz	Z_{source} Ω	Z_{load} Ω
1780	1.96 - j4.09	1.94 - j2.90
1804	1.90 - j3.86	1.88 - j2.67
1840	1.82 - j3.53	1.80 - j2.42
1880	1.76 - j3.16	1.73 - j1.99
1900	1.72 - j2.97	1.70 - j1.82

Z_{source} = Test circuit impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

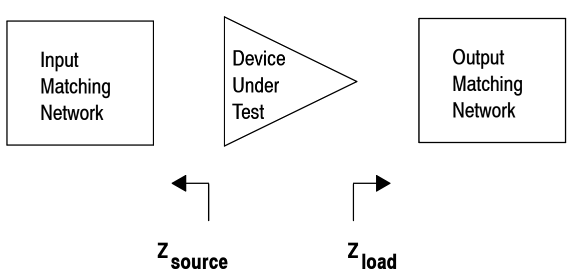
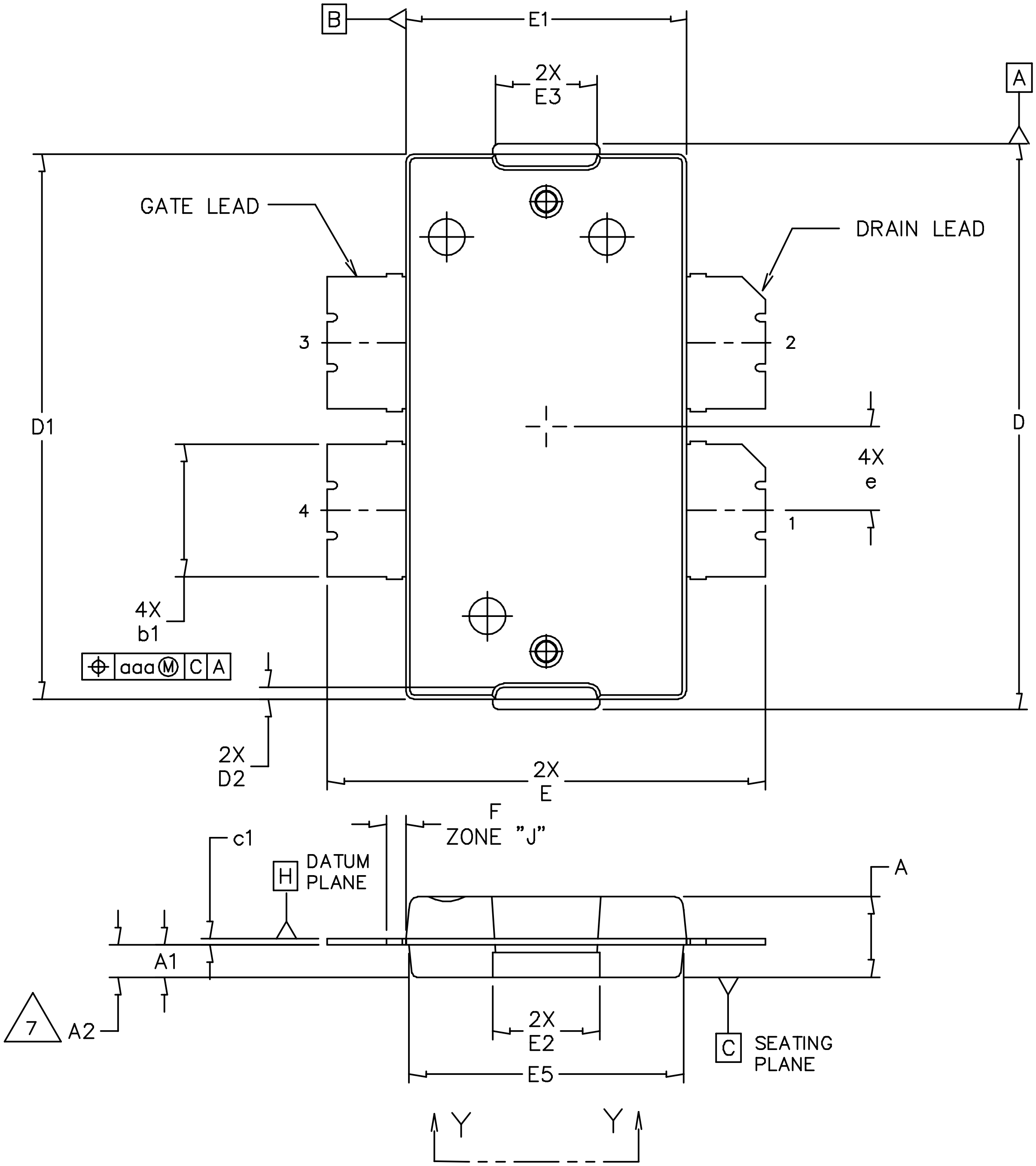
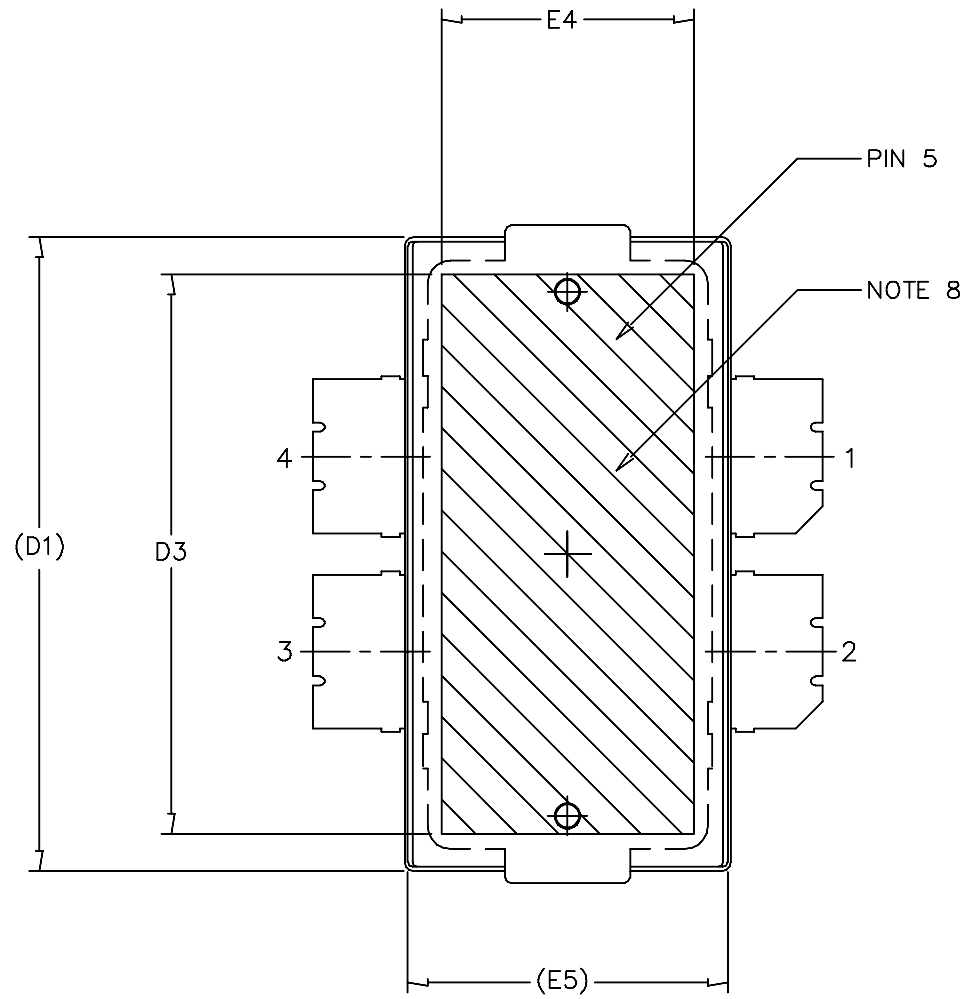


Figure 25. Series Equivalent Source and Load Impedance — 1805-1880 MHz

PACKAGE DIMENSIONS



© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: TO–270 4 LEAD, WIDE BODY	DOCUMENT NO: 98ASA10577D	REV: D
	CASE NUMBER: 1486–03	13 AUG 2007
	STANDARD: NON–JEDEC	



© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE	
TITLE: TO−270 4 LEAD, WIDE BODY	DOCUMENT NO: 98ASA10577D	REV: D	
	CASE NUMBER: 1486−03	13 AUG 2007	
	STANDARD: NON−JEDEC		

NOTES:

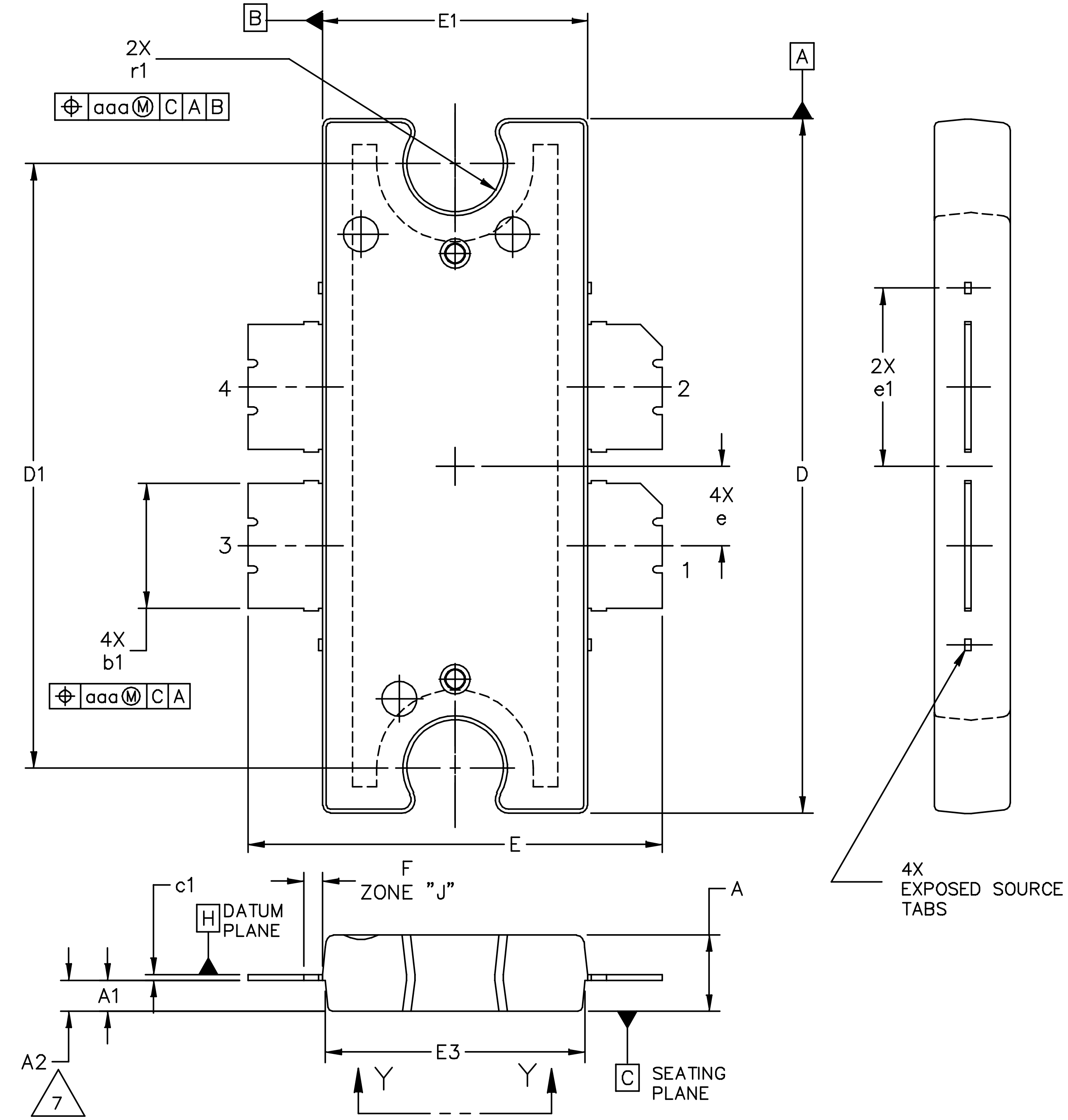
1. CONTROLLING DIMENSION: INCH
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
3. DATUM PLANE -H- IS LOCATED AT THE TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.
4. DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 PER SIDE. DIMENSIONS "D" AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS "b1" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 TOTAL IN EXCESS OF THE "b1" DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION A2 APPLIES WITHIN ZONE "J" ONLY.
8. HATCHING REPRESENTS THE EXPOSED AREA OF THE HEAT SLUG.

STYLE 1:

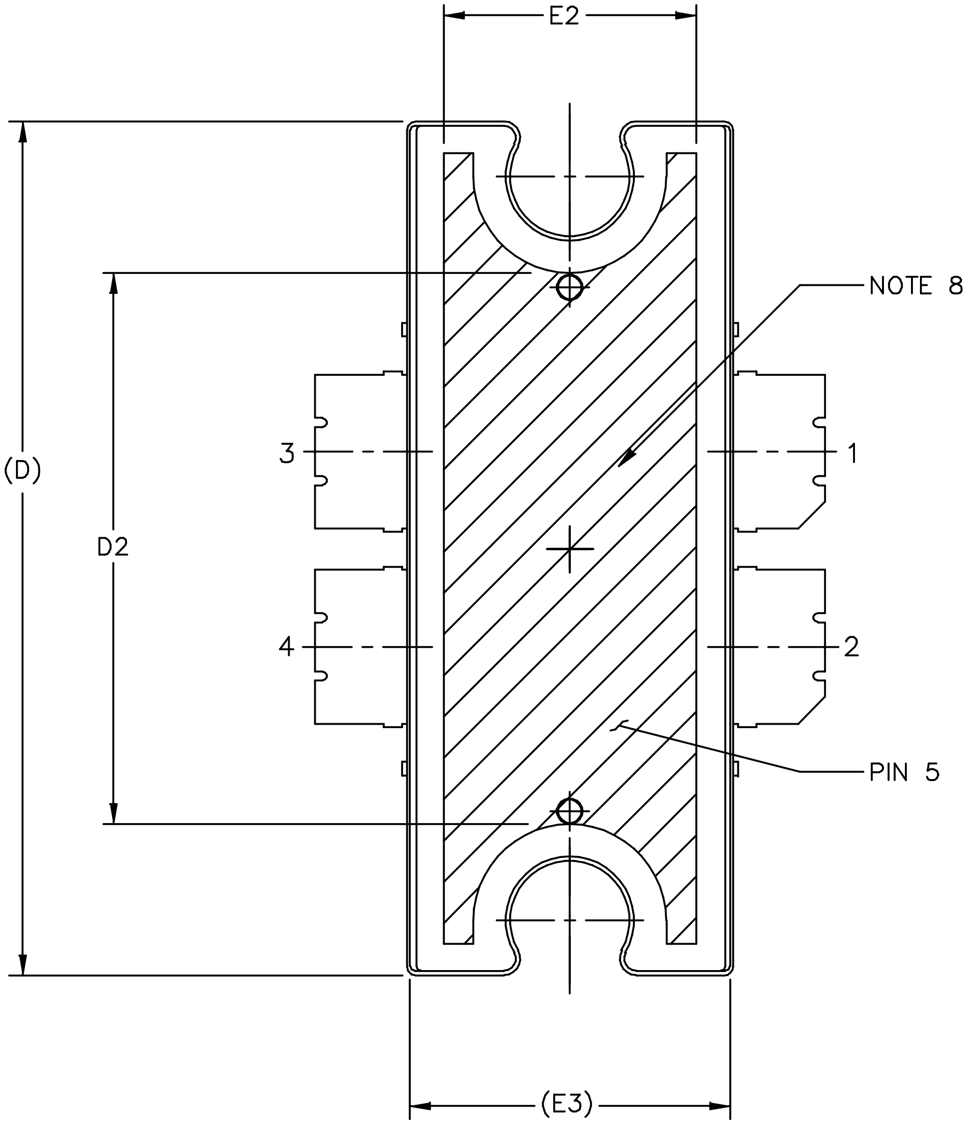
PIN 1 - DRAIN PIN 2 - DRAIN
PIN 3 - GATE PIN 4 - GATE
PIN 5 - SOURCE

DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX	DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX
A	.100	.104	2.54	2.64	F	.025 BSC		0.64 BSC	
A1	.039	.043	0.99	1.09	b1	.164	.170	4.17	4.32
A2	.040	.042	1.02	1.07	c1	.007	.011	.18	.28
D	.712	.720	18.08	18.29	e	.106 BSC		2.69 BSC	
D1	.688	.692	17.48	17.58	aaa	.004		.10	
D2	.011	.019	0.28	0.48					
D3	.600	---	15.24	---					
E	.551	.559	14	14.2					
E1	.353	.357	8.97	9.07					
E2	.132	.140	3.35	3.56					
E3	.124	.132	3.15	3.35					
E4	.270	---	6.86	---					
E5	.346	.350	8.79	8.89					

MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE	
TITLE: TO-270 4 LEAD WIDE BODY	DOCUMENT NO: 98ASA10577D	REV: D
	CASE NUMBER: 1486-03	13 AUG 2007
	STANDARD: NON-JEDEC	



© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: TO−272 4 LEAD, WIDE BODY	DOCUMENT NO: 98ASA10575D	REV: E
	CASE NUMBER: 1484−04	31 AUG 2007
	STANDARD: NON−JEDEC	



© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: TO−272 4 LEAD, WIDE BODY	DOCUMENT NO: 98ASA10575D	REV: E
	CASE NUMBER: 1484−04	31 AUG 2007
	STANDARD: NON−JEDEC	

NOTES:

1. CONTROLLING DIMENSION: INCH
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M−1994.
3. DATUM PLANE H IS LOCATED AT THE TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.
4. DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 PER SIDE. DIMENSIONS "D" AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
5. DIMENSIONS "b1" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 TOTAL IN EXCESS OF THE "b1" DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. DATUM A AND B TO BE DETERMINED AT DATUM PLANE H.
7. DIMENSION A2 APPLIES WITHIN ZONE "J" ONLY.
8. HATCHING REPRESENTS EXPOSED AREA OF THE HEAT SLUG. HATCHED AREA SHOWN IS ON THE SAME PLANE.

STYLE 1:
PIN 1 − DRAIN   PIN 2 − DRAIN
PIN 3 − GATE   PIN 4 − GATE
PIN 5 − SOURCE

DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX	DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX
A	.100	.104	2.54	2.64	b1	.164	.170	4.17	4.32
A1	.039	.043	0.99	1.09	c1	.007	.011	.18	.28
A2	.040	.042	1.02	1.07	r1	.063	.068	1.60	1.73
D	.928	.932	23.57	23.67	e	.106 BSC		2.69 BSC	
D1	.810 BSC		20.57 BSC		e1	.239 INFO ONLY		6.07 INFO ONLY	
D2	.600	−−−	15.24	−−−	aaa	.004		.10	
E	.551	.559	14	14.2					
E1	.353	.357	8.97	9.07					
E2	.270	−−−	6.86	−−−					
E3	.346	.350	8.79	8.89					
F	.025 BSC		0.64 BSC						

	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: TO−272 4 LEAD WIDE BODY	DOCUMENT NO: 98ASA10575D	REV: E
	CASE NUMBER: 1484−04	31 AUG 2007
	STANDARD: NON−JEDEC	

PRODUCT DOCUMENTATION

Refer to the following documents to aid your design process.

Application Notes

- AN1907: Solder Reflow Attach Method for High Power RF Devices in Plastic Packages
- AN1955: Thermal Measurement Methodology of RF Power Amplifiers
- AN3263: Bolt Down Mounting Method for High Power RF Transistors and RFICs in Over-Molded Plastic Packages

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
2	Dec. 2008	• Modified data sheet to reflect RF Test Reduction described in Product and Process Change Notification number, PCN13232, p. 1, 2 • Changed Storage Temperature Range in Max Ratings table from -65 to +175 to -65 to +150 for standardization across products, p. 1 • Removed Total Device Dissipation from Max Ratings table as data was redundant (information already provided in Thermal Characteristics table), p. 1 • Added Case Operating Temperature limit to the Maximum Ratings table and set limit to 150°C, p. 1 • Operating Junction Temperature increased from 200°C to 225°C in Maximum Ratings table, related “Continuous use at maximum temperature will affect MTTF” footnote added and changed 200°C to 225°C in Capable Plastic Package bullet, p. 1 • Corrected V_{DS} to V_{DD} in the RF test condition voltage callout for $V_{GS(Q)}$, On Characteristics table, p. 2 • Removed Forward Transconductance from On Characteristics table as it no longer provided usable information, p. 2 • Updated Part Numbers in Tables 6, 7, Component Designations and Values, to RoHS compliant part numbers, p. 3, 9 • Removed lower voltage tests from Fig. 6, Power Gain versus Output Power, due to fixed tuned fixture limitations, p. 5 • Replaced Fig. 13, MTTF versus Junction Temperature with updated graph. Removed $Amps^2$ and listed operating characteristics and location of MTTF calculator for device, p. 7 • Replaced Case Outline 1486-03, Issue C, with 1486-03, Issue D, p. 14-16. Added pin numbers 1 through 4 on Sheet 1. • Replaced Case Outline 1484-04, Issue D, with 1484-04, Issue E, p. 17-19. Added pin numbers 1 through 4 on Sheet 1, replacing Gate and Drain notations with Pin 1 and Pin 2 designations. • Added Product Documentation and Revision History, p. 20

How to Reach Us:

Home Page:
www.freescale.com

Web Support:
http://www.freescale.com/support

USA/Europe or Locations Not Listed:
Freescale Semiconductor, Inc.
Technical Information Center, EL516
2100 East Elliot Road
Tempe, Arizona 85284
1-800-521-6274 or +1-480-768-2130
www.freescale.com/support

Europe, Middle East, and Africa:
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
www.freescale.com/support

Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064
Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor China Ltd.
Exchange Building 23F
No. 118 Jianguo Road
Chaoyang District
Beijing 100022
China
+86 10 5879 8000
support.asia@freescale.com

For Literature Requests Only:
Freescale Semiconductor Literature Distribution Center
P.O. Box 5405
Denver, Colorado 80217
1-800-441-2447 or +1-303-675-2140
Fax: +1-303-675-2150
LDCForFreescaleSemiconductor@hibbertgroup.com

Document Number: MRF6S18100N
Rev. 2, 12/2008