6 and 4 Channel, "Clickless" Serial Input Balance/Master Volume Controls

SSM2160/SSM2161

FEATURES

Digitally-Controlled "Clickless" Level Adjustment
SSM2160: Six Channels
SSM2161: Four Channels
Master Control has 128 1 dB Steps
Each Channel has 32 1 dB Steps
Step Sizes Can Be Changed Using External Resistors
High Gain Accuracy
100 dB Gain Range
Power On Mute
Excellent Audio Characteristics:
–100 dBu SNR (0 dBu = 0.775 V rms, V_S = ±5 V)
+10 dBu Headroom (V_S = ±5 V)
0.008% THD+N (@ 1 kHz, V_{IN} = –10 dBu, Unity Gain)
–80 dB Crosstalk (@ 1 kHz)
Single or Dual Supply Operation

APPLICATIONS

Dolby* Pro-Logic Master Volume/Balance Control
Home THX† Systems
DSP Soundfield Processors
Automotive Audio Systems
HDTV Audio Systems

GENERAL DESCRIPTION

The SSM2160 and SSM2161 allow digital control of volume for six and four channels, respectively, with a master level control. "Clicking" normally encountered with resistor-ladder attenuators is eliminated by using high performance Voltage Controlled Amplifiers (VCAs) in the signal path. The VCA control ports are driven by DACs with controlled output rate-of-change to insure noiseless volume changes. Each channel is controlled by a dedicated 5-bit DAC, providing 32 steps of adjustment. In addition, a master 7-bit DAC feeds every control port, with 128 steps. Therefore, a balance can be achieved among all channels over a 32 step range, and the master control allows adjustment over its entire range while maintaining the desired channel-to-channel balance. Master and channel step sizes are nominally 1 dB; master step sizes can be reduced by an external resistor. Approximately 80 dB of attenuation and up to 20 dB of gain is possible. Upon power-up, the output is automatically muted.

The SSM2160/SSM2161 can operate from single supplies of 8 V to 14 V and dual supplies from ±4 V to ±7 V. An on-chip buffered supply splitter provides an analog common for single-supply applications.

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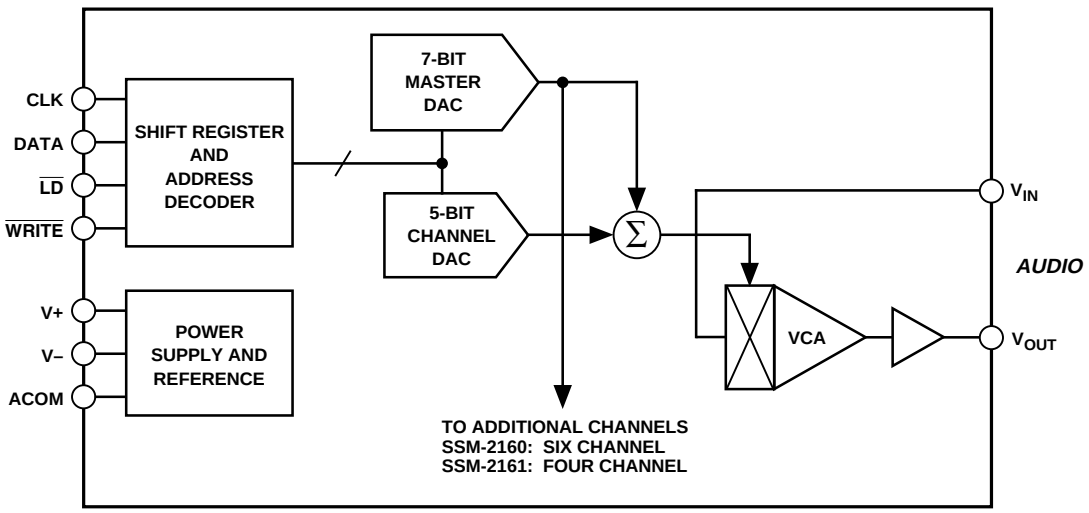
†Home THX is a registered trademark of Lucasfilm, Ltd.

FUNCTIONAL BLOCK DIAGRAM



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SSM2160/SSM2161–SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

(V_S = ±5 V, A_V = 0 dB, 0 dBu = 0.775 Vrms, V_{IN} = 0 dBu, f_{AUDIO} = 1 kHz, f_{CLK} = 250 kHz, R_L = 10 kΩ, –40°C < T_A < +85°C, unless otherwise noted. Typical specifications apply at T_A = +25°C.)

Parameter	Conditions	Min	Typ	Max	Units
AUDIO PERFORMANCE					
Noise	V_{IN} = GND, 20 kHz Bandwidth		–100		dBu
Headroom	Clip Point = 1% THD+N		+10		dBu
Total Harmonic Distortion Plus Noise	2nd and 3rd Harmonics Only				
	A_V = 0 dB		0.008	TBD	%
	A_V = –10 dB		0.02	TBD	%
Channel Separation	Any Channel to Another		80		dB
ANALOG INPUT					
Input Offset Voltage			10		mV
Input Impedance			10		kΩ
GAIN CONTROL ELEMENTS					
Default Step Size – Master	A_VMASTER = 0 dB to –60 dB		1.0		dB
Default Step Size – Channel	A_VCHANNEL = 0 dB to +20 dB		1.0		dB
Gain Error	Relative to Same Channel				
	A_VMASTER = 0 dB			0.25	dB
	A_VMASTER = –20 dB			0.25	dB
	A_VMASTER = –40 dB			1	dB
	A_VMASTER = –60 dB			2	dB
Gain Match Error	Channel-to-Channel; Same Level Setting				
	A_VMASTER = 0 dB			0.25	dB
	A_VMASTER = –20 dB			0.25	dB
	A_VMASTER = –20 dB, A_VCH = +20 dB			0.25	dB
	A_VMASTER = –40 dB			1	dB
	A_VMASTER = –60 dB			2	dB
Power On Mute Attenuation	V_{IN} = +10 dBu		–100		dB
ANALOG OUTPUT					
Output Impedance			5		Ω
Mute Output Impedance			5		Ω
Output Current			±2		mA
Minimum Resistive Load Drive			1		kΩ
Maximum Capacitive Drive			TBD		pF
Offset Voltage	Channel Muted		10		mV
CONTROL SECTION					
Logic Input LO				0.8	V
Logic Input HI		2.0			V
Logic Input Current	Logic LO or HI		1		µA
Clock Frequency		1		2000	kHz
Timing Characteristics	See Timing Diagram				
ANALOG COMMON OUTPUT					
Output Voltage	See Note 1	–5		+5	%
Output Impedance			5.0		Ω
POWER SUPPLIES					
Supply Voltage Range	Dual Supply	±4		±15	V
	Single Supply	+8		+15	V
Supply Current	Positive		17	28	mA
	Negative		17	28	mA
Power Supply Rejection Ratio	Dual Supply		TBD		dB

NOTES

[1]Analog Common Output is used in single supply applications. It is nominally half the voltage between V+ and V–, e.g., $\frac{V+-(V-)}{2}$.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage
- Dual Supply ..... ±18 V
- Single Supply ..... +18 V

Analog Input Voltage ..... $\pm V_S$
Analog Output Voltage ..... $\pm V_S$
Logic Input Voltage ..... $\pm V_S$
Operating Temperature Range ..... –40°C to +85°C
Storage Temperature ..... –65°C to +150°C
Junction Temperature (T_J) ..... +150°C
Lead Temperature (Soldering, 60 sec) ..... +300°C

THERMAL CHARACTERISTICS

Thermal Resistance[2]

24-Pin Plastic DIP (SSM2160)
- θ_{JA} ..... 60°C/W
- θ_{JC} ..... 30°C/W

24-Pin SOIC (SSM2160)
- θ_{JA} ..... 71°C/W
- θ_{JC} ..... 23°C/W

20-Pin Plastic DIP (SSM2161)
- θ_{JA} ..... 65°C/W
- θ_{JC} ..... 26°C/W

20-Pin SOIC (SSM2161)
- θ_{JA} ..... 84°C/W
- θ_{JC} ..... 24°C/W

ESD RATINGS

883 (Human Body) Model ..... TBD kV
EIAJ Model ..... TBD V

NOTES

[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

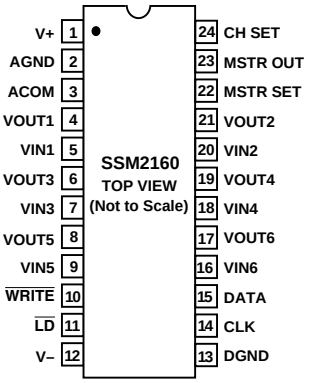
[2]θ_{JA} is specified for worst-case conditions, i.e., θ_{JA} is specified for device in socket for P-DIP and device soldered in circuit board for SOIC package.

ORDERING GUIDE

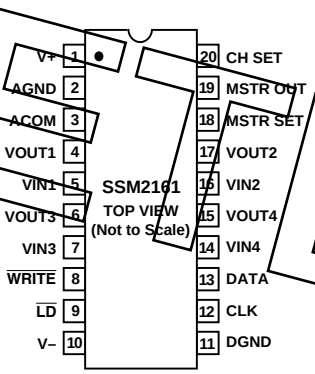
Model	Temperature Range	Package Option
SSM2160P	–40°C to +85°C	24-Lead Plastic DIP
SSM2160S	–40°C to +85°C	24-Lead SOL
SSM2160S-REEL	–40°C to +85°C	24-Lead SOL
SSM2161P	–40°C to +85°C	20-Lead Plastic DIP
SSM2161S	–40°C to +85°C	20-Lead SOL
SSM2161S-REEL	–40°C to +85°C	20-Lead SOL

PIN CONFIGURATIONS

24-Lead Epoxy DIP and SOIC



20-Lead Epoxy DIP and SOIC



CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the SSM2160/SSM2161 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

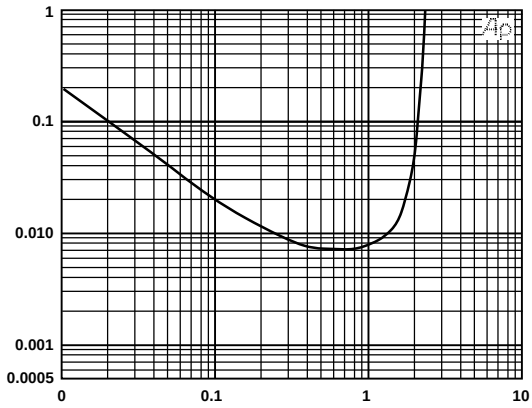


Figure 1. THD vs. Amplitude (Gain = 0 dB, V_{SY} = ±5 V)

MASTER DAC:	**0 0 0 0 0 0 0**	**–127 dB**
	1 1 1 1 1 1 1	**0 dB**
CHANNEL DACs:	**0 0 0 0 0**	**+31 dB**
	1 1 1 1 1	**0 dB**

Figure 2. Data Settings for DACs

SELECTION	MSB ADDRESS MODE					LSB ADDRESS			MSB DATA MODE		LSB DATA
7-BIT MASTER DAC	1	X	X	X	X	0	0	0	0		
5-BIT CHANNEL DAC 1	1	X	X	X	X	0	0	1	0	1	X
5-BIT CHANNEL DAC 2	1	X	X	X	X	0	1	0	0	1	X
5-BIT CHANNEL DAC 3	1	X	X	X	X	0	1	1	0	1	X
5-BIT CHANNEL DAC 4	1	X	X	X	X	1	0	0	0	1	X
5-BIT CHANNEL DAC 5	1	X	X	X	X	1	0	1	0	1	X
5-BIT CHANNEL DAC 6	1	X	X	X	X	1	1	0	0	1	X
NO DAC SELECTED	1	X	X	X	X	1	1	1	0	1	X

X = "DON'T CARE"
SHADED AREA IS DATA

0 = MUTE,
1 = UN-MUTE

Figure 3. Interface Characteristics, DAC Address/Data Decoding Truth Table

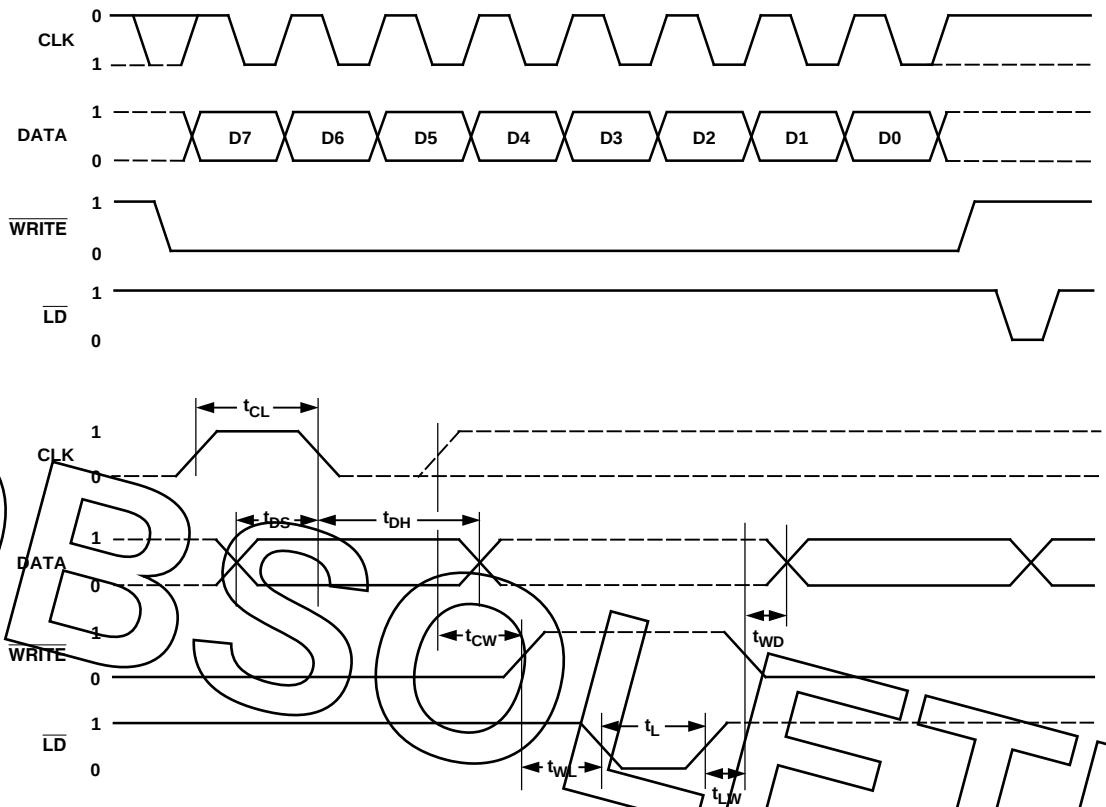


Figure 4. Timing Diagrams

NOTES
1. An idle HI (CLK-H) or idle LO (CLK-LO) clock may be used. Data is latched on the negative edge.
2. For **SPI** or **microwire** three-wire bus operation, tie $\overline{LD}$ to $\overline{WRITE}$ and use $\overline{WRITE}$ pulse to drive both pins. (This generates an automatic internal $\overline{LD}$ signal.)
3. If an idle HI clock is used, t_{CW} and t_{WL} are measured from the final negative transition to the idle state.
4. The first data byte selects an address (MSB HI), and subsequent MSB LO states set gain levels. Refer to the Address/Data Decoding Truth Table.
5. Data must be sent MSB first.
6. The SSM2160/SSM2161 will power up with all channel outputs muted, thus preventing "start-up blasting." To insure a smooth start-up, data should be sent to first initialize the Master DAC, then to set the individual channel DAC levels.

Table I. Timing Description

Timing Symbol	Description	Typical Time (ns)
t_{CL}	Input Clock Pulse Width	TBD
t_{DS}	Data Setup Time	TBD
t_{DH}	Data Hold Time	TBD
t_{CW}	Negative CLK-LO Edge to End of Write	TBD
t_{LW}	End of Load Pulse to Next Write	TBD
t_{WD}	Start of Write to Data	TBD
t_{WL}	End of Write to Start of Load	TBD
t_{L}	Load Pulse Width	TBD

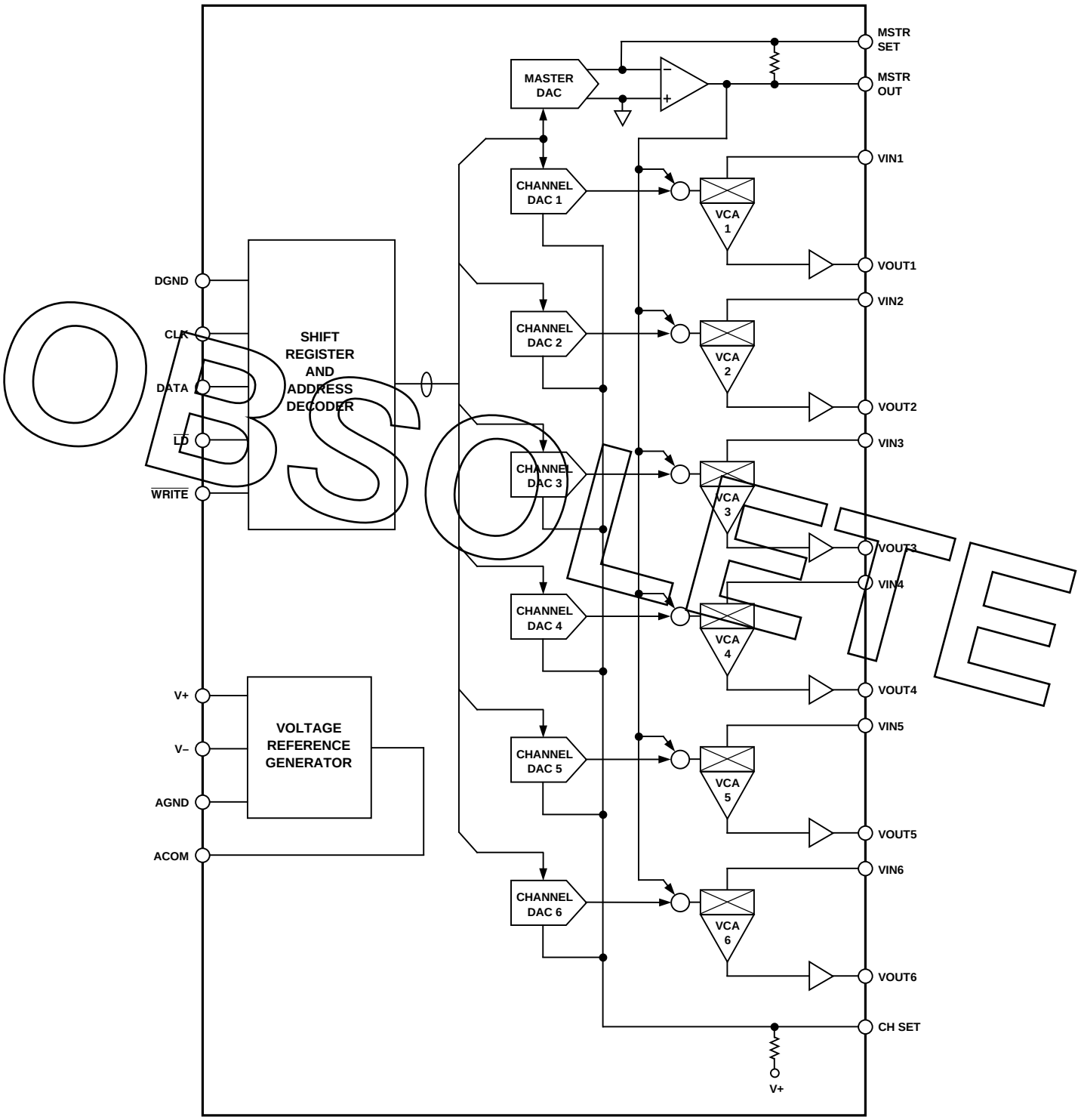
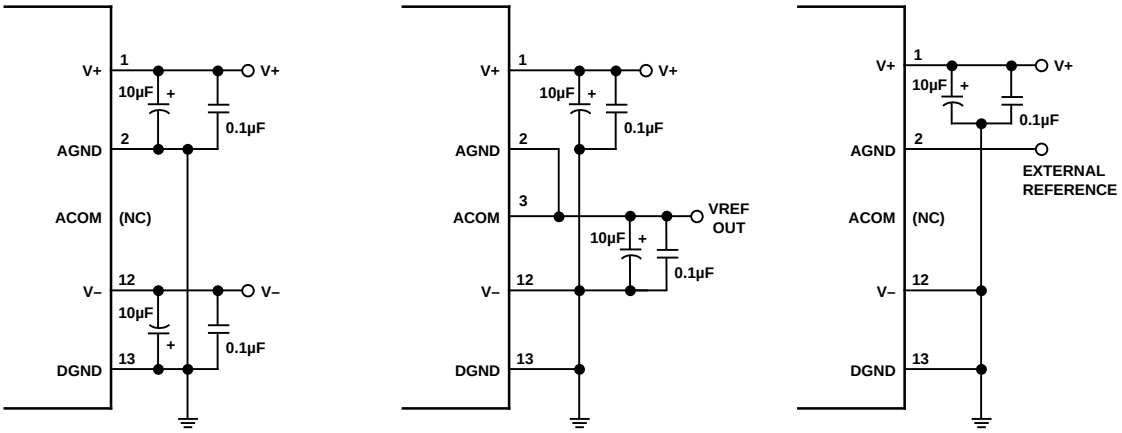
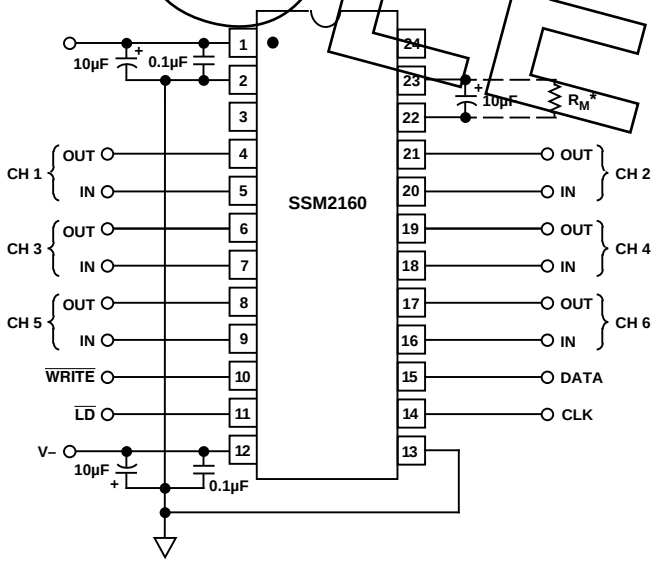


Figure 5. SSM2160 Functional Diagram (SSM2161 Same but with Channels 5 and 6 Omitted)



a. Dual Supply *b. Single Supply* *c. Single Supply Using External Reference*

Figure 6. SSM2160 Power Supply Connections



To change step sizes: Master DAC:
*Use formula $R_M = 1400X/(1-X)$:
where "X" equal desired step size in dB.
Note: Step sizes indicated are approximate.

Figure 7. Typical Application Circuit (Dual Supply)