National Semiconductor

100315

OBSOLETE
October 19, 2009

Low-Skew Quad Clock Driver

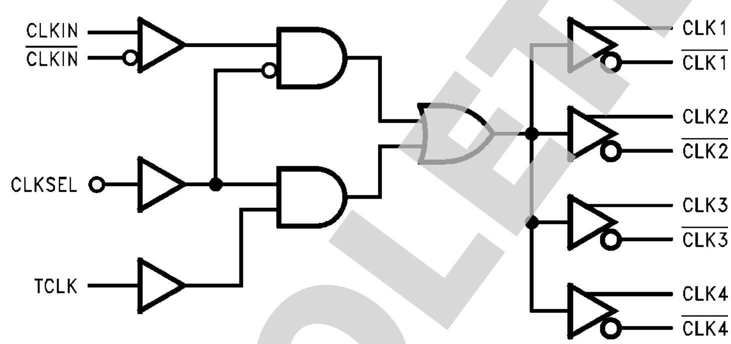
General Description

The 100315 contains four low skew differential drivers, designed for generation of multiple, minimum skew differential clocks from a single differential input. This device also has the capability to select a secondary single-ended clock source for use in lower frequency system level testing. The 100315 is a 300 Series redesign of the 100115 clock driver.

Features

- Low output to output skew (≤50 ps)
- Differential inputs and outputs
- Secondary clock available for system level testing
- 2000V ESD protection
- Voltage compensated operating range: −4.2V to −5.7V
- Standard Microcircuit Drawing (SMD) 5962-9469601

Logic Diagram



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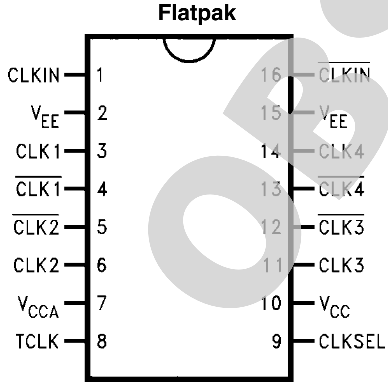
Connection Diagram

Flatpak



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Pin Names	Description
CLKIN, $\overline{CLKIN}$	Differential Clock Inputs
CLK_{1-4}, $\overline{CLK}_{1-4}$	Differential Clock Outputs
TCLK	Test Clock Input (Note 1)
CLKSEL	Clock Input Select (Note 1)

Note 1: TCLK and CLKSEL are single-ended inputs, with internal 50 kΩ pulldown resistors.

Truth Table

CLKSEL	CLKIN	$\overline{CLKIN}$	TCLK	CLK_N	$\overline{CLK_N}$
L	L	H	X	L	H
L	H	L	X	H	L
H	X	X	L	L	H
H	X	X	H	H	L

L = Low Voltage Level
H = High Voltage Level
X = Don't Care

Absolute Maximum Ratings (Note 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Above which the useful life may be impaired	
Storage Temperature	−65°C to +150°C
Maximum Junction Temperature (T_J)	
Ceramic	+175°C
Case Temperature under Bias (T_C)	−55°C to +125°C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
Input Voltage (DC)	V_{CC} to +0.5V
Output Current (DC Output HIGH)	−50 mA
Operating Range (Note 2)	−5.7V to −4.2V
ESD (Note 3)	≥2000V

Recommended Operating Conditions

Case Temperature (T_C)	
Military	−55°C to +125°C
Supply Voltage (V_{EE})	−5.7V to −4.2V

Note 2: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 3: ESD testing conforms to MIL-STD-883, Method 3015.

Military Version DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND (Note 6)

Symbol	Parameter	Min	Typ	Max	Units	T_C	Conditions		Notes
V_{OH}	Output HIGH Voltage	−1025		−870	mV	0°C to +125°C	$V_{IN} = V_{IH(Max)}$ or $V_{IL(Min)}$	Loading with 50Ω to −2.0V	(Note 4, Note 5, Note 6)
		−1085		−870	mV	−55°C			
V_{OL}	Output LOW Voltage	−1830		−1620	mV	0°C to +125°C			
		−1830		−1555	mV	−55°C			
V_{OHC}	Output HIGH Voltage	−1035			mV	0°C to +125°C	$V_{IN} = V_{IH(Min)}$ or $V_{IL(Max)}$	Loading with 50Ω to −2.0V	(Note 4, Note 5, Note 6)
		−1085			mV	−55°C			
V_{OLC}	Output LOW Voltage			−1610	mV	0°C to +125°C			
				−1555	mV	−55°C			

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DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND (Note 6)

Symbol	Parameter	Min	Typ	Max	Units	T_C	Conditions	Notes
V_{DIFF}	Input Voltage Differential	150			mV	−55°C to +125°C	Required for Full Output Swing	(Note 4, Note 5, Note 6)
V_{CM}	Common Mode Voltage	V_{CC} − 2.0		V_{CC} − 0.5	V	−55°C to +125°C		(Note 4, Note 5, Note 6)
V_{IH}	Single-Ended Input High Voltage	−1165		−870	mV	−55°C to +125°C	Guaranteed HIGH Signal for All Inputs	(Note 4, Note 5, Note 6, Note 7)
V_{IL}	Single-Ended Input Low Voltage	−1830		−1475	mV	−55°C to +125°C	Guaranteed LOW Signal for All Inputs	(Note 4, Note 5, Note 6, Note 7)
I_{IH}	Input HIGH Current CLKIN, $\overline{CLKIN}$			150	µA	−55°C to +125°C	V_{IN} = $V_{IH(Max)}$	(Note 4, Note 5, Note 6)
	TCLK			450	µA			
	CLKSEL			380	µA			
I_{CBO}	Input Leakage Current	−10			µA	−55°C to +125°C	V_{IN} = V_{EE}	(Note 4, Note 5, Note 6)
I_{EE}	Power Supply Current, Normal	−80		−25	mA	−55°C to +125°C		(Note 4, Note 5, Note 6)

Note 4: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals −55°C), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 5: Screen tested 100% on each device at −55°C, +25°C, and +125°C, Subgroups 1, 2, 3, 7, and 8.

Note 6: Sample tested (Method 5005, Table I) on each manufactured lot at −55°C, +25°C, and +125°C, Subgroups A1, 2, 3, 7, and 8.

Note 7: Guaranteed by applying specified input condition and testing V_{OH}/V_{OL}.

AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = −55°C		T_C = +25°C		T_C = +125°C		Units	Conditions	Notes
		Min	Max	Min	Max	Min	Max			
t_{PLH} t_{PHL}	Propagation Delay CLKIN, $\overline{CLKIN}$ to $CLK_{(1-4)}$, $\overline{CLK}_{(1-4)}$	0.58	0.88	0.63	0.88	0.72	1.02	ns	Figures 1, 2	(Note 8, Note 9, Note 10)
t_{PLH} t_{PHL}	Propagation Delay, TCLK to $CLK_{(1-4)}$, $\overline{CLK}_{(1-4)}$	0.30	1.60	0.30	1.50	0.40	1.70	ns		
$t_{S\ G-G}$	Skew Gate to Gate (Note 12)		120		100		120	ps		(Note 10)
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.30	0.90	0.25	0.85	0.20	0.85	ns		

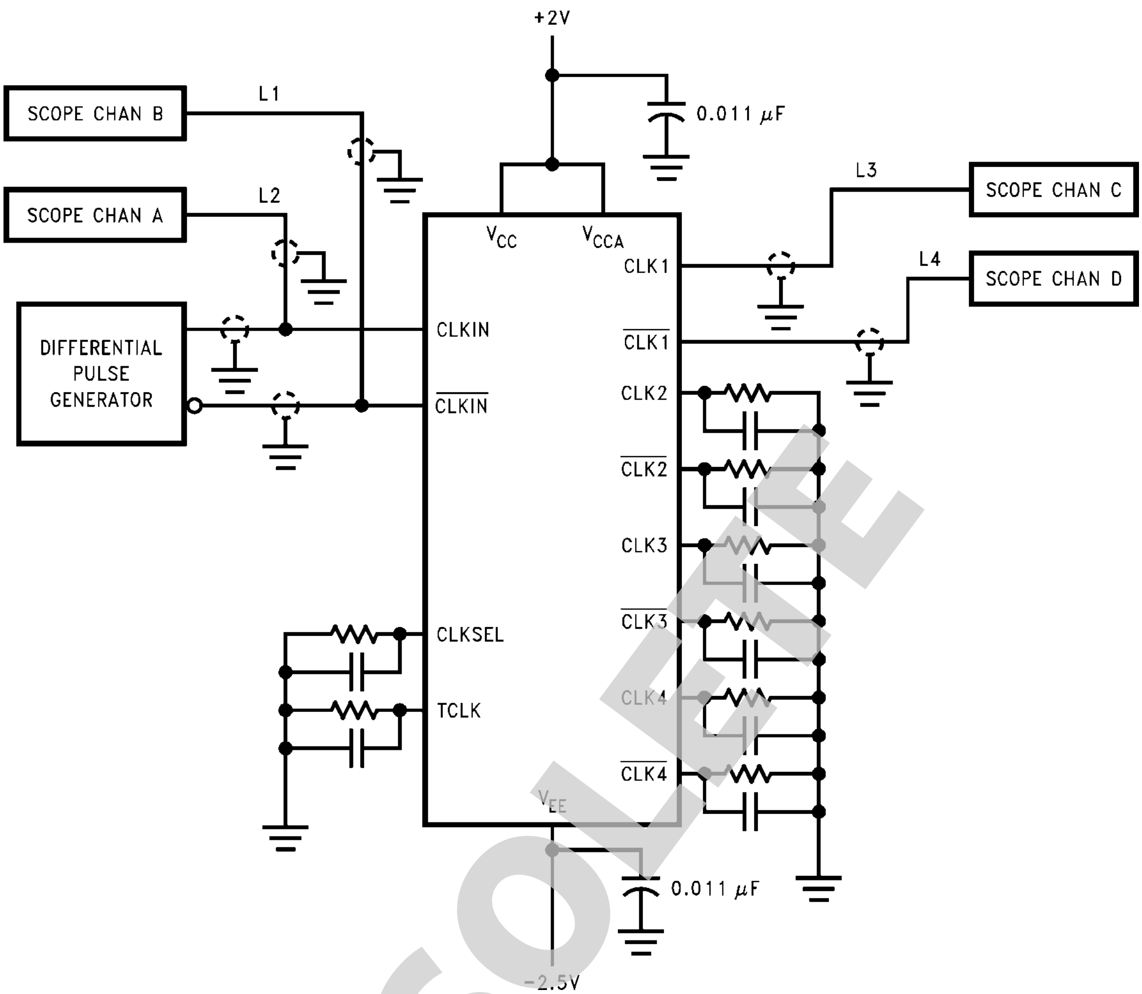
Note 8: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals −55°C, then testing immediately after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 9: Screen tested 100% on each device at +25°C temperature only, Subgroup A9.

Note 10: Sample tested (Method 5005, Table I) on each manufactured lot at +25°C, Subgroup A9, and at +125°C and −55°C temperatures, Subgroups A10 and A11.

Note 11: Not tested at +25°C, +125°C and −55°C temperature (design characterization data).

Note 12: Maximum output skew for any one device.



Note 13: Shown for testing CLKIN to CLK1 in the differential mode.

Note 14: L1, L2, L3 and L4 = equal length 50Ω impedance lines.

Note 15: All unused inputs and outputs are loaded with 50Ω in parallel with ≤3 pF to GND.

Note 16: Scope should have 50Ω input terminator internally.

FIGURE 1. AC Test Circuit

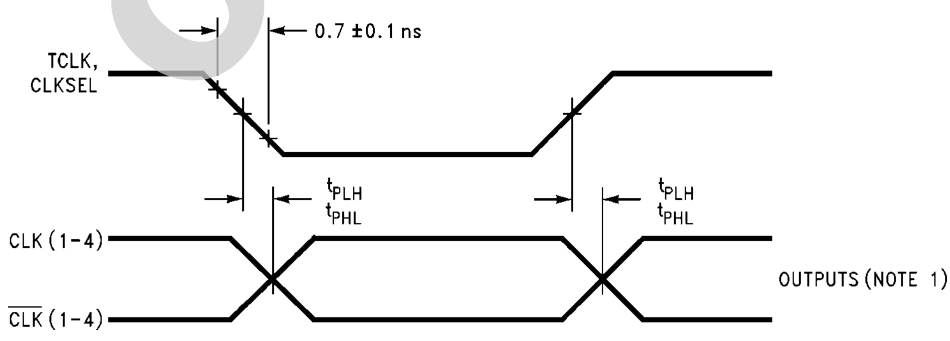


FIGURE 2. Propagation Delay, TCLK, CLKSEL to Outputs

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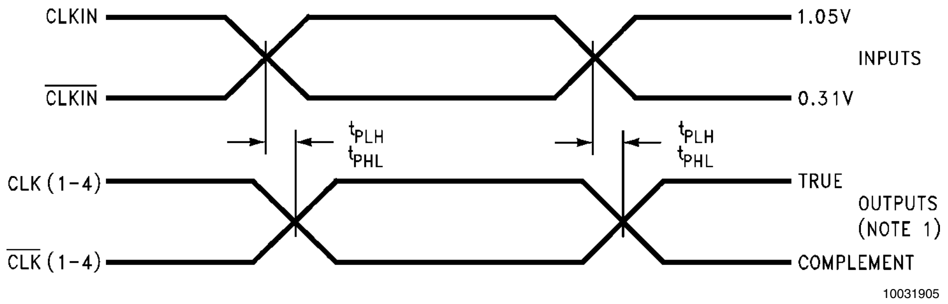
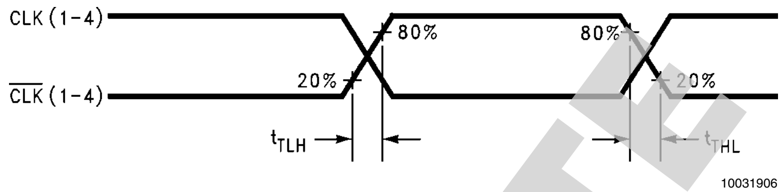


FIGURE 3. Propagation Delay, CLKIN/CLKIN to Outputs



Note 17: The output to output skew, which is defined as the difference in the propagation delays between each of the four outputs on any one 100115 shall not exceed 75 ps.

FIGURE 4. Transition Times

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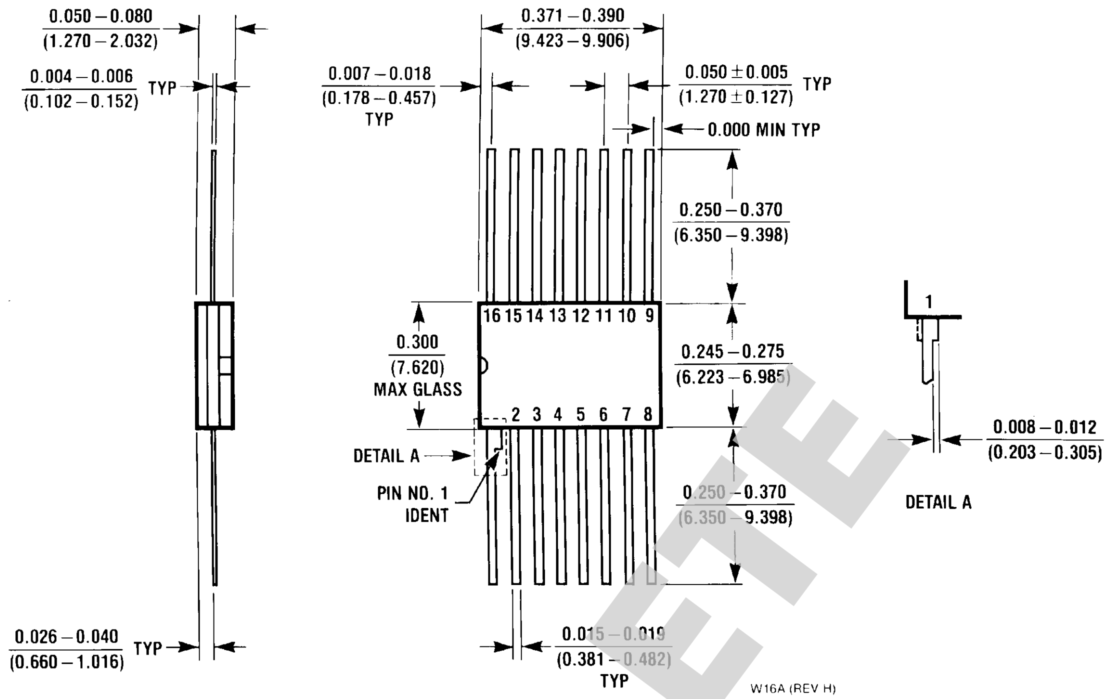
Physical Dimensions inches (millimeters) unless otherwise noted



16 Lead Ceramic Flatpak (F)
NS Package Number W16A

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Notes

Notes

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