



### FEATURES:

- Enhanced N channel FET with no inherent diode to Vcc
- Bidirectional signal flow
- 24:12 Mux/Demux switches connect inputs to outputs
- Individual controls for each bank
- Zero propagation delay, zero ground bounce
- Undershoot clamp diodes on all switch and control inputs
- TTL-compatible control inputs
- Available in 48-pin QVSOP package

### APPLICATIONS:

- Logic replacement
- Video, audio, graphics switching, muxing
- Hot-swapping, hot-docking
- Voltage translation (5V to 3.3V)
- Bus funneling

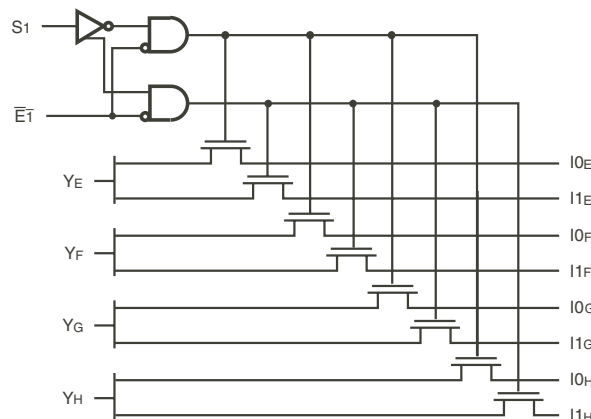
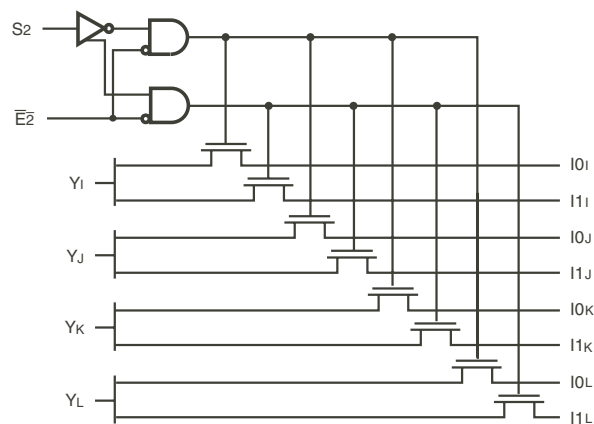
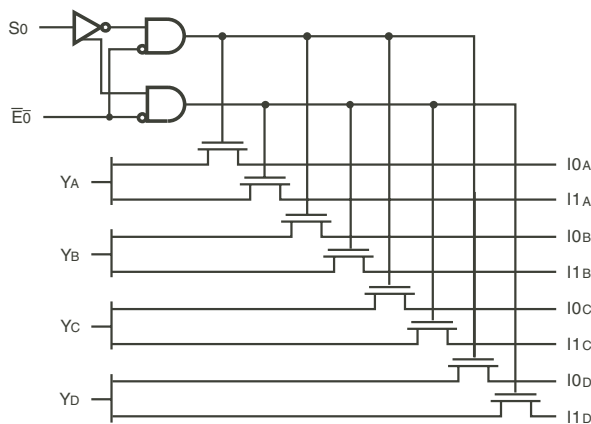
### DESCRIPTION:

The QS33X257 is a high-speed CMOS TTL-compatible 24:12 multiplexer/demultiplexer. The QS33X257 is functionally compatible to three of the QuickSwitch version of the 74F257, 74FCT257, and the 74ALS/AS/LS257 Quad 2:1 multiplexers. The low ON resistance of the QS33X257 allows inputs to be connected to outputs without adding propagation delay and without generating additional ground bounce noise. This part will be used in wide bus multiplexing where board space is at a premium.

Mux/Demux devices provide an order of magnitude faster speed than equivalent logic devices.

The QS33X257 is characterized for operation at -40°C to +85°C.

### FUNCTIONAL BLOCK DIAGRAM

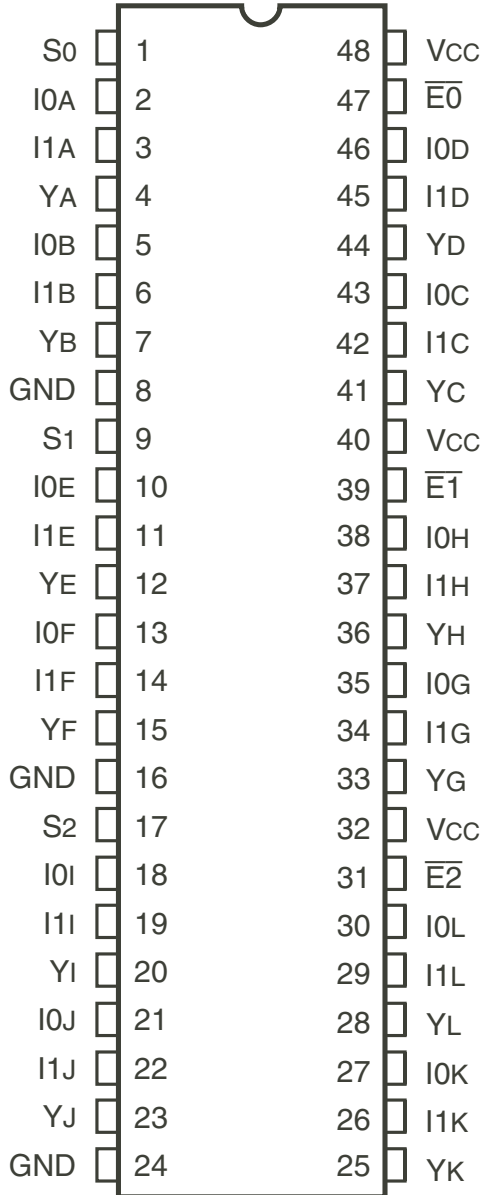


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**INDUSTRIAL TEMPERATURE RANGE**

**AUGUST 2012**

## PIN CONFIGURATION



QVSOP  
TOP VIEW

## ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Description	Max	Unit
VTERM <sup>(2)</sup>	Supply Voltage to Ground	-0.5 to +7	V
VTERM <sup>(3)</sup>	DC Switch Voltage Vs	-0.5 to +7	V
VTERM <sup>(3)</sup>	DC Input Voltage VIN	-0.5 to +7	V
VAC	AC Input Voltage (pulse width $\leq$ 20ns)	-3	V
IOUT	DC Output Current Max. Sink Current/Pin	120	mA
P <sub>MAX</sub>	Maximum Power Dissipation	0.5	W
TSTG	Storage Temperature	-65 to +150	°C

### NOTE:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- Vcc terminals.
- All terminals except Vcc.

## CAPACITANCE

(TA = +25°C, f = 1.0MHz, VIN = 0V, VOUT = 0V)

Pins		Typ.	Max. <sup>(1)</sup>	Unit
Control Pins		4	5	pF
Quickswitch Channels (Switch OFF)	Demux	5	7	pF
	Mux	9	10	

### NOTE:

- This parameter is measured at characterization but not tested.

## PIN DESCRIPTION

Pin Names	I/O	Description
Ixx	I/O	Data Inputs
Sx	I	Select Input
$\overline{E}x$	I/O	Enable Input
Yx	I/O	Data Outputs

## FUNCTION TABLE(1)

Enable		Outputs				Function
$\overline{E}x$	Sx	YA	YB	Yc	YD	
H	X	Z	Z	Z	Z	Disable
L	L	IOA	IOB	IOC	IOX	Select 0
L	H	I1A	I1B	I1C	I1X	Select 1

### NOTE:

- H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Don't Care  
Z = High-Impedance

## DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

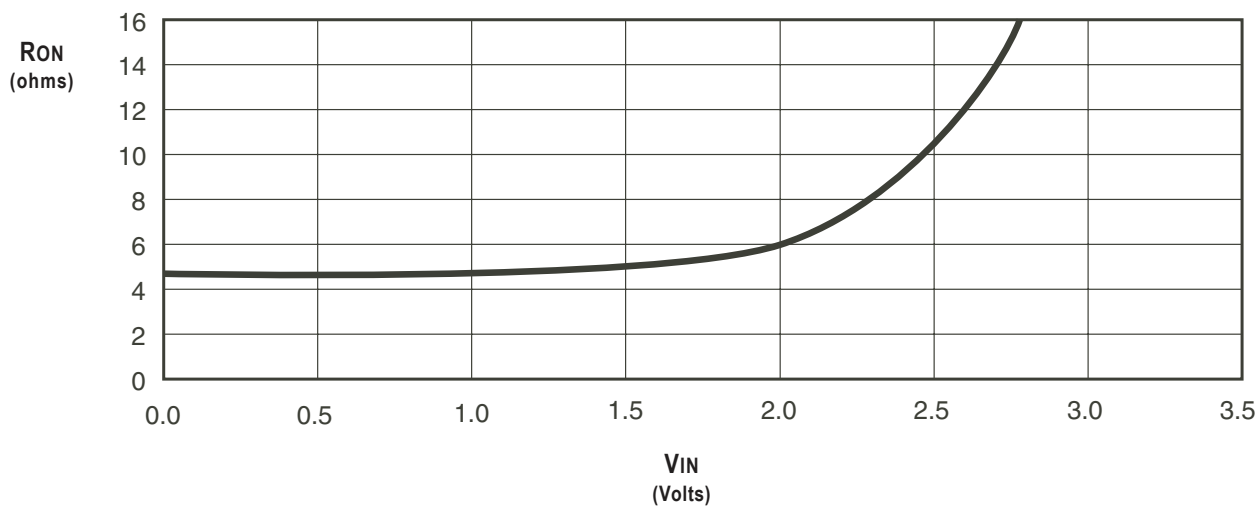
Industrial:  $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 5\%$

Symbol	Parameter	Test Conditions	Min.	Typ. <sup>(1)</sup>	Max.	Unit
$V_{IH}$	Input HIGH Level	Guaranteed Logic HIGH for Control Pins	2	—	—	V
$V_{IL}$	Input LOW Level	Guaranteed Logic LOW for Control Pins	—	—	0.8	V
$I_{IN}$	Input Leakage Current (Control Inputs)	$0\text{V} \leq V_{IN} \leq V_{CC}$	—	—	$\pm 1$	$\mu\text{A}$
$I_{OZ}$	Off-State Output Current (Hi-Z)	$0\text{V} \leq V_{OUT} \leq V_{CC}$	—	—	$\pm 1$	$\mu\text{A}$
RON	Switch ON Resistance	$V_{CC} = \text{Min.}, V_{IN} = 0\text{V}, I_{ON} = 30\text{mA}$	—	5	7	$\Omega$
		$V_{CC} = \text{Min.}, V_{IN} = 2.4\text{V}, I_{ON} = 15\text{mA}$	—	10	15	
VP	Pass Voltage <sup>(2)</sup>	$V_{IN} = V_{CC} = 5\text{V}, I_{OUT} = -5\mu\text{A}$	3.7	4	4.2	V

### NOTES:

1. Typical values are at  $V_{CC} = 5.0\text{V}$ ,  $T_A = 25^{\circ}\text{C}$ .
2. Pass Voltage is guaranteed but not production tested.

## TYPICAL ON RESISTANCE vs VIN AT VCC = 5V



## POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions <sup>(1)</sup>	Max.	Unit
I <sub>CCQ</sub>	Quiescent Power Supply Current	V <sub>CC</sub> = Max., V <sub>IN</sub> = GND or V <sub>CC</sub> , f = 0	9	μA
ΔI <sub>CC</sub>	Power Supply Current per Control Input HIGH <sup>(2)</sup>	V <sub>CC</sub> = Max., V <sub>IN</sub> = 3.4V, f = 0	1.5	mA
I <sub>CCD</sub>	Dynamic Power Supply Current per MHz <sup>(3)</sup>	V <sub>CC</sub> = Max., I and Y pins open Control Inputs Toggling at 50% Duty Cycle	0.25	mA/MHz

### NOTES:

- For conditions shown as Min. or Max., use the appropriate values specified under DC Electrical Characteristics.
- Per TLL driven input (V<sub>IN</sub> = 3.4V, control inputs only). I and Y pins do not contribute to ΔI<sub>CC</sub>.
- This current applies to the control inputs only and represents the current required to switch internal capacitance at the specified frequency. The I and Y inputs generate no significant AC or DC currents as they transition. This parameter is guaranteed but not production tested.

## SWITCHING CHARACTERISTICS OVER OPERATING RANGE

T<sub>A</sub> = -40°C to +85°C, V<sub>CC</sub> = 5.0V ± 5%;

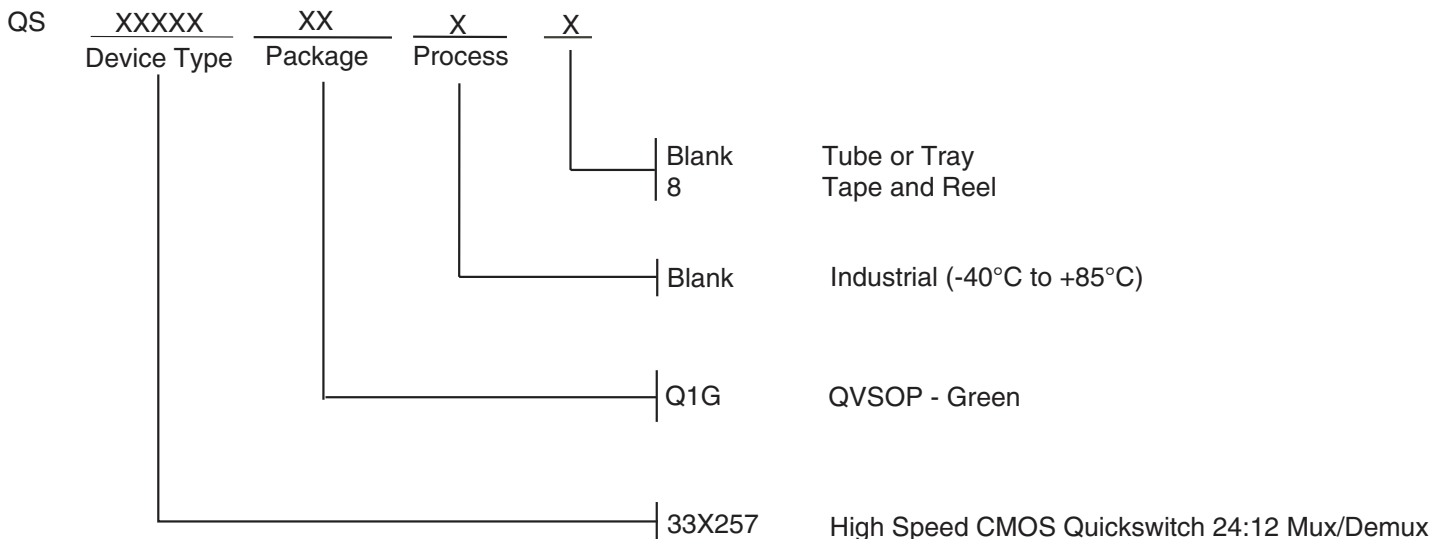
C<sub>LOAD</sub> = 50pF, R<sub>LOAD</sub> = 500Ω unless otherwise noted.

Symbol	Parameter	Min. <sup>(1)</sup>	Typ.	Max.	Unit
t <sub>PLH</sub>	Data Propagation Delay <sup>(2,3)</sup>	—	0.25	—	ns
t <sub>PHL</sub>	I <sub>x</sub> to Y	—	—	—	—
t <sub>PZL</sub>	Switch Turn-on Delay	0.5	—	5.2	ns
t <sub>PZH</sub>	S <sub>x</sub> to Y	—	—	—	—
t <sub>PLZ</sub>	Switch Turn-off Delay	0.5	—	4.8	ns
t <sub>PHZ</sub>	$\bar{E}_x$ to Y	—	—	—	—
t <sub>PLZ</sub>	Switch Turn-off Delay <sup>(2)</sup>	0.5	—	5	ns
t <sub>PHZ</sub>	$\bar{E}_x$ to Y, S <sub>x</sub> to Y	—	—	—	—

### NOTES:

- Minimums are guaranteed but not production tested.
- This parameter is guaranteed but not production tested.
- The bus switch contributes no propagation delay other than the RC delay of the ON resistance of the switch and the load capacitance. The time constant for the switch alone is of the order of 0.25ns for C<sub>L</sub> = 50pF. Since this time constant is much smaller than the rise and fall times of typical driving signals, it adds very little propagation delay to the system. Propagation delay of the bus switch, when used in a system, is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side.

## ORDERING INFORMATION



## Datasheet Document History

10/01/08	Pg. 5	Updated the ordering information by removing the "IDT" notation.
08/13/12	Pg. 5	Updated the ordering information by removing non RoHS part and by adding Tape and Reel information.



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