TPS63700EVM-139

This user's guide describes the characteristics, operation, and use of the TPS63700EVM-139 evaluation module (EVM). This EVM contains Texas Instruments TPS63700 dc/dc inverter IC that is capable of providing a negative output power supply from a positive input voltage. This user's guide includes EVM specifications, recommended test setup, test results, bill of materials (BOM), and a schematic diagram.

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1 Introduction

The Texas Instruments TPS63700EVM-139 evaluation module uses a TPS63700 dc/dc inverter IC that is capable of providing a negative output power supply from a positive input voltage. The goal of the EVM is to facilitate evaluation of the TPS63700.

1.1 Performance Specification Summary

Table 1 provides a summary of the TPS63700EVM-139 performance specifications. All specifications are given for an ambient temperature of 25°C.

Table 1. Typical Performance Specification Summary

	CONDITION	VOLTAGE RANGE (V)			CURRENT RANGE (mA)		
		MIN	TYP	MAX	MIN	TYP	MAX
VIN		2.7	3.3	5.5			2000
VOUT	V_I = 3.3 V	–12.64	–12	–11.44		150	
	V_I = 5 V					200	

1.2 Modifications

To aid user customization of the EVM, the board was designed with devices having 0603 or larger footprints. A real implementation would likely occupy less total board space.

Changing components can improve or degrade EVM performance. For example, using inductors with larger dc resistances lowers efficiency of the solution.

2 Input/Output Connector Descriptions

J1–VIN This is the positive connection to the input power supply. The leads to the input supply should be twisted and kept as short as possible.

J2–GND This is the return connection to the input power supply.

J3–OUT This is the negative output of the inverting dc/dc converter.

J4–GND This is the return connection for the load on the inverting dc/dc converter.

JP1–EN The enable pin for the IC is pulled to GND through a resistor to disable the device. Placing a jumper across this header connects the enable pin to V_{IN} and enables the device.

2.1 Test Setup

The absolute maximum input voltage is 6 V. The TPS63700 is designed to operate with a maximum input voltage of 5.5 V. Connect a power supply set between 2.7 V and 5.5 V output voltage and current limit set to at least 2 A. Short jumper JP1 to enable the IC.

2.2 Test Results

Below are the test results at T_A = 25°C using this EVM:

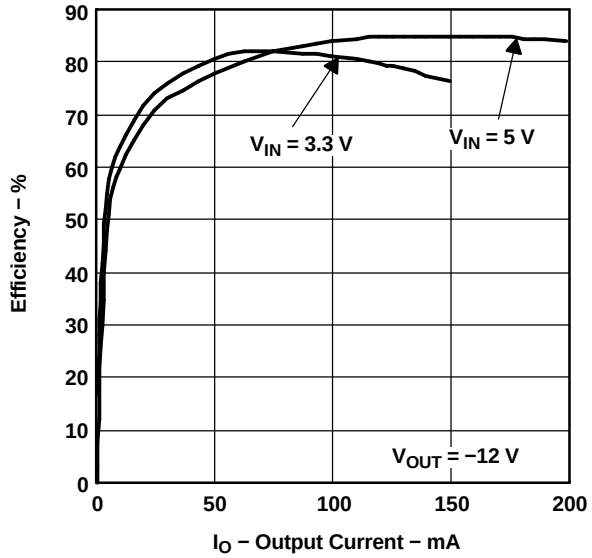

Figure 1. Efficiency vs. Output Current

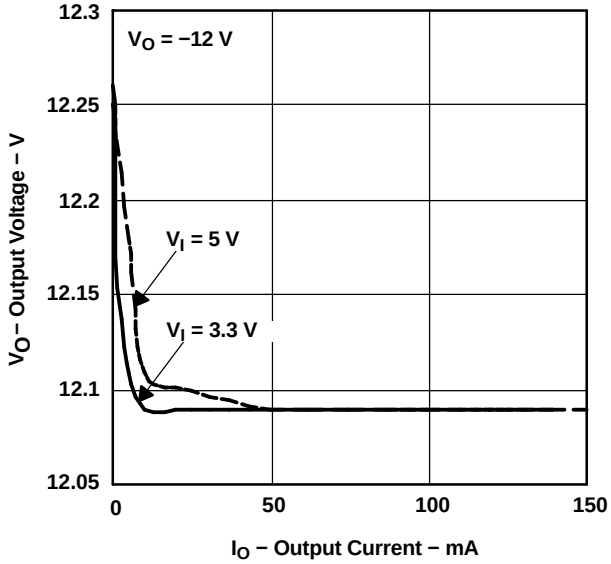

Figure 2. Output Voltage vs. Output Current

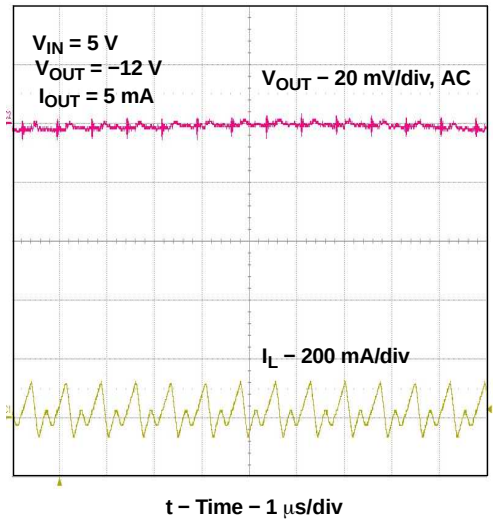

Figure 3. Output Ripple in Discontinuous Conduction Mode

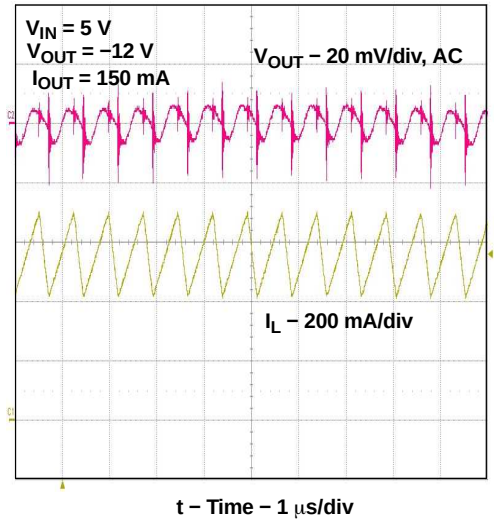

Figure 4. Output Ripple in Continuous Conduction Mode

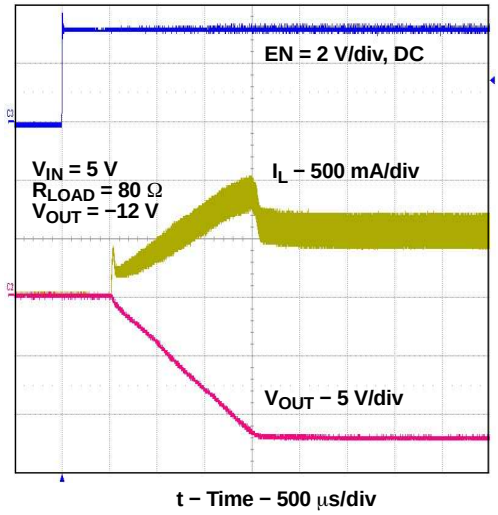

Figure 5. Startup After Enable

3 Board Layout

Board layout is critical for all switch mode power supplies. Figure 6, Figure 7, and Figure 8 show the board layout for the HPA139 PWB. The switching nodes with high-frequency noise are isolated from the noise-sensitive feedback circuitry, and careful attention has been given to the routing of high-frequency current loops. See the data sheet (SLVS530) for more specific layout guidelines.

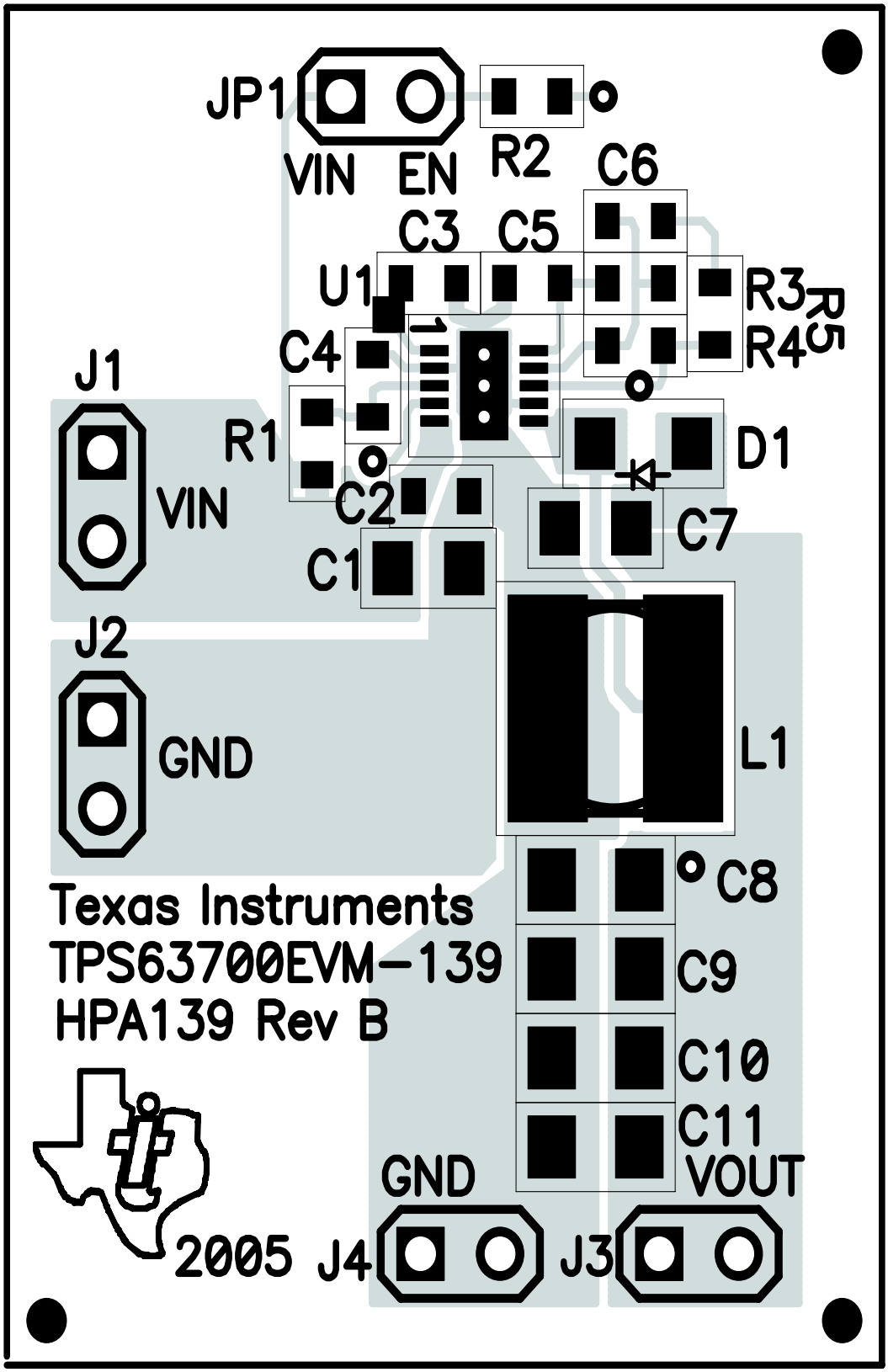

Figure 6. Top Assembly Layer

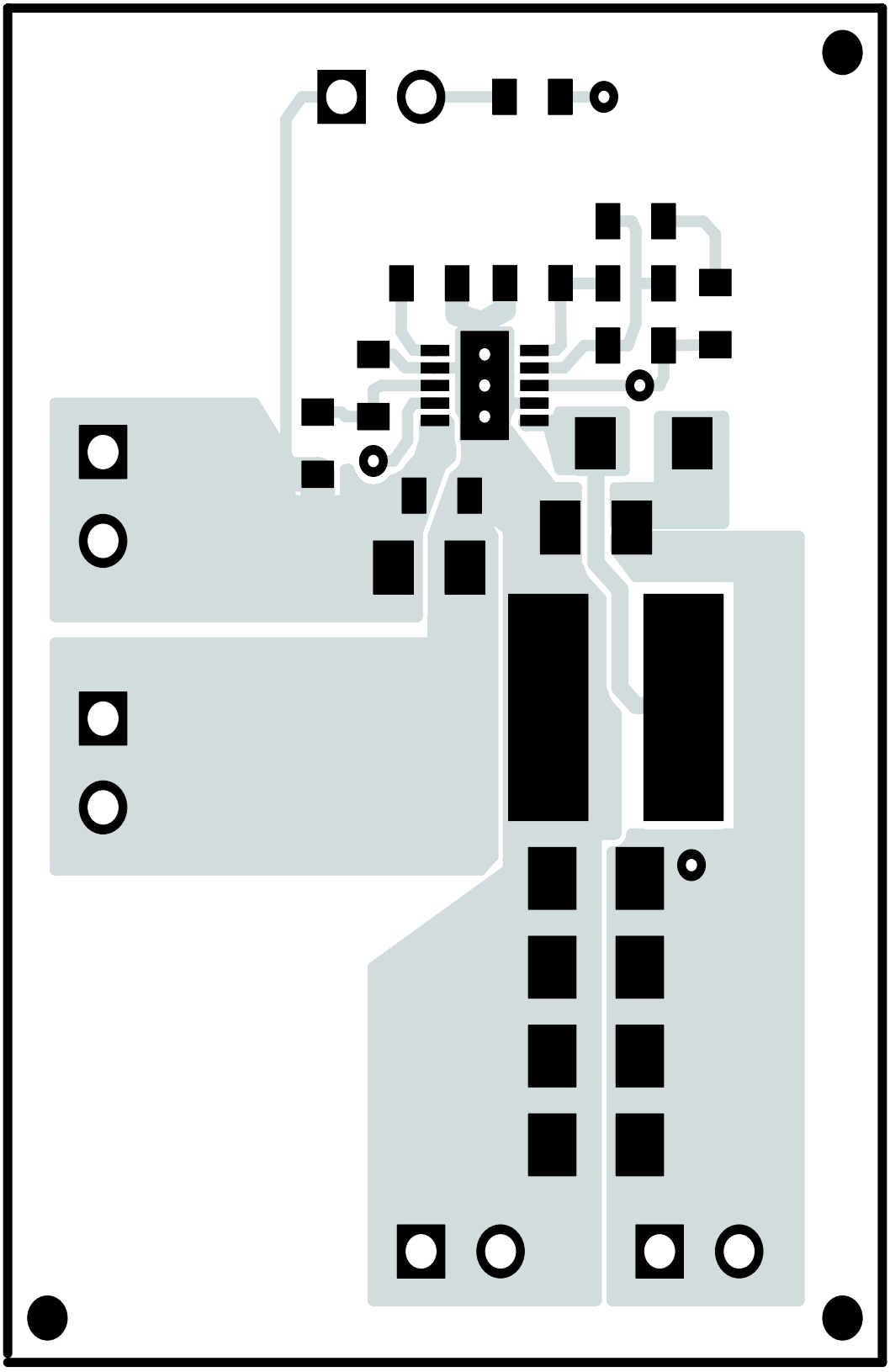

Figure 7. Top Layer

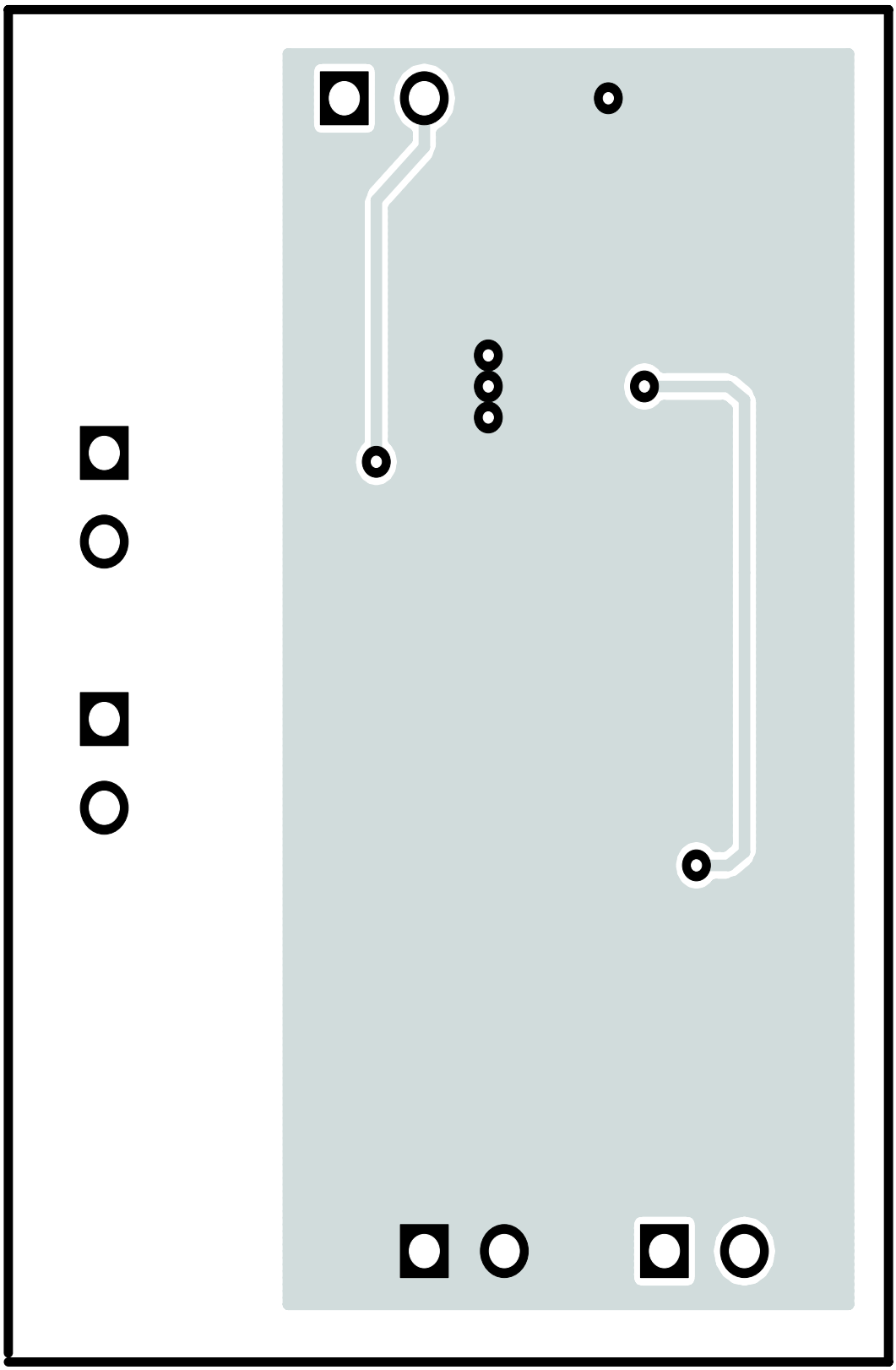

Figure 8. Bottom Layer

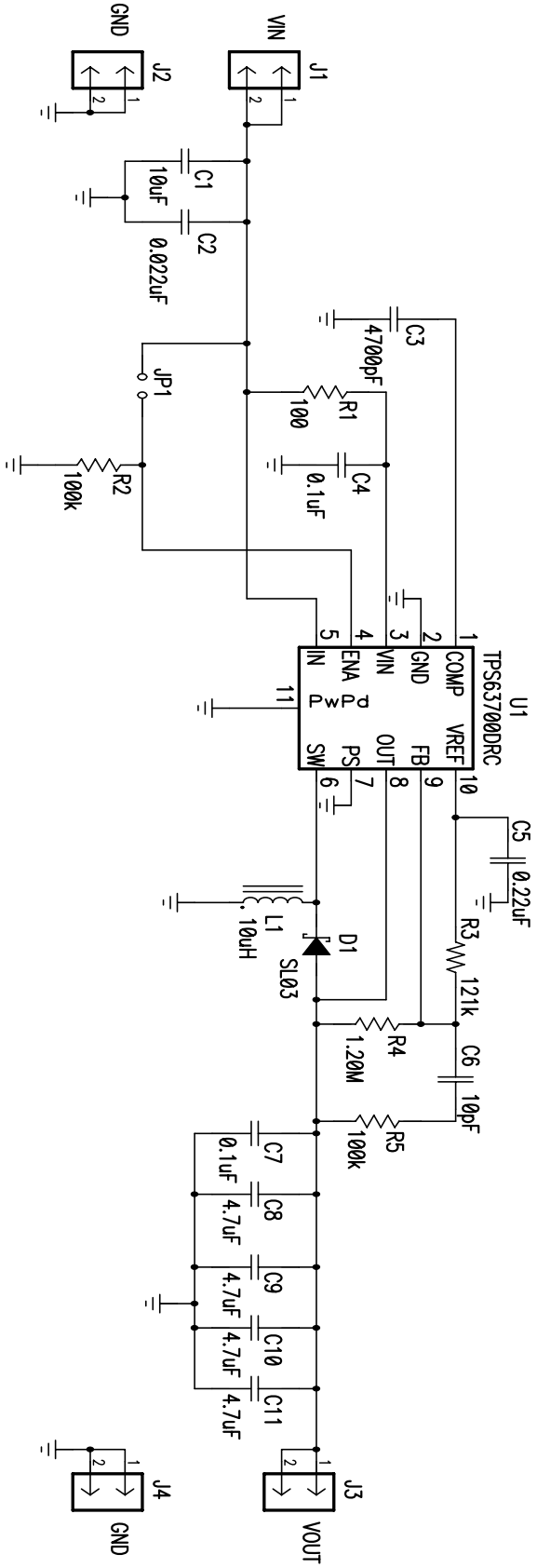

Figure 9. Schematic

4 Bill of Materials and Schematic

4.1 Bill of Materials

Table 2. HPA139 Bill of Materials

COUNT	REF DES	VALUE	DESCRIPTION	SIZE	PART NUMBER	MFR
1	C1	10uF	Capacitor, Ceramic, 10V, X5R, 10%	0805	C2012X5R1A106K	TDK
1	C2	0.022uF	Capacitor, Ceramic, 50V, X7R, 10%	0603	C1608X7R1H223KB	TDK
1	C3	4700pF	Capacitor, Ceramic, 50V, X7R, 10%	0603	C1608X7R1H472KB	TDK
1	C4	0.1uF	Capacitor, Ceramic, 50V, X7R, 10%	0603	C1608X7R1H104KB	TDK
1	C5	0.22uF	Capacitor, Ceramic, 16V, X7R, 10%	0603	C1608X7R1C224KB	TDK
1	C6	10pF	Capacitor, Ceramic, 50V, C0G, 5%	0603	C1608C0G1H100DB	TDK
1	C7	0.1uF	Capacitor, Ceramic, 50V, X7R, 10%	0805	C2012X7R1H104K	TDK
4	C8, C9, C10, C11	4.7uF	Capacitor, Ceramic, 25V, X7R, 20%	1206	C3216X7R1E475M	TDK
1	D1		Diode, Schottky Rectifier, 1.1A, 30 V	DO-219AB	SL03	Vishay
4	J1, J2, J3, J4		Header, 2-pin, 100mil spacing, (36-pin strip)	0.100 x 2	PTC36SAAN	
1	JP1		Header, 2-pin, 100mil spacing, (36-pin strip)	0.100 x 2	PTC36SAAN	
1	L1	10uH	Inductor, SMT Power, 1.2A, 124milliohms	0.224 inch	CDRH5D18NP-100NB	Sumida
1	R1	100	Resistor, Chip, 1/16W, 1%	0603	Std	Std
2	R2, R5	100k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R3	121k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R4	1.20M	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	U1		IC, Buck Boost DC-DC Inverter, 200 mA Output Typical	QFN-10	TPS63700DRC	TI
1	--		PCB, 1.515 In x 1.1 In x 0.062 In		HPA139	Any
1	--		Shunt, 100-mil, Black	0.100	929950-00	3M

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of 2.7 V to 5.5 V and the output voltage range of -12.64 V to -11.44 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 125°C. The EVM is designed to operate properly with certain components above 85°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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