FAIRCHILD SEMICONDUCTOR®

November 2012

FSA801 — USB2.0 High-Speed (480 Mbps), UART, and Audio Switch with Negative Signal Capability

Features

- 3:1 Switch Handles:
  - Audio Headsets
  - UART
  - Up to Two High- and Low-Speed USB Data
- USB Charger Detection and Indication, Compliant with USB Battery Charging Specification, Rev 1.1
  - Supports Data Contact Detect (DCD)
- Negative-Swing-Capable Audio Channel
- Built-in Termination Resistors for Audio Pop Reduction
- Simple Switch Control Using Three Select Pins
- 28 V Over-Voltage Tolerance on V_{BUS}

Applications

- Cell Phones, MP3 Players, PDAs

Description

The FSA801 is a 3:1 USB accessory switch that enables USB data, stereo and mono audio, microphone, and UART data to share a common connector port. Two ports are designed for high-speed USB 2.0 signaling, while also capable of full-speed USB and UART communication. The architecture allows audio signals to swing below ground so a common USB and headphone jack can be used for personal media players and portable peripheral devices.

FSA801 detects wall chargers through a dedicated pin that provides the baseband with charger detection. The charger function is compliant with USB Battery Charging Specification, Rev 1.1, implementing Data Contact Detect (DCD) before detecting a charger. The FSA801 indicates if a Dedicated Charging Port (DCP) or a Charging Downstream Port (CDP) has been connected.

The FSA801 meets both USB Rev. 2.0 and micro-USB specifications.

Ordering Information

Part Number	Operating Temperature Range	Top Mark	Package
FSA801UMX	-40 to +85°C	KL	16-Lead Quad, 1.8 x 2.6 mm Ultrathin Molded Leadless Package (UMLP)

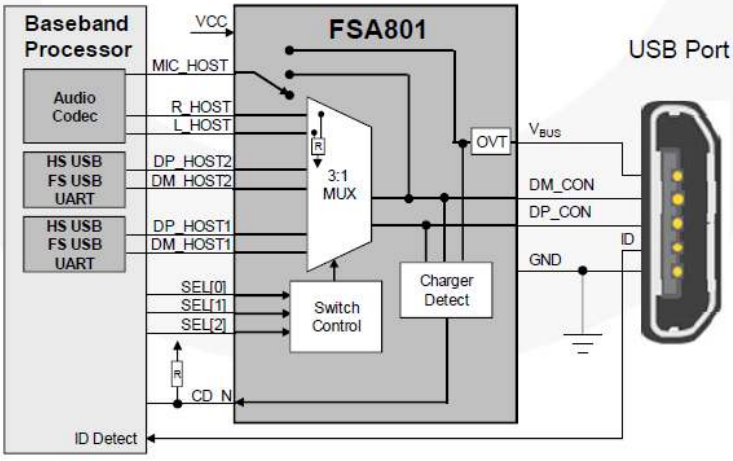


Figure 1. Typical Application

Functional Description

The FSA801 USB2.0 accessory switch is designed to consolidate wired accessories for portable devices, such as cellular telephones and portable audio players. The benefits of consolidation include reduced space requirements from a reduction of connectors and their size. The micro-USB connector, for example, reduces connector height and depth, allowing for slimmer overall designs. Using the USB industry standard and a common connector type for accessories such as chargers and headsets, greatly reduces the waste associated with new phone purchases by allowing re-use of the accessories.

Using just five wires for all connection types considerably reduces the cost of wired accessories and simplifies their construction. The FSA801 facilitates adopting this methodology because it is designed to redirect the DP/DM pins from the USB connector to one of three ports at the baseband's discretion. Additional flexibility is provided by the ability of the microphone line to be switched from either the DP_CON or VBUS pin.

The VBUS pin is protected up to 28 V without damage to the FSA801.

USB Charger Detection / Data Contact Detect

The FSA801 senses the presence of USB chargers per the *USB Battery Charging Specification, Version 1.1*. This specification uses V_{BUS} status and measurements on DP_CON / DM_CON pins to determine that a charging device might be attached. The 'CD_N' pin goes to a low state, indicating the presence of a charger. The charger-detect algorithm executes when V_{BUS} is valid. The charger-detection algorithm detects both Dedicated Charging Ports (DCP) and Charging Downstream Ports (CDP).

In this implementation, per the *USB Battery Charging Specification, Version 1.1*, the FSA801 implements Data Contact Detect (DCD) to insure the D+ and D- pins have made contact before the dedicated charger detection is performed.

Since the BC1.1 charger detection algorithm applies and detects signals on the D+ and D- lines, any additional loading effects from portable device host side of the switch would cause the results to be invalid. To prevent interference due to any loading, the FSA801 only performs charger detection when all switches are open. Additionally, if all switches are open and V_{BUS} is present, the FSA801 does not close any switch path until the DCD circuitry detects contact with the D+/D- pins and the charger detection is complete. If the D+/D- pins never contact, but V_{BUS} is present, the USB switches cannot be closed when configuring from SEL[2:0]='000' to SEL[2:0]='001' or SEL[2:0]='010'. To override this blocking, first switch to a non-USB mode (one of the audio modes, SEL[2:0]='011','100' or '101'), and then to the desired USB mode.

If the USB physical layer device that the FSA801 is connected to also performs DCD, it should not start until after the FSA801 has time to finish its detection function (since the delay between VBUS connection and D+/D- connection is not defined, this detection function time cannot be defined either).

Glitches on VBUS that occur when V_{BUS} is not driven (positive voltage spikes and on-off situations at the beginning of a cable attach) are automatically filtered by the DCD state machine timing.

To manually reset the FSA801 to search for a charger again, switch to SEL[2:0]='111' for a minimum of 30 µs. After this state machine is reset, the next time that SEL[2:0]='000' (all switches open) for a minimum of 30 µs, the FSA801 begins the charger detection sequence.

PLEASE NOTE: The FSA801 is guaranteed to operate down to 2.4 V. If the FSA801 V_{CC} is connected directly to a battery and falls below 2.4 V, the FSA801 may not correctly detect a charger. If a charger is applied, the V_{CC} should start to rise above 2.4 V. In this situation, the FSA801 does not automatically check for a charger again, so the FSA801 should be placed in SEL[2:0]='111' for 30 µs (min.), then SEL[2:0]='000' for 30 µs (min.) to perform the charger detection again.

Applications with Multiple USB Controllers

When operating with two USB controllers, it is recommended to configure the switches to OPEN before switching to the other (second) USB interface. The OPEN setting duration should be long enough for the accessory to go to a SE0 state, so when the switch is set to the other (second) USB port, the new controller re-enumerates.

Mode Descriptions

The FSA801 has three select pins to control the switching operations, SEL[0], SEL[1], and SEL[2] described in Table 1.

Table 1. Selection Truth Table

SEL[2]	SEL[1]	SEL[0]	Switch Action	Description
0	0	0	OPEN	Open all switch paths (device in low-power mode)
0	0	1	USB1, UART	Closes USB1 path to D+/D-, default condition(1) - DP_CON connected to DP_HOST1 - DM_CON connected to DM_HOST1
0	1	0	USB2, UART	Closes USB2 path to D+/D- - DP_CON connected to DP_HOST2 - DM_CON connected to DM_HOST2
0	1	1	AUDIO	Closes audio path to D+/D- only, no microphone switched - DP_CON connected to R_HOST - DM_CON connected to L_HOST
1	0	0	MONO AUDIO with MIC on D+(2)	Closes audio path to DM_CON and microphone on DP_CON pin. This is a mono-audio application. - DP_CON connected to MIC - DM_CON connected to L_HOST
1	0	1	STEREO AUDIO with MIC on VBUS(2)	Closes audio path to D+/D- and microphone on V_{BUS} pin. This mode is typically used for stereo headset with microphone. - DP_CON connected to R_HOST - DM_CON connected to L_HOST - V_{BUS} connected to MIC
1	1	0	Undefined	Reserved; do not use.
1	1	1	Charger Detection Reset	Charger Detection Reset. Selecting this mode for greater than 30 µs resets the FSA801 to check for a charger, the next time a SEL[2:0] state of ‘000’ is applied for more than 30 µs.

Notes:

1. The SELECT pins are CMOS inputs and should not be left in a floating condition. Some applications require the UART path be in the CLOSED position on power-up for initial programming of the device under test. If that condition is desired, the three SELECT pins should be pulled to the correct levels with external resistors that should exceed 100 KΩ to reduce the static power consumption. In other applications, adding weak pull-down resistors to GND defaults the device to all paths open (low-power mode).
2. When the audio switch is in the OPEN position, the R and L are terminated to GND with internal termination resistors to discharge any stray capacitance that could cause audio pop.

Pin Configuration

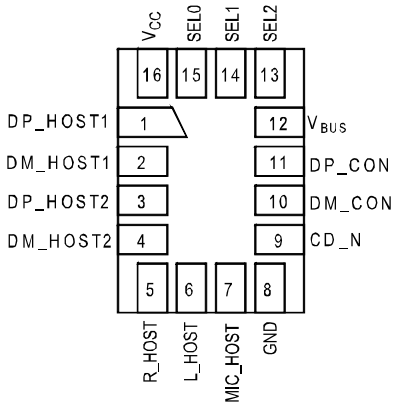


Figure 2. 16-Pin, UMLP Pin Assignments (Top-Through View)

Pin Descriptions

Name	Pin #	Description
USB, UART Interface		
DP_HOST1	1	D+ signal, dedicated USB port to be connected to the resident USB or UART transceiver on the phone.
DM_HOST1	2	D- signal, dedicated USB port to be connected to the resident USB or UART transceiver on the phone.
DP_HOST2	3	D+ signal, dedicated USB port to be connected to the resident USB or UART transceiver on the phone.
DM_HOST2	4	D- signal, dedicated USB port to be connected to the resident USB or UART transceiver on the phone.
Audio Interface		
R_HOST	5	Right audio channel from phone audio codec.
L_HOST	6	Left audio channel from phone audio codec.
MIC_HOST	7	Connected to the phone audio codec MIC input pin.
Power Interface		
V_{CC}	16	Input voltage supply pin to be connected to the phone battery output.
Connector Interface		
V_{BUS}	12	Input voltage supply pin to be connected to the V_{BUS} pin of the USB connector.
GND	8	Ground.
DP_CON	11	Connected to the USB connector D+ pin; depending on the FSA801 signaling mode, this pin can share DP_HOST1, DP_HOST2 or R_HOST signals.
DM_CON	10	Connected to the USB connector D- pin; depending on the FSA801 signaling mode, this pin can share DM_HOST1, DM_HOST2 or L_HOST signals.
Charger Detection		
CD_N	9	Active-LOW, open-drain output pin; requires pull-up resistor to baseband I/O voltage supply
Switch Control		
SEL[2:0]	13-15	Switch selection pins; *refer to Table 1 for truth table.*

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter			Min.	Max.	Unit
V_{CC}	Supply Voltage from Battery / Baseband			-0.5	6.0	V
V_{BUS}	Voltage from Mini/Micro–USB Connector			-0.5	28.0	V
V_{SW}	Switch I/O Voltage	USB/UART Path Active		-0.5	V_{BUS} +0.5	V
		Stereo/Mono Audio Path Active		V_{CC}-8.5	V_{CC} +0.5	
		All Other Channels		-0.5	V_{CC} +0.5	
I_{IK}	Input Clamp Diode Current			-50		mA
I_{SW}	Switch I/O Current (Continuous)	USB			50	mA
		Audio			60	
		All Other Channels			50	
I_{SWPEAK}	Peak Switch Current (Pulsed at 1ms Duration, <10% Duty Cycle)	USB			150	mA
		Audio			150	mA
		All Other Channels			150	mA
T_{STG}	Storage Temperature Range			-65	+150	°C
T_J	Maximum Junction Temperature				+150	°C
T_L	Lead Temperature (Soldering, 10 Seconds)				+260	°C
ESD	IEC 61000-4-2 System	USB Connector Pins (D+, D-, V_{BUS})	Air Gap		15	kV
			Contact		8	
	Human Body Model, JEDEC JESD22-A114		All Pins		3	
	Charged Device Model, JEDEC JESD22-C101		All Pins		2	

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter		Min.	Max.	Units
V_{CC}	Battery Supply Voltage		2.7	4.4	V
V_{SW}	Switch I/O Voltage	USB/UART Path Active	0	4.4	V
		Audio Path Active	V_{CC}-7.0	2.0	V
		Mic Path Active	0	V_{CC}-1	V
T_A	Operating Temperature		-40	+85	ºC

Switch Path DC Electrical Characteristics

All typical values are at 25°C unless otherwise specified.

Symbol	Parameter	V_{CC} (V)	Conditions	T_A = -40 to +85°C			Unit
				Min.	Typ.	Max.	
Host Interface Pins (SEL[2:0])							
V_{IH}	Input High Voltage	3.2 to 4.4		1.3			V
V_{IL}	Input Low Voltage	3.2 to 4.4				0.7	V
I_{IN}	Control Input Leakage	0 to 4.4	V_{SW}=0 to V_{CC}	-1		1	µA
I_{OZ}	Off State Leakage	4.4	0 ≤ DP_CON, DM_CON, DP_HOSTn, DM_HOSTn, R_HOST, L_HOST ≤ 3.6 V	-2		2	µA
Charger Detect Pin (CD_N)							
V_{OL}	Output Low Voltage	3.2 to 4.4	I_{OL}=10 mA			0.4	V
V_{BUS} Pin							
V_{BUSTH}	Charger Detect Threshold	3.2 to 4.4			3.3		V
I_{BUSIN}	V_{BUS} Input Leakage	0 to 4.4			2	10	µA
Switch Off Characteristics							
I_{OFF}	Power Off Leakage Current	0	All Ports Except MIC & Audio Path V_{SW}=0 V to 4.4 V, Figure 7			10	µA
USB Switch On Paths							
R_{ONUSB}	HS USB Range Switch On Resistance	3.2 to 4.4	V_{DP_CON/DM_CON}=0 V, 0.4 V, I_{ON}=8 mA, Figure 6		6	9	Ω
R_{ONUART}	UART Range Switch On Resistance	3.2 to 4.4	V_{DP_CON/DM_CON}=0 V, 3.2 V, I_{ON}=8 mA, Figure 6		8		Ω
Audio R/L Switch On Paths							
R_{ONAUD}	Audio Switch On Resistance	3.2 to 4.4	$V_{L/R}$=-0.8 V, 0.8 V, I_{ON}=30 mA, Figure 6			3	Ω
R_{FLAT}	Audio R_{ON} Flatness[3]	3.8			0.16		Ω
R_{TERM}	Internal Termination Resistors				1		kΩ
MIC Switch On Path							
R_{ONMIC}	Switch On Resistance	3.2 to 4.4	SEL[2:0]=100 (MIC to DP_CON), V_{SW}=0 V, 1.6 V, I_{ON}=8 mA, Figure 6		15		Ω
			SEL[2:0]=101 (MIC to VBUS), V_{SW}=0 V, 1.6 V, I_{ON}=8 mA, Figure 6		28		Ω
Total Switch Current Consumption							
I_{CCSL}	Battery Supply Sleep Mode Average Current	3.2 to 4.4	Static Current During Sleep Mode (SEL[2:0]=0)			1	µA
I_{CCWK}	Battery Supply Active Mode Average Current	3.2 to 4.4	USB/UART Mode		20	35	µA
			Audio Mode (SEL[2:0]=011), V_{BUS}=0 V			1	µA
			Audio Mode (SEL[2:0]=100, 101)		20	35	µA
I_{CCSELT}	Increase in I_{CCSL}/I_{CCWK} Current per Control Voltage and V_{CC}	3.2 to 4.4	V_{SEL} = 2.8 V and V_{CC} = 4.4 V			8	µA
			V_{SEL} = 1.8 V and V_{CC} = 4.4 V			10	µA

Note:

3. Flatness is defined as the difference between the maximum and minimum values of on resistance over the specified range of conditions.

Switch Path AC Electrical Characteristics[4]

All typical value are for V_{CC} =3.8 V at 25°C unless otherwise specified.

Symbol	Parameter		V_{CC} (V)	Conditions	T_A = -40 to +85°C			Unit	Figure
					Min.	Typ.	Max.		
Xtalk	Active Channel Crosstalk DP_CON to DM_CON	Audio Mode	3.8	f=20 kHz, R_T=32 Ω, C_L=0 pF		-95		dB	Figure 9
		USB Mode	3.8	f=1 MHz, R_T=50 Ω, C_L=0 pF		-78			
				f=240 MHz, R_T=50 Ω, C_L=0 pF		-36			
	Active Channel Crosstalk MIC	MIC on VBUS to R_HOST, L_HOST	3.8	f=20 kHz, R_T=32 Ω, C_L=0 pF		-93			
		MIC on DP_CON to L_HOST	3.8	f=20 kHz, R_T=32 Ω, C_L=0 pF		-105			
O_{IRR}	Off Isolation Rejection Ratio	Audio Rejection L_HOST to DM_CON, R_HOST to DP_CON	3.8	f=20 kHz, R_T=32 Ω, C_L=0 pF		-100		dB	Figure 8
		MIC Rejection MIC_HOST to DP_CON	3.8	f=20 kHz, R_T=50Ω, C_L=0pF		-110			
		MIC Rejection MIC_HOST to VBUS	3.8	f=20 kHz, R_T=50 Ω, C_L=0 pF		-110			
		USB Rejection DM_HOST to DM_CON, DP_HOST to DP_CON	3.8	f=1 MHz, R_T=50 Ω, C_L=0 pF		-85			
				f=240 MHz, R_T=50 Ω, C_L=0 pF		-35			
PSRR	Power Supply Rejection Ratio MIC on VBUS or MIC on DP_CON, to VCC or GND		3.8	Power Supply Noise 300Mv_{PP}, f=217Hz		-110		dB	
THD+N	Total Harmonic Distortion + Noise (Audio Path)		3.8	20 Hz to 20 kHz, R_L=16 Ω, Input Signal Range 1.6 V_{PP}		0.10		%	Figure 13
				20 Hz to 20 kHz, R_L=32 Ω, Input Signal Range 1.6 V_{PP}		0.07		%	Figure 13
t_{CDR}	Charger Detection Reset Time: Minimum time in Selected State to Reset Charger Detection State Machine.		3.8	SEL[2:0]='111'	30			µs	
t_{CDL}	Charger Detection Start Time: Minimum Time in Selected State to Start Charger Detection sequence		3.8	SEL[2:0]='000'	30			µs	

Note:

4. Guaranteed by characterization, not production tested.

Capacitance

Symbol	Parameter	V_{CC} (V)	Conditions	T_A = -40 to +85°C		Unit	Figure
				Typ.	Max.		
C_{IN}	Select Pins Capacitance[5]	0	V_{BIAS}=0.2 V	2.5		pF	Figure 11
$C_{OFF(D+, D-)}$	D+, D- On Capacitance (HS USB Mode)[5]	3.8	V_{BIAS}=0.2 V, f=1 MHz	4.7		pF	Figure 11
$C_{ON(D+, D-)}$	D+, D- On Capacitance (HS USB Mode)[5]	3.8	V_{BIAS}=0.2 V, f=1 MHz	7.6		pF	Figure 12

Note:

5. Guaranteed by characterization, not production tested.

High-Speed USB Eye Compliance Results

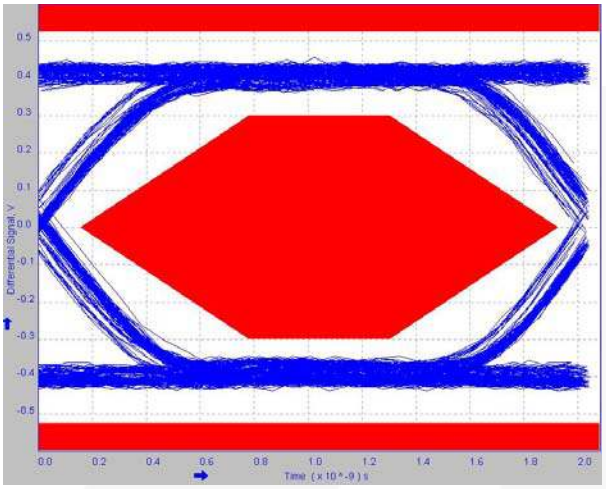


Figure 3. High-Speed Test Results (DP_CON/DM_CON – DP_HOST1/DM_HOST1)

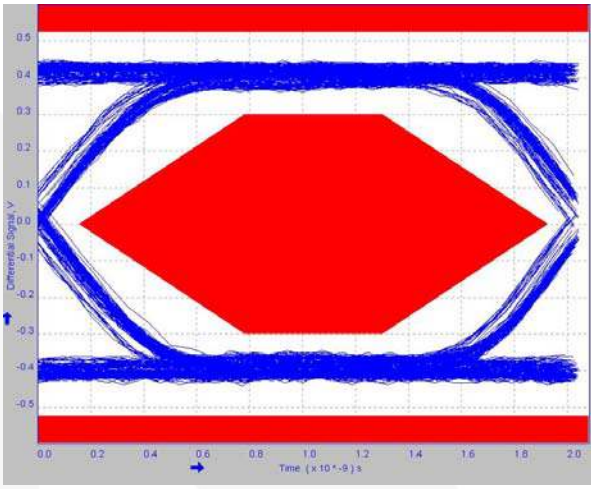


Figure 4. High-Speed Test Results (DP_CON/DM_CON – DP_HOST2/DM_HOST2)

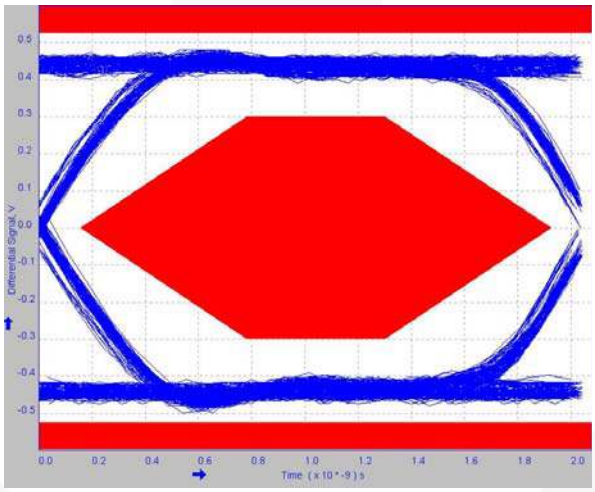


Figure 5. High-Speed Eye Compliance Input Signal

Test Diagrams

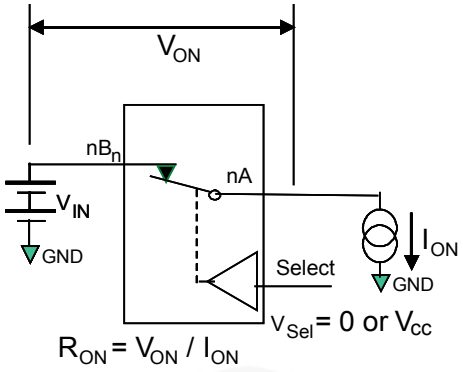
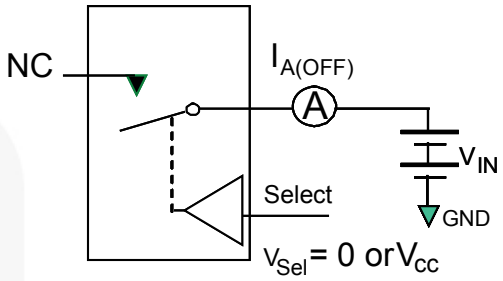


Figure 6. On Resistance



**Each switch port is tested separately.

Figure 7. Off Leakage

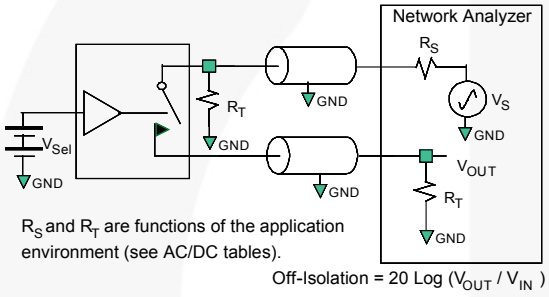


Figure 8. Channel Off Isolation

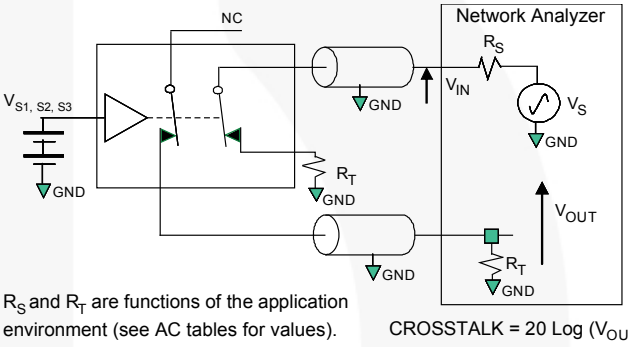
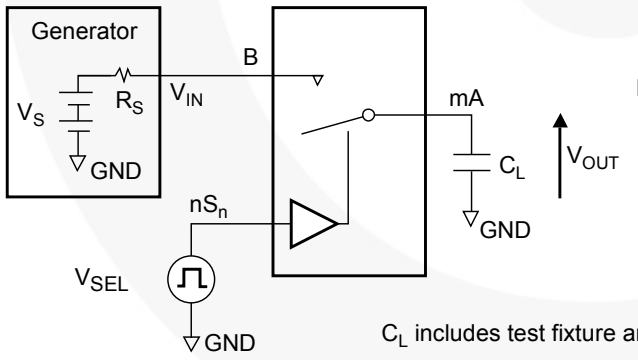


Figure 9. Active Channel Crosstalk



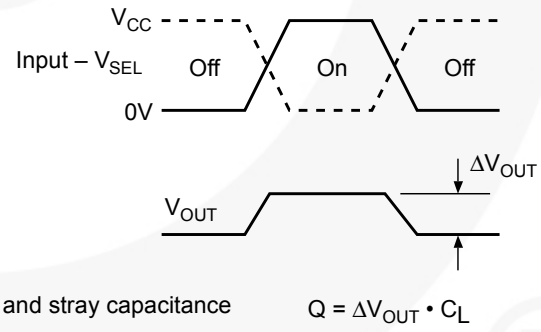


Figure 10. Charge Injection Test

Test Diagrams (Continued)

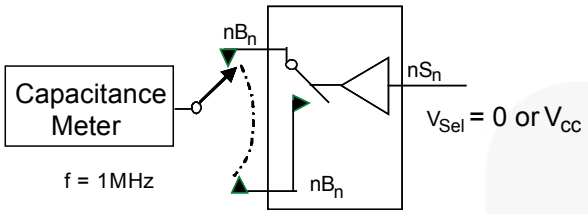


Figure 11. Channel Off Capacitance

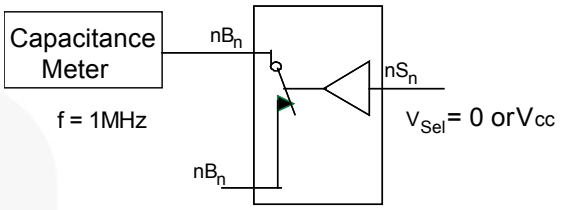
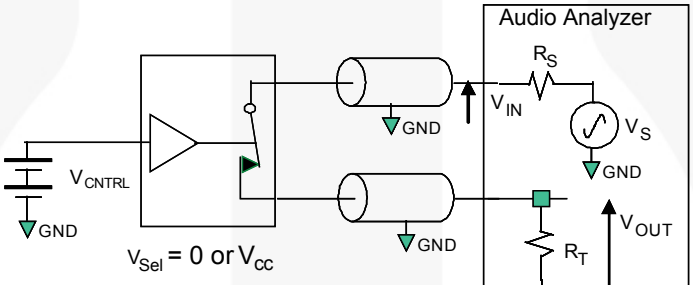


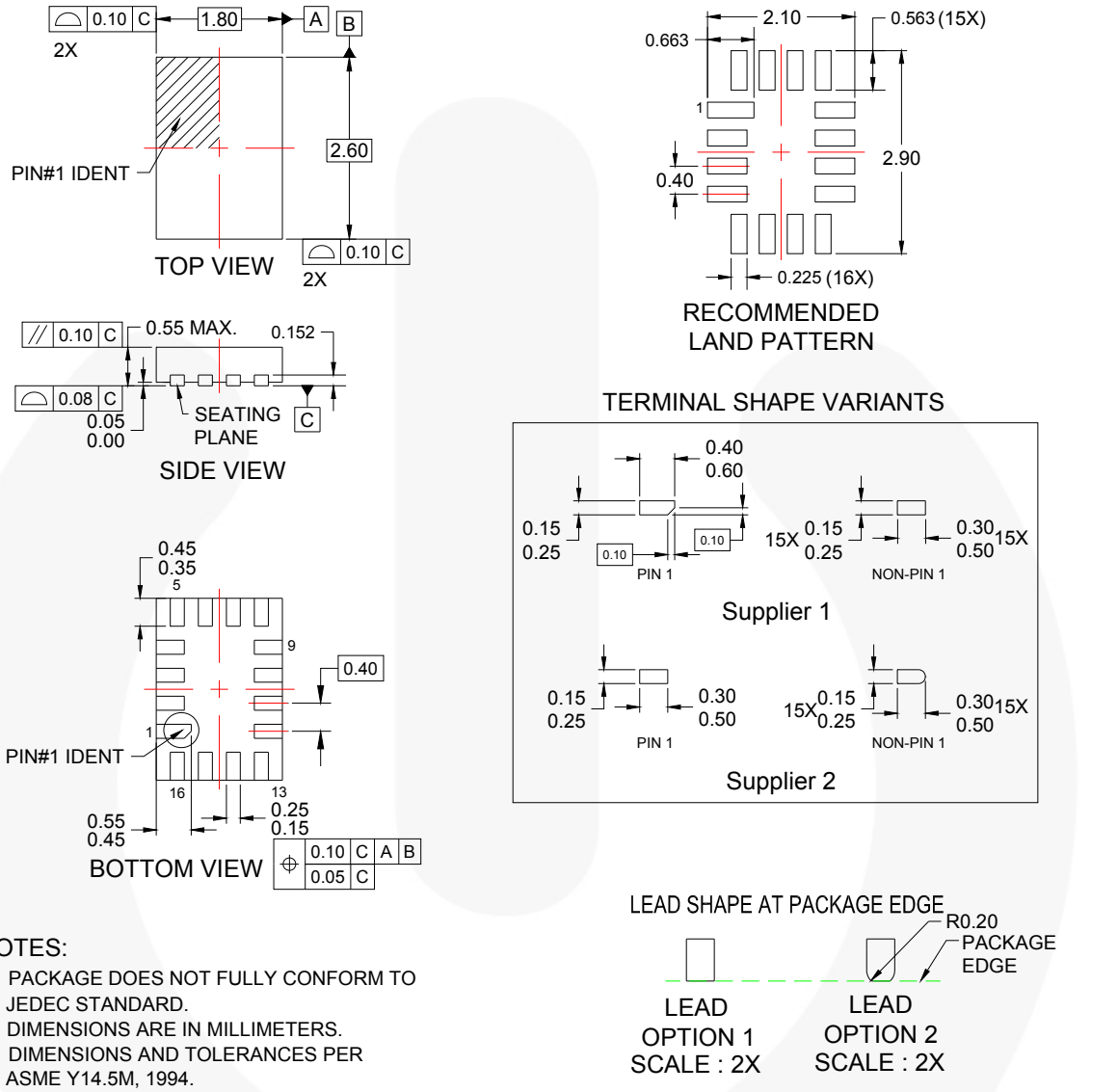
Figure 12. Channel On Capacitance



R_S and R_T are functions of the application environment (see AC Tables for specific values).

Figure 13. Total Harmonic Distortion + Noise

Physical Dimensions



NOTES:

A. PACKAGE DOES NOT FULLY CONFORM TO JEDEC STANDARD.
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
D. LAND PATTERN RECOMMENDATION IS BASED ON FSC DESIGN ONLY.
E. DRAWING FILENAME: MKT-UMLP16Arev4.
F. TERMINAL SHAPE MAY VARY ACCORDING TO PACKAGE SUPPLIER, SEE TERMINAL SHAPE VARIANTS.

Figure 14. 16-Lead, Ultrathin Molded Leadless Package (UMLP)

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings:
http://www.fairchildsemi.com/packaging/.

FAIRCHILD SEMICONDUCTOR®

TRADEMARKS

The following includes registered and unregistered trademarks and service marks, owned by Fairchild Semiconductor and/or its global subsidiaries, and is not intended to be an exhaustive list of all such trademarks.

2Cool™
AccuPower™
AX-CAP™*
BitSiC™
Build it Now™
CorePLUS™
CorePOWER™
CROSSVOLT™
CTL™
Current Transfer Logic™
DEUXPEED®
Dual Cool™
EcoSPARK®
EfficientMax™
ESBC™
F®
Fairchild®
Fairchild Semiconductor®
FACT Quiet Series™
FACT®
FAST®
FastvCore™
FETBench™
FlashWriter®*
FPS™
F-PFS™
FRFET®
Global Power Resource℠
GreenBridge™
Green FPS™
Green FPS™ e-Series™
Gmax™
GTO™
IntelliMAX™
ISOPLANAR™
Making Small Speakers Sound Louder and Better™
MegaBuck™
MICROCOUPLER™
MicroFET™
MicroPak™
MicroPak2™
MillerDrive™
MotionMax™
mWSaver™
OptoHiT™
OPTOLOGIC®
OPTOPLANAR®
PowerTrench®
PowerXS™
Programmable Active Droop™
QFET®
QS™
Quiet Series™
RapidConfigure™
™
Saving our world, 1mW/W/kW at a time™
SignalWise™
SmartMax™
SMART START™
Solutions for Your Success™
SPM®
STEALTH™
SuperFET®
SuperSOT™-3
SuperSOT™-6
SuperSOT™-8
SupreMOS®
SyncFET™
Sync-Lock™
SYSTEM GENERAL®*
The Power Franchise®
the power franchise
TinyBoost™
TinyBuck™
TinyCalc™
TinyLogic®
TINYOPTO™
TinyPower™
TinyPWM™
TinyWire™
TranSiC™
TriFault Detect™
TRUECURRENT®*
μSerDes™
SerDes
UHC®
Ultra FRFET™
UniFET™
VCX™
VisualMax™
VoltagePlus™
XS™

* Trademarks of System General Corporation, used under license by Fairchild Semiconductor.

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION, OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS. THESE SPECIFICATIONS DO NOT EXPAND THE TERMS OF FAIRCHILD'S WORLDWIDE TERMS AND CONDITIONS, SPECIFICALLY THE WARRANTY THEREIN, WHICH COVERS THESE PRODUCTS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.

As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

ANTI-COUNTERFEITING POLICY

Fairchild Semiconductor Corporation's Anti-Counterfeiting Policy. Fairchild's Anti-Counterfeiting Policy is also stated on our external website, www.fairchildsemi.com, under Sales Support.

Counterfeiting of semiconductor parts is a growing problem in the industry. All manufacturers of semiconductor products are experiencing counterfeiting of their parts. Customers who inadvertently purchase counterfeit parts experience many problems such as loss of brand reputation, substandard performance, failed applications, and increased cost of production and manufacturing delays. Fairchild is taking strong measures to protect ourselves and our customers from the proliferation of counterfeit parts. Fairchild strongly encourages customers to purchase Fairchild parts either directly from Fairchild or from Authorized Fairchild Distributors who are listed by country on our web page cited above. Products customers buy either from Fairchild directly or from Authorized Fairchild Distributors are genuine parts, have full traceability, meet Fairchild's quality standards for handling and storage and provide access to Fairchild's full range of up-to-date technical and product information. Fairchild and our Authorized Distributors will stand behind all warranties and will appropriately address any warranty issues that may arise. Fairchild will not provide any warranty coverage or other assistance for parts bought from Unauthorized Sources. Fairchild is committed to combat this global problem and encourage our customers to do their part in stopping this practice by buying direct or from authorized distributors.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

Rev. I62