

UM11593

PTN3816EVM evaluation board

Rev. 1.0 — 8 June 2021

User manual

Document information

Information	Content
Keywords	PTN3816, DisplayPort, Linear Redriver
Abstract	This user manual demonstrates application board capability of interfacing a DisplayPort monitor with a host computer through full size DP connector cable. The application board is intended for use as an evaluation and customer demonstration tool, as well as a reference design.



Revision history

Rev	Date	Description
v.1.0	20210608	Initial version

1 Important notice

NXP provides the enclosed product(s) under the following conditions:

This evaluation kit is intended for use of ENGINEERING DEVELOPMENT OR EVALUATION PURPOSES ONLY. It is provided as a sample IC pre-soldered to a printed circuit board to make it easier to access inputs, outputs, and supply terminals. This evaluation board may be used with any development system or other source of I/O signals by simply connecting it to the host MCU or computer board via off-the-shelf cables. This evaluation board is not a Reference Design and is not intended to represent a final design recommendation for any particular application. Final device in an application will be heavily dependent on proper printed circuit board layout and heat sinking design as well as attention to supply filtering, transient suppression, and I/O signal quality.

The goods provided may not be complete in terms of required design, marketing, and or manufacturing related protective considerations, including product safety measures typically found in the end product incorporating the goods. Due to the open construction of the product, it is the user's responsibility to take any and all appropriate precautions with regard to electrostatic discharge. In order to minimize risks associated with the customers applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards. For any safety concerns, contact NXP sales and technical support services.

2 Introduction

PTN3816 is a DisplayPort high-performance linear redriver, suitable for DisplayPort Upstream (DP source side) and Downstream (DP sink side) applications. It addresses high-speed signal integrity enhancement requirements for the implementation of DisplayPort interfaces in various system platforms and applications.

This document explains in detail how the PTN3816EVM evaluation board should be connected in a system to interface between a host PC and a DisplayPort monitor. The document also illustrates using DIP switch settings to configure the transmitters' and receivers' equalizer settings on the PTN3816EVM evaluation board.

3 Finding kit resources and information on the NXP web site

NXP Semiconductors provides online resources for this evaluation board and its supported device(s) on <http://www.nxp.com>.

The information page for PTN3816EVM evaluation board is at <http://www.nxp.com/PTN3816EVM>. The information page provides overview information, documentation, software and tools, parametrics, ordering information and a Getting Started tab. The Getting Started tab provides quick-reference information applicable to using the PTN3816EVM evaluation board, including the downloadable assets referenced in this document.

3.1 Collaborate in the NXP community

The NXP community is for sharing ideas and tips, ask and answer technical questions, and receive input on just about any embedded design topic.

The NXP community is at <http://community.nxp.com>.

4 Get started

The NXP analog product development boards provide an easy-to-use platform for evaluating NXP products. The boards support a range of analog, mixed-signal and power solutions. They incorporate monolithic integrated circuits and system-in-package devices that use proven high-volume technology. NXP products offer longer battery life, a smaller form factor, reduced component counts, lower cost, and improved performance in powering state-of-the-art systems.

This section will guide you through the process of setting up and using the PTN3816EVM evaluation board.

4.1 Kit contents/packing list

The PTN3816EVM contents include:

- Assembled and tested evaluation board in an anti-static bag
- Quick Start Guide

4.2 Minimum system requirements

This evaluation board requires a Windows PC workstation. Meeting these minimum specifications should produce great results when working with this evaluation board.

- One PC/Notebook with DisplayPort connector
- One DisplayPort Monitor
- One micro USB cable to provide power to EVK
- Two DisplayPort cables (one to be connected between PC and EVK, and the other one to be plugged between EVK and DisplayPort monitor)
- EVK board

5 Get to know the hardware

5.1 Board features

- DisplayPort connections to PC and Monitor
- Onboard jumper settings for equalizer gain and output swing level

5.2 Board description

The PTN3816EVM evaluation board is designed to redrive DisplayPort signal outputs from a host graphics card, and interface with a DisplayPort monitor or a DP-to-HDMI level shifter on the other side. There is a row of DIP switches on the EVM that can change PTN3816's equalizer, output swing linearity and flat gain settings of the redriver channels.

The PTN3816EVM evaluation board's power is supplied from a micro-USB connector, and an on-board LDO converts 5 V input to both 3.3 V and 1.8 V. 3.3 V is only used to provide power to a downstream cable or level shifter dongle. 1.8 V is used for PTN3816.

5.3 Board components

Overview of the PTN3816EVM evaluation board is shown in [Figure 1](#).



Figure 1. PTN3816EVM evaluation board

5.4 Block diagram

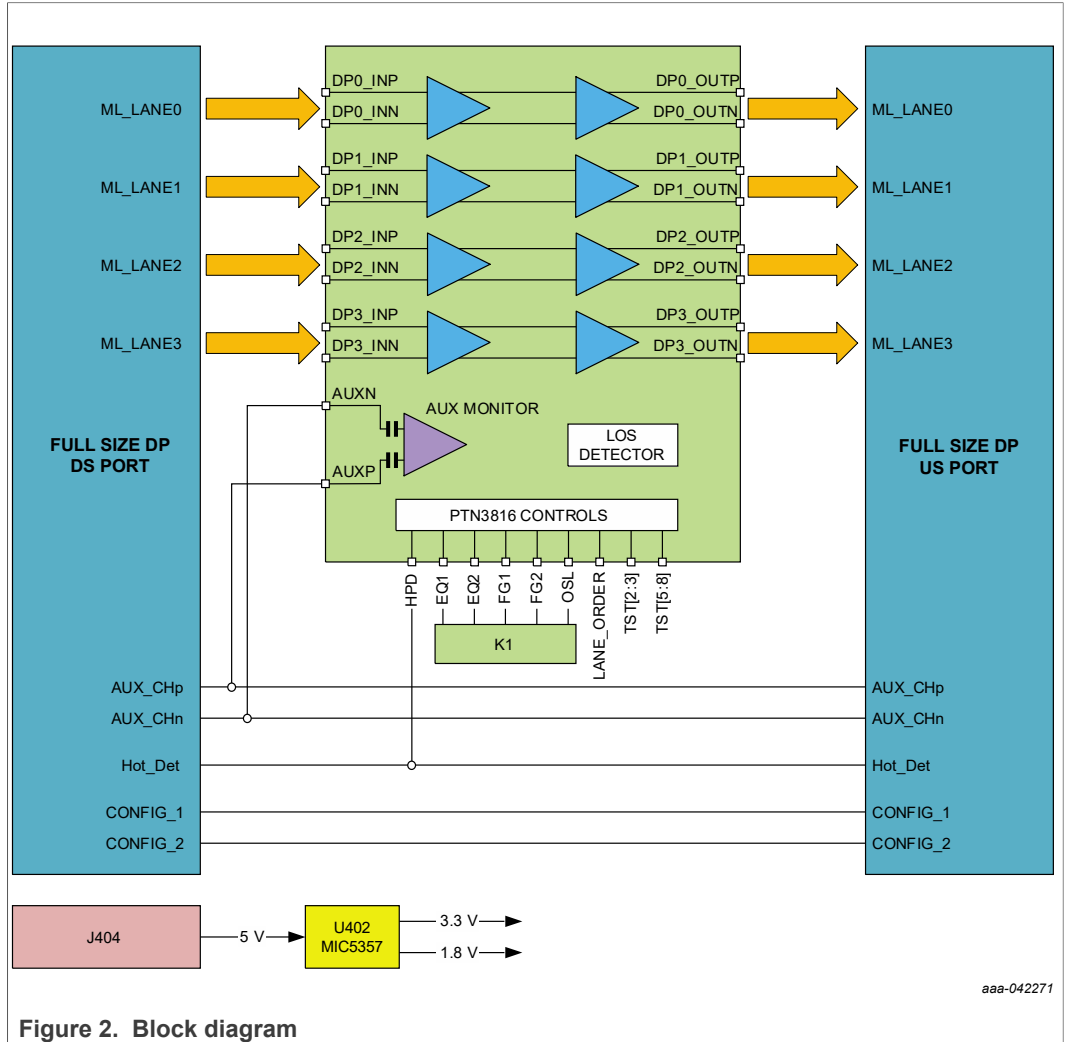


Figure 2. Block diagram

5.5 PTN3816EVM evaluation board schematics

5.5.1 PTN3816EVM evaluation board schematic

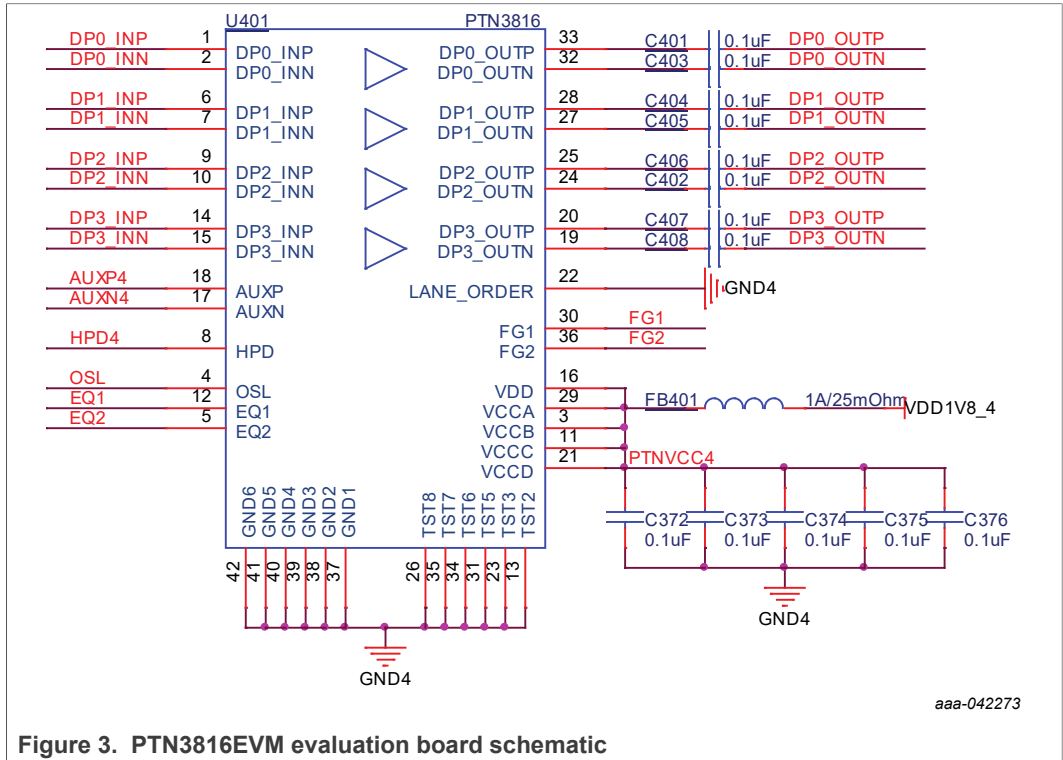
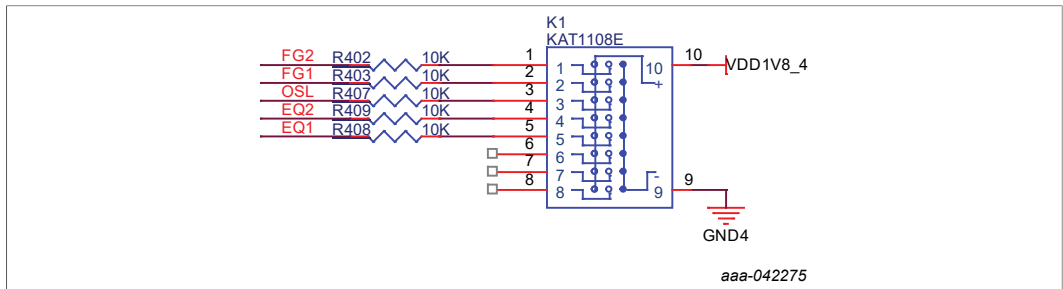


Figure 3. PTN3816EVM evaluation board schematic

5.5.2 PTN3816EVM evaluation board control switches



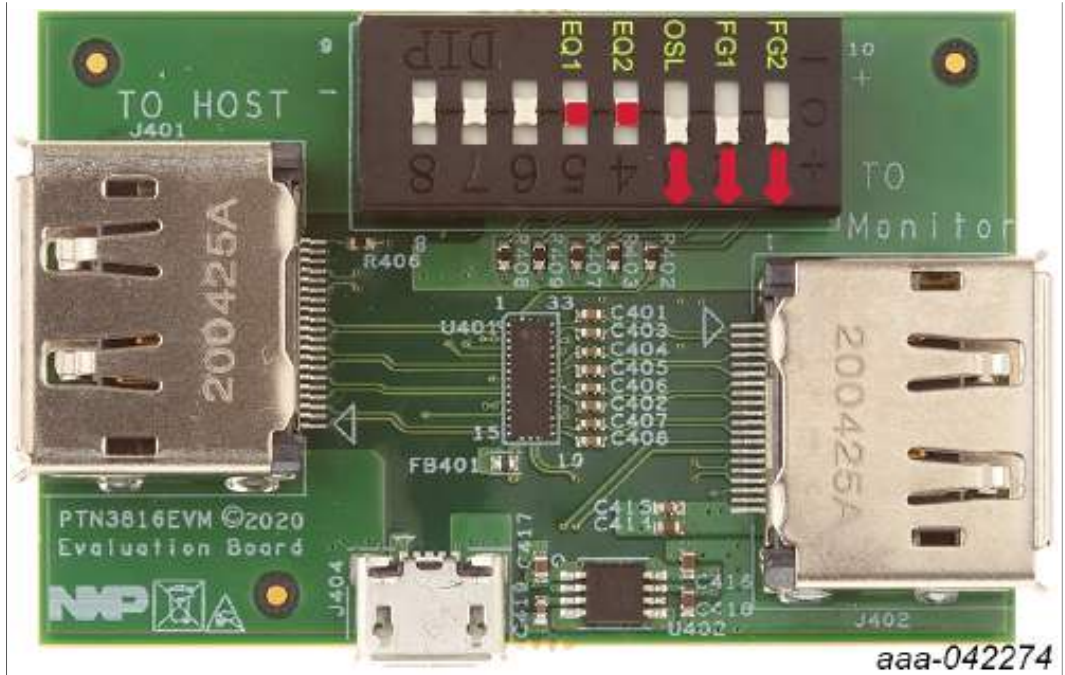


Figure 4. PTN3816EVM evaluation board control switches

By default, the DIP switches are set to the following configurations. The settings are suitable for 2-meter DP cable connected on both sides of the evaluation board (2-meter cable between host PC and EVM, and 2-meter cable between EVM to a DisplayPort monitor). User should change the setting if longer cable or channel conditions are degraded.

- Flat gain = -0.7 dB; FG2 = 1, FG1 = 1
- Output swing linearity = 950 mVppd; OSL = 1
- Equalizer = 10.2 dB @ 8.1 Gbps; EQ2 = HiZ, EQ1 = HiZ

Table 1. Flat gain configuration

FG2	FG1	Flat gain (dB) of individual DP lanes			
		Lane 3	Lane 2	Lane 1	Lane 0
LOW	LOW	0.7	0.7	0.7	0.7
LOW	OPEN	0.7	0.7	0.7	-0.7
LOW	HIGH	0.7	0.7	-0.7	0.7
OPEN	LOW	0.7	0.7	-0.7	-0.7
OPEN	OPEN	0.7	-0.7	0.7	0.7
OPEN	HIGH	0.7	-0.7	-0.7	0.7
HIGH	LOW	-0.7	0.7	0.7	0.7
HIGH	OPEN	-0.7	-0.7	0.7	0.7
HIGH	HIGH	-0.7	-0.7	-0.7	-0.7

Table 2. OSL configuration

OSL	Line driver output swing linearity (OSL) governing -1 dB compression level
OPEN	650 mVppd
LOW	800 mVppd
HIGH	950 mVppd

Table 3. EQ[2:1] configuration: Flat gain -0.7 dB

Peaking Gain is the equalization gain at specific frequency relative to gain at 100 MHz and for typical Flat Gain (FG) value of -0.7 dB

EQ2	EQ1	Unit	Gain at 100 MHz	0.81 GHz	1.35 GHz	2.7 GHz	4.05 GHz	6.75 GHz	8 GHz	10 GHz
LOW	OPEN	dB	-1.1	-0.1	-0.2	0.6	1.3	2.6	3.4	3.8
OPEN	LOW	dB	-1.1	0.0	-0.1	0.8	1.6	3.1	4.0	4.6
HIGH	HIGH	dB	-1.1	0.3	0.2	1.6	2.6	4.7	5.9	7.2
HIGH	OPEN	dB	-1.1	0.9	1.0	2.7	4.0	6.9	8.4	10.2
HIGH	LOW	dB	-1.0	1.6	2.0	4.0	5.8	9.3	11.1	13.3
OPEN	HIGH	dB	-1.0	2.3	2.8	5.3	7.4	11.4	13.4	15.9
LOW	HIGH	dB	-1.0	3.1	3.8	6.7	9.1	13.6	15.8	18.4
OPEN	OPEN	dB	-0.9	3.7	4.7	7.7	10.2	15.2	17.5	20
LOW	LOW	dB	-0.9	3.7	4.7	7.7	10.2	15.2	17.6	20

Table 4. EQ[2:1] configuration: Flat gain 0.7 dB

Peaking Gain is the equalization gain at specific frequency relative to gain at 100 MHz and for typical Flat Gain (FG) value of 0.7 dB

EQ2	EQ1	Unit	Gain at 100 MHz	0.81 GHz	1.35 GHz	2.7 GHz	4.05 GHz	6.75 GHz	8 GHz	10 GHz
LOW	OPEN	dB	0.5	-0.2	-0.4	-0.1	0.1	1.0	1.6	2.0
OPEN	LOW	dB	0.5	-0.1	-0.3	0.1	0.4	1.5	2.3	2.8
HIGH	HIGH	dB	0.5	0.1	0.0	0.7	1.3	3.0	4.1	5.4
HIGH	OPEN	dB	0.5	0.6	0.5	1.6	2.6	5.1	6.6	8.4
HIGH	LOW	dB	0.6	1.1	1.3	2.8	4.2	7.5	9.3	11.6
OPEN	HIGH	dB	0.6	1.7	2.0	4.0	5.7	9.7	11.7	14.2
LOW	HIGH	dB	0.6	2.4	2.8	5.3	7.4	11.9	14.2	16.8
OPEN	OPEN	dB	0.7	2.9	3.7	6.2	8.6	13.6	15.9	18.4
LOW	LOW	dB	0.7	2.9	3.7	6.2	8.6	13.6	16.0	18.4

5.5.3 DisplayPort upstream and downstream connectors

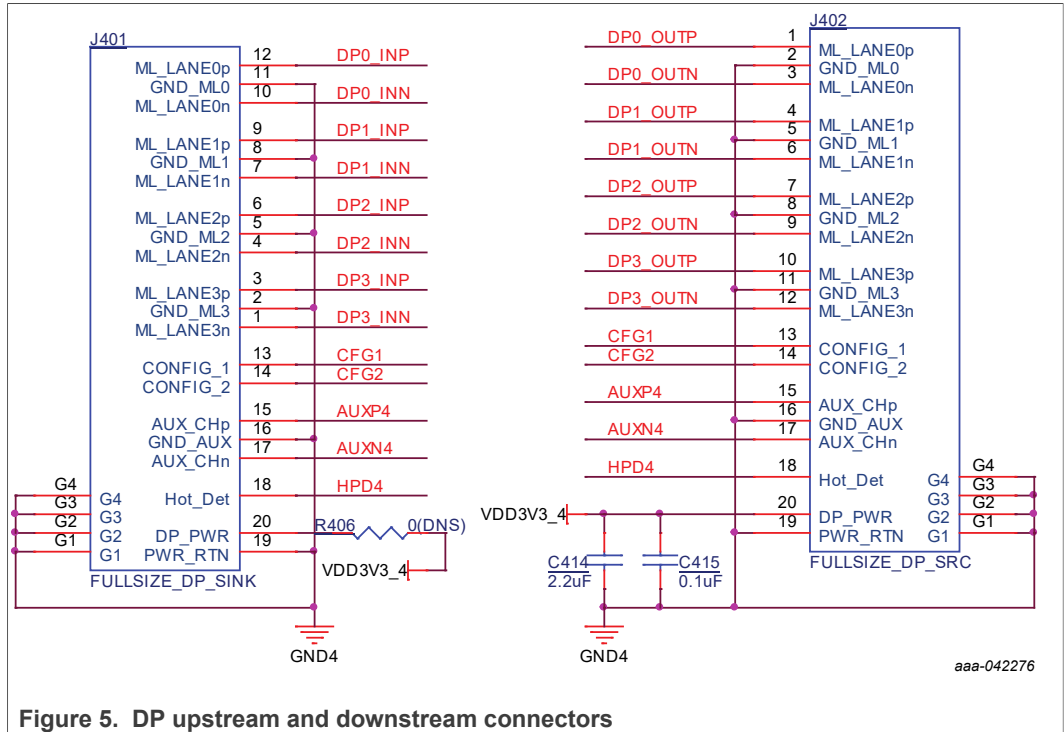


Figure 5. DP upstream and downstream connectors

5.5.4 Power supplies

Power to the add-in-card can be supplied from either PCIe gold finger's 3.3 V, or from an external 5 V barrel input. When all eight pieces of PTN3816 are active, the AIC can consume up to 2 A of current. It is recommended to use external 5 V supply (close J17 pin 1-2) for evaluation.

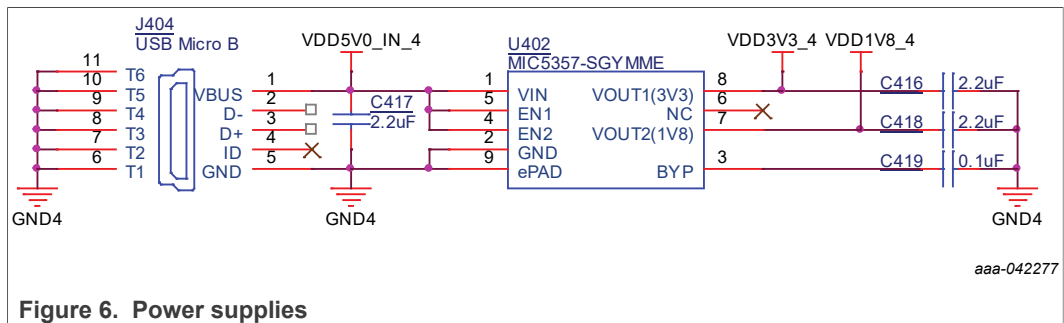
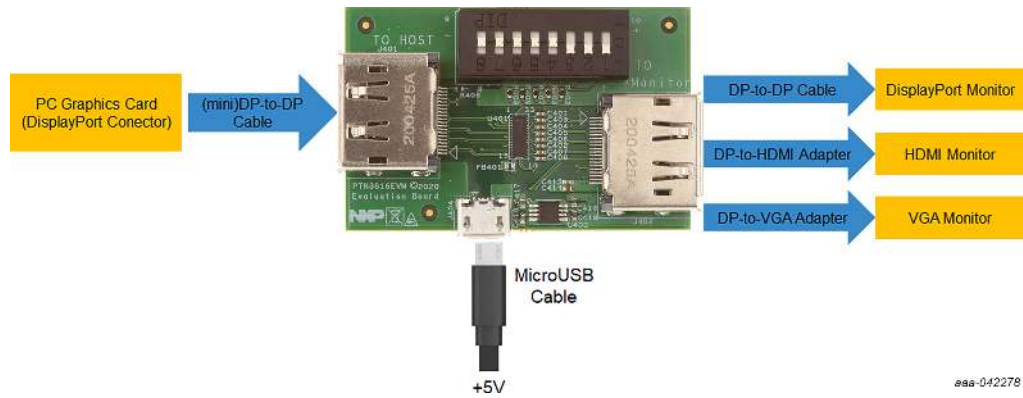


Figure 6. Power supplies

6 Configure the hardware



The PTN3816EVM evaluation board should be powered with a 5 V power supply using a MicroUSB cable (J404). DisplayPort connector on the left side of the board (J401, marked as “TO HOST”) should be connected to a PC’s graphics card through a DisplayPort Cable. DisplayPort connector on the right side of the board (J402, marked as “TO Monitor”) can connect to one of the following for evaluation purposes:

- DP-2-DP cable → to DisplayPort monitor
- DP-2-HDMI adapter → to HDMI monitor
- DP-2-VGA adapter → to VGA monitor

7 Legal information

7.1 Definitions

Draft — A draft status on a document indicates that the content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included in a draft version of a document and shall have no liability for the consequences of use of such information.

7.2 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors. In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory. Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification. Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products. NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or

the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Evaluation products — This product is provided on an "as is" and "with all faults" basis for evaluation purposes only. NXP Semiconductors, its affiliates and their suppliers expressly disclaim all warranties, whether express, implied or statutory, including but not limited to the implied warranties of non-infringement, merchantability and fitness for a particular purpose. The entire risk as to the quality, or arising out of the use or performance, of this product remains with customer. In no event shall NXP Semiconductors, its affiliates or their suppliers be liable to customer for any special, indirect, consequential, punitive or incidental damages (including without limitation damages for loss of business, business interruption, loss of use, loss of data or information, and the like) arising out of the use of or inability to use the product, whether or not based on tort (including negligence), strict liability, breach of contract, breach of warranty or any other theory, even if advised of the possibility of such damages. Notwithstanding any damages that customer might incur for any reason whatsoever (including without limitation, all damages referenced above and all direct or general damages), the entire liability of NXP Semiconductors, its affiliates and their suppliers and customer's exclusive remedy for all of the foregoing shall be limited to actual damages incurred by customer based on reasonable reliance up to the greater of the amount actually paid by customer for the product or five dollars (US\$5.00). The foregoing limitations, exclusions and disclaimers shall apply to the maximum extent permitted by applicable law, even if any remedy fails of its essential purpose.

Translations — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

Security — Customer understands that all NXP products may be subject to unidentified or documented vulnerabilities. Customer is responsible for the design and operation of its applications and products throughout their lifecycles to reduce the effect of these vulnerabilities on customer's applications and products. Customer's responsibility also extends to other open and/or proprietary technologies supported by NXP products for use in customer's applications. NXP accepts no liability for any vulnerability. Customer should regularly check security updates from NXP and follow up appropriately. Customer shall select products with security features that best meet rules, regulations, and standards of the intended application and make the ultimate design decisions regarding its products and is solely responsible for compliance with all legal, regulatory, and security related requirements concerning its products, regardless of any information or support that may be provided by NXP. NXP has a Product Security Incident Response Team (PSIRT) (reachable at PSIRT@nxp.com) that manages the investigation, reporting, and solution release to security vulnerabilities of NXP products.

7.3 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

NXP — wordmark and logo are trademarks of NXP B.V.

Tables

Tab. 1.	Flat gain configuration	8	Tab. 3.	EQ[2:1] configuration: Flat gain -0.7 dB	9
Tab. 2.	OSL configuration	9	Tab. 4.	EQ[2:1] configuration: Flat gain 0.7 dB	9

Figures

Fig. 1.	PTN3816EVM evaluation board	5	Fig. 4.	PTN3816EVM evaluation board control switches	7
Fig. 2.	Block diagram	6	Fig. 5.	DP upstream and downstream connectors	10
Fig. 3.	PTN3816EVM evaluation board schematic	7	Fig. 6.	Power supplies	10

Contents

1	Important notice	3
2	Introduction	3
3	Finding kit resources and information on the NXP web site	3
3.1	Collaborate in the NXP community	3
4	Get started	4
4.1	Kit contents/packing list	4
4.2	Minimum system requirements	4
5	Get to know the hardware	4
5.1	Board features	4
5.2	Board description	4
5.3	Board components	4
5.4	Block diagram	6
5.5	PTN3816EVM evaluation board schematics	7
5.5.1	PTN3816EVM evaluation board schematic	7
5.5.2	PTN3816EVM evaluation board control switches	7
5.5.3	DisplayPort upstream and downstream connectors	10
5.5.4	Power supplies	10
6	Configure the hardware	11
7	Legal information	12

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© NXP B.V. 2021.

All rights reserved.

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 8 June 2021
Document identifier: UM11593