NAU8402
Stereo 24-bit DAC with 2Vrms Line Out

1. GENERAL DESCRIPTION

The NAU8402 is a high quality 24-bit stereo DAC with 2Vrms analog output capability. This device includes an integrated charge pump enabling true ground referenced outputs and full 5.6Vpp output levels, while operating from only a single 3.3V supply voltage.

Additionally, the NAU8402 includes automatic pop/click elimination features and high immunity to power supply and other system noise. This enables fast and efficient system integration while minimizing external component costs.

The NAU8402 is specified for operation from -40°C to +85°C. AEC-Q100 & TS16949 compliant device is available upon request.

2. FEATURES

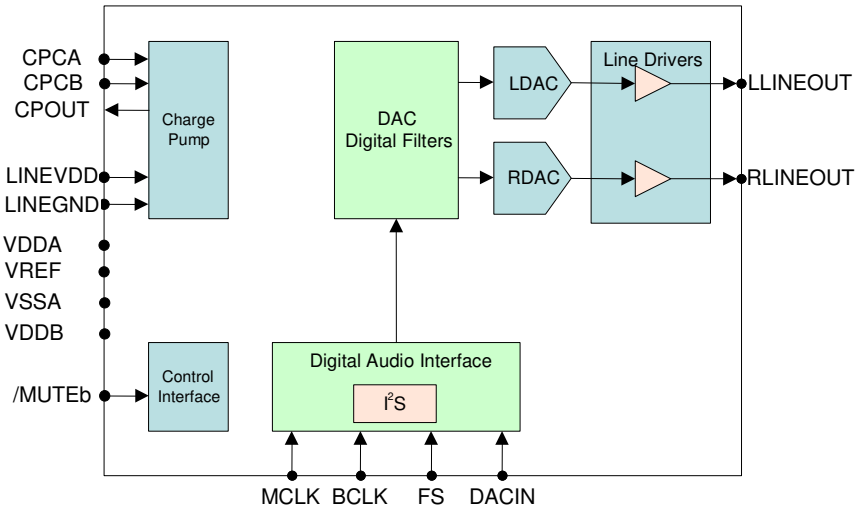
Stereo 24-bit DAC
- Full 2Vrms output using only 3.3Vdc supply
- True Ground Referenced analog outputs
- Audio Performance
  - 98dB SNR A-weighted performance
  - -82dB THD+N
  - 68dB PSRR at 1kHz
  - 108dB channel separation at 1kHz
- Up to 96 kHz audio sample rate
- Automatic pop/click elimination and output muting for power-on and no-signal conditions

Interfaces
- I^2S slave supporting up to 96 kHz sample rate determined by clock frequency ratios.
- Supports either 12.288MHz or 24.576MHz master clock frequency w/auto rate detection for sampling rate 24k, 48k and 96k Hz
- Supports either 11.290MHz or 22.579MHz for sampling rate 44.1kHz

Low Power, Low Voltage
- Nominal Operating Voltage: 3.3V

Additional features
- Low external parts count
- High system noise immunity
- Package: 16-pin TSSOP (Green/ROHS)
- Operating voltage: 3.3-3.6V
- Operating temperature range: -40° to +85°C

Applications
- Game Consoles
- DVD players
- Set top boxes
- Digital TVs



3. PIN CONFIGURATION

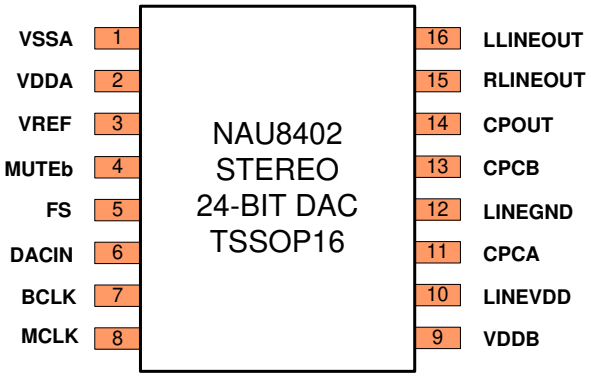


Figure 1: NAU8402 Pin-Out

4. PIN DESCRIPTION

Pin Name	Pin	Functionality	A/D	Pin Type
VSSA	1	Analog Ground	A	O
VDDA	2	Analog Supply	A	I
VREF	3	Decoupling internal analog mid supply reference	A	O
/MUTE	4	Mute enabled, 1= Mute disabled	D	I
FS	5	Frame Sync	D	I
DACIN	6	Digital Audio Data Input	D	I
BCLK	7	Bit Clock	D	I
MCLK	8	Master Clock	D	I
VDDB	9	Digital IO Supply	D	I
LINEVDD	10	Line Out Charge Pump Supply	A	I
CPCA	11	Charge Pump Capacitor Node A	A	O
LINEGND	12	Line Out Charge Pump Ground	A	I
CPCB	13	Charge Pump Capacitor Node B	A	O
CPOUT	14	Charge Pump Decoupling Output	A	O
RLINEOUT	15	Right Channel Line Output	A	O
LLINEOUT	16	Left Channel Line Output	A	O

Table 1: Pin Description

Notes

1. Unused analog input pins should be left as no-connection.
2. Any unused digital input pin must be tied high or low as appropriate.

5. Table of Contents

6. List of Figures

7. List of Tables

8. ABSOLUTE MAXIMUM RATINGS

DESCRIPTION	SYMBOL	CONDITION	MIN	MAX	Units
VDDB, LineVDD , VDDA supply voltages	VDD	VDD–VSS	-0.3	4.5	V
Digital Input Voltage range	DV_{IN}	DV_{IN} – VSS	VSS – 0.3	VDDB + 0.30	V
Analog Input Voltage	AV_{IN}	AV_{IN} – VSSA	VSSA – 0.3	VDDA + 0.30	V
Temperature range	TA		-40	+150	°C
Storage Temperature	Tst		-65	+150	°C

CAUTION: Do not operate at or near the maximum ratings listed for extended period of time. Exposure to such conditions may adversely influence product reliability and result in failures not covered by warranty. These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.

9. OPERATING CONDITIONS

Condition	Symbol	Min Value	Typical Value	Max Value	Units
Supply voltages	LineVDD, VDDA	3.0	3.3	3.6	V
Supply voltage	VDDB	1.7	3.3	3.6	V
Ground	LINEGND, VSSA		0		V
Operating Temperature	TA	-40		+85	°C

10. ELECTRICAL CHARACTERISTICS

VDDA = VDDB = LINEVDD = 3.3V, MCLK – 256fs, T_A = +25°C, 1kHz signal, fs = 48kHz, 24-bit audio data unless otherwise stated.

PARAMETER	SYM	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Full Scale Output Voltage			2	2.1	2.2	Vrms
Signal to Noise Ratio (2)	SNR	A-weighted	-	98	-	dB
		Un-weighted	-	96	-	dB
Dynamic Range(2)	DNR	24-bit A-weighted	-	98	-	dB
		24-bit Un-weighted	-	96	-	dB
		16-bit A-Weighted	-	94	-	dB
		16-bit Un-Weighted	-	92	-	dB
Total Harmonic Distortion + Noise Level(1)	THD+N	24-bit 0dB A-Weighted	-	-82	-	dB
		24-bit -20dB A-Weighted	-	-96	-	dB
		16-bit 0dB A-Weighted	-	-82	-	dB
		16-bit -20dB A-Weighted	-	-93	-	dB
Power Supply Rejection Ratio (2)	PSRR	100Hz	-	73	-	dB
		1kHz	-	68	-	dB
		20kHz	-	58	-	dB
Channel Separation(2)		1kHZ	-	108	-	dB
		20Hz to 20kHz	-	96		dB
System Absolute Phase			-	0	-	Degrees
Channel Level Matching			-	0	-	dB
Output Offset			-	0	±8	mV

Notes:
1) THD+N is measured as rms value of the noise plus the harmonic distortion components relative to the full scale output level.
2) Performance tests are conducted using a 20Khz low pass filter and A weighted filter where specified. The 20Khz low pass filter removes inaudible out of band noise.

10.1. ANALOG OUTPUT LEVELS

VDDA = VDDB = LINEVDD = 3.3V, MCLK – 256fs, T_A = +25°C, 1kHz signal, fs = 48kHz, 24-bit audio data unless otherwise stated.

PARAMETER	SYM	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output Level	Vout	0dBFs	2.0	2.1	2.2	Vrms
Load Resistance	Rload	0dBFs	5		47	kΩ
Load Capacitance	Cload	On R/LLINEOUT	-	0	100	pF

10.2. POWER CONSUMPTION

VDDA = VDDB = LINEVDD = 3.3V, MCLK – 256fs, T_A = +25°C, 1kHz signal, fs = 48kHz, 24-bit audio data unless otherwise stated.

CONDITIONS	IVDDA (mA)	IVDDB (mA)	ILINEVDD (mA)	ITOTAL (mA)
/MUTE = 0, No clocks*	0.3	0.10	0	0.4
/MUTE = 0	1.66	1	1.22	3.88
/MUTE = 1	3.92	2.27	1.38	7.57

11. FUNCTIONAL DESCRIPTION

The NAU8402 is a high quality 24-bit stereo DAC with 2Vrms analog output capability. This device includes an integrated charge pump enabling true ground referenced outputs and full 5.6Vpp output levels, while operating from only a single 3.3V supply voltage. Additionally, the NAU8402 includes automatic pop/click elimination features and high immunity to power supply and other system noise.

11.1. DIGITAL SIGNAL PATH

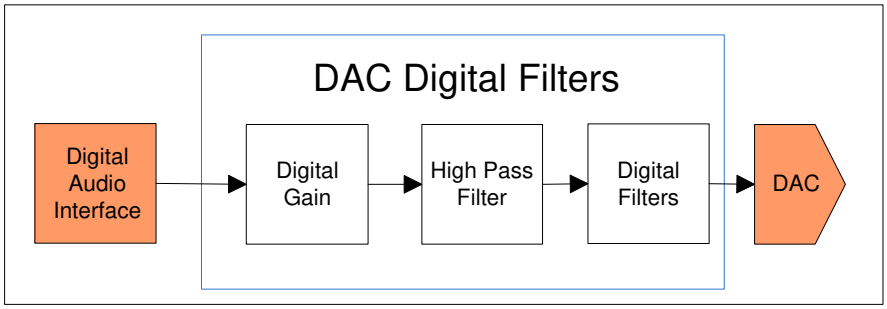


Figure 2: NAU8402 Digital Signal Path

The DAC digital block uses 24-bit signal processing to generate analog audio from a 16-bit digital sample stream input. The DAC coding scheme is in two's complement format and the full-scale output level is proportional to VDDA. With a 3.3V supply voltage, the full-scale output level is $2.1V_{RMS}$.

This DAC block consists of a digital gain stage, a high pass filter, and a digital interpolation filter and sigma-delta modulator. The digital gain stage is used in coordination with the mute function to ramp the volume up and down when going into and out of the mute state as described below.

The high pass filter is a simple first order DC blocking filter, with a 3dB cut-off frequency of FS x $7.7x10^{-5}$. Filter operation and settings are always the same for both left and right channels.

11.2. DIGITAL AUDIO INTERFACE

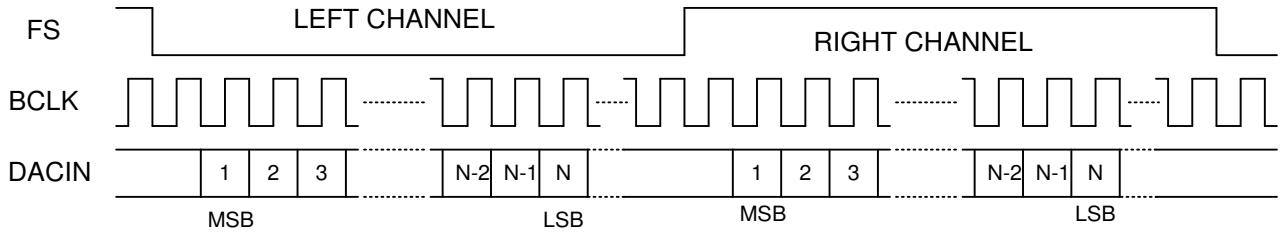


Figure 3: NAU8402 Digital Interface Timing Diagram

Channel selection is governed by the Frame Sync (FS). When FS is low, the data transfer is for Left channel. When FS is high, the data transfer is for Right channel. DACIN MSB starts from the 2nd BCLK after FS transition.

The I2S data interface supports up to 24-bits of data using 32 BCLK cycles per channel (64 per frame sync). In the 32-bit I2S data format the DAC will truncate the 8 LSBs and only use 24 bits. In the 16-bit I2S data format, 16 LSBs must be padded with zeros.

11.3. POWER ON AND OFF RESET

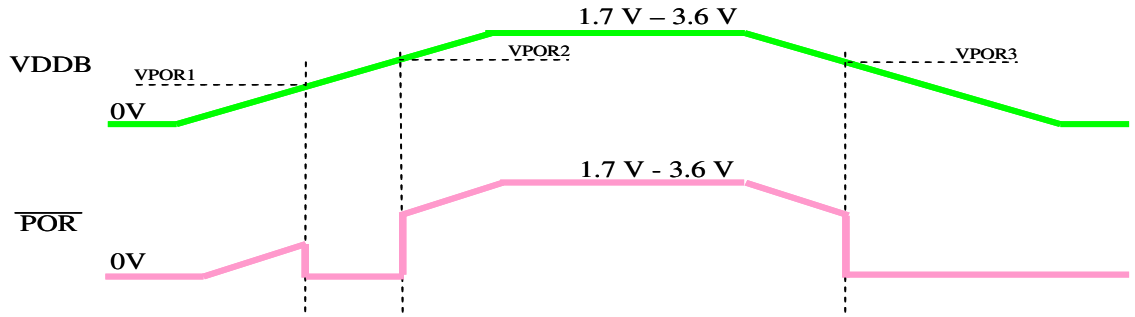


Figure 4: Power on and off Reset sequence

The NAU8402 includes a power on and off reset circuit on chip. The circuit resets the internal logic control at VDDB power up. The NAU8402 does not have an external reset pin. The reset function is automatically generated internally when power supplies are too low for reliable operation. The internal reset is generated any time that VDDB is lower than is required for reliable maintenance of internal logic conditions. The reset threshold voltage for VDDB is approximately 0.5Vdc. Note that this is a much lower voltage than required for normal operation of the chip. The values are mentioned here as general guidance as to overall system design.

If the VDDB supply is coming up, an internal reset condition is asserted once the VDDB supply reaches an internal threshold of VPOR1. During this time, all registers and controls are set to the hardware determined initial conditions. Externally applied clocks during this time will be ignored, and any expected actions will be invalid.

As VDDB, increases above the VPOR1 threshold, an internal reset pulse is generated which extends the reset condition for an additional time. The duration of this extended reset, time is approximately 50 microseconds to 100 microseconds, but may vary with the supply ramp rate. The reset condition remains asserted during this time. Once VDDB reaches a

second threshold VPOR2, the internal reset will be de-asserted. If VDDB at any time becomes lower than its respective threshold voltage, a new reset condition will result. The reset condition will continue until VDDB is higher than the VPOR2 threshold.

When VDDB reaches VPOR3 threshold during the power off ramp of VDDB, the internal reset will be asserted again.

11.4. DEVICE CLOCKING

The NAU8402 requires the MCLK/FS ratio to be 256±3 or 512±3 MCLK cycles per FS. The NAU8402 has an automatic clock detection circuitry that validates the MCLK/FS ratio. The following table describes appropriate clock relationships.

FS (kHz)	BCLK (kHz)	MCLK (MHz)	MCLK/FS RATIO
24	1536	12.288	512
44.1	2822.4	11.290	256
44.1	2822.4	22.579	512
48	3072	12.288	256
48	3072	24.576	512
96	6144	24.576	256

Table 2: MCLK And Sample Rate Frequencies

When the circuit detects a valid MCLK/FS ratio, the DAC clock starts running at $f_{MCLK}/4$. However, the charge pump clock starts running at $f_{MCLK}/128$ (96 KHz for 12.288 MHz master clock) immediately after MCLK is detected
After a valid MCLK/FS ratio has been detected the line driver will powers up after a delay determined by the sampling rate according to the following table.

FS (kHz)	Line Driver Power Up Time (ms)
24	682
44.1	371
48	341
96	170

Table 3: Line Driver Power Up Delay

All clocks run continuously after start up as long as MCLK remains present. FS and BCLK signals are internally synchronized to MCLK for clock detection and do not require external synchronization.

12.5MUTE / UN-MUTE SEQUENCE AND OPERATING MODES

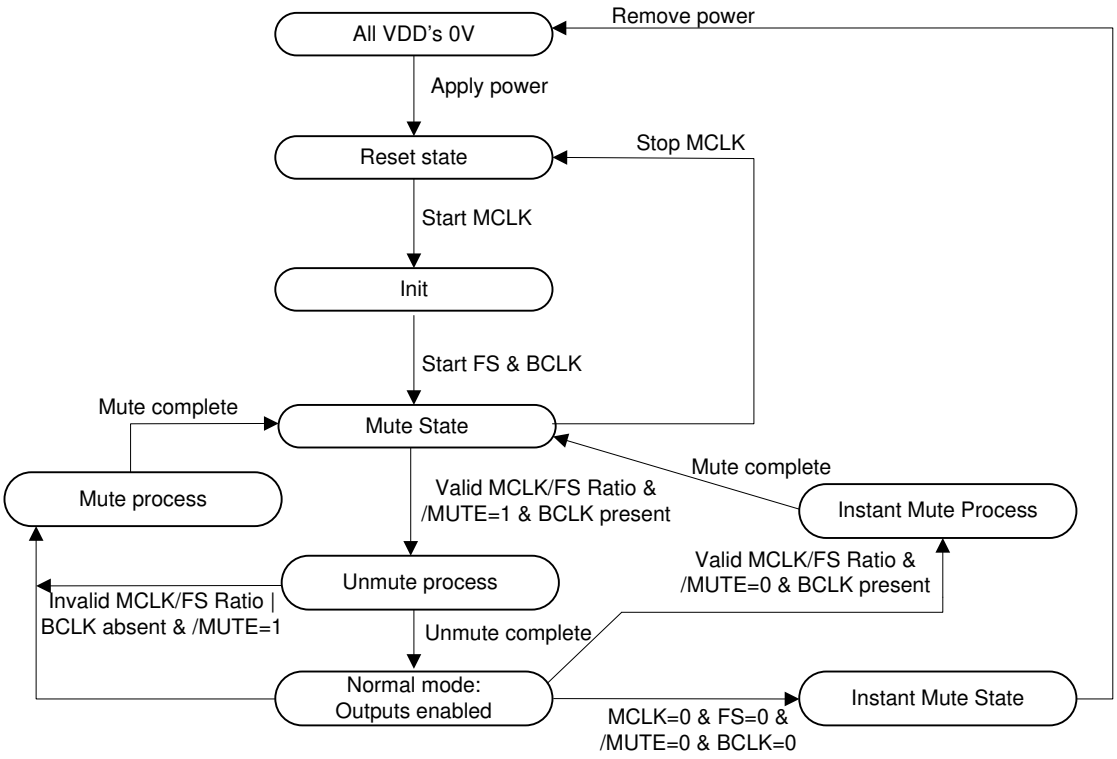


Figure 5: Mute / Un-mute Sequence

The NAU8402 power-up sequence is as follows:

- Apply power
- Start MCLK, FS & BCLK
- The device initializes in the mute state upon application of clocks. The device begins the un-mute process once all three un-mute conditions are met:
    - Valid MCLK/FS ratio of 256±3 or 512±3 MCLK cycles per FS has been detected.
    - BCLK is present.
    - /MUTE is high.
- In the un-mute process, the line driver performs a soft un-mute. This will take 341ms for the initial un-mute after power up (see Table 3) and 2000 samples (42 ms for 48kHz FS) for any consecutive un-mute with the clocks running. Once the line driver has been un-muted, the digital volume ramps up from full digital mute to -127.5dB and then to full scale in 256 samples.
  .
- After the un-mute process completes, the device enters normal mode with analog outputs enabled and remains there until any of the un-mute conditions are no longer true.

The NAU8402 has three mute sequences:

- The device enters the Mute process when /MUTE is high and BCLK is absent or the MCLK/FS ratio is invalid. In the Mute process, the digital volume ramps from full scale to -127.5dB, and then to full digital mute, in 1K samples at 0.125 dB per step. Once the digital volume reaches 0, the line driver performs a soft mute in 2K samples. Note that the MCLK needs to keep running in order to keep the charge pump running during the mute process.
- The device enters the Instant Mute Process when /MUTE is low and BCLK, FS & MCLK are valid. In the Instant Mute Process, the line driver output is muted instantly, while the digital volume ramps from full scale to -127.5dB, and then to full digital mute, in 1K samples at 0.125 dB per step. For minimal pops it is advised to send 8000 consecutive zero samples to the digital DAC input prior to entering the Instant Mute Process;
- The device enters the Instant Mute State when all clocks are absent and /MUTE is low. Supply power may be removed after reaching the Instant Mute State. For minimal pops it is advised to send 8000 consecutive zero samples to the digital DAC input prior to entering the Instant Mute Process;

Once the device is in the Mute State, the user may stop MCLK to enter the low power reset state. MCLK should not be stopped prior to full completion of the mute sequence. During the Mute State, the charge pump will continue to operate as long as the master clock is present.

12.6POWER SUPPLY

12.6.1 VREF

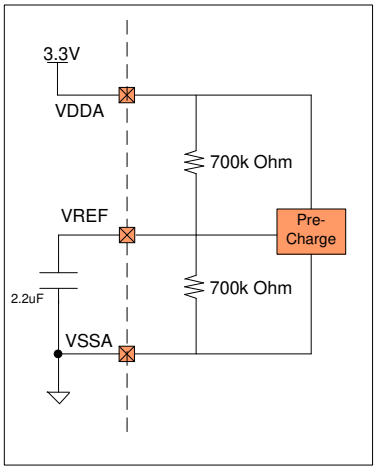


Figure 6: VREF Connections

The NAU8402 includes a mid-supply reference circuit. It is decoupled to VSSA through the VREF pin by means of a bypass capacitor. The VREF voltage is used as the DAC reference. Therefore, the bypass capacitor needs to be large in order to achieve good power supply rejection at low frequencies. Typically, a 2.2uF capacitor can be used to obtain good power supply rejection. However, a larger values can also be chosen. A larger value will increase the rise time of VREF and therefore it will delay the valid line output signal. Due to the high impedance nature of the VREF pin, it is important to use a low leakage decoupling capacitor. A pre-charge circuit pre-charges the capacitor close to VDDA/2 at power up in order to reduce the rise time for fast line out availability.

12.6.2 CHARGE PUMP

The NAU8402 contains a charge pump to generate a negative supply for the ground referenced stereo line out DAC. The charge pump operates from the LINEVDD supply, which perform the following tasks.

- Firstly, it connects the 220 nF CPC capacitor between CPCA & CPCB to the LINEVDD supply voltage.
- Secondly, it discharges the CPC capacitor charge onto the CPOUT pin, which is decoupled through another 4.7uF capacitor.

For optimal performance, connect the charge pump capacitors close to the pins. Increasing the CPOUT decoupling capacitor will help to reduce the supply ripple, but will increase the charge pump settling time.

The charge pump starts running at $f_{MCLK}/128$ (96 kHz for 12.288 MHz master clock) once MCLK has been applied. During the mute condition, the charge pump will continue to operate as long as the master clock is present.

12.6.3 POWER DOMAINS

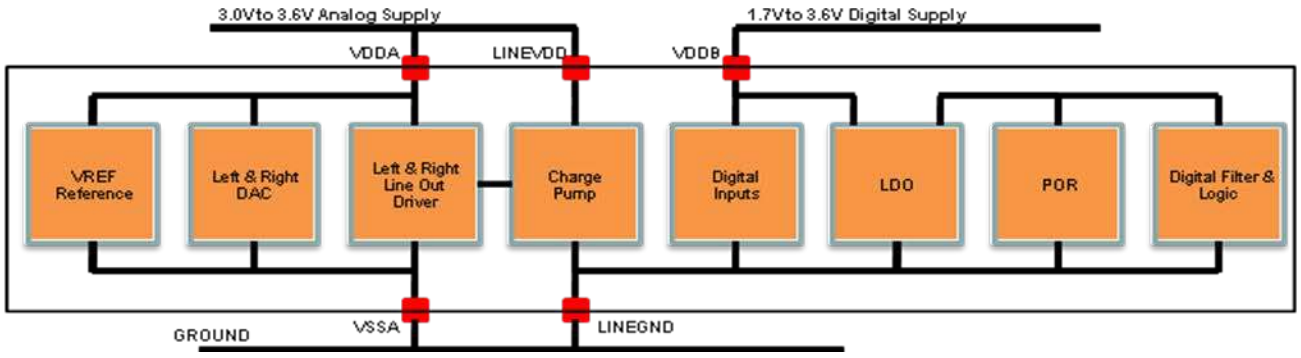


Figure 7: Power Domains

The NAU8402 has two ground pins and three power supply pins.

The VSSA ground pin is used to supply the low noise analog circuits, such as the DAC, the references and the line out drivers.

The LINEGND pin supplies the switching circuits, such as the Charge pump, the digital inputs and the logic.

The VDDA supply pin and supplies the DACs, references and line out drivers. VDDA needs to be connected to a low noise 3.3V +/- 10% supply voltage. The VREF reference is generated from VDDA and VSSA and is typically (VDDA+VSSA)/2.

The LINEVDD supply pin supplies the Charge pump. LINEVDD needs to be connected to a 3.3V +/- 10% supply voltage. The charge pump provides the negative supply CPOUT for the line out drivers and is typically –LINEVDD.

The VDDB supply pin supplies the digital input buffers and the logic LDO. VDDB needs to be connected to a 1.7V to 3.6V supply voltage. The logic LDO will turn on as soon as power is applied to VDDB and it will supply the internal POR and logic supply.

12. AUDIO INTERFACE TIMING DIAGRAM

12.1. AUDIO INTERFACE MODE

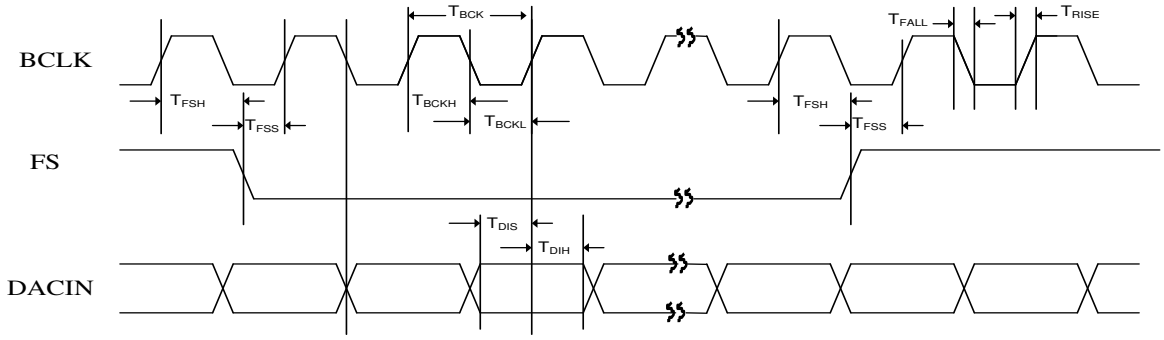


Figure 8: Audio Interface Mode Timing Diagram

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
T_{BCK}	BSCK Cycle Time	50	---	---	ns
T_{BCKH}	BSCK High Pulse Width	20	---	---	ns
T_{BCKL}	BSCK Low Pulse Width	20	---	---	ns
T_{FSS}	FS to BLCK Rising Setup Time	20	---	---	ns
T_{FSH}	BCLK Rising Edge to FA Hold Time	20	---	---	ns
T_{RISE}	Rise Time for All Audio Interface Signals	---	---	10	ns
T_{FALL}	Fall Time for All Audio Interface Signals	---	---	10	ns
T_{DIS}	DACIN to BLCK Rising Edge Setup Time	15	---	---	ns
T_{DIH}	BCLK Rising Edge to DACIN Hold Time	15	---	---	ns

Table 4: Audio Interface Timing Parameters

12.2. SYSTEM CLOCK (MCLK) TIMING DIAGRAM

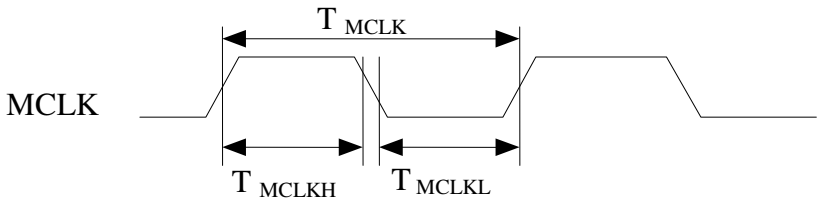


Figure 9: MCLK Timing Diagram

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
MCLK Cycle Time	T_{MCLK}		40			ns
MCLK High Pulse Width	T_{MCLKH}		16	---	---	ns
MCLK Low Pulse Width	T_{MCLKL}		16	---	---	ns

Table 5: MCLK Timing Parameter

13. FILTER CHARACTERISTICS

13.1. DIGITAL FILTER CHARACTERISTICS

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
High Pass Filter					
High Pass Filter Corner Frequency	-3dB		$7.7x10^{-5}$		fs
	-0.5dB		$2.2x10^{-4}$		fs
	-0.1dB		$4.5x10^{-4}$		fs
DAC Filter					
Passband	+/- 0.035dB	0	0.465		fs
	-6dB		0.5		fs
Passband Ripple				+/-0.035	dB
Stopband		0.546			fs
Stopband Attenuation	f > 0.546*fs	-55			dB
Group Delay			28		1/fs

Table 6: Digital Filter Characteristics

TERMINOLOGY

1. Stop Band Attenuation (dB) – the degree to which the frequency spectrum is attenuated (outside audio band)
2. Pass-band Ripple – any variation of the frequency response in the pass-band region

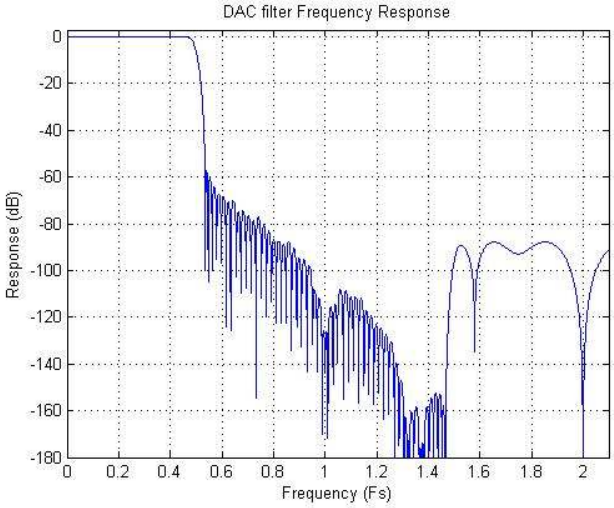


Figure 10: DAC Filter Frequency Response

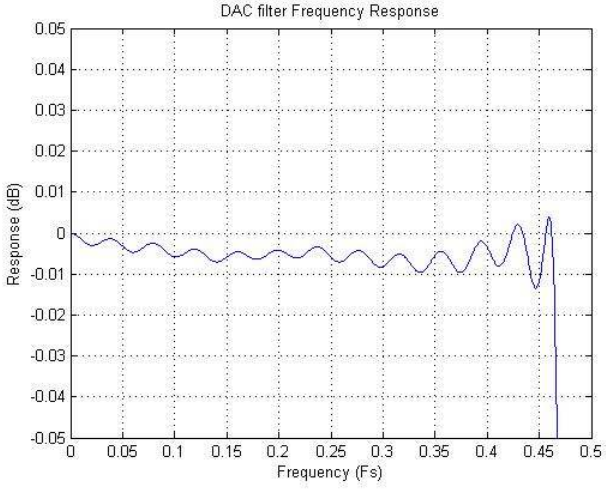


Figure 11: DAC Filter Ripple

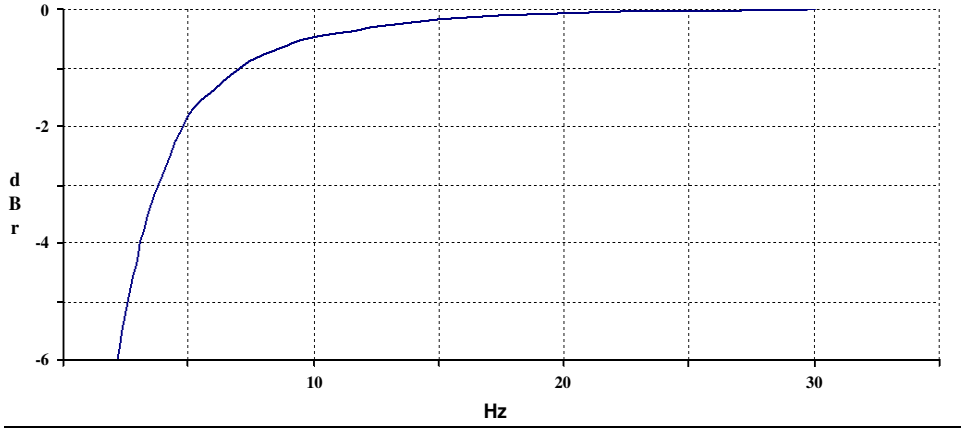


Figure 12: HPF Frequency Response

13.2. ANALOG FILTER CHARACTERISTICS

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
ADC Filter					
Passband	-6dB		0.20322		fmclk

Table 7: Analog Filter Characteristics

14. TYPICAL APPLICATION

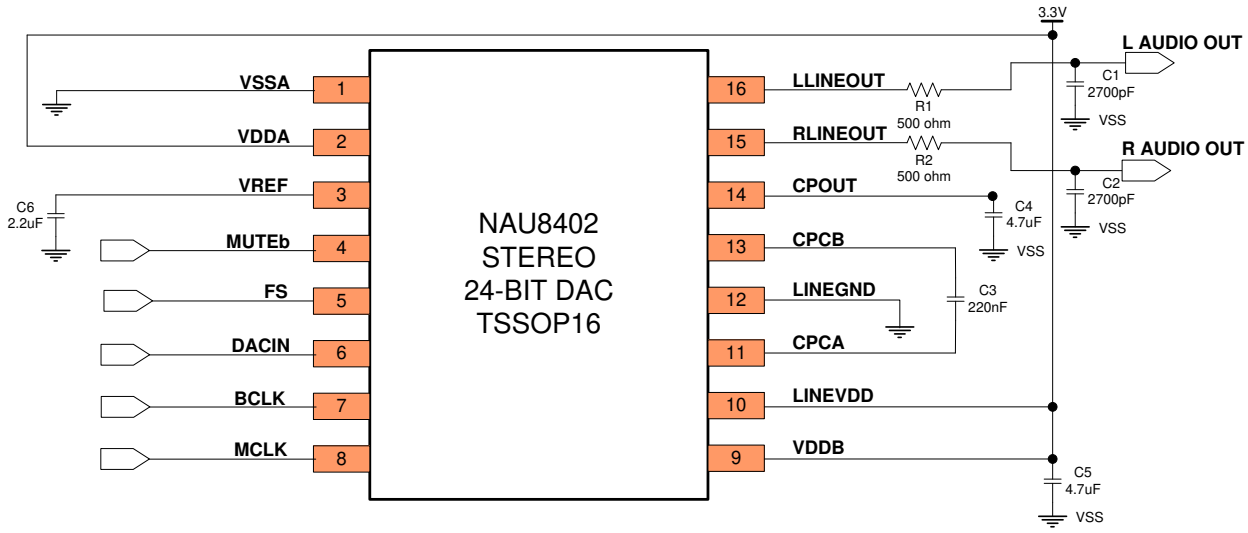


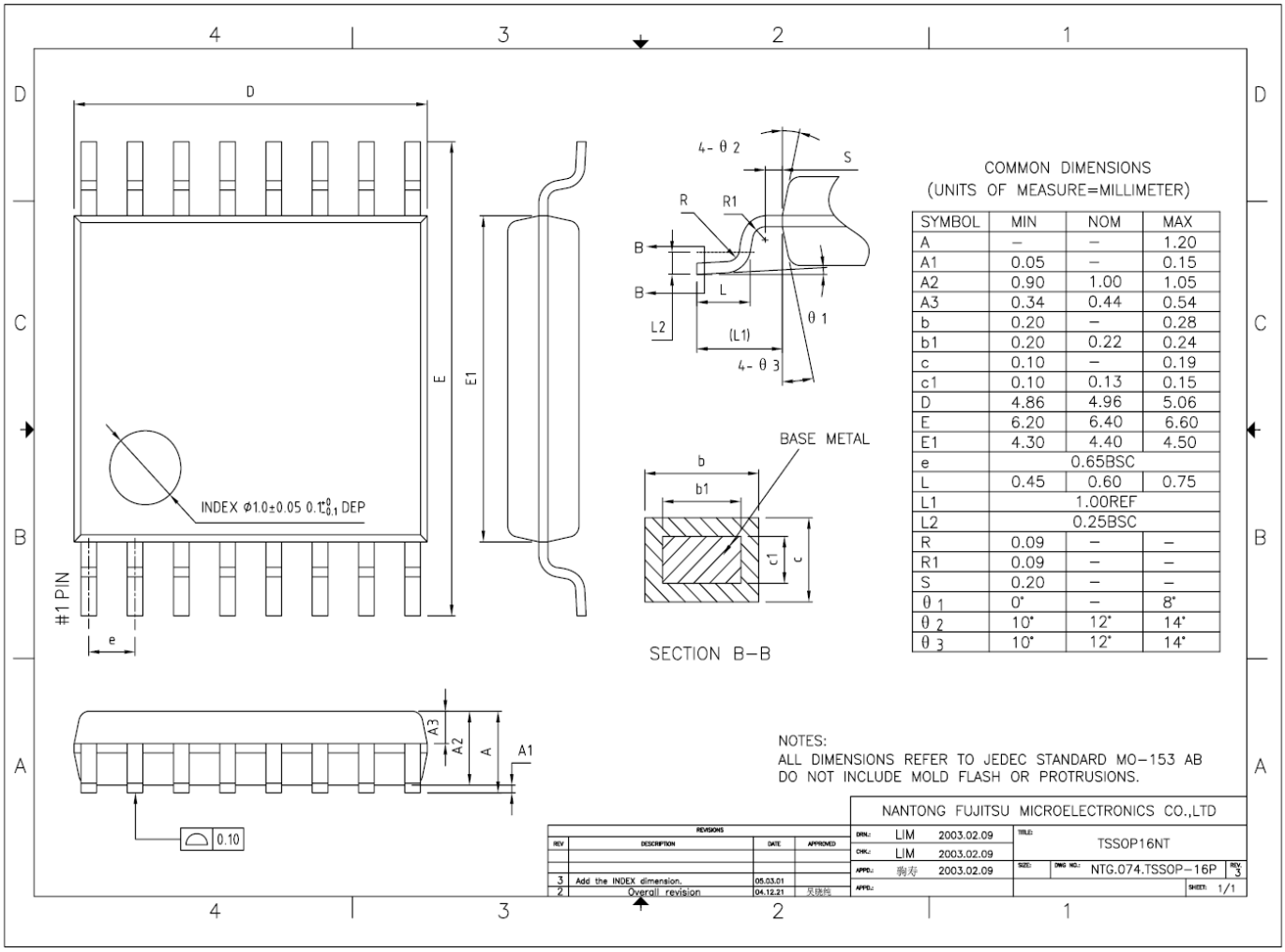
Figure 13: Application Diagram

Note 1: The NAU8402 L/R LINEOUT levels are (2.1 x 3.3/VDDA) Vrms. Using, the application circuit above, the 0dBFs level at the L & R AUDIO OUT terminals will be 2 Vrms, when a 10-kΩ load is applied. In order to estimate the output level variation, one should consider the VDDA supply voltage accuracy, the accuracy of the load and 500-Ω resistance and the NAU8402 output level variation.

Note 2: The 500-Ω series resistor will effectively reduce the impact of glitches that may be present on line out connectors. In addition, the 500-Ω 2700pF RC combination reduces the DAC out of band noise. The -3dB cut-off is at 118 kHz.

Note 3: For optimum performance, separate the left and right lineout traces and RC network by a VSS trace on the PCB.

15. PACKAGE SPECIFICATION: TSSOP-16



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	–	–	1.20
A1	0.05	–	0.15
A2	0.90	1.00	1.05
A3	0.34	0.44	0.54
b	0.20	–	0.28
b1	0.20	0.22	0.24
c	0.10	–	0.19
c1	0.10	0.13	0.15
D	4.86	4.96	5.06
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e		0.65BSC	
L	0.45	0.60	0.75
L1		1.00REF	
L2		0.25BSC	
R	0.09	–	–
R1	0.09	–	–
S	0.20	–	–
θ 1	0°	–	8°
θ 2	10°	12°	14°
θ 3	10°	12°	14°

16. ORDERING INFORMATION

Part Number	Dimension	Package	Package Material
NAU8402WG	4.96x6.4 mm	TSSOP-16	Green

NAU8402 _ _

Package Material:

G = Pb-free Package

Package Type:

W = 16-Pin TSSOP Package

17. REVISION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
0.5	October 12th, 2010		Initial Revision
0.8	November 17th, 2010	19 7	Added ordering part numbers for T&R and tray Added foot note for off sate power consumption
1.1	December 10th, 2010	19	Changed ordering number to conform to the Audio Product part numbering system
1.2	February, 2011	23, 24 16 Various	Revised Mute / Un-mute sequences and diagram Updated T_{FSS} description Updated format and descriptions
1.3	April, 2011	7 7, 8 8 11 11, 14 17 18 19 21	Updated THD+N Level typical Corrected Output Level min and max and Output offset typical Updated Power Consumption Table Corrected DAC Clock Output Level min and max Clarified that Charge Pump clock starts with MCLK Updated Digital Filter Characteristics Added Analog Filter Characteristics Updated Applications Diagram. CPOUT Capacitor changed. Corrected ordering information
1.4	June , 2011	1 7, 8 8 19	Updated Block diagram and features list updated Corrected typical SNR, THD, and PSRR numbers, Updated Power Consumption Table Added note 3. Ground traces recommendation.
1.5		12	Updated the un-mute description. 'In the un-mute process, the line driver performs a soft un-mute in 2K samples (42 ms for 48kHz FS). Once the line driver has been un-muted, the digital volume ramps up from full digital mute to -127.5dB and then to full scale in 256 samples.' hanged to 'In the un-mute process, the line driver performs a soft un-mute. This will take 341ms for the initial un-mute after power up (see Table 3) and 2000 samples (42 ms for 48kHz FS) for any consecutive un-mute with the clocks running. Once the line driver has been un-muted, the digital volume ramps up from full digital mute to -127.5dB and then to full scale in 256 samples.'
1.6	August, 2012	each	Remove the word "Preliminary" from footer
1.6.1	March 28, 2013	1 11	Added SR 44.1kHz supported in section 2 FEATURES Added SR 44.1kHz in section 11.4 DEVICE CLOCKING
1.7	Jan 9,2015	1	Updated AECQ100 description

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