Operational Amplifier, Low Power, Rail-to-Rail

NCV952

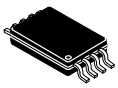
The NCV952 is a dual, low power, operational amplifier fully specified for 3 V, 5 V and 24 V operation. Rail−to−rail output performance over the supply range of 2.7 V to 26 V provides increased dynamic range in single−supply and split−supply applications. This device offers a gain−bandwidth of 3.5 MHz and a slew rate of 1 V/μs, with only 0.7 mA of quiescent current. The NCV952 is available in a space saving 8−pin TSSOP8 package.

Features

- Rail−to−rail Input Common Mode Voltage Range
- Rail−to−rail Output Swing
- Wide Supply Range: 2.7 V to 26 V
- Excellent Gain−bandwidth and Speed: 3.5 MHz at 1 V/μs with 3 V Supply
- Low Quiescent Current: 0.7 mA at V_S = 3 V per Channel
- PSRR: 105 dB Typical
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These Devices are Pb−free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- General Purpose Operational Amplifier
- Active Filters
- Signal Conditioning Amplifiers/ADC Buffers
- Set−top Boxes
- Laptop/Notebook Computers
- Transformer/Line Drivers
- Personal Entertainment Systems
- Cell Phones and Other Portable Communications
- Portable Headphone Speaker Drivers
- Instrumentation and Sensoring

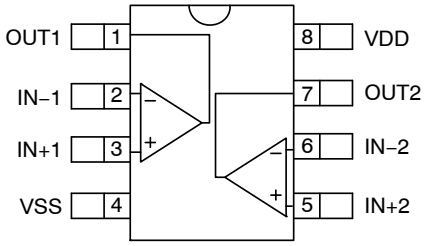


TSSOP−8
CASE 948S

MARKING DIAGRAM

V52 = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

PIN CONNECTIONS



ORDERING INFORMATION

Device	Package	Shipping†
NCV952DTBR2G	TSSOP−8 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

Table 1. PIN DESCRIPTION

Pin	Name	Type	Description
1	OUT1	Output	Output of opamp 1
2	IN−1	Input	Inverting input of opamp 1
3	IN+1	Input	Non−inverting input of opamp 1
4	VSS	Power	Negative supply. A bypass capacitor of 0.1 μF to ground is recommended as close as possible to this pin.
5	IN+2	Input	Non−inverting input of opamp 2
6	IN−2	Input	Inverting input of opamp 2
7	OUT2	Output	Output of opamp 2
8	VDD	Power	Positive supply. A bypass capacitor of 0.1 μF to ground is recommended as close as possible to this pin.

Table 2. ABSOLUTE MAXIMUM RATINGS (Over operating free−air temperature, unless otherwise stated)

Parameter	Symbol	Limit	Unit
Supply Voltage (V_{DD}− V_{SS})	V_S	28	V
INPUT AND OUTPUT PINS			
Input Voltage	V_{IN}	V_{SS} − 0.3 to V_{DD} + 0.3	V
Differential Input Voltage (Note 1)	V_{ID}	±1	V
TEMPERATURE			
Storage Temperature	T_{STG}	−65 to +150	°C
Junction Temperature	T_J	+150	°C
ESD RATINGS (Note 2)			
Human Body Model	HBM	2500	V
Machine Model	MM	300	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Input differential voltage is the non−inverting pin with respect to the inverting pin. If V_{ID} > ±1 V, the maximum input current must not exceed ±1 mA; an input series resistor must be used to limit the input current.
2. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per AEC−Q100−002 (JEDEC standard: JESD22−A114)
   ESD Machine Model tested per AEC−Q100−003 (JEDEC standard: JESD22−A115)

Table 3. THERMAL INFORMATION (Note 3)

Parameter	Symbol	Value	Unit
Junction to Ambient (Note 4)	θ_{JA}	140	°C/W
Junction to Case Top (Note 4)	ψ_{JT}	34	°C/W

3. Short−circuits can cause excessive heating and destructive dissipation. Values are typical.
4. Multilayer board, 1 oz. copper, 400 mm^2 copper area, both junctions heated equally.

Table 4. RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Limit	Unit
Operating Supply Voltage	V_S	2.7 to 26	V
Specified Operating Range	T_A	−40 to +125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Table 5. ELECTRICAL CHARACTERISTICS AT V_S = 3.0 V
At T_A = +25°C, R_L = 10 kΩ connected to mid−supply, V_{CM} = V_{OUT} = midsupply, unless otherwise noted.
Boldface limits apply over the specified temperature range, T_A = −40°C to +125°C, guaranteed by characterization and/or design.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			0.6	6.0	mV
					8.0	mV
Offset Voltage Drift	ΔV/ΔT			2.0		μV/°C
Input Bias Current	I_{IB}			55	100	nA
					200	nA
Input Offset Current	I_{OS}			1.0	30	nA
					80	nA
Input Common Mode Range	V_{CM}		V_{SS} − 0.2		V_{DD} + 0.2	V
Common Mode Rejection Ratio	CMRR	V_{SS} + 0.15 < V_{CM} < V_{DD} − 0.15	50	80		dB
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 600 Ω	V_{DD} − 0.2	V_{DD} − 0.08		V
Output Voltage Low	V_{OL}	R_L = 600 Ω		V_{SS} + 0.10	V_{SS} + 0.25	V
Short Circuit Current	I_{SC}		10			mA
NOISE PERFORMANCE						
Voltage Noise Density	e_N	f = 1 kHz, no load		25		nV/√Hz
DYNAMIC PERFORMANCE						
Open Loop Voltage Gain	A_{VOL}	V_O = 2 Vpp, R_L = 600 Ω		88		dB
Gain Bandwidth Product	GBWP	R_L = 2 kΩ		3.5		MHz
Gain Margin	A_M	R_L = 600 Ω, C_L = 100 pF		8		dB
Phase Margin	ψM	R_L = 600 Ω, C_L = 100 pF		56		°
Slew Rate	SR	R_L = 10 kΩ		1.0		V/μS
Total Harmonic Distortion + Noise	THD+N	V_{OUT} = 2 Vpp, f_{IN} = 10 kHz, A_V = 2, R_L = 10 kΩ		0.008		%
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = 2.7 V to 26 V	60	105		dB
Quiescent Current	I_{DD}	No load, V_{CM} = V_S/2, per channel		0.7	1.3	mA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Table 6. ELECTRICAL CHARACTERISTICS AT V_S = 5.0 V
At T_A = +25°C, R_L = 10 kΩ connected to mid−supply, V_{CM} = V_{OUT} = midsupply, unless otherwise noted.
Boldface limits apply over the specified temperature range, T_A = −40°C to +125°C, guaranteed by characterization and/or design.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			0.6	6.0	mV
					8.0	mV
Offset Voltage Drift	ΔV/ΔT			2.0		μV/°C
Input Bias Current	I_{IB}			55	100	nA
					200	nA
Input Offset Current	I_{OS}			1.0	30	nA
					80	nA
Input Common Mode Range	V_{CM}		V_{SS} − 0.2		V_{DD}+0.2	V
Common Mode Rejection Ratio	CMRR	V_{SS} + 0.15 < V_{CM} < V_{DD} − 0.15	50	85		dB
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 600 Ω	V_{DD}−0.30	V_{DD}−0.10		V
Output Voltage Low	V_{OL}	R_L = 600 Ω		V_{SS}+0.14	V_{SS}+0.30	V
Short Circuit Current	I_{SC}		10			mA
NOISE PERFORMANCE						
Voltage Noise Density	e_N	f = 1 kHz, no load		25		nV/√Hz
DYNAMIC PERFORMANCE						
Open Loop Voltage Gain	A_{VOL}	V_O = 2 Vpp, R_L = 600 Ω		88		dB
Gain Bandwidth Product	GBWP	R_L = 2 kΩ		3.6		MHz
Gain Margin	A_M	R_L = 600 Ω, C_L = 100 pF		9		dB
Phase Margin	ψM	R_L = 600 Ω, C_L = 100 pF		60		°
Slew Rate	SR	R_L = 10 kΩ		1.0		V/μS
Total Harmonic Distortion + Noise	THD+N	V_{OUT} = 4 Vpp, f_{IN} = 10 kHz, A_V = 2, R_L = 10 kΩ		0.008		%
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = 2.7 V to 26 V	60	105		dB
Quiescent Current	I_{CC}	No load, V_{CM} = V_S/2, per channel		0.75	1.4	mA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Table 7. ELECTRICAL CHARACTERISTICS AT V_S = 24 V
At T_A = +25°C, R_L = 10 kΩ connected to mid−supply, V_{CM} = V_{OUT} = midsupply, unless otherwise noted.
Boldface limits apply over the specified temperature range, T_A = −40°C to +125°C, guaranteed by characterization and/or design.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			0.6	6.0	mV
					8.0	mV
Offset Voltage Drift	ΔV/ΔT			4.5		μV/°C
Input Bias Current	I_{IB}			55	100	nA
					200	nA
Input Offset Current	I_{OS}			1.0	30	nA
					80	nA
Input Common Mode Range	V_{CM}		V_{SS} − 0.2		V_{DD}+0.2	V
Common Mode Rejection Ratio	CMRR	V_{SS} + 0.15 < V_{CM} < V_{DD} − 0.15	50	100		dB
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 2 kΩ	V_{DD}−0.30	V_{DD}−0.10		V
Output Voltage Low	V_{OL}	R_L = 2 kΩ		V_{SS}+0.14	V_{SS}+0.30	V
Short Circuit Current	I_{SC}		10			mA
NOISE PERFORMANCE						
Voltage Noise Density	e_N	f = 1 kHz, no load		25		nV/√Hz
DYNAMIC PERFORMANCE						
Open Loop Voltage Gain	A_{VOL}	V_O = 2 Vpp, R_L = 2 kΩ		88		dB
Gain Bandwidth Product	GBWP	R_L = 10 kΩ		3.0		MHz
Gain Margin	A_M	R_L = 10 kΩ, C_L = 100 pF		9.0		dB
Phase Margin	ψM	R_L = 10 kΩ, C_L = 100 pF		70		°
Slew Rate	SR	R_L = 10 kΩ		1.0		V/μS
Total Harmonic Distortion + Noise	THD+N	V_{OUT} = 10 Vpp, f_{IN} = 10 kHz, A_V = 2, R_L = 10 kΩ		0.013		%
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = 2.7 V to 26 V	60	105		dB
Quiescent Current	I_{CC}	No load, V_{CM} = V_S/2, per channel		0.95	1.4	mA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTICS

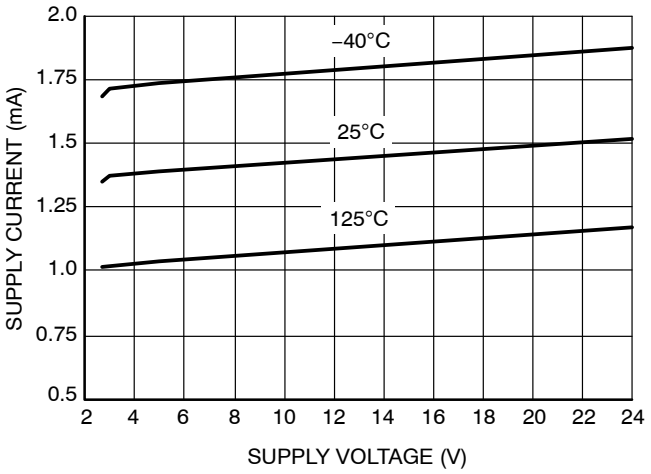


Figure 1. Supply Current vs. Supply Voltage

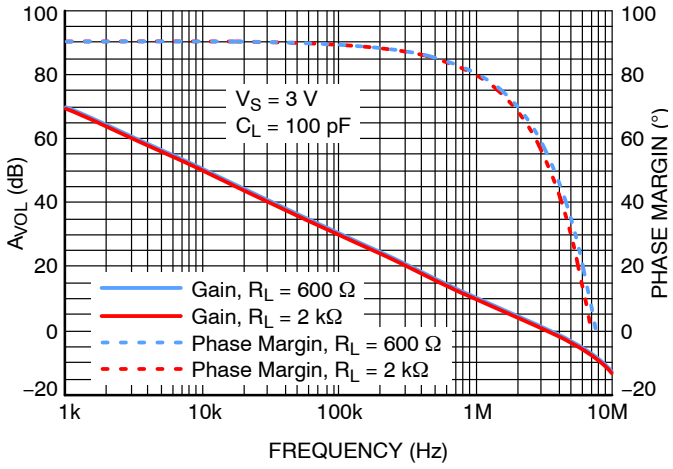


Figure 2. Open Loop Gain and Phase Margin vs. Frequency

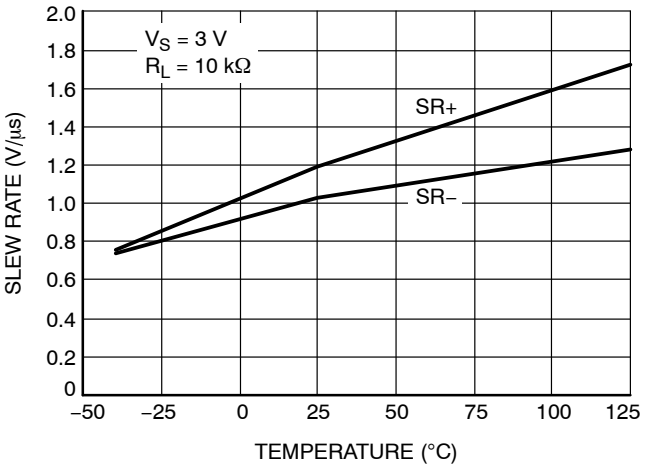


Figure 3. Slew Rate vs. Temperature

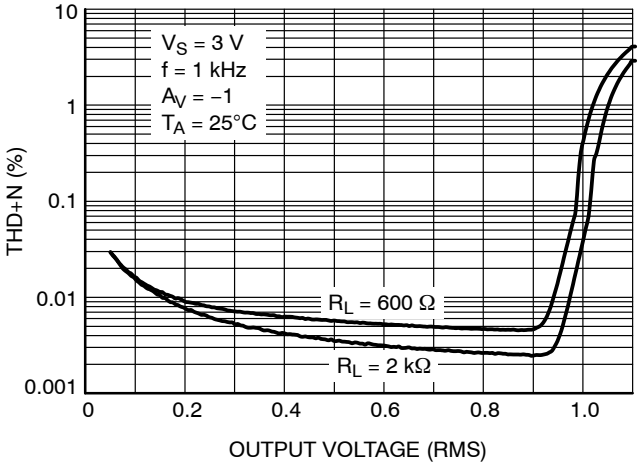


Figure 4. THD+N vs. Output Voltage

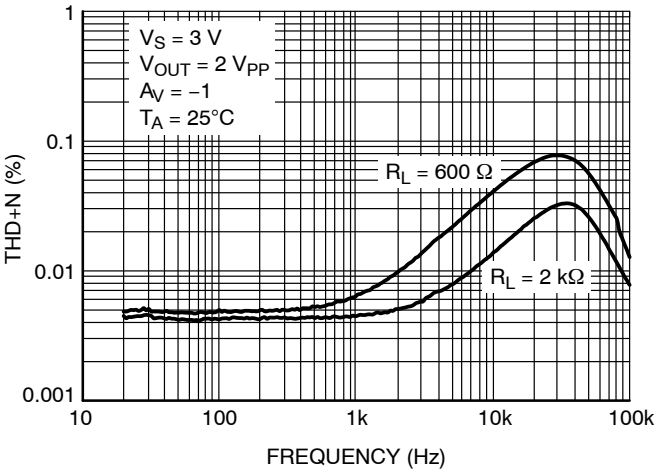


Figure 5. THD+N vs. Frequency

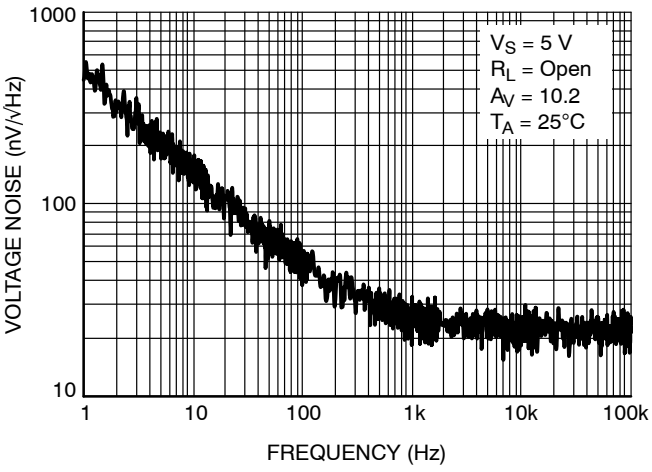


Figure 6. Input Voltage Noise vs. Frequency

TYPICAL CHARACTERISTICS

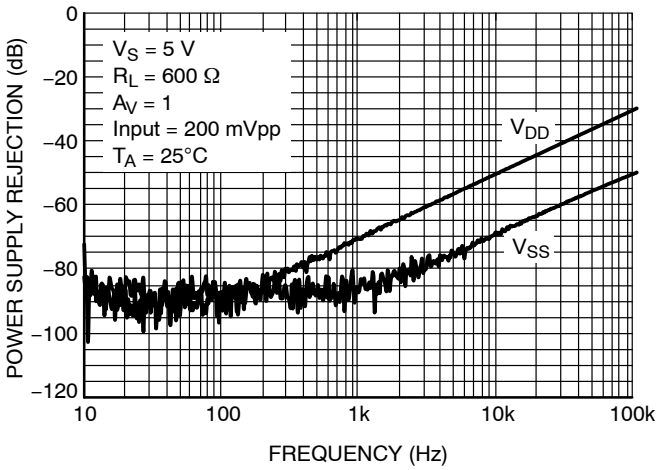


Figure 7. PSRR vs. Frequency

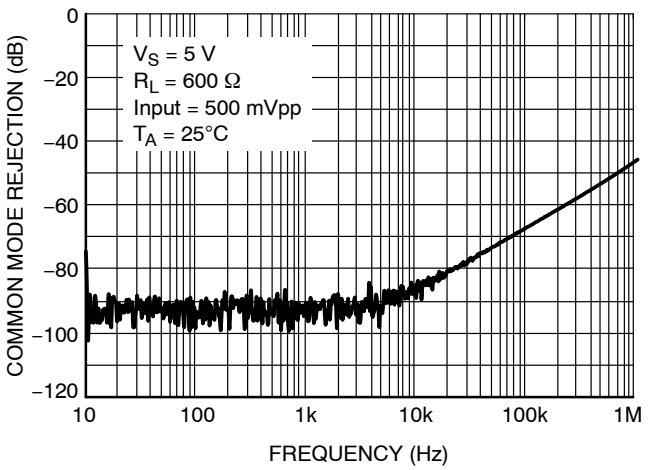


Figure 8. CMRR vs. Frequency

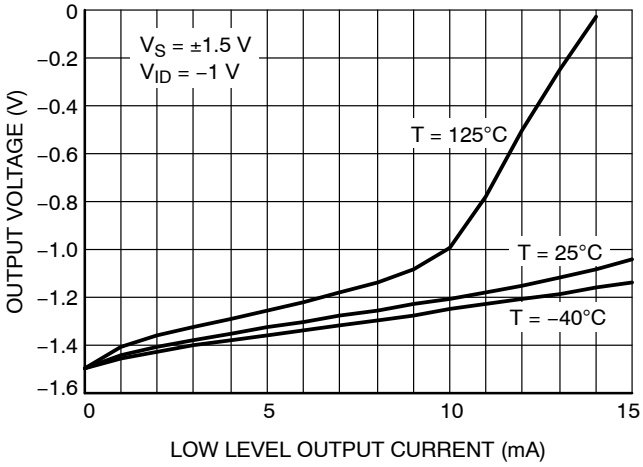


Figure 9. Low Level Output Voltage vs. Output Current at 3 V Supply

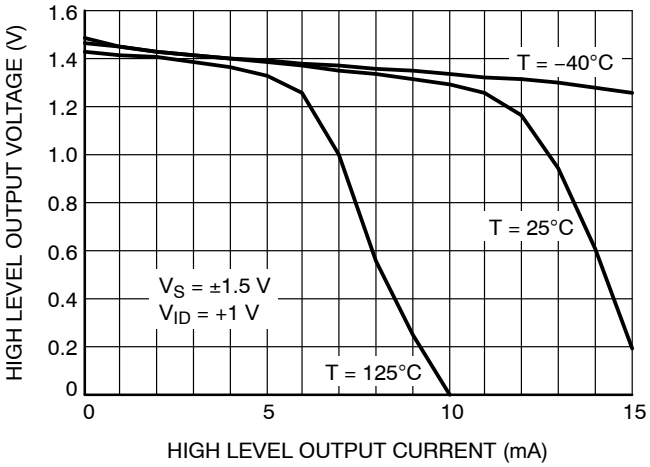


Figure 10. High level Output Voltage vs. Output Current at 3 V Supply

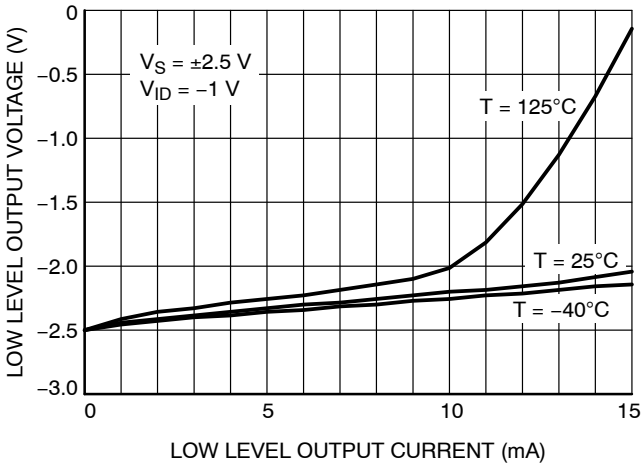


Figure 11. Low Level Output Voltage vs. Output Current at 5 V Supply

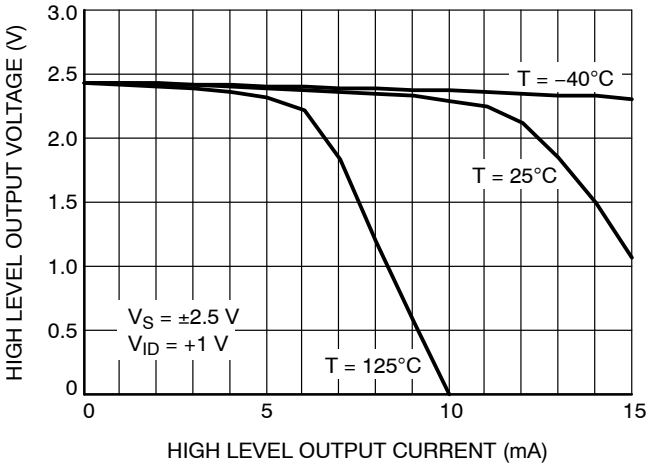


Figure 12. High Level Output Voltage vs. Output Current at 5 V Supply

TYPICAL CHARACTERISTICS

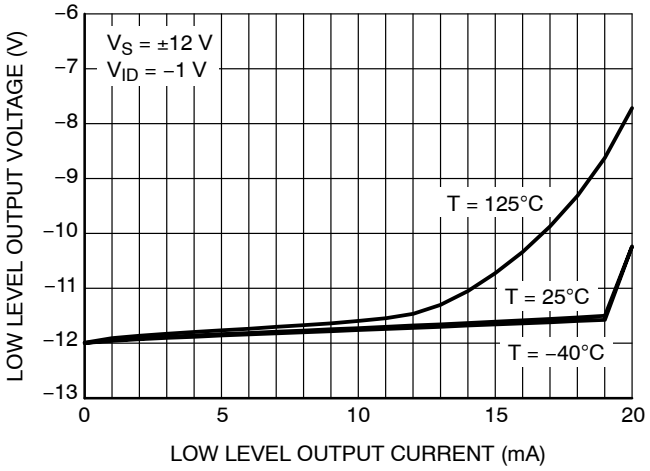


Figure 13. Low Level Output Voltage vs. Output Current at 24 V Supply

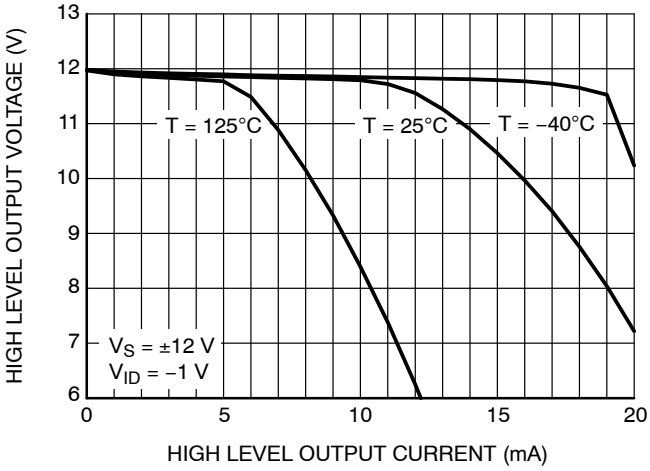


Figure 14. High Level Output Voltage vs. Output Current at 24 V Supply

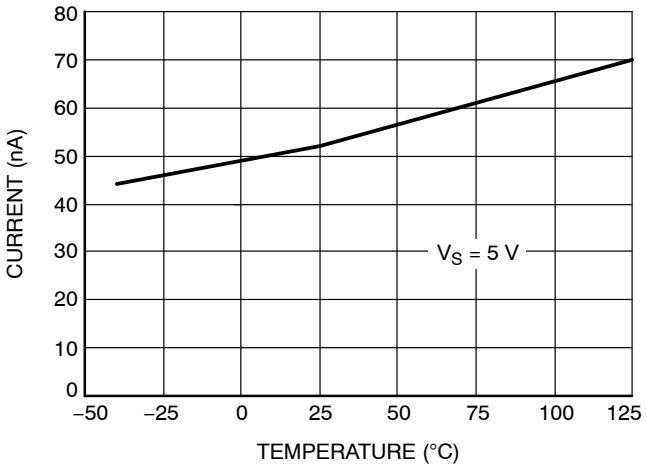


Figure 15. Input Bias Current vs. Temperature

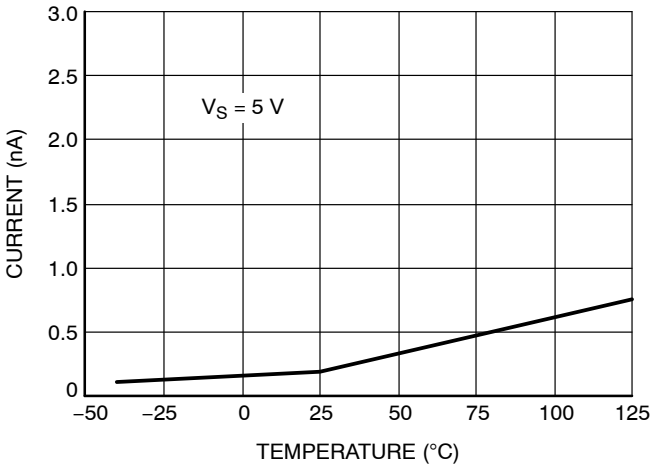


Figure 16. Input Offset Current vs. Temperature

TYPICAL CHARACTERISTICS

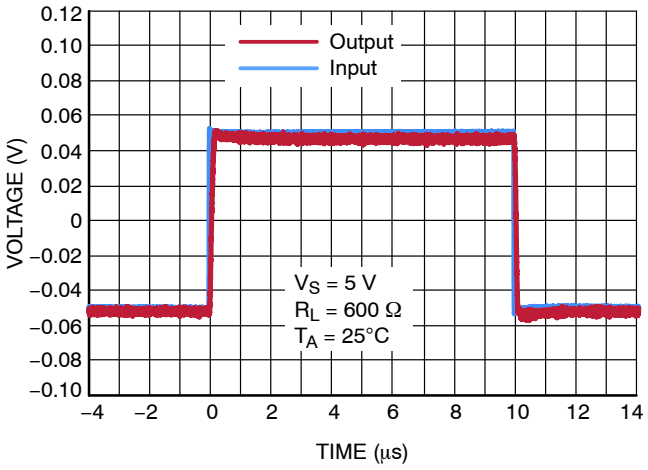


Figure 17. Noninverting Small Signal Transient Response

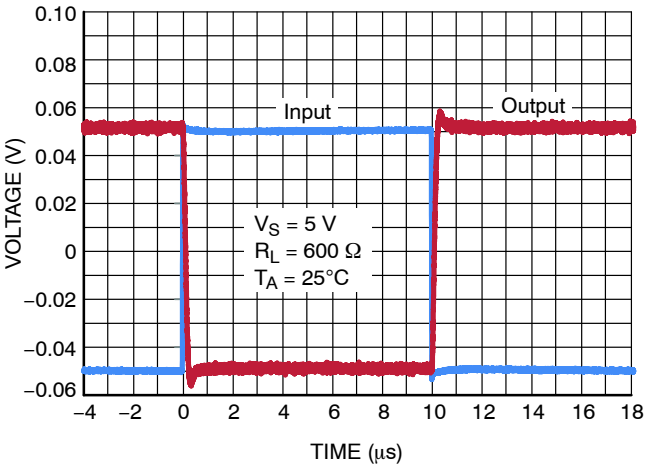


Figure 18. Inverting Small Signal Transient Response

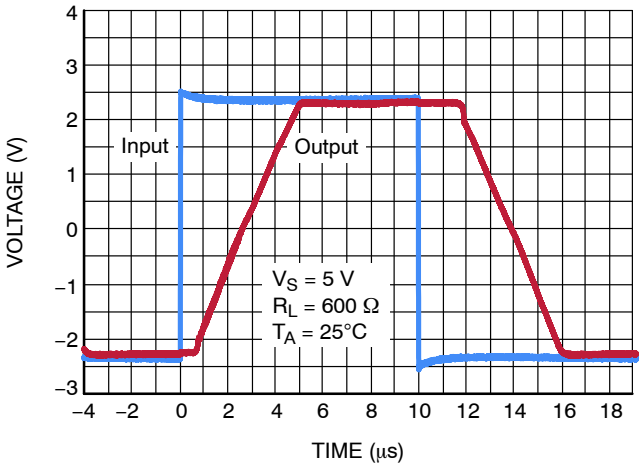


Figure 19. Noninverting Large Signal Transient Response

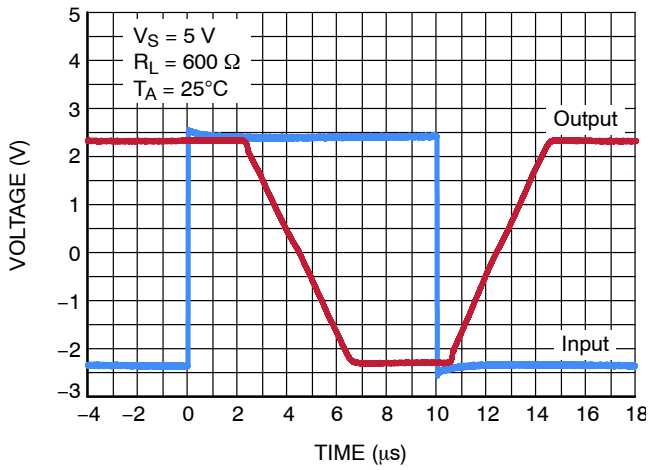


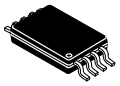
Figure 20. Inverting Large Signal Transient Response

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

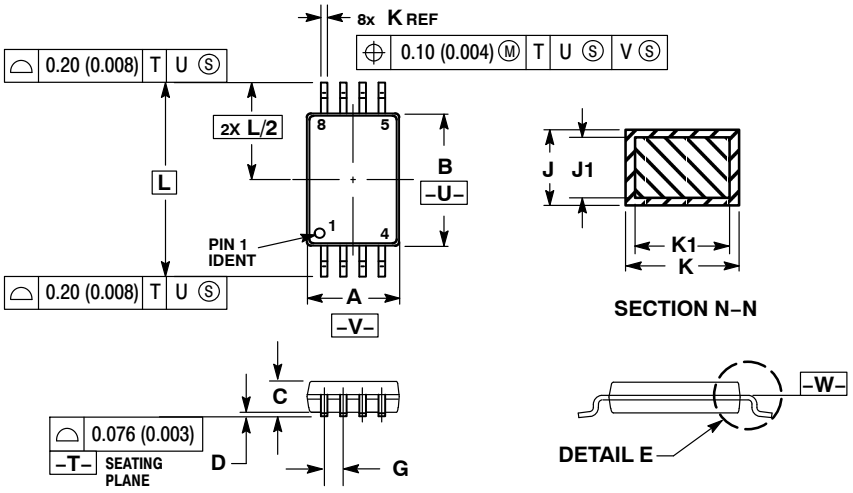
ON Semiconductor®

TSSOP−8
CASE 948S−01
ISSUE C

DATE 20 JUN 2008



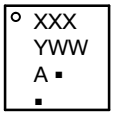
SCALE 2:1



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	2.90	3.10	0.114	0.122
B	4.30	4.50	0.169	0.177
C	---	1.10	---	0.043
D	0.05	0.15	0.002	0.006
F	0.50	0.70	0.020	0.028
G	0.65 BSC		0.026 BSC	
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

GENERIC MARKING DIAGRAM*



XXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

DOCUMENT NUMBER:	98AON00697D	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.	
STATUS:	ON SEMICONDUCTOR STANDARD		
NEW STANDARD:			
DESCRIPTION:	TSSOP−8		PAGE 1 OF 2

ISSUE	REVISION	DATE
O	RELEASED FOR PRODUCTION.	18 APR 2000
A	ADDED MARKING DIAGRAM INFORMATION. REQ. BY V. BASS.	13 JAN 2006
B	CORRECTED MARKING DIAGRAM PIN 1 LOCATION AND MARKING. REQ. BY C. REBELLO.	13 MAR 2006
C	REMOVED EXPOSED PAD VIEW AND DIMENSIONS P AND P1. CORRECTED MARKING INFORMATION. REQ. BY C. REBELLO.	20 JUN 2008

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales