Features

- Configurable pulse width modulation (PWM) output
- NFC contact-less interface compliant to ISO/IEC 18000-3 mode 1 (ISO/IEC 15963)
- Constant light output (CLO) with 8 configurable reference points
- Integrated operation-time counter (OTC) and on/off counter
- Non-volatile memory (NVM) including UID and 20 bytes free memory for user data
- Configurable pulse width modulation (PWM) output
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Description

The NLM0011 is a dual-mode NFC wireless configuration IC with PWM output. It is compatible with existing analog LED-driver designs and with the NFC-programming specification from the Module-Driver Interface Special Interest Group (MD-SIG). This device is primarily designed for LED applications to enable NFC programming. In addition, advanced features such as the constant lumen output (CLO) as well as the on/off counting are integrated, and there is no need for an additional microcontroller. Since the NLM0011 is designed to work together with mainstream analog driver ICs, there are no firmware development efforts needed. It can be easily adapted into existing designs to replace the “plug-in resistor” current configuration concept. The NLM0010 is a light version without CLO function.

Table of contents

1 General

General information of NLM0011/ NLM0010 are given here.

The NLM0011/NLM0010 belongs to the "NFC-PWM Series" product family and is used in LED lighting applications together with a current adjustable LED driver.

The NLM0011/NLM0010 operates in two operating modes:

- Configuration Mode - exclusively used to configure the device via NFC

  The NLM0011/NLM0010 enables a LED lighting module manufacturer to configure the LED lighting control of the module according to the characteristics of connected LED light. This configuration step completes the LED module manufacturing process and can be done contactless without powering the LED module. The final configuration of the LED module is done via Near Field Communication (NFC) between the configuration station and the LED module. The NLM0011/NLM0010 chip provides the NFC transceiver functions of the LED module and includes a non volatile memory (NVM) for storing the configuration data. The configuration data usually consist of the LED driver current setpoint value and a life time adjustment . The life time adjustment function compensates the aging effect of the LEDs by adjusting the LED setpoint current value according to the accumulated operating hours of the LEDs (NLM0011 only). Therefore the NLM0011 counts the operating hours of the connected LED and adjusts the LED current set point value to a aging function, which is configured via near field communication during the configuration step. In configuration mode, the content of the NVM can be read out via NFC by an external NFC reader. In configuration mode the NLM0011/NLM0010 is powered by the harvested energy of the NFC field. The device only enters the configuration mode, if the external supply voltage V_{CC} is switched off, before applying the NFC field. After completion of NFC configuration the NFC field has to be removed before applying a supply on pin V_{CC} in order to release the configuration as valid. The configuration mode is left by removing the NFC reader field. During NFC configuration mode the PWM output is inactive and switched to High Impedance ("High-Z").
- Lighting Operational Mode - exclusively used to provide a stored configuration in lighting application

  In lighting Operational Mode the NLM0011/NLM0010 is powered from the external Vcc source of the lighting module. The NLM0011/NLM0010 enters the lighting operational mode, if an external V_{CC} source is present and the device is not in configuration mode. After powering up, means applying external V_{CC} and no NFC field is present, when applying external V_{CC}, the NLM0011/NLM0010 reads the LED current setpoint value configuration from the integrated NVM and configures a pulse width modulation (PWM) unit. The PWM cycle period and duty cycle contain the information of the LED current setpoint value. The PWM data are output of the chip and will be converted into an analog value externally or directly delivered to the LED controller (depending on the used external LED controller). The operation hours are counted and the LED current setpoint value is adjusted according to the aging function by changing the PWM output accordingly (NLM0011 only). That also implies that the NLM0011/NLM0010 accumulates the overall operating hours of the LEDs . That also requires to count the power on times, to store the current value of operating hours periodically into the NVM and to detect a power off event of the lighting system, in order to store the current value of operating hours at the moment of power off. In lighting operational mode the NLM0011/NLM0010 does not communicate and does not respond to external NFC link partners and hence no external NVM access is possible. That means applying an NFC field to the device which already entered the lighting operational does not have any effect.

2 Feature Overview

NLM0011/NLM0010 product features are given here.

Product Features

Contactless Interface

- Physical interface and Anti collision compliant to ISO/ IEC 18000-3 mode 1 (ISO/IEC 15693)
  - contactless transmission of data and supply energy
  - data rate up to 26.69 kbit/s
  - operation frequency: 13.56 MHz
  - Anti-collision method complying with ISO/IEC 18000-3 mode 1 with identification rate of up to 50 tags/s
- AFI according ISO/IEC 18000-3 mode 1
- Read / write distance up to 150 cm (influenced by external circuitry i.e. reader and antenna design)

Command Set

- Support of error codes 01_H, $0F_H$, 10_H, 12_H according to ISO/ IEC 18000-3 mode 1
- If a command is sent to the NLM0011/NLM0010 which has an invalid frame length no response is returned
- Following command set is supported:
  - Inventory (command code 01_H)
  - StayQuiet (command code 02_H)
  - ReadSingleBlock (command code 20_H)
  - WriteSingleBlock (command code 21_H)
  - Select (command code 25_H)
  - ResetToReady (command code 26_H)
  - WriteAFI (command code 27_H)
  - LockAFI (command code 28_H)
  - WriteByte (custom command - ISO command code $A0_H$; custom embedded command code 90_H)

Non Volatile Memory (NVM)

An Infineon EEPROM is used.

- size 576 Bit
- User area 52 bytes, organized in 13 free user blocks
- Each block organized in 4 bytes
- Service area 12 bytes
- Unique chip identification number
- Each block can be permanently locked against overwriting
- EEPROM programming time per page < 4 ms
- EEPROM endurance minimum 100,000 erase/write cycles
- Data retention minimum 10 years

Supply Concept

operation mode dependent:

- in Lighting Operation mode the chip is supplied by external voltage source
  - external supply voltage in the range of 3 … 5V
  - internal voltage regulator (LDO) is generating a stabilized internal supply
  - if external supply voltage is present, then the device cannot be supplied by harvesting energy from the NFC field

  - if external supply voltage is present, NVM cannot accessed by external reader
  - the device is detecting switch off of external power supply by observing the external supply voltage level and detecting the resulting under voltage condition. The system has stored energy - internal and external capacitance - to save the current system status into the NVM before the power disappears.
- in configuration mode the device is supplied from the harvested energy of the electromagnetic field of the NFC reader.

LED Current Setpoint Definition by PWM

- typical logical levels of PWM output are 0V (logic Low) and 2.8V (logic High)
- period/ Frequency of PWM signal programmable between 1kHz and 30kHz
- Duty cycle programmable between 0% and 100%
- resolution/ granularity depends on PWM Frequency (~14.73 bit@ 1kHz; ~9.82bit@30kHz)

Operational Time Counting (OTC)

The Device is counting the operation hours and stores the value of overall operation time every 4 hours into the NVM. The device detects a power-off event and stores the current value of operation into the NVM before the chip is switched off.

On/ Off Counting

The device is counting the number of power on/ power off cycles and stores it in NVM.

Constant Lumen Output (CLO) (NLM0011 only)

The device is able to adjust the LED current setpoint value depending on an aging function over operating time. The aging function is end customer defined and stored in the NVM within device configuration. The aging function is defined between reference points. The setpoint value is interpolated between the setpoints, by taking the actual accumulated operating time into account. This feature is not available in NLM0010.

3 Application Overview

The intended application use case is explained here.

The application use case of NLM0011/NLM0010 in lighting operation mode looks like that :

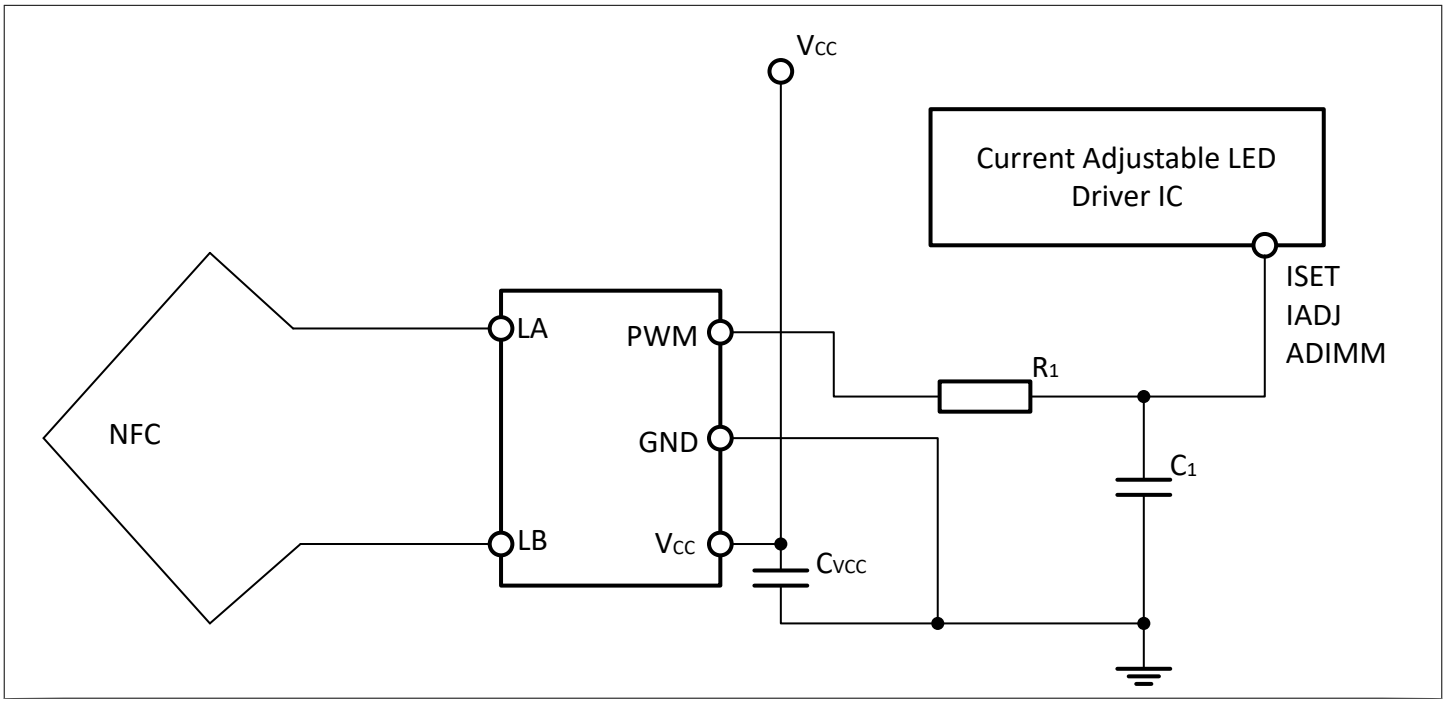


Figure 1 NLM0011 Application View

The NLM0011/NLM0010 chip is connected to the LED driver circuit. The driver circuit controls the current of the LEDs. The setpoint value of the current is stored in integrated NVM of the NLM0011/NLM0010. According to the NVM content the NLM0011/NLM0010 generates a PWM output, which corresponds to the value of the setpoint. Usually the PWM data pulses are converted into an analog voltage by an external R/C circuitry. This analog voltage is the reference setpoint for the LED current regulation loop of the module. The analog value of the setpoint is determined by the period and duty cycle of the PWM output, the time constant of the R/C circuitry and the voltage swing of the PWM output driver. The NLM0011/NLM0010 provides only the setpoint definition of the LED current of the regulation loop. The NLM0011/NLM0010 does not execute the regulation loop or any parts of the regulation loop. Within LED lighting systems the setpoint definition is usually called "ISET".

Some LED drivers/ controller accept the direct PWM input and convert the PWM data into a setpoint value internally. In that case no R/C circuitry is needed between the NLM0011 /NLM0010 and the LED driver.

A complete application example based on Infineon XDPL8105 LED controller is shown next:

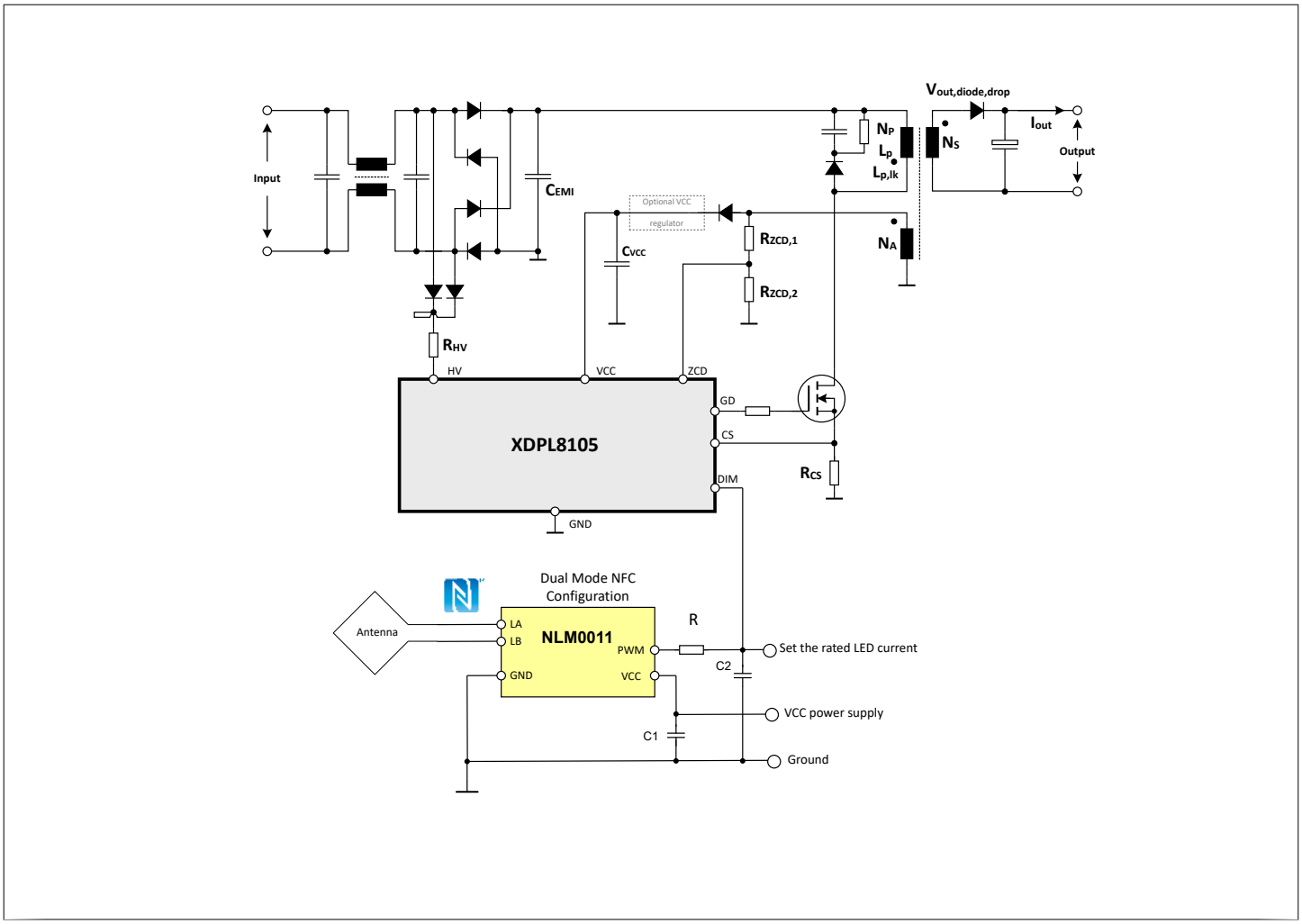


Figure 2 Application example

The parameters of the PWM output are period and duty cycle. Both have to be configured during NFC configuration. The values of the configuration parameters have to be calculated according to the requirements of the application. Using an external R/C circuitry with a given time constant, the duty cycle and period of the PWM can be calculated to generate any value between minimum and maximum output voltage of the digital PWM output driver.

The calculated parameters including the aging function are written into the NVM of the NLM0011/NLM0010 during NFC configuration. That can only be done if the NLM0011/NLM0010 is powered off. The NLM0011/NLM0010 will harvest the energy from the electromagnetic NFC field and supply itself in that case.

4 Pin Description

The pin description of NLM0011/NLM0010 is given here.

Table 1 Pin Description

Package Pin	Name	Type	Characteristics	Remark
1	PWM	digital Output (Push Pull)	see Table 20	Pulse Width Modulated signal containing the ISET information
2	GND	Ground	Supply	Ground
3	V_{CC}	Power	Supply, see Table 20	Supply Voltage
4	LA	I/O	Analog	Antenna Coil A
5	LB	I/O	Analog	Antenna Coil B

5 Functional Description

The functional description of the NLM0011 is given here.

The basic structure and functional blocks of NLM0011/NLM0010 are shown in the block diagram below.

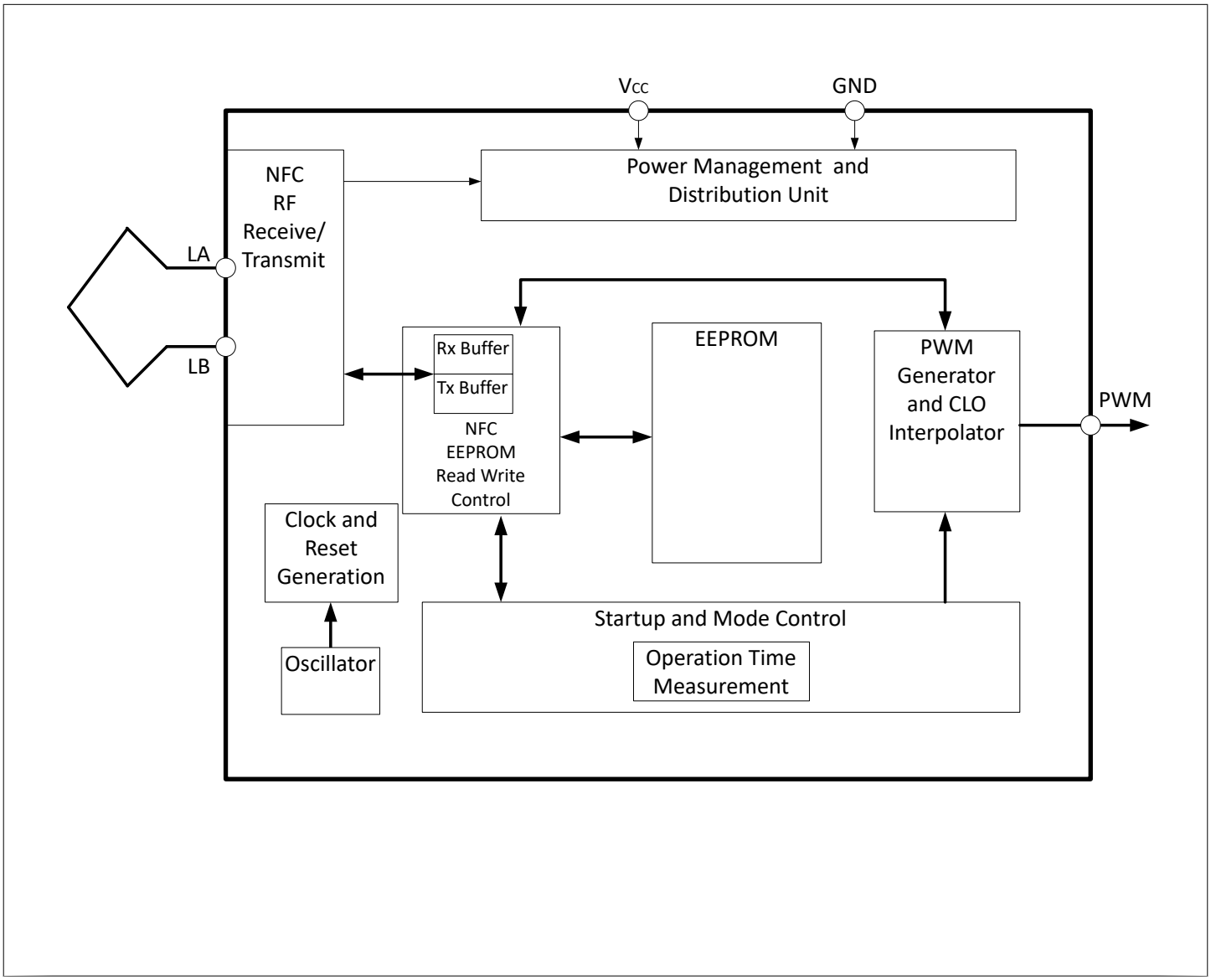


Figure 3 Block Diagram

NFC RF-Receive Transmit:

The RF and analog circuitry for contactless NFC communication is provided here. That includes voltage rectifier, voltage regulator for energy harvesting, as well as signal modulator and demodulator.

NFC EEPROM Read/ Write Control:

That functional block provides read and write access control to the EEPROM. It supports ISO commands and block/ page access to the NVM. It can be triggered by NFC in case of an external triggered access to the NVM or by the start up and mode control for an internal triggered access to the NVM.

EEPROM:

NVM in EEPROM technology. Basic key figures are given inFeature Overview. Detailed description is provided in Memory Organization

Start up and Mode Control:

This functional block detects the mode of operation and provides the proper start up for the two operating modes. In lighting operational mode, it configures and updates the PWM Generator and counts the operational hours. It updates the NVM by operational hours periodically or if the chip underruns a undervoltage emergency threshold limit. It interpolates the CLO setting as well, according to the configured aged function . The interpolation result changes the PWM frequency and duty cycle parameter dynamically, which are delivered to the PWM generator. In configuration mode it provides NFC reader access to the NVM and responds to NFC reader commands. It is implemented as a hard coded finite state machine.

PWM Generator and CLO Interpolator:

That functional block is configured by the start up and mode control with the PWM period and duty cycle setting. It is only active in lighting operational mode and generates the PWM output according to configuration and CLO until the chip is switched off (CLO function is only available in NLM0011).

Power Management and Distribution:

This unit includes the voltage regulators and under voltage lockout detection and control function. The chip can either be supplied by energy harvested from the NFC field or by an external V_{CC} source. In case an external V_{CC}source is present the NLM0011 chip enters the lighting operational mode and no NFC operation incl. energy harvesting is possible anymore.

Clock and Reset Generation/ Oscillator:

Internal clocks and resets are generated here. Architectural clock gating control is done as well. In configuration mode the clock of 13,56 MHz is derived from the external NFC carrier by a clock recovery unit within the NFC Transceiver. In lighting operational mode the clock is provided by internal oscillator running at 27,12MHz.

6 Memory Organization

The EEPROM structure and Organization is described here.

In general the EEPROM memory is organized in 18 blocks each with a block size of 4 byte. Blocks 00_Hh to $0C_H$ are freely available for user and application data. Blocks $0D_H$ to 11_H are used to store chip configuration and individualization data.

	Block address	Byte and Bit Index of a block			
		3	2	1	0
		Bit[31:24]	Bit[23:16]	Bit[15:8]	Bit[7:0]
Service Area	11_H	Block Lock Information (2 bits per block)			
	10_H	Service Data			
	$0F_H$	AFI	Service Data		
	$0E_H$	UID[63:32]			
	$0D_H$	UID[31:0]			
Application and User Area	$0C_H$	Application and User Data			
	$0B_H$	Application and User Data			
	...	Application and User Data			
	01_H	Application and User Data			
	00_H	Application and User Data			

Figure 4 General Memory Structure

In NLM0011/ NLM0010 product the EEPROM is utilized as follows:

The UID Structure $0E_H$/ $0D_H$

The UID record contains the User Identification data, which is defined by the ISO/ IEC standard and Infineon.

Table 2 UID Block $0E_H$

Bit index of UID / Description			
[63:56]	[55:48]	[47:40]	[39:32]
ISO $E0_H$	ISO IFX 05_H	Family Code Byte	UID[39:32]

Table 3 UID Block $0D_H$

Bit index of UID / Description
[31:0]
UID[31:0]

Table 4 UID Fields Description

Abbreviation	Description
ISO	According to ISO/IEC 18000-3 mode 1 fixed to $E0_H$
ISO IFX	According to ISO/IEC 7816-6 the IC Manufacturer Code (IC Mfg code)is assigned to 05_H.
Family Code Byte	Identification within the NLM0011/NLM0010 product family, the value is : • $B8_H$ for product NLM0011 (design steps A11, A12, A13) • $B9_H$ for product NLM0011(design step A14) • $B0_H$ for product NLM0010 (design steps A11, A12, A13) • $B1_H$ for product NLM0010(design step A14) for the NLM0011/NLM0010 Version 1.0

Following table defines the coding for the Family Code byte of the UID (bit 47 - bit 40):

Table 5 Family Code Byte

Bit index of UID / Description		
[47:45]	[44]	[43:40]
Memory Size and Memory Identification: The 576-Bit EEPROM is identified by the fixed value 101_B	Type Identifier: It is fixed to 1_B for NLM0011/ NLM0010.	Chip Type: NLM0011 is identified by $1xxx_B$ NLM0010 is identified by $0xxx_B$

The UID field UID[39:0] is reserved to store Infineon specific manufacturing information.

The Lock Block 11_H

Memory block 11_H contains the information to protect an individual block in the memory against overwriting. The structure of this block is described in following table.

Table 6 Lock Block 11_H

Bit index of block 11_H	Description
[31:30]	Lock information for block $0F_H$. 10_B the block can be read and written, others the block is protected against write access (read only)
[29:28]	Lock information for block $0E_H$. 10_B the block can be read and written, others the block is protected against write access (read only)
[27:26]	Lock information for block $0D_H$. 10_B the block can be read and written, others the block is protected against write access (read only)
[25:24]	Lock information for block $0C_H$. 10_B the block can be read and written, others the block is protected against write access (read only)
[23:22]	Lock information for block $0B_H$. 10_B the block can be read and written, others the block is protected against write access (read only)

(table continues...)

Table 6 (continued) Lock Block 11_H

Bit index of block 11_H	Description
[21:20]	Lock information for block $0A_H$. 10_B the block can be read and written, others the block is protected against write access (read only)
[19:18]	Lock information for block 09_H. 10_B the block can be read and written, others the block is protected against write access (read only)
[17:16]	Lock information for block 08_H. 10_B the block can be read and written, others the block is protected against write access (read only)
[15:14]	Lock information for block 07_H. 10_B the block can be read and written, others the block is protected against write access (read only)
[13:12]	Lock information for block 06_H. 10_B the block can be read and written, others the block is protected against write access (read only)
[11:10]	Lock information for block 05_H. 10_B the block can be read and written, others the block is protected against write access (read only)
[9:8]	Lock information for block 04_H. 10_B the block can be read and written, others the block is protected against write access (read only)
[7:6]	Lock information for block 03_H. 10_B the block can be read and written, others the block is protected against write access (read only)
[5:4]	Lock information for block 02_H. 10_B the block can be read and written, others the block is protected against write access (read only)
[3:2]	Lock information for block 01_H. 10_B the block can be read and written, others the block is protected against write access (read only)
[1:0]	Lock information for block 00_H. 10_B the block can be read and written, others the block is protected against write access (read only)

The initial value of this block is 02 AA AA AA_H, which indicates that block $0F_H$ and the UID are protected against overwriting.

Issuing a WriteBlock or a WriteByte command to block 11_H performs a write cycle to the memory. The only possible transition is 1 to 0 for each bit of this block. Therefore, unlocking of a block is not possible.

The change of lock information must be executed as a “Read-Modify-Write” operation. Firstly the block must be read, then all appropriate bits have to be changed, and finally the information should be written back to the block. The write operation should be performed in a secure environment.

Note: Changing bits from ’0’ to ’1’ will lead to unexpected chip behavior and should not be performed. The response to a write command including incorrect changed bits is not valid.

Example:

Assuming a NLM0011/ NLM0010 chip, which has not been configured in any way, the Lock Block (11_H) contains data 02 AA AA AA_H (i.e. only block $0F_H$ and UID are write protected).

To lock i.e. block 06_H from being re-written, the following operations should be performed in a secure environment. The command example includes the ISO Flags and the CRC:

- Read content of block 11_H with “Read single block” command
  - Command example for read single block 02 20 11 4F 51_H
  - Response 00 AA AA AA 02 D4 BC_H
  - Memory content of block 11_H is 02 AA AA AA_H
- Modify bits [13:12] to 00_B
  - Result is 02 AA 8A AA_H
- Write modified value to block 11_H with “Write single block” command
  - Command example for write single block 02 21 11 AA 8A AA 02 1C $F5_H$
  - Acknowledge Response 00 78 $F0_H$
  - Memory content of block 11_H is now 02 AA 8A AA_H

After this sequence, block 06_H is locked and cannot be changed anymore.

The Service Block 10_H

Block 10_H can only be written with the WriteByte command. Bits [31:24] and bits [23:20] are writable, the rest of block 10_H is read only.

Table 7 Service Block 10_H

Bit Index	Abbreviation	Description
[31:24]	RFI	Reserved for Infineon
[23:22]	AFILOCK	These two bits are internally used to lock the AFI byte. 10_BAFI byte is writable 00_BAFI is locked
[21:20]	LOCK	These two bits are used to lock Byte 3 of page 10_H. 10_BByte 3 (bit(31:24)) are writable 00_HByte 3 (bit(31:24)) bit are read only
[19:0]	Configuration Data	Used by Infineon for chip configuration

AFI Block $0F_H$

Block $0F_H$ holds the AFI Byte in bit [31:24]. This byte can only be written using the WriteAFI command. This block is write only.

Note:Writing the AFI with the WriteAFI command should be performed in a secure environment.

Table 8 AFI Block $0F_H$

Bit Index	Abbreviation	Description
[31:24]	AFI	Application Family Identifier complying to ISO/IEC 18000-3 mode 1
[23:0]	RFU	Reserved for Future Use

Application and User Data Memory

The application and user data memory contains in total 13 EEPROM (address 00_H to $0C_H$) blocks.
Every block consists of 4 Bytes. Hence in total 52 Bytes are available for application and customer specific needs.
The user data memory is allocated as follows:

Block address	Byte and Bit Index of a block			
	3	2	1	0
	Bit[31:24]	Bit[23:16]	Bit[15:8]	Bit[7:0]
$0C_H$	Reserved for Application and End Customer		Access Code #1 (20-bit)	
$0B_H$	FR	PWM Period I_{max}	Reserved for Application and End Customer	Assignment CTRL (4-bit)
$0A_H$	Operating Time Hours (4*(4+3) bit (16-bit with ECC per nibble))			
09_H	On/ Off count		Switch Off Time (2*(4+3) bit (8-bit with ECC per nibble))	
08_H	Reserved for Application and End Customer			
07_H	Reserved for Application and End Customer			
06_H	Reserved for Application and End Customer			
05_H	Reserved for Application and End Customer			
04_H	Reserved for Application and End Customer			
03_H	Reserved for Application and End Customer		Access Code #2 (20-bit)	
02_H	Duty Cycle Correction Step4	Duty Cycle Correction Step3	Duty Cycle Correction Step2	Duty Cycle Correction Step1
01_H	Duty Cycle Correction Step8	Duty Cycle Correction Step7	Duty Cycle Correction Step6	Duty Cycle Correction Step5
00_H	T_{on} Time (Duty Cycle I_{max})		Duty Cycle Correction (CLO 2 MSBs per Step)	

Figure 5 User Data Memory 00_H to $0C_H$

Based on the feature set of NLM0011/ NLM0010 following amount of memory is required by following features:

Access Code Section:

5 Bytes are required to store two 20-bit wide access codes (block address $0C_H$ and 03_H). The access code concept is described separately in Application and User Memory Access Control .

Operating Time Recording:

The operating time is stored as a 16-Bit integer value and updated by increment value every 4 hours of operation. Therefore the number of operating hours corresponds to the 16-Bit integer value multiplied by four. The 16-bit word consists of 4 nibbles. Every nibble contains a 3-bit ECC check sum. The ECC is able to detect and correct a single bit error within the nibble, in case the value is falsified within the NVM. The ECC is also able to detect two bit errors, but cannot correct them properly. Hence 28-bits are required to store the operating time (4 data nibbles with 3 additional ECC-bits: 4*7bit=28 bit). The 28-bit value is stored at address $0A_H$.

Furthermore the current time, when the device is powered off need to be stored. This is an offset time to the 16-bit value of operating hours. This time offset has a value of 0 hours to 4 hours. It is stored in one byte, where the two most significant bits represent the time offset in hours and the 6 low significant bits represent the time offset in minutes. This byte consists of two nibbles, where every nibble is protected by 3 additional ECC check bits. Hence 2*(4+3) bits (→ 14-bits) are required to store the offset time at switch off event.

In case of switch off the power the On/off counter is incremented and the value is stored (16-bit). Switch off Time and on/off counter are located at address 09_H.

Constant Lumen Output (CLO):

The User Memory needs to store the value of the PWM period and the PWM duty cycle of 100% current set point. Both values are given as 15-Bit integer numbers. The bit "FR" defines the slope of the CLO function. Furthermore the CLO table setting points need to be stored. Up to eight setting points are required. One byte is required per setting point. The 4 most significant bits are used to store the time information (means operation time reference point as multiples of 8192 hours), the 4 low significant bits are used to store the four low significant bits of duty cycle offset information in percent to 50%. Two additional bytes are required to store the most significant bit per duty cycle and step (to achieve full resolution of 50% offset). The duty cycle offset is internally processed as parts of 128. No redundancy need to be provided for these parameters, since they are rarely written.

So in total 12 Bytes are required to configure the PWM according to the CLO table.

Additional Memory:

24 additional bytes are available for application and end user specific purposes (read- and writable).

7 Application and User Memory Access Control

This section describes the access control and access protection of the user memory.

From application point of view the user area of the NVM is separated into two exclusive logical areas. One area is usually reserved for the ligthing power module manufacturer and the other area is usually used by the luminator manufacturer. The area 1 (module area) allocates the blocks at addresses 09_H to $0C_H$. The area 2 (luminator area) allocates the blocks at addresses 00_H to 03_H. The blocks at addresses 04_H to 08_H , which are reserved for application and end customer specific data, can be assigned to either area 1 or area 2.

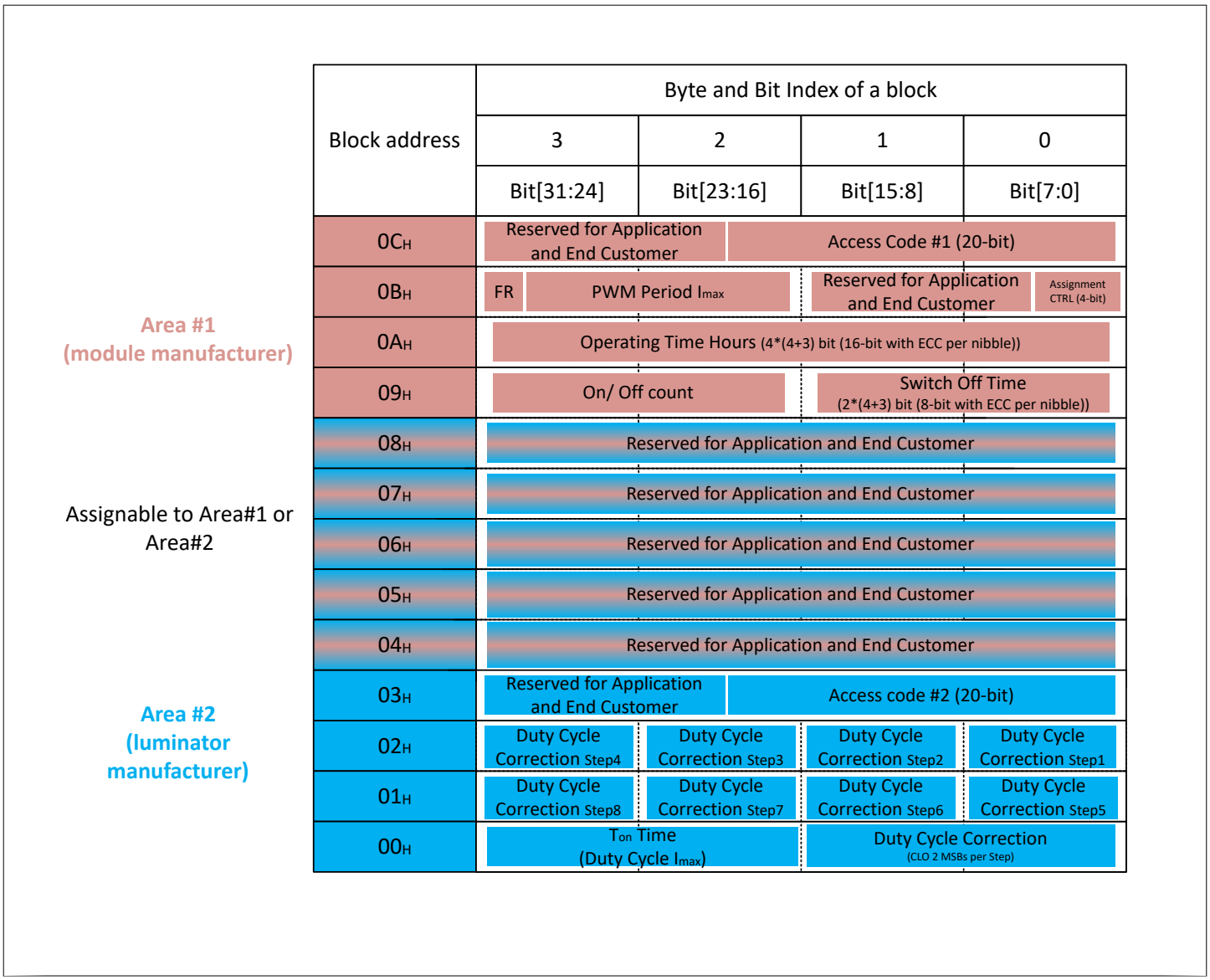


Figure 6 User Memory Areas

The assignment of the blocks at addresses 04_H to 08_H is controlled by the content of block at address $0B_H$ bit 3 down to 0.

Table 9 block 08_H down to block 04_H assignment

block $0B_H$ Bit(3:0)	Block 08_H	Block 07_H	Block 06_H	Block 05_H	Block 04_H
0100_B	Area #1	Area #1	Area #1	Area #1	Area #1
0101_B	Area #1	Area #1	Area #1	Area #1	Area #2

(table continues...)

Table 9 (continued) block 08_H down to block 04_H assignment

block $0B_H$ Bit(3:0)	Block 08_H	Block 07_H	Block 06_H	Block 05_H	Block 04_H
0110_B	Area #1	Area #1	Area #1	Area #2	Area #2
0111_B	Area #1	Area #1	Area #2	Area #2	Area #2
1000_B	Area #1	Area #2	Area #2	Area #2	Area #2
1001_B	Area #2	Area #2	Area #2	Area #2	Area #2
others	Area #1	Area #1	Area #1	Area #1	Area #1

In NFC configuration mode, it is required to control the access of the two areas and to prevent unauthorized access into an area. Therefore two access codes are defined. The access codes are located in the blocks $0C_H$ and 03_H.

The authorization concept can be described like that (the VICC is the NLM0011/ NLM0010 chip herein and the VCD is the NFC Reader herein):

- VCD has to identify and authorize itself by providing an access code to the VICC
- Two access codes are stored in the NVM
  - Area 1 access code at block $0C_H$
  - Area 2 access code at block 03_H
- VCD provides an access code request (transmits an access code) to VICC
- VICC compares the received access code with the stored access code
  - In case of Match: memory access is authorized from now (as long as VICC does not change into power-off state)
  - In case of No Match: memory access is not authorized
- Authorized Memory Access Means:
  - Read Access:
    - NFC requests ReadSingleBlock/ReadMultipleBlock are served and responded by the VICC by providing the read data of the requested NVM block , except Block $0C_H$/ 03_H
      - Read rights in both Area 1 and Area 2 (no matter which of the two access codes are used) are given
      - ReadSingleBlock/ReadMultipleBlock request to block $0C_H$ or 03_H: The VICC will not send back the content of the block to VCD. The value 00000000_H will always be returned back instead of.
  - Write Access:
    - NFC requests WriteSingleBlock/Write Byte are served and responded by the VICC regular , if Authorization with Access Code #1 was done (complete user memory area can be written)
    - In case the Authentication was done with Access Code #2 and no Authentication with Access Code #1 was done, write access only possible to area #2 (luminator area)
- Non Authorized memory access (and read access to block at address $0C_H$/ 03_H when authorized) means:
  - If a ReadSingleBlock/ReadMultipleBlock request by VCD is not authorized: The VICC responds to the ReadSingleBlock/ReadMultipleBlock request by non error read response and data value 00000000_H.
  - If a WriteSingleBlock request by VCD is not authorized: The VCC responds with error response and error code $0F_H$

Response to ReadSingleBlock Request (Read access not authorized):

SOF	Flags 00_H	00000000_H	CRC	EOF

Response to ReadSingleBlock Request to block $0C_H/03_H$ (Read access authorized):

SOF	Flags 00_H	00000000_H	CRC	EOF

Response to WriteSingleBlock or WriteByte Request (Write access not authorized):

SOF	Flags	Error Code $0F_H$	CRC	EOF

Figure 7 Access controlled responses

The authorization procedure is defined as follows:

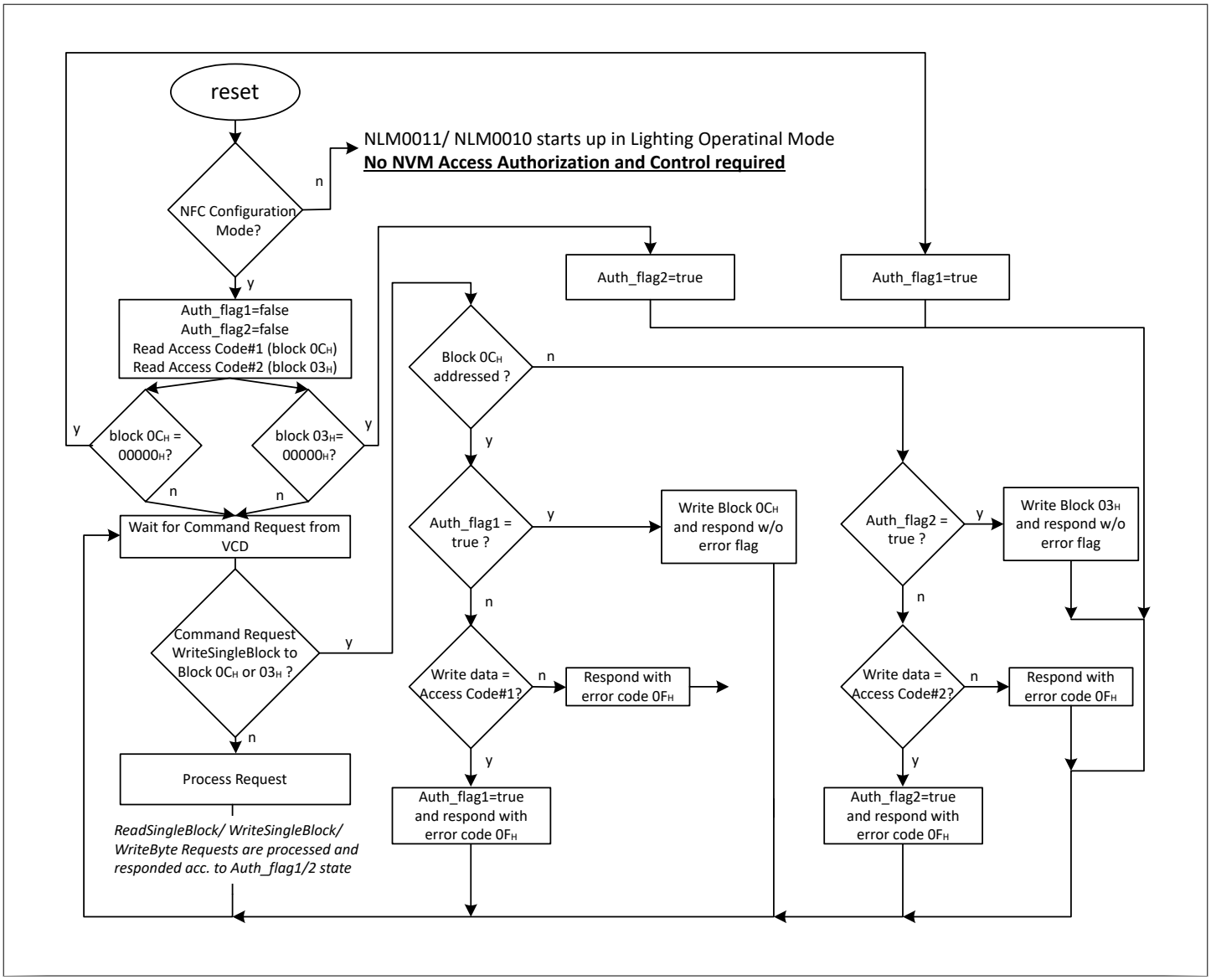


Figure 8 Access Authorization Flow Chart

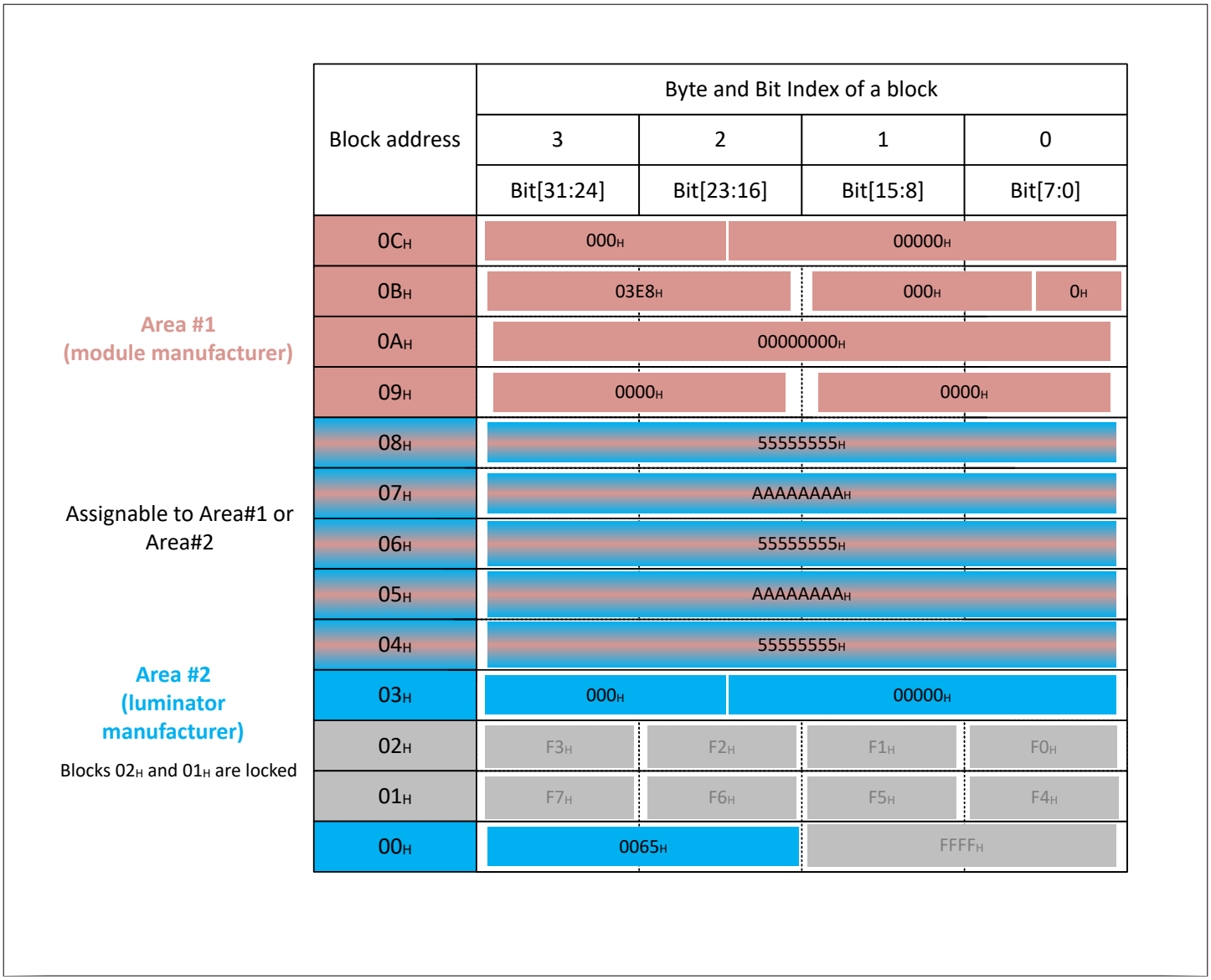
8 NLM0011/NLM0010 EEPROM Shipment Content (Infineon to Customer)

User memory Delivery content (NLM0011 - product with CLO):

	Block address	Byte and Bit Index of a block			
		3	2	1	0
		Bit[31:24]	Bit[23:16]	Bit[15:8]	Bit[7:0]
Area #1 (module manufacturer)	$0C_H$	000_H		00000_H	
	$0B_H$	$03E8_H$		000_H	0_H
	$0A_H$	00000000_H			
	09_H	0000_H		0000_H	
Assignable to Area#1 or Area#2	08_H	55555555_H			
	07_H	$AAAAAAAA_H$			
	06_H	55555555_H			
	05_H	$AAAAAAAA_H$			
	04_H	55555555_H			
Area #2 (luminator manufacturer)	03_H	000_H		00000_H	
	02_H	$F3_H$	$F2_H$	$F1_H$	$F0_H$
	01_H	$F7_H$	$F6_H$	$F5_H$	$F4_H$
	00_H	0065_H		$FFFF_H$	

Figure 9 EEPROM Delivery Content User Memory with CLO

User memory Delivery content (NLM0010 - product w/o CLO):



Block address	Byte and Bit Index of a block			
	3	2	1	0
	Bit[31:24]	Bit[23:16]	Bit[15:8]	Bit[7:0]
$0C_H$	000_H	00000_H		
$0B_H$	$03E8_H$	000_H		0_H
$0A_H$	00000000_H			
09_H	0000_H	0000_H		
08_H	55555555_H			
07_H	$AAAAAAAA_H$			
06_H	55555555_H			
05_H	$AAAAAAAA_H$			
04_H	55555555_H			
03_H	000_H	00000_H		
02_H	$F3_H$	$F2_H$	$F1_H$	$F0_H$
01_H	$F7_H$	$F6_H$	$F5_H$	$F4_H$
00_H	0065_H	$FFFF_H$		

Figure 10 EEPROM Delivery Content User Memory without CLO

UID Content (Block $0E_H$ and $0D_H$): content according to UID Description in chapter Memory Organization.

For product without enabled CLO function (NLM0010), the family code byte is set to $B1_H$.

For product with enabled CLO function (NLM0011), the family code byte is set to $B9_H$.

Service Data (Block 10_H and $0F_H$): content according to Service Data Description in chapter Memory Organization.

In block $0F_H$ the AFI byte is written by value 00_H for all NFC PWM series related products. All bits, which are reserved for future use, are written by value 0_B.

Block Lock Information (Block 11_H):

For the product with enabled CLO feature all blocks of the user data area are read- and write-able. For the product without CLO feature the blocks 01_H and 02_H are permanently locked .

The UID (blocks $0E_H$ and block $0D_H$) is locked. The blocks $0F_H$ and 10_H are locked as well.

The parameters PWM Period I_{max} (Block $0B_H$ Bit (30:16)) and Duty Cycle I_{max}(Block 00_HBit(31:16)) are initially programmed to 27,12kHz(value $03E8_H$) and 10 % (value 0065_H). The bit 31 of Block $0B_H$"FR" has to be programmed to 0_B(non inverting PWM output).

9 Constant Lumen Output (CLO) and Operating Time Counting (OTC)

Constant Lumen output control is only available in product NLM0011. Operating Time Counting (OTC) is available in products NLM0011 and NLM0010.

The purpose of the constant lumen output control (CLO) is, to compensate the aging of the LEDs in a lighting system. Usually the lighting strength of a LED degrades over the operating time. That results in the effect, that the emitted light becomes darker. This degradation of the LED can be compensated by increasing the LED current over lifetime according to a LED dependent aging function/model. Hence the NLM0011 chip has to adapt the LED current set point according to the aging function by changing the duty cycle of the PWM output.

The aging function of the LED is modeled by a linear model over time with eight reference points. The actual duty cycle as function of the actual operating time OTC has to be calculated by linear interpolation between two neighbored reference points. The principle is shown in the following image (for simplicity only 4 reference points out of 8 possible reference points are shown).

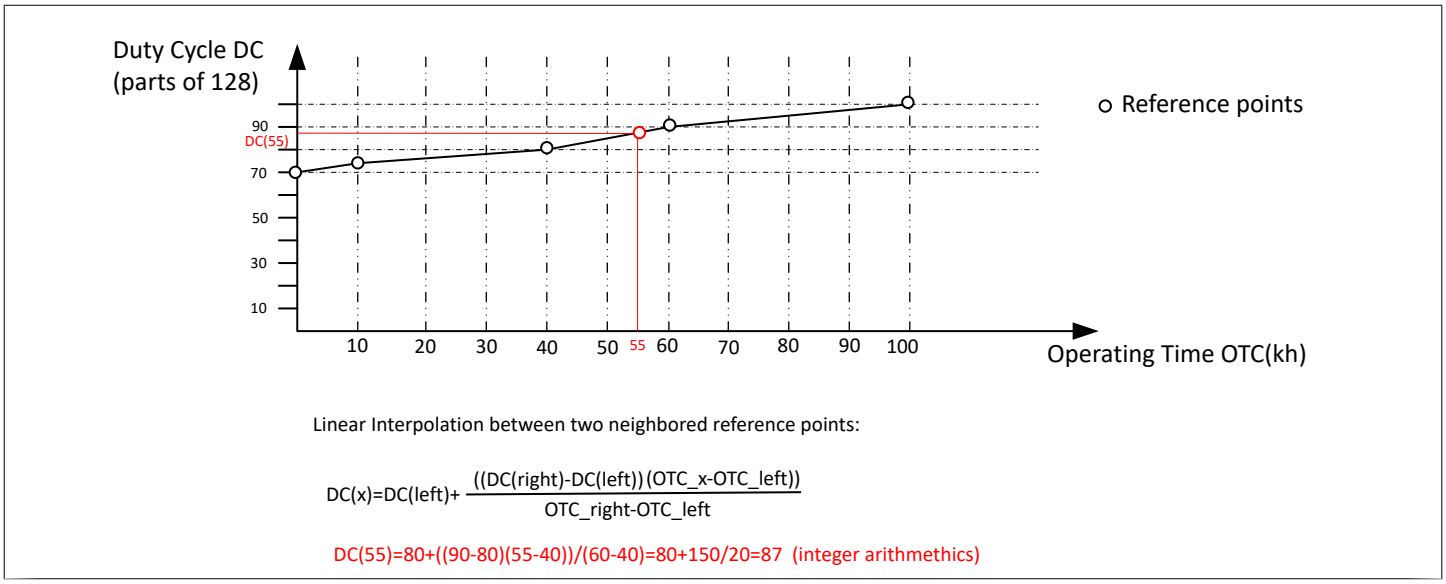


Figure 11 Constant Lumen Output Principle

A reference point is characterized by the lighting operation time and the belonging duty cycle of the PWM output, which defines the set point of the LED current. The reference point data have to be configured in the user memory area (blocks 02_H, 01_H and block 00_H Byte (1:0)). A reference point is represented by a 10-bit value, containing the operation time and the belonging target duty cycle information.

- A single reference value of operating time is stored in 4-bit format. Reference values for operating time are represented as multiples of 8192 (reference operating time in hours is equal to the 4-bit value of NVM multiplied by 8192). Hence the reference values for operating time cover the range from 0 h to 122880 h (in steps of multiples of 8192 hours).
- A single reference value of duty cycle is stored in 6-Bit format. The 6-Bit value represents the offset value of parts of 128 to 64/128. Hence the reference values for duty cycle cover a range from 64/128 (→ 50%) to 128/128(→ 100%).

The detailed memory layout for storing the CLO table is given as follows:

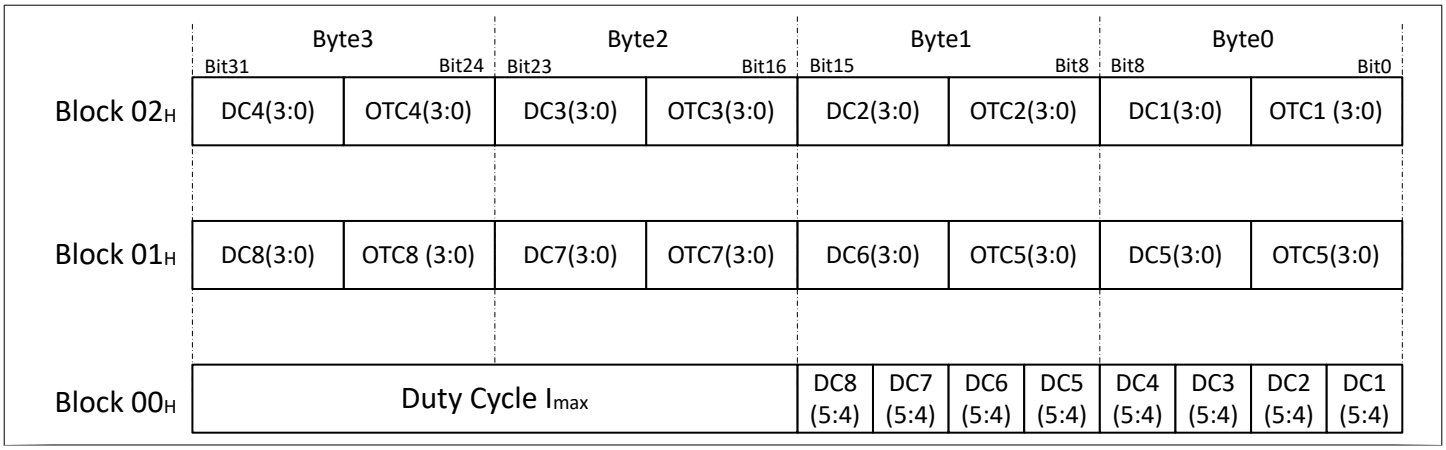


Figure 12 CLO Table Memory Layout

Example:The following example describes, how to calculate the 10-bit reference value of a particular reference point to be stored in the NVM. Let's assume a reference point at an operating time of 66000 hours and a target duty cycle of 82% of the duty cycle definition of I_{max} (value of block 00_H, Byte(3:2)):

- The 4-bit value of operating time OTC : → 66000/8192=8,06 → integer rounding 8 → 1000_B
- The 6-bit value of duty cycle:
  - Convert the given percentage value into parts of 128: → 82/100=X/128 → X=104,96 → integer rounding 105
  - Calculate the offset to 64 parts of 128: → 105-64=41 → 101001_B

The NLM0011/ NLM0010 chip is continuously counting the operation time and is continuously interpolating the resulting duty cycle. The interpolation result is then multiplied with the value of Duty Cycle I_{max} (value of block 00_H, Byte(3:2)) and this product is then divided by 128. This value is then used by the PWM generator and generates a PWM signal of frequency PWM period I_{Max} (value of block $0B_H$, Byte(3:2)) with the calculated duty cycle.

Monotonous falling CLO curves are supported in NLM0011 in chip version A14 (indicated by family code byte value $B9_H$).In order to enable a falling CLO curve the Bit "FR" (bit 31 of NVM block address $0B_H$) has to be programmed to value 1_B (for rising CLO curves the default 0_B has to be used. In case of falling CLO curve the covered CLO range is 64 parts of 128 down to 0 of duty cycle I_{max} (for rising CLO curve the covered range is 64 parts of 128 to 128 parts of 128 of duty cycle I_{max}).

The reference point duty cycle value for a falling CLO curve has to be entered as :

CLO reference point (falling curve) = 64 - *<desired value (0...64)>*

Example:

Table 10 CLO Duty Cycle Reference values

reference point number	desired value (parts of 128 of Duty Cycle I_{max})	CLO table value
Step 1	64	0
Step 2	56	8
Step 3	42	22
Step 4	31	33
Step 5	27	37
Step 6	19	45
Step 7	13	51
Step 8	3	61

Note: Only strict monotonous falling or rising CLO curves are supported.

The operation time is counted and the NVM value of operation time (block $0A_H$) is incremented/ updated every 4 hours. Hence the 16-bit value multiplied by four represents the operating time in hours. Once the value $FFFF_H$ is reached, the operating time counting stops and keeps the value $FFFF_H$. The current operating time is saved into the NVM with an accuracy of 30 seconds in case the external supply voltage V_{CC} is switched off . Here the remainder time with respect to the last regular 4 hours update is stored (hours and minutes).

Furthermore the number of power cycles is counted and stored in block 09_H (Byte(3:2)). The value is incremented, when external supply voltage V_{CC} is switched off.

In order to save the housekeeping data into the NVM in case of switching off the external supply, the chip integrates an under voltage lockout detection. An external capacitor on V_{CC} is required to provide the required energy for saving the housekeeping data in case of power off.

The NVM Memory layout of the OTC related content looks like:

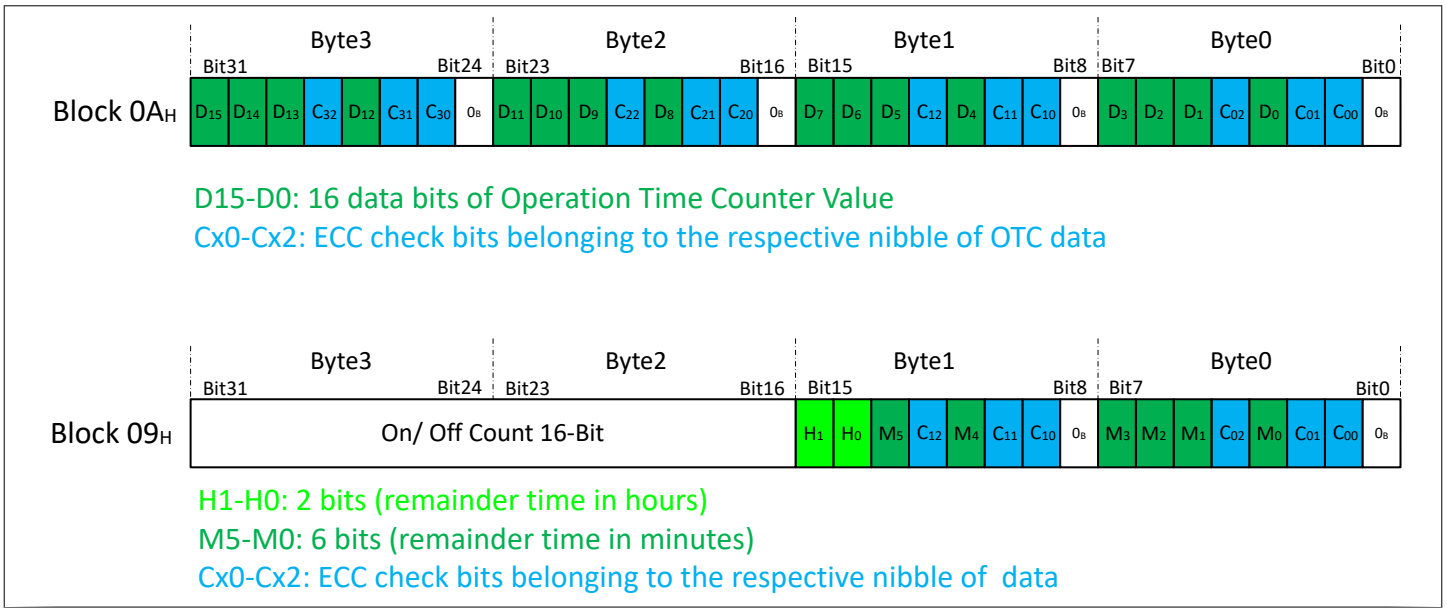


Figure 13 OTC related NVM content

Note: The OTC related content contains redundancy for error detection and correction (Bits C_{xx}). It is possible to detect and correct a single bit error per four data bits. In case the blocks $0A_H$ or 09_H are written by NFC the VCD has to calculate the respective ECC check bits and to assemble the block content.

10 PWM Overview

The NLM0011/NLM0010 is generating a pulse width modulated digital signal output. This PWM signal is characterized by its frequency , the duty cycle and the voltage swing.

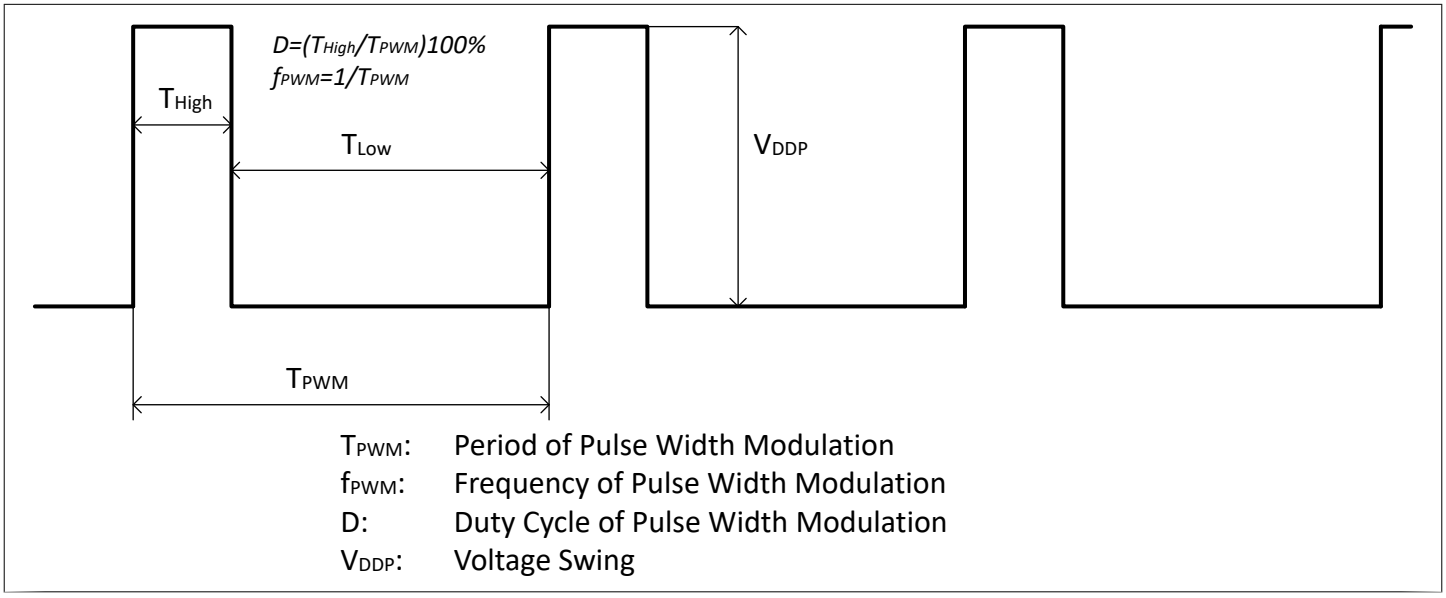


Figure 14 PWM Output Characteristics

The signal output is generated from an internal clock derived from an internal oscillator running at frequency of 27,12 MHz.

The length of period of the PWM signal T_{PWM} is derived from the content of NVM block $0B_H$ (Byte (3:2)). This 16-bit value represents the number of internal clock ticks, which are required to achieve the desired frequency.

Example: If a PWM frequency of 25kHz (→ Period of 40us) is desired, then the NVM value needs to be $043D_H$ (27120kHz/ 25kHz=1084,8 → rounded to 1085).

The maximum value of T_{High} is derived from the content of NVM block 00_H (Byte (3:2)). This 16-bit value represents the number of internal clock ticks, which are required to achieve the desired logical HIGH output time. It represents as well the value of 100% Duty Cycle according to the constant lumen output table.

Example: Referring to previous example: If a maximum duty cycle of 75% is desired, then the maximum high time is 30us. Hence the NVM value needs to be $032E_H$ (1085x0,75 = 813,75 → rounded to 814).

The constant lumen output calculation unit of the NLM0011 chip finally adapts this value according to the current interpolation result.

*Example: Referring to previous example: Lets assume the constant lumen output interpolation unit calculates a current duty cycle of 80% (or 102 parts of 128), then the effective current duty cycle will be 75*80%=60%.*

11 NLM0011/ NLM0010 Command Set

Description of NLM0011 Command Set

Error Codes

The following ISO/IEC 18000-3 mode 1 compliant error codes are implemented in the NLM0011/NLM0010:

Table 11 NLM0011 Error Codes

Error Code	Meaning
01_H	The command is not supported
$0F_H$	Error with no specific information given or a specific error code is not supported.
10_H	The specified block is not available (does not exist).
12_H	The specified block is locked and cannot be changed (read only).

Invalid frame length handling

If a command is sent to the NLM0011/ NLM0010 which has an invalid frame length no response is returned.

Flag handling

The NLM0011/NLM0010 ignores following flags. Commands are executed regardless of the state of these flag bits.

- Protocol Extension flag
- RFU flag
- Option flag (special meaning only for Stay quiet, Select, Reset to ready and Inventory command)

Command Set

The following command set is supported:

Table 12 NLM0011/NLM0010 Command Set

Available Commands	Command Type)**	Available Modes)**
Inventory	M	U
Stay quiet (state storage in state recovery)	M	A
Read single block	O	A/S/U
Write single block	O	A/S/U
Read Multiple Block	O	A/S/U
Select	O	A
Reset to ready	O	A/S/U
Write AFI	O	A/S/U
Lock AFI	O	A/S/U
Write Byte	C	A/S/U

)* M … Mandatory; O … Optional; C … Custom

)** A … Addressed; S … Selected; U … Unaddressed

Inventory (command code 01_H)

Implementation compliant to ISO/IEC 18000-3 mode 1.

Note:For a masked inventory the number of mask bytes has to correspond to the length defined in the mask length field.

StayQuiet (command code 02_H)

Implementation based on ISO/IEC 18000-3 mode 1.

Note:The NLM0011/NLM0010 responds after successful execution of the Stay Quiet command with set option_flag with an acknowledge. The NLM0011/NLM0010 also responds with an acknowledge if the chip is already in Quiet state.

Table 13 Response Format for Stay Quiet command with set option_flag

SOF	Flags	CRC	EOF
	00_H	16-Bit	

This feature can be used to ensure that the addressed chip really could be set to the Quiet state. If the reader does not detect an acknowledge it can be assumed that the addressed chip is not present.

ReadSingleBlock (command code 20_H)

Implementation compliant to ISO/IEC 18000-3 mode 1. Block $0F_H$ is read protected. Reading this block results in an error response with error code $0F_H$. Sending the ReadSingleBlock command with set option_flag results in the error code 01_H(command not supported).

WriteSingleBlock (command code 21_H)

Implementation compliant to ISO/IEC 18000-3 mode 1. The UID (block $0D_H$ and $0E_H$), the Service block (block 10_H), the AFI byte (block $0F_H$) cannot be written with the Write Single Block command. The NLM0011/NLM0010 returns the error code 12_H. Sending the WriteSingleBlock command with set option_flag results in the error code 01_H(command not supported).

ReadMultipleBlock (command code 23_H)

Implementation compliant to ISO/IEC 18000-3 mode 1. Block $0F_H$ is read protected. Reading this block results in an error response with error code $0F_H$. Sending the ReadMultipleBlock command with set option_flag results in the error code 01_H(command not supported).

Select (command code 25_H)

Implementation compliant to ISO/IEC 18000-3 mode 1. A chip already in selected state will reply an acknowledge response (response value 00_H) on a subsequent Select command.

ResetToReady (command code 26_H)

Implementation based on ISO/IEC 18000-3 mode 1.

Note:If the NLM0011/ NLM0010 is already in the Ready state, it will not respond to a subsequent ResetToReady command. With this feature a reader only detects chips in Quiet state and reset them to the Ready state.

If the chip is in Quiet state it will respond to an unaddressed ResetToReady command and set its state to Ready. If a chip is in the Selected state, it will move to the Ready state after a ResetToReady command. The ResetToReady command must be issued with set select_flag. If the ResetToReady is issued unaddressed or addressed, the chip will stay in Selected state and will not send a response as defined in ISO/IEC 18000-3 mode 1.

WriteAFI (command code 27_H)

Implementation compliant to ISO/IEC 18000-3 mode 1. Sending the WriteAFI command with set option_flag results in the error code 01_H (command not supported).

LockAFI (command code 28_H)

Implementation compliant to ISO/IEC 18000-3 mode 1. Sending the LockAFI command with set option_flag results in the error code 01_H (command not supported).

WriteByte (customcommand)

ISO-Command code = $A0_H$

NLM0011/ NLM0010 Embedded Command Code = 90_H

The Write Byte command writes the data of the specified byte. In the case of successful programming the chip sends back an acknowledge build up by 3 bytes. If access conditions are set to read only the chip returns the error code 12_H (write protected block). For any other error, error code $0F_H$ is returned.

Table 14 WriteByte Request Format

SOF	Flags	Command Code	Parameters	Data	CRC	EOF
	8-Bit	$A0_H$	05_H; [UID]	90_H ADDR0 00_H Byte 8-Bit	16-Bit	

Table 15 WriteByte Parameter Field

Code	Description	Comment
05_H	IC manufacturer code of Infineon	Mandatory
UID	UID for addressed command	mandatory for set Addressed flag, not included for Selected or Unaddressed command

Table 16 WriteByte Data Field

Code	Description	Comment
90_H	command code for WriteByte	
ADDR0	block address	address range 00_H ... $0C_H$ and 11_H
00_H	RFU	
Byte	byte address in block	address range 0_H ... 3_H; bit [7..2] are ignored and shall be set to '0'.
8-Bit	byte data to be written	

Response Format (no errors):

Table 17 WriteByte regular response

SOF	Flags	CRC	EOF
	00_H	16-Bit	

Response in case of Errors:

Table 18 WriteByte Error Response

SOF	Flags	Data	CRC	EOF
	01_H	Error Code)*	16-Bit	

)* The Error Code is defined according to ISO/IEC 18000-3 mode 1.

Note:The WriteByte command to block 11_H and to bytes 2 and 3 in block 10_H should be performed as "Read-Modify-Write" operation and in a secure environment .

As default the WriteByte command to the following memory location is not possible (write protected block):

- UID block $0D_H$
- UID block $0E_H$
- AFI block $0F_H$
- Service block 10_H, byte 0 and 1; for byte 2 refer to Memory Map description
- Additionally, service block 10_H, byte 3 can only be written if it is not locked by block 10_H bit (21:20).

12 NLM0011/ NLM0010 Electrical Characteristics

Absolute Maximum Ratings

Table 19 Absolute Maximum Ratings

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Input peak voltage between LA-LB	V_{Inpeak}			3.6	V_{Peak}	
Absolute Maximum Field Strength for indefinite exposure without damage. The chip functionality can be affected.	H_{absmax}			10	A/m	Conditions: $T_{joperating}$ = 110°C
Absolute Maximum Field Strength for exposure for up to 10 seconds without damage. The chip is not guaranteed to function	$H_{absmax12}$			12	A/m	Conditions: $T_{joperating}$ = 110°C
Input peak voltage at V_{CC}	V_{Peak}			5.5	V	
Storage Temperature	$T_{Storage}$	-40		150	°C	

Stresses above the maximum values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability, including EEPROM data retention and erase/write endurance. Maximum ratings are absolute ratings. Exceeding only one of these values may cause irreversible damage to the integrated circuit. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied.

Operational Conditions and Parameters

Table 20 Operational Conditions and Parameters

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
external supply voltage range	V_{CC}	3.0	3.3	5.5	V	
Operating field strength	H_{absmax}	0.15		5	A/m	According ISO/IEC 18000-3 mode 1
Nominal terminal voltage (between LA and LB)	V_{ACNOM}			2.95	V	

(table continues...)

Table 20 (continued) Operational Conditions and Parameters

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Ambient Temperature in lighting operational mode	T_{JL}	-40		105	°C	The ambient temperature is defined as the temperature of the surface of the package. Permanent operation at high temperature (ambient temperature above 90°C) could impact the product lifetime. In such case, please contract Infineon FAE to evaluate the application profile.
Ambient Temperature in NFC Configuration mode	T_{NFC}	-20		85	°C	The ambient temperature is defined as the temperature of the surface of the package.
Frequency of PWM output	f_{PWM}	0.9		40	kHz	measured between two rising edges
Duty Cycle of PWM output	D	0		100	%	$D=T_{High}/T_{PWM}$
Duty Cycle accuracy	D_{ACC}			0.1	%	
High Voltage of PWM Output	V_{DDP_H}	2.65	2.8	2.9	V	Test Condition: Load 10uA; 25°C
Low Voltage of PWM Output	V_{DDP_L}	0		0.2	V	Test Condition: Load 2mA; 25°C
Driving Strength of PWM Output	I_{PWM}			2	mA	
Power Consumption in Configuration Mode	P_{CM}			2	mW	Configuration Mode (NFC Operation and NVM read/write access)
Power Consumption in Lighting Operating Mode	P_{OM}		3.3	5.6	mW	Lighting Operation Mode (PWM Generation, CLO, operating time recording); V_{CC}=3.3V

(table continues...)

Table 20 (continued) Operational Conditions and Parameters

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Resonance Capacitance between terminals LA and LB	C_{chip}		23.5		pF	Conditions: T_A = 25°C, V_{LaLb}= 1.6Vrms
Startup Time in Operational lighting mode	$T_{Startup}$			15	ms	Time between V_{cc} present and first PWM pulse generated
ESD Hardness	V_{ESD}			2	kV	Human Body Model
EEPROM write/ erase cycles per block	W_{cycles}	100000				@T=85°C
EEPROM Data Retention	D_R	10			years	@T=25°C
EEPROM Failure Rate	FR_{EEPROM}			20000	dpm	@10 years Retention
V_{CC} capacitor	C_{VCC}	22			µF	

13 Package Outline

Applicable package

Product Package is PG-SOT23-5-1.

Package Drawing and Dimension

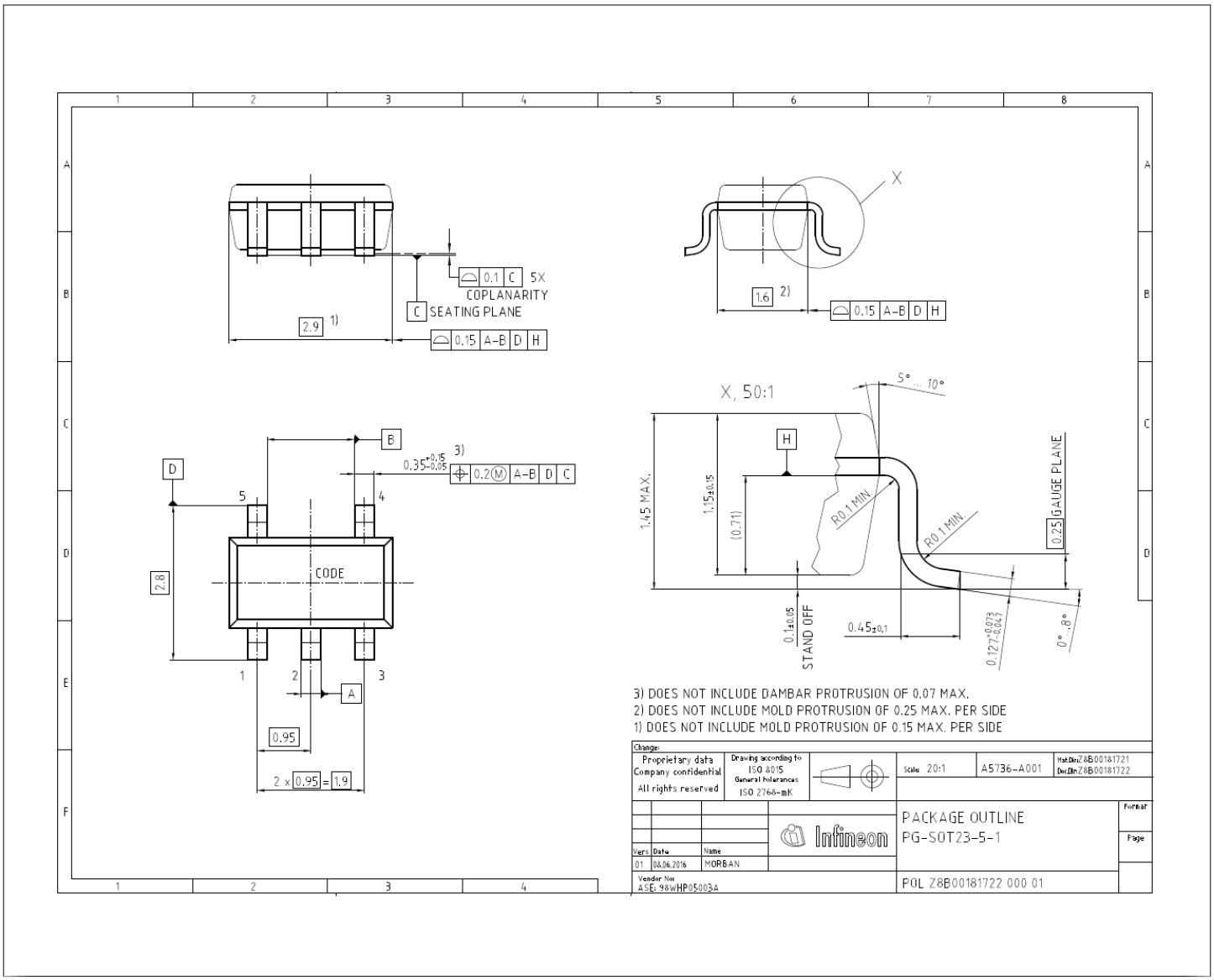


Figure 15 Package Outline PG-SOT23-5-1

Revision history

Document version	Date of release	Description of changes
1.2	11-09-2018	• added NLM0010 specific information
1.3	04-02-2019	• added Support of falling CLO curves
2.0	06-11-2019	• finalize electrical characteristics
2.1	03-09-2023	• added Support of ReadMultipleBlock command

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