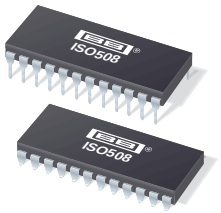
BURR-BROWN®



ISO508

For most current data sheet and other product information, visit www.burr-brown.com

Uni-Directional ISOLATED DIGITAL COUPLERS

FEATURES

- LOW POWER CONSUMPTION: < 12mW per Channel Typ.
- 1500Vrms ISOLATION: 100% Tested by Partial Discharge
- ASYNCHRONOUS OR SYNCHRONOUS OPERATION
- DOUBLE BUFFERED DESIGN FOR EASY INTEGRATION INTO BUS-BASED SYSTEMS
- TRI-STATE OUTPUTS
- 24-PIN PDIP OR GULL WING PACKAGES
- 2MWORDS/SEC TRANSFER RATE
- 1μSEC TRANSIENT RECOVERY

APPLICATIONS

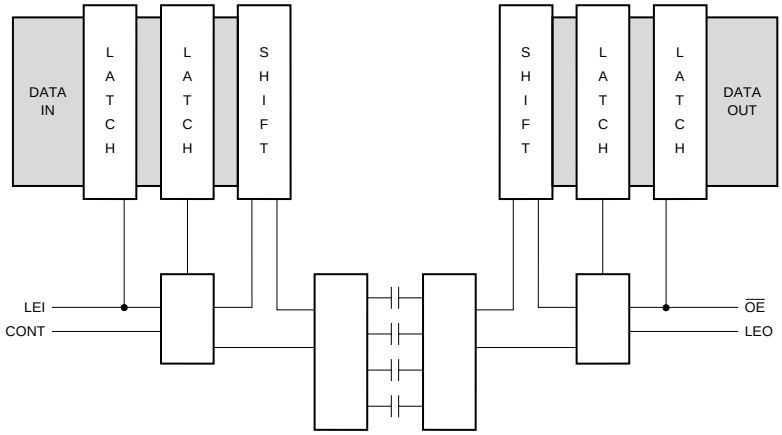
- PARALLEL ADCs/DACs
- DIGITAL INTERFACES
- DIGITAL TRANSMISSION
- GROUND-LOOP ISOLATION

DESCRIPTION

ISO508 is an 8-channel, isolated, digital coupler based on the Burr-Brown capacitive barrier technology. The ISO508 has additional circuitry to ensure DC accuracy and overcome the edge-sensitive nature of normal capacitive devices even on power-up conditions. The novel circuitry involved will restore the correct output after a transient interruption should that be necessary.

The ISO508 is designed with input and output buffers for ease of integration into a μP bus system. The output buffer has tri-state capability, and by the use of OE, the output data bus lines can be made to go high impedance. This feature of the ISO508, which allows multiple access to a data bus, requires extra circuitry when using an alternative solution.

ISO508 will transfer an 8-bit word at rates up to 2Mwords/s without the skew problems associated in implementing this function with optocouplers. The ISO508 is available in 24-pin PDIP or 24-pin Gull Wing packages. Both are specified for operation from –40°C to +85°C.



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Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

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SPECIFICATIONS

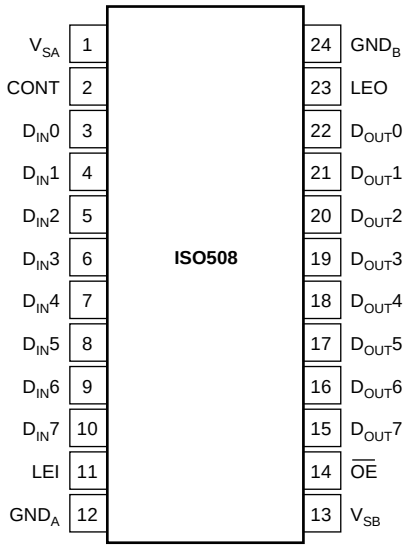
At T_A = +25°C, and V_S = +5V, unless otherwise noted.

PARAMETER		CONDITIONS	ISO508P, P-U MIN	ISO508P, P-U TYP	ISO508P, P-U MAX	UNITS
ISOLATION						
Rated Voltage, Continuous	V_{ISO}	50Hz, 60Hz	1500			V
Partial Discharge Voltage		1s, 5x5pC/cycle[1]	2500			V
Barrier Impedance				>10^{14}, 10		ΩpF
Leakage Current		240V, 60Hz		1		µA
		2500V, 50Hz			12	µA
Creepage Distance		PDIP = "P" Package		11		mm
Internal Isolation Distance		PDIP = "P" Package		0.1		mm
Transient Recovery Time		5kV/µs Edge			1	µs
DC CHARACTERISTICS						
High Level Input Voltage	V_{IH}	See Note 2	2			V
Low Level Input Voltage	V_{IL}	See Note 2			0.8	V
Input Pull-Down Current (Cont, $\overline{OE}$)	I_{PD}	V_{IN} = 5V	5		50	µA
Input Leakage Current	I_L	LEI, LEO, D0-7		1		nA
High Z Leakage Current	I_H			1		nA
Input Capacitance	C_{IN}			5		pF
High Level Output Voltage	V_{OH}	V_S = 4.4 - 4.5, I_{OH} = 6mA	V_S – 1			V
Low Level Output Voltage	V_{OL}	I_{OL} = 6mA			0.4	V
Output Short-Circuit Current	I_{OS}	1 second, max		30		mA
TIMING						
LE Width (LOW)	t_{WL}		50			ns
LE Width (HIGH)	t_{IL}		15			ns
Data Set-Up to LEI	t_{SU}	LEI HI to LO	0			ns
Data Hold from LEI	t_H	LEI HI to LO	20			ns
Propagation Delay	t_{PD}	Data In to Data Out (Cont)			1000	ns
		LEI LOW to Data Out (Sync)			520	ns
Data Output Delay	t_{DD}	LEO High to Data Out Change			35	ns
Output Rise and Fall Time	t_{OD}	10% to 90%, C_L = 50pF		9	14	ns
Output Enable	$t_{\overline{OE}}$	$\overline{OE}$ to Data Valid High or Low			35	ns
Output Disable	t_{DIS}	$\overline{OE}$ to Data Hi-Z			25	ns
Skew		Between any 2 Channels		5		ns
Max Data Transfer Rate (Sync)			2			Mw/s
(Cont)			1			Mw/s
POWER						
Supply Voltage	V_{SA}, V_{SB}	Either Side	4.5		5.5	V
Supply Current	I_{SA}	Transmit Side DC		5	10	mA
		Transmit Side DC Max Rate		7	15	mA
Supply Current	I_{SB}	Receive Side DC		8	12	mA
		Receive Side Max Rate		12	20	mA
TEMPERATURE RANGE						
Operating			–40		+85	°C
Storage			–40		+125	°C
Thermal Resistance, θ_{JA}				75		°C/W

NOTES: (1) All devices receive a 1s test. Failure criterion is 5 pulses of ≥ 5pC per cycle. (2) Logic inputs are HCT-type and thresholds are a function of power supply voltage with approximately 400mV hysteresis.

PIN CONFIGURATION

Top View **DIP**



ABSOLUTE MAXIMUM RATINGS

Supply Voltage: V_{SA}	–0.5V to +6V
V_{SB}	–0.5V to +6V
Maximum Input Current, any Input Pin	20mA
Continuous Isolation Voltage	1500Vrms
Storage Temperature	–40°C to +125°C
Lead Temperature (soldering, 10s)	+260°C

PACKAGE INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER(1)
ISO508P	24-Pin Plastic DIP	167
ISO508P-U	24-Pin Gull Wing Surface Mount	167-4

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

FUNCTIONAL DESCRIPTION

NAME	FUNCTION
D_{IN} (0 - 7)	Input Data Bus. Inputs are CMOS/TTL compatible.
D_{OUT} (0 - 7)	Output Data Bus. Outputs are TTL compatible.
LEI	Input Latch Enable. Latch enable signal for the input data buffer. A logic LOW will latch the input data preventing further changes being made before data transmission across the barrier, and transmit if in synchronous mode. A logic HIGH will allow the data to pass from the input pins to the input buffer.
LEO	Output Latch Enable. Latch enable signal for the output data buffer. A logic LOW will latch the internal data to the output pins and prevent further changes to the output data. A logic HIGH will allow the internal data to be passed to the output pins as soon as it becomes available.
CONT	Synchronous/Asynchronous Mode Select. A logic HIGH selects asynchronous mode. A logic LOW selects synchronous mode.
$\overline{OE}$	Output Tri-State Enable. Makes the output data pins high impedance to allow multiple parallel access to the data bus. A logic HIGH will make D_{OUT} (0 - 7) high impedance. A logic LOW will allow D_{OUT} (0 - 7) to be driven to the correct logic level.

ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

OPERATION

ISO508 has two modes of operation: synchronous and asynchronous. The mode is selected by the CONT pin. CONT held low selects synchronous operation while CONT held high will select asynchronous operation. In synchronous mode the user has control of the time at which the data is transmitted across the barrier, while in asynchronous mode the data is continually transmitted across the barrier under the internal logic control. The input latches and output latches are level sensitive.

SYNCHRONOUS MODE

With CONT held low, the input data is transmitted across the barrier under the control of LEI. When LEI is held low, no data is passed to the input buffer and no barrier transmission takes place. When LEI goes high, data is transferred to the input buffer. On the falling edge of LEI the data is then transmitted across the barrier.

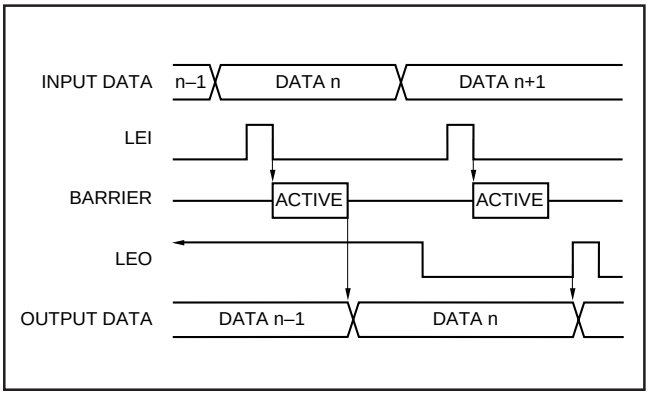


FIGURE 1. Data Transfer—Synchronous Mode.

If LEI is taken high when transmission is in progress, the input data is recaptured in the input buffer without interfering with the transmitting data. If LEI then goes low while transmission is still in progress the current transmission will be terminated and restarted with the new data. The last full data transmission will not be affected.

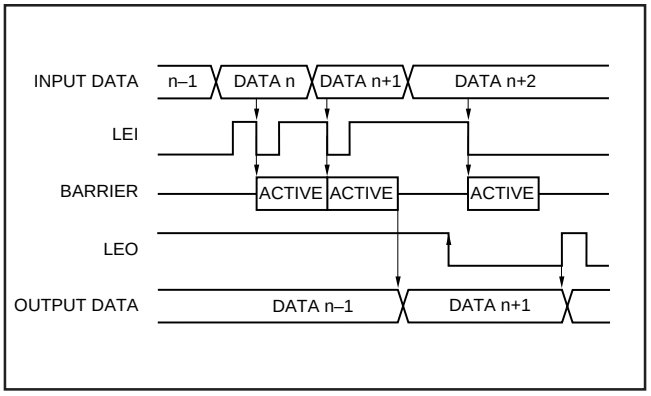


FIGURE 2. Data Transfer—Synchronous Mode Restart.

The output data changes under the control of LEO. If LEO is high at the end of a transmission, the output data will change immediately the transmission is complete. If LEO is low at the end of transmission, the output data will change when LEO goes high. In both cases all data bits will change together guaranteeing the specified skew performance. Transmitted data can be ignored selectively, if desired, by maintaining LEO low until the desired data is available.

ASYNCHRONOUS MODE

When CONT is held high, the internal transmission circuit is in control and will initiate data transmission asynchronously at 1MWords/s i.e., 1Mbps on each of the 8 channels.

The asynchronous mode runs continuously under the internal controls. LEI can serve as an input data latch, but will not control the data transmission across the barrier. As in the synchronous mode, LEI and LEO can be used to select of ignore input or output data respectively.

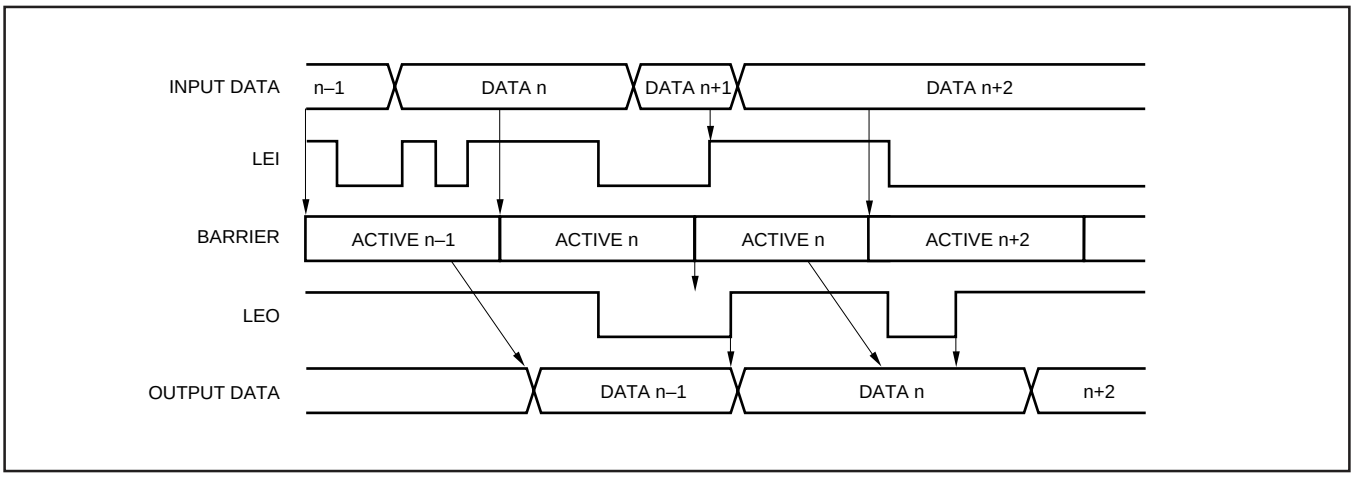


FIGURE 3. Data Transfer—Asynchronous Mode.

DATA CORRUPTION

In either synchronous or asynchronous mode if the data is upset by a transient the complete transmission is invalid. However, in asynchronous mode the data is being sent continuously and will therefore correct the corrupted information within a maximum of 1µs. In synchronous mode, data transfer is under the control of the user, and retransmission would be required by the software.

DATA TRANSMISSION AND JITTER

Because the internal 20MHz clock is free-running, two "jitter" conditions are possible. In synchronous mode when LEI goes low data will be transmitted (clocked) across the barrier. Depending on when LEI goes low, in relation to the internal clock cycle, will determine the "jitter" between successive input data transfers. This can be maximum of 50ns.

In asynchronous mode the input data is transferred by the internal clock and logic control, i.e., 2 sync. Clock cycles., (S_0, and S_1), 8 data clock cycles. Depending on when the input data is presented, in relation to the start of the data block transmission, will determine the "jitter" between successive input data transfers. This can be maximum of 500ns.

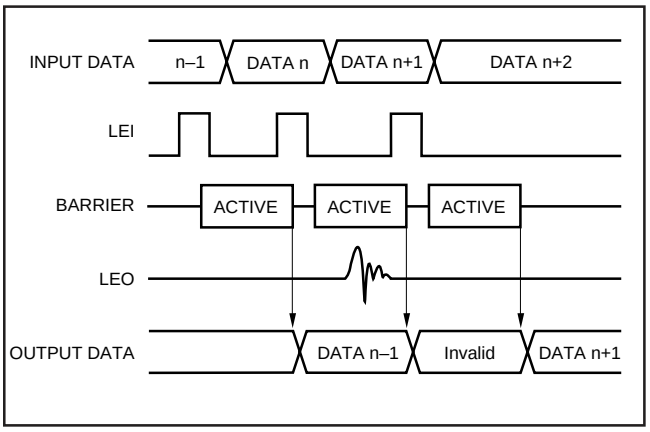


FIGURE 4. Data Corruption.

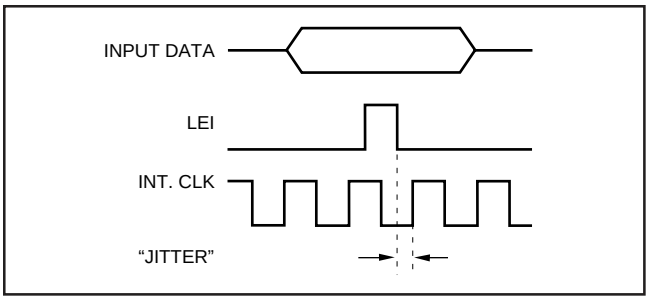


FIGURE 5. Jitter in Synchronous Mode.

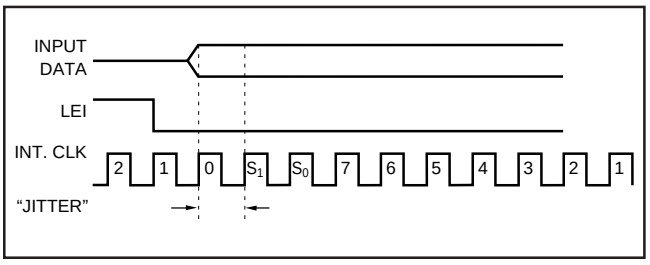


FIGURE 6. Jitter in Asynchronous Mode.

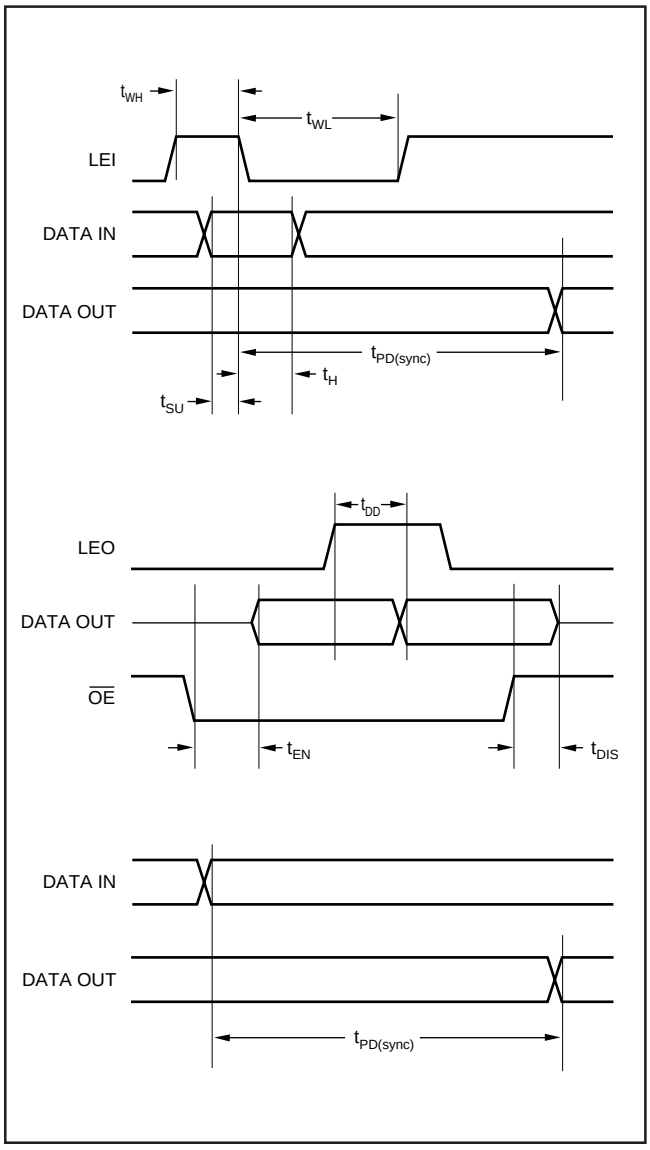


FIGURE 7. Timing Diagrams.

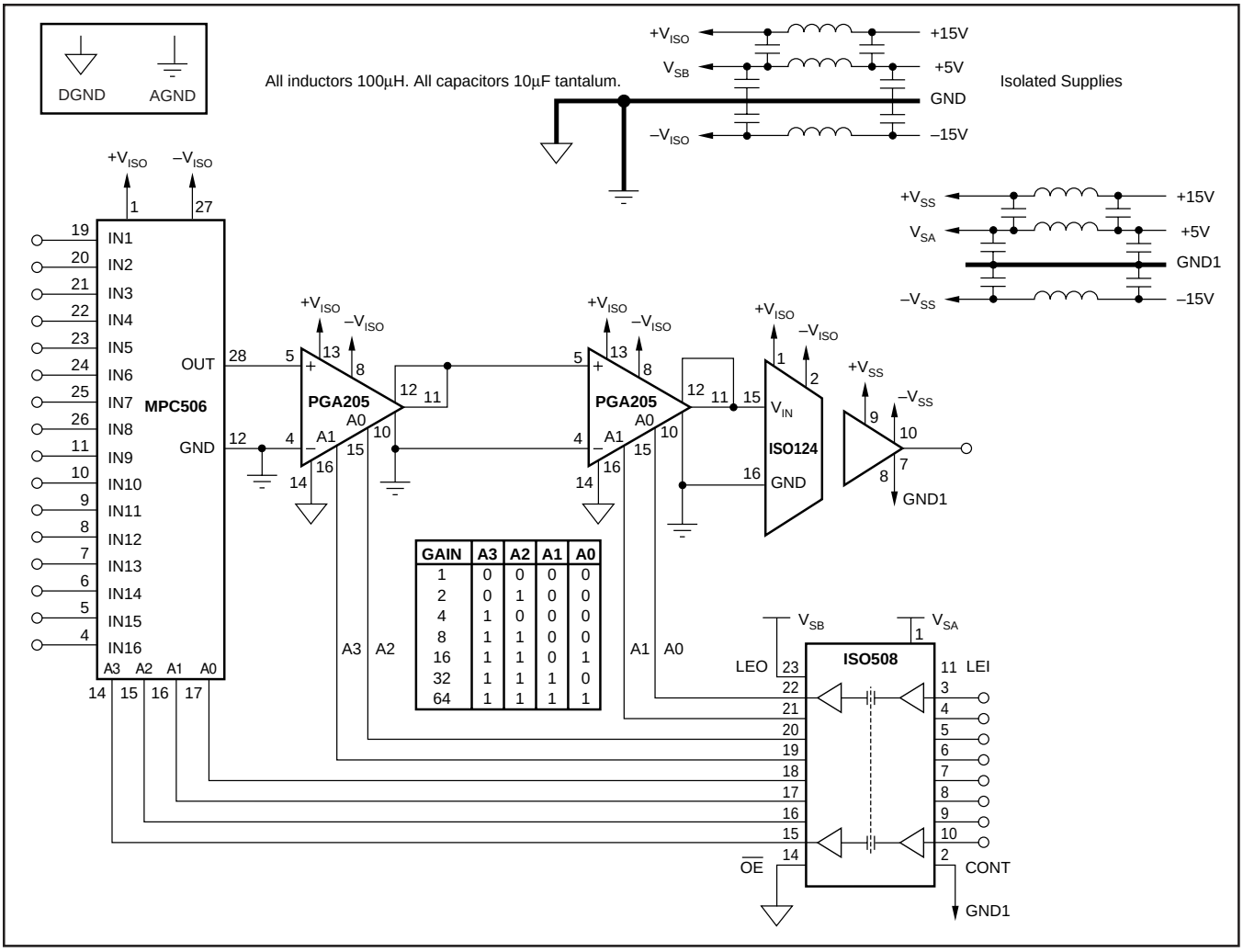


FIGURE 8. Isolated 16-Channel Variable Gain DAS.

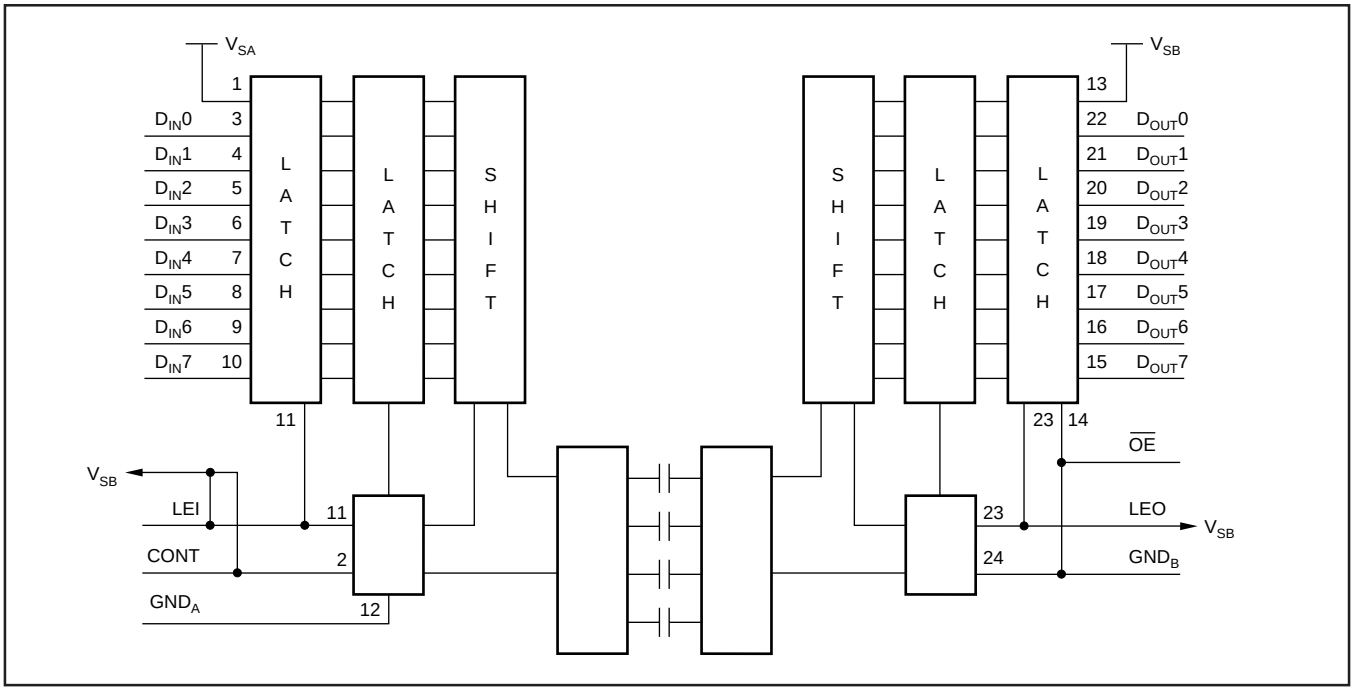


FIGURE 9. Isolated 8-Channel Output Bus (Asynchronous Operation).

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