

# 74AHCT17A

Hex buffer Schmitt trigger

Rev. 2 — 7 August 2023

Product data sheet

## 1. General description

The 74AHCT17A is a hex buffer with Schmitt-trigger inputs, capable of transforming slowly changing input signals into sharply defined, jitter-free output signals.

Designed to operate over a  $V_{CC}$  range from 4.5 V to 5.5 V, the inputs are TTL compatible. This range allows the device to be used to translate from 3.3 V to 5 V.

This device is fully specified for partial Power-down applications using  $I_{OFF}$ . The  $I_{OFF}$  circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

## 2. Features and benefits

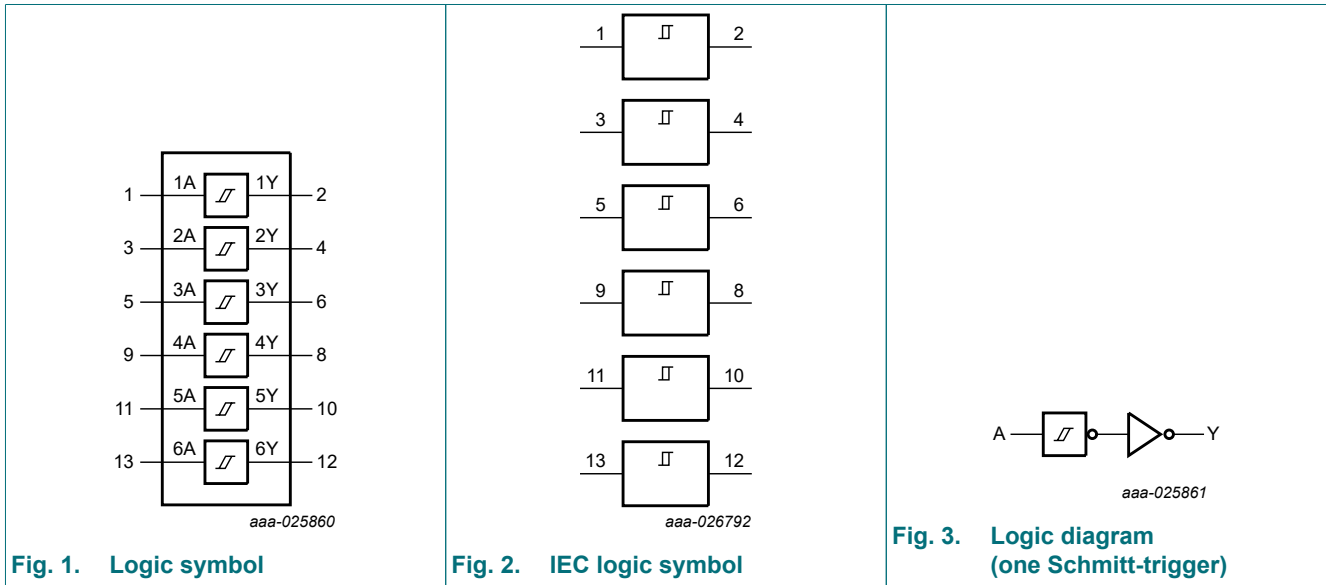
- Direct interface with TTL levels
- Supply voltage range from 4.5 V to 5.5 V
- Typical  $t_{pd}$  of 3.2 ns at 5 V
- Typical  $V_{OL(p)} < 0.8$  V at  $V_{CC} = 5$  V,  $T_{amb} = 25$  °C
- Typical  $V_{OH(v)} > 2.3$  V at  $V_{CC} = 5$  V,  $T_{amb} = 25$  °C
- Supports mixed-mode voltage operation on all ports
- $I_{OFF}$  circuitry provides partial Power-down mode operation
- Latch-up performance exceeds 250 mA per JESD 78 Class II
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 3000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 2000 V
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

## 3. Ordering information

Table 1. Ordering information

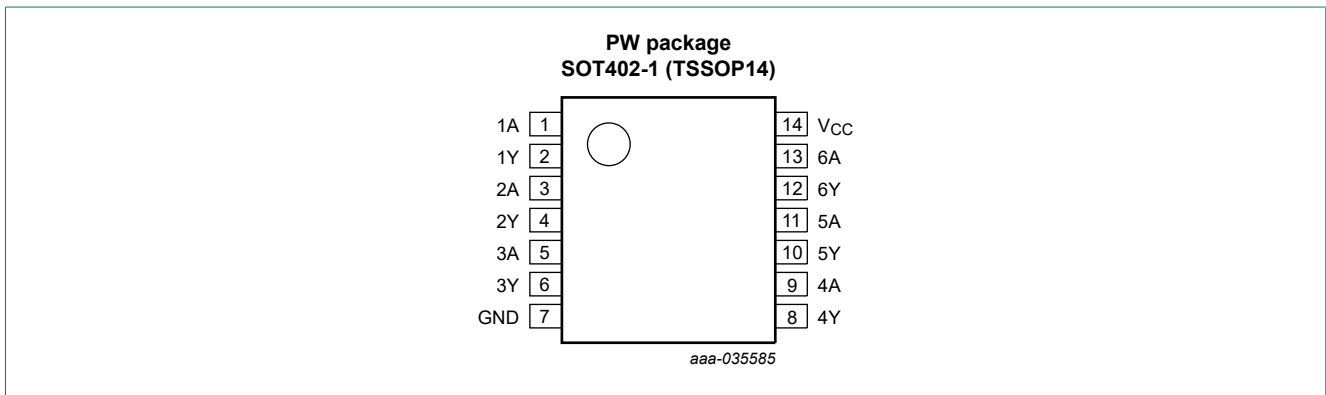
Type number	Package			Version
	Temperature range	Name	Description	
<a href="#">74AHCT17APW</a>	-40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	<a href="#">SOT402-1</a>

### 4. Functional diagram



### 5. Pinning information

#### 5.1. Pinning



#### 5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1A, 2A, 3A, 4A, 5A, 6A	1, 3, 5, 9, 11, 13	data input
1Y, 2Y, 3Y, 4Y, 5Y, 6Y	2, 4, 6, 8, 10, 12	data output
GND	7	ground (0 V)
V <sub>CC</sub>	14	supply voltage

## 6. Functional description

**Table 3. Function table**

*H = HIGH voltage level; L = LOW voltage level.*

Input	Output
nA	nY
L	L
H	H

## 7. Limiting values

**Table 4. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).*

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+7.0	V
$V_I$	input voltage	[1]	-0.5	+7.0	V
$V_O$	output voltage	output HIGH or LOW state	[2][3]	$V_{CC} + 0.5$	V
		output power-down	[2]	+7.0	V
$I_{IK}$	input clamping current	$V_I < 0$ V	-20	-	mA
$I_{OK}$	output clamping current	$V_O < 0$ V	-20	-	mA
$I_O$	output current	$V_O = 0$ V to $V_{CC}$	-	$\pm 25$	mA
$I_{CC}$	supply current		-	75	mA
$I_{GND}$	ground current		-75	-	mA
$T_{stg}$	storage temperature		-65	+150	°C
$P_{tot}$	total power dissipation	$T_{amb} = -40$ °C to +125 °C [4]	-	500	mW

[1] If the input current ratings are observed, the minimum input voltage ratings may be exceeded.

[2] If the output current ratings are observed, the output voltage ratings may be exceeded.

[3] This value is limited to 7 V maximum.

[4] For SOT402-1 (TSSOP14) package:  $P_{tot}$  derates linearly with 7.3 mW/K above 81 °C.

## 8. Recommended operating conditions

**Table 5. Recommended operating conditions**

*Voltages are referenced to GND (ground = 0 V).*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{CC}$	supply voltage		4.5	5.0	5.5	V
$V_I$	input voltage		0	-	5.5	V
$V_O$	output voltage	output HIGH or LOW state	0	-	$V_{CC}$	V
		output power-down	0	-	5.5	V
$T_{amb}$	ambient temperature		-40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 5.0$ V $\pm$ 0.5 V	-	-	1	ms/V

## 9. Static characteristics

**Table 6. Static characteristics**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
V <sub>T+</sub>	positive-going threshold voltage	V <sub>CC</sub> = 4.5 V	-	-	1.9	-	1.9	-	1.9	V
		V <sub>CC</sub> = 5.5 V	-	-	2.1	-	2.1	-	2.1	V
V <sub>T-</sub>	negative-going threshold voltage	V <sub>CC</sub> = 4.5 V	0.5	-	-	0.5	-	0.5	-	V
		V <sub>CC</sub> = 5.5 V	0.6	-	-	0.6	-	0.6	-	V
V <sub>H</sub>	hysteresis voltage	V <sub>CC</sub> = 4.5 V	0.4	-	1.4	0.4	1.4	0.4	1.4	V
		V <sub>CC</sub> = 5.5 V	0.4	-	1.5	0.4	1.5	0.4	1.5	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>CC</sub> = 4.5 V								
		I <sub>O</sub> = -50 μA	4.4	-	-	4.4	-	4.4	-	V
		I <sub>O</sub> = -8 mA	3.94	-	-	3.8	-	3.7	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>CC</sub> = 4.5 V								
		I <sub>O</sub> = 50 μA	-	-	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 8 mA	-	-	0.36	-	0.44	-	0.55	V
I <sub>OFF</sub>	power-off leakage current	V <sub>I</sub> or V <sub>O</sub> = GND to 5.5 V; V <sub>CC</sub> = 0 V	-	-	0.5	-	5	-	5	μA
I <sub>I</sub>	input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND; V <sub>CC</sub> = 0 V to 5.5 V	-	-	±0.1	-	±1	-	±1	μA
I <sub>CC</sub>	supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 5.5 V	-	-	2	-	20	-	20	μA
ΔI <sub>CC</sub>	additional supply current	per input pin; V <sub>CC</sub> = 5.5 V; V <sub>I</sub> = 3.4 V; I <sub>O</sub> = 0 A; other pins at V <sub>CC</sub> or GND	-	-	1.35	-	1.5	-	1.5	mA

9.1. Transfer characteristics waveforms

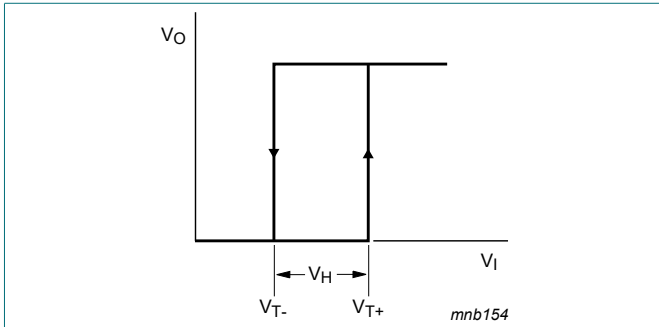


Fig. 4. Transfer characteristics

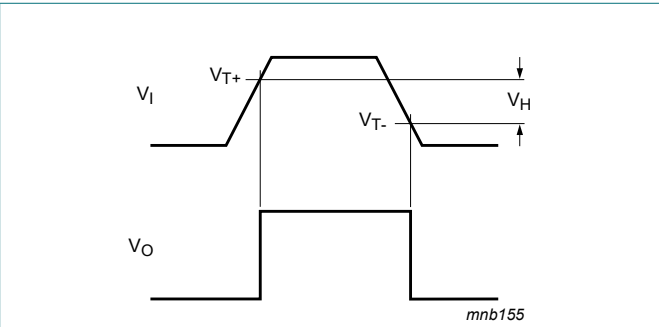
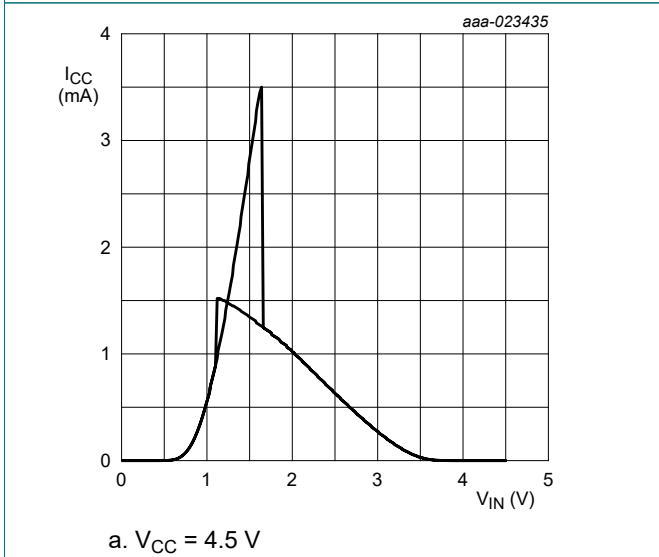
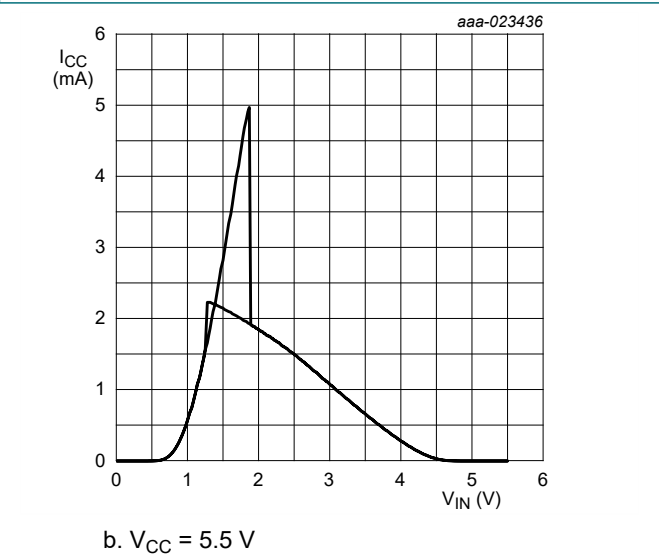


Fig. 5. Transfer characteristics definitions



a.  $V_{CC} = 4.5 \text{ V}$



b.  $V_{CC} = 5.5 \text{ V}$

Fig. 6. Typical transfer characteristics

## 10. Dynamic characteristics

**Table 7. Dynamic characteristics**

$GND = 0\text{ V}$ . For test circuit, see Fig. 8.

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	Min	Max	
$t_{pd}$	propagation delay	$nA$ to $nY$ ; see Fig. 7 [2]								
		$V_{CC} = 4.5\text{ V}$ to $5.5\text{ V}$								
		$C_L = 15\text{ pF}$	-	3.2	8.3	1	9.9	1	10.6	ns
		$C_L = 50\text{ pF}$	-	5.0	9.8	1	11.3	1	12.1	ns
$C_I$	input capacitance	$V_I = V_{CC}$ or $GND$ ; $V_{CC} = 5\text{ V}$	-	2	6	-	6	-	6	pF
$C_O$	output capacitance	$V_O = V_{CC}$ or $GND$ ; $V_{CC} = 5\text{ V}$	-	5	-	-	-	-	-	pF
$C_{PD}$	power dissipation capacitance	per buffer; $C_L = 0\text{ pF}$ ; $f = 10\text{ MHz}$ ; $V_I = GND$ to $V_{CC}$ [3]	-	9.8	-	-	-	-	-	pF

[1] Typical values are measured at  $T_{amb} = 25\text{ °C}$  and  $V_{CC} = 5\text{ V}$ .

[2]  $t_{pd}$  is the same as  $t_{PLH}$  and  $t_{PHL}$ .

[3]  $C_{PD}$  is used to determine the dynamic power dissipation  $P_D$  ( $\mu\text{W}$ ).

$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$  where:

$f_i$  = input frequency in MHz;

$f_o$  = output frequency in MHz;

$C_L$  = output load capacitance in pF;

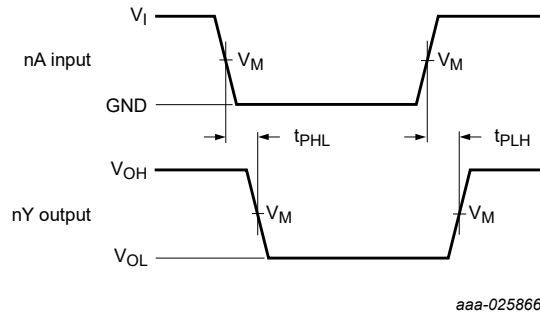
$V_{CC}$  = supply voltage in Volts.

**Table 8. Noise characteristics**

$GND = 0\text{ V}$ . For test circuit, see Fig. 8.

Symbol	Parameter	Conditions	$T_{amb} = 25\text{ °C}$			Unit
			Min	Typ	Max	
<b><math>V_{CC} = 5\text{ V}</math>; <math>C_L = 50\text{ pF}</math></b>						
$V_{OL(p)}$	LOW-level output voltage (peak)		-	0.4	0.8	V
$V_{OL(v)}$	LOW-level output voltage (valley)		-0.8	-0.2	-	V
$V_{OH(v)}$	HIGH-level output voltage (valley)		-	4.5	-	V
$V_{IH(AC)}$	AC HIGH-level input voltage		2	-	-	V
$V_{IL(AC)}$	AC LOW-level input voltage		-	-	0.8	V

10.1. Waveforms and test circuit

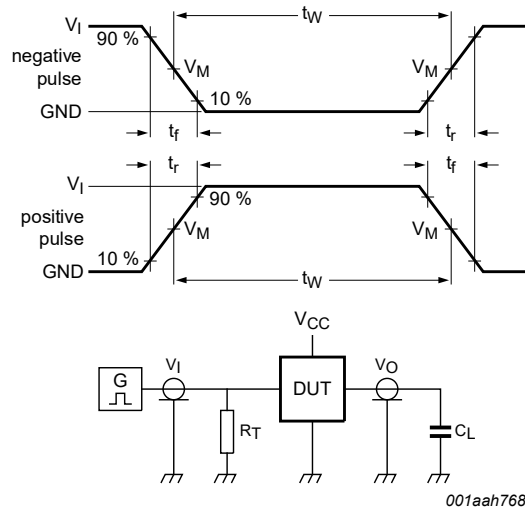


Measurement points are given in [Table 9](#).  
 $V_{OL}$  and  $V_{OH}$  are typical voltage output levels that occur with the output load.

Fig. 7. Propagation delay input (nA) to output (nY)

Table 9. Measurement points

Input	Output
$V_M$	$V_M$
1.5 V	$0.5V_{CC}$



Test data is given in [Table 10](#).  
 Definitions test circuit:  
 $R_T$  = Termination resistance should be equal to output impedance  $Z_o$  of the pulse generator;  
 $C_L$  = Load capacitance including jig and probe capacitance.

Fig. 8. Test circuit for measuring switching times

Table 10. Test data

Input	Load	Test
$V_I$	$C_L$	$t_{PLH}, t_{PHL}$
GND to 3 V	15 pF, 50 pF	

### 11. Package outline

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1

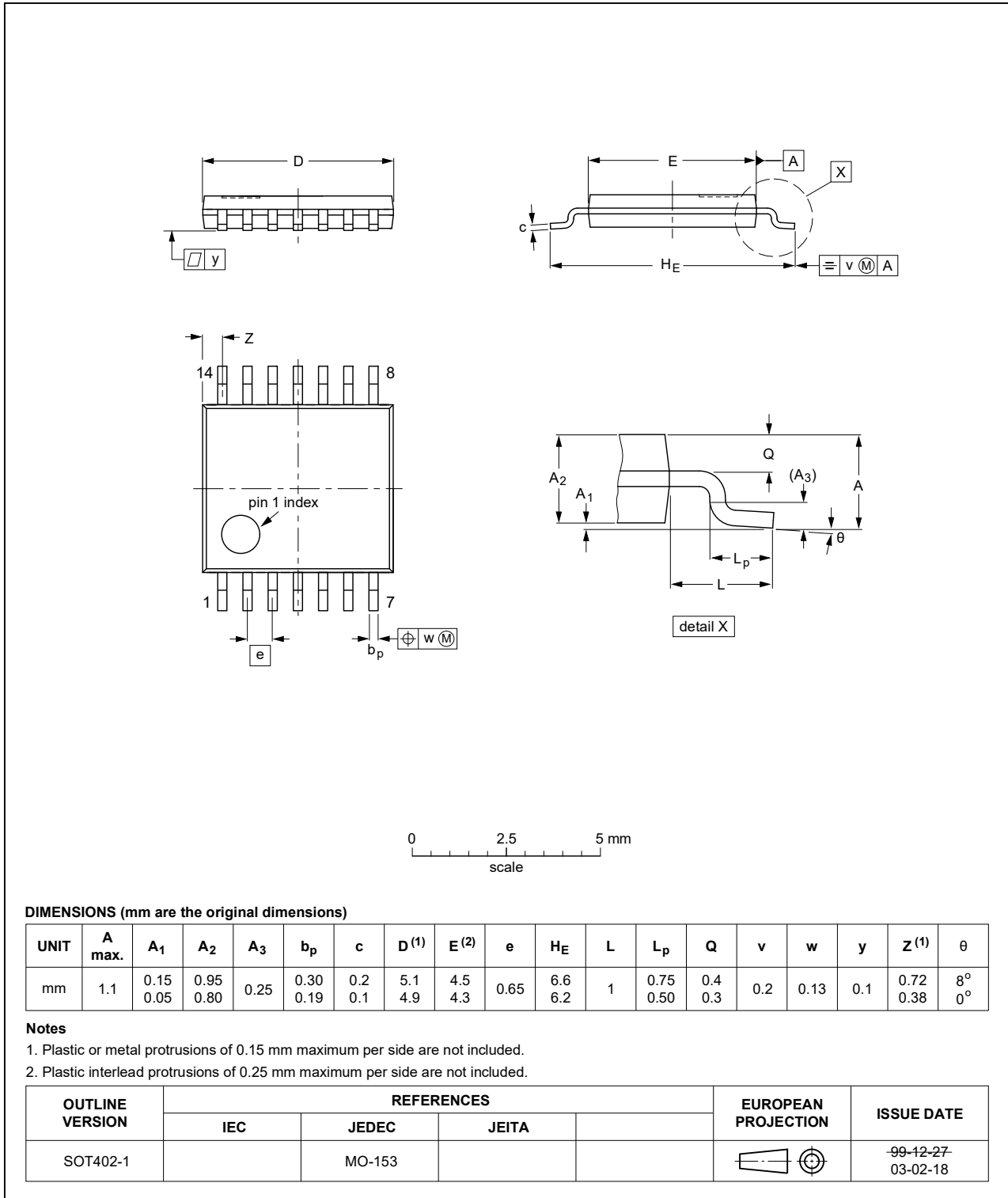


Fig. 9. Package outline SOT402-1 (TSSOP14)



## 12. Abbreviations

Table 11. Abbreviations

Acronym	Description
CDM	Charge Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
TTL	Transistor-Transistor Logic

## 13. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AHCT17A v.2	20230807	Product data sheet	-	74AHCT17A v.1
Modifications:	<ul style="list-style-type: none"> <li><a href="#">Section 2</a>: ESD specification updated according to the latest JEDEC standard.</li> <li><a href="#">Section 7</a>: Derating values for <math>P_{tot}</math> total power dissipation updated.</li> </ul>			
74AHCT17A v.1	20170518	Product data sheet	-	-

## 14. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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