FAIRCHILD SEMICONDUCTOR®

April 2010

FAN7930
Critical Conduction Mode PFC Controller

Features

- PFC Ready Signal
- Input Voltage Absent Detection Circuit
- Maximum Switching Frequency Limitation
- Internal Soft-Start and Startup without Overshoot
- Internal Total Harmonic Distortion (THD) Optimizer
- Precise Adjustable Output Over-Voltage Protection
- Open-Feedback Protection and Disable Function
- Zero Current Detector
- 150μs Internal Startup Timer
- MOSFET Over-Current Protection
- Under-Voltage Lockout with 3.5V Hysteresis
- Low Startup and Operating Current
- Totem-Pole Output with High State Clamp
- +500/-800mA Peak Gate Drive Current
- 8-Pin SOP

Applications

- Adapter
- Ballast
- LCD TV, CRT TV
- SMPS

Description

The FAN7930 is an active power factor correction (PFC) controller for boost PFC applications that operate in critical conduction mode (CRM). It uses a voltage-mode PWM that compares an internal ramp signal with the error amplifier output to generate a MOSFET turn-off signal. Because the voltage-mode CRM PFC controller does not need rectified AC line voltage information, it saves the power loss of an input voltage sensing network necessary for a current-mode CRM PFC controller.

FAN7930 provides over-voltage protection, open-feedback protection, over-current protection, input-voltage-absent detection, and under-voltage lockout protection. The PFC-ready pin can be used to trigger other power stages when PFC output voltage reaches the proper level with hysteresis. The FAN7930 can be disabled if the INV pin voltage is lower than 0.45V and the operating current decreases to a very low level. Using a new variable on-time control method, THD is lower than the conventional CRM boost PFC ICs.

Related Resources

AN-8035 — Design Consideration for Boundary Conduction Mode PFC Using FAN7930

Ordering Information

Part Number	Operating Temperature Range	Top Mark	Package	Packing Method
FAN7930M	-40 to +125°C	FAN7930	8-Lead Small Outline Package (SOP)	Rail
FAN7930MX				Tape & Reel

Application Diagram

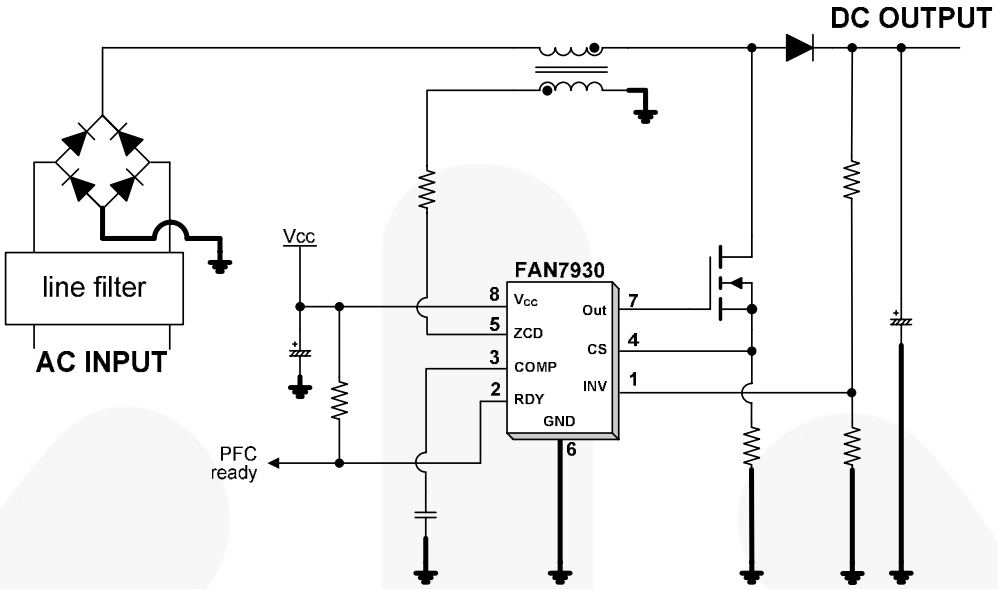

Figure 1. Typical Boost PFC Application

Internal Block Diagram

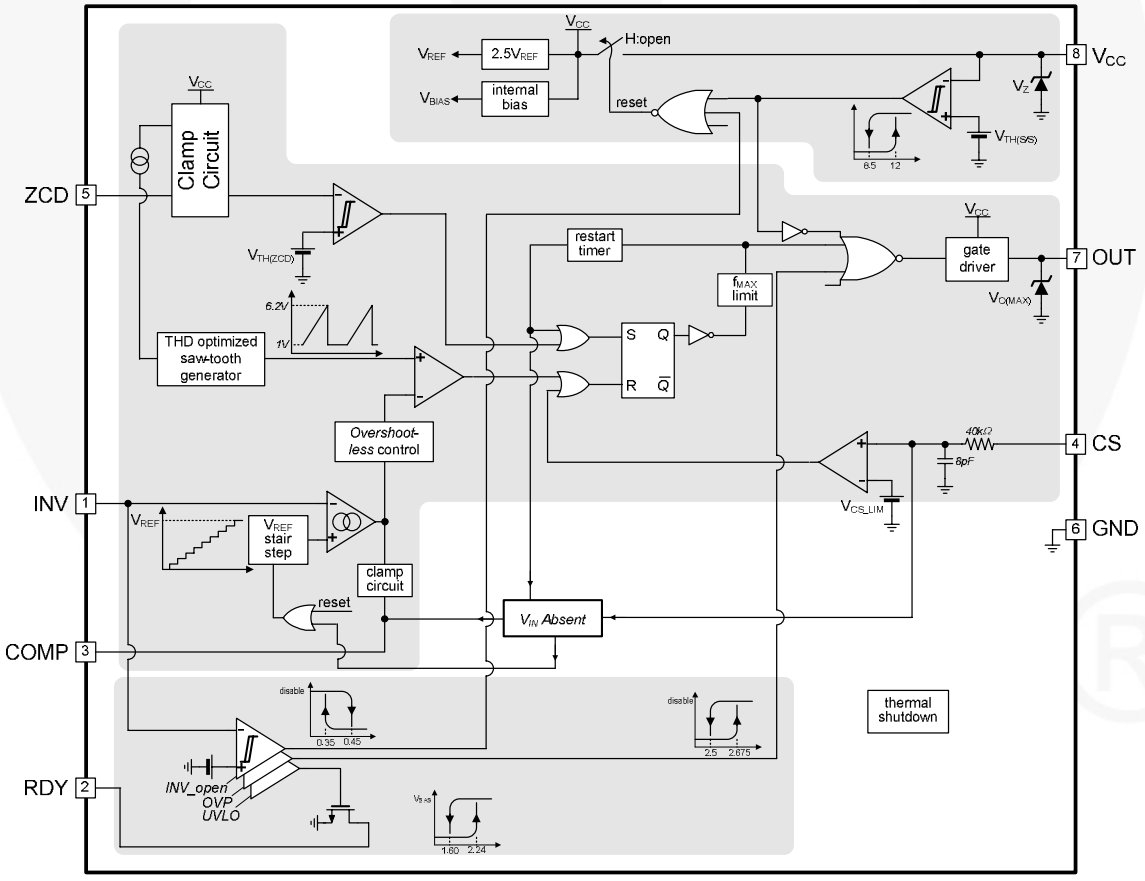

Figure 2. Functional Block Diagram

Pin Configuration

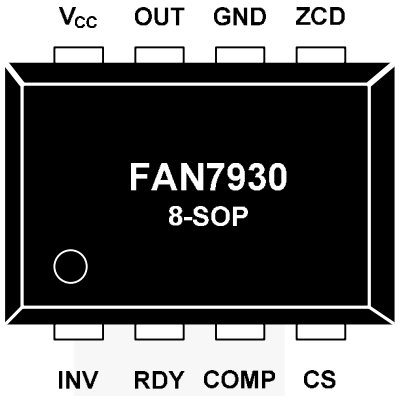

Figure 3. Pin Configuration (Top View)

Pin Definitions

Pin #	Name	Description
1	INV	This pin is the inverting input of the error amplifier. The output voltage of the boost PFC converter should be resistively divided to 2.5V.
2	RDY	This pin is used to detect PFC output voltage reaching a pre-determined value. When output voltage reaches 89% of rated output voltage, this pin is pulled HIGH, which is an (open drain) output type.
3	COMP	This pin is the output of the transconductance error amplifier. Components for the output voltage compensation should be connected between this pin and GND.
4	CS	This pin is the input of the over-current protection comparator. The MOSFET current is sensed using a sensing resistor and the resulting voltage is applied to this pin. An internal RC filter is included to filter switching noise.
5	ZCD	This pin is the input of the zero-current detection block. If the voltage of this pin goes higher than 1.5V, then goes lower than 1.4V, the MOSFET is turned on.
6	GND	This pin is used for the ground potential of all the pins. For proper operation, the signal ground and the power ground should be separated.
7	OUT	This pin is the gate drive output. The peak sourcing and sinking current levels are +500mA and -800mA, respectively. For proper operation, the stray inductance in the gate driving path must be minimized.
8	V_{CC}	This is the IC supply pin. IC current and MOSFET drive current are supplied using this pin.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{CC}	Supply Voltage			V_Z	V
I_{OH}, I_{OL}	Peak Drive Output Current		-800	+500	mA
I_{CLAMP}	Driver Output Clamping Diodes V_O>V_{CC} or V_O<-0.3V		-10	+10	mA
I_{DET}	Detector Clamping Diodes		-10	+10	mA
V_{IN}	Error Amplifier Input, Output, ZCD and RDY Pin(1)		-0.3	8.0	V
	CS Input Voltage(2)		-10.0	6.0	
T_J	Operating Junction Temperature			+150	°C
T_A	Operating Temperature Range		-40	+125	°C
T_{STG}	Storage Temperature Range		-65	+150	°C
ESD	Electrostatic Discharge Capability	Human Body Model, JESD22-A114		2.5	kV
		Charged Device Model, JESD22-C101		2.0	

Notes:
1. When this pin is supplied by external power sources by accident, its maximum allowable current is 50mA.
2. In case of DC input, acceptable input range is -0.3V~6V: within 100ns -10V~6V is acceptable, but electrical specifications are not guaranteed during such a short time.

Thermal Impedance

Symbol	Parameter	Min.	Max.	Unit
Θ_{JA}	Thermal Resistance, Junction-to-Ambient(3)	150		°C/W

Note:
3. Regarding the test environment and PCB type, please refer to JESD51-2 and JESD51-10.

Electrical Characteristics

V_{CC} = 14V, T_A = -40°C~+125°C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{CC} Section						
V_{START}	Start Threshold Voltage	V_{CC} Increasing	11	12	13	V
V_{STOP}	Stop Threshold Voltage	V_{CC} Decreasing	7.5	8.5	9.5	V
HY_{UVLO}	UVLO Hysteresis		3.0	3.5	4.0	V
V_Z	Zener Voltage	I_{CC}=20mA	20	22	24	V
V_{OP}	Recommended Operating Range		13		20	V
Supply Current Section						
I_{START}	Startup Supply Current	$V_{CC}=V_{START}$-0.2V		120	190	µA
I_{OP}	Operating Supply Current	Output Not Switching		1.5	3.0	mA
I_{DOP}	Dynamic Operating Supply Current	50kHZ, C_l=1nF		2.5	4.0	mA
I_{OPDIS}	Operating Current at Disable	V_{INV}=0V	90	160	230	µA
Error Amplifier Section						
V_{REF1}	Voltage Feedback Input Threshold1	T_A=25°C	2.465	2.500	2.535	V
ΔV_{REF1}	Line Regulation	V_{CC}=14V~20V		0.1	10.0	mV
ΔV_{REF2}	Temperature Stability of V_{REF1}[4]			20		mV
$I_{EA,BS}$	Input Bias Current	V_{INV}=1V~4V	-0.5		0.5	µA
$I_{EAS,SR}$	Output Source Current	$V_{INV}=V_{REF}$ -0.1V		-12		µA
$I_{EAS,SK}$	Output Sink Current	$V_{INV}=V_{REF}$ +0.1V		12		µA
V_{EAH}	Output Upper Clamp Voltage	V_{INV}=1V, V_{CS}=0V	6.0	6.5	7.0	V
V_{EAZ}	Zero Duty Cycle Output Voltage		0.9	1.0	1.1	V
g_m	Transconductance[4]		90	115	140	µmho
Maximum On-Time Section						
$t_{ON,MAX1}$	Maximum On-Time Programming 1	T_A=25°C, V_{ZCD}=1V	35.5	41.5	47.5	µs
$t_{ON,MAX2}$	Maximum On-Time Programming 2	T_A=25°C, I_{ZCD}=0.469mA	11.2	13.0	14.8	µs
Current-Sense Section						
V_{CS}	Current Sense Input Threshold Voltage Limit		0.7	0.8	0.9	V
$I_{CS,BS}$	Input Bias Current	V_{CS}=0V~1V	-1.0	-0.1	1.0	µA
$t_{CS,D}$	Current Sense Delay to Output[4]	dV/dt=1V/100ns, from 0V to 5V		350	500	ns

Continued on the following page…

Electrical Characteristics

V_{CC} = 14V, T_A = -40°C~+125°C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
Zero-Current Detect Section						
V_{ZCD}	Input Voltage Threshold[4]		1.35	1.50	1.65	V
HY_{ZCD}	Detect Hysteresis[4]		0.05	0.10	0.15	V
V_{CLAMPH}	Input High Clamp Voltage	I_{DET}=3mA	5.5	6.2	7.5	V
V_{CLAMPL}	Input Low Clamp Voltage	I_{DET}= -3mA	0	0.65	1.00	V
$I_{ZCD,BS}$	Input Bias Current	V_{ZCD}=1V~5V	-1.0	-0.1	1.0	µA
$I_{ZCD,SR}$	Source Current Capability[4]	T_A=25°C			-4	mA
$I_{ZCD,SK}$	Sink Current Capability[4]	T_A=25°C			10	mA
$t_{ZCD,D}$	Maximum Delay From ZCD to Output Turn-On[4]	dV/dt=-1V/100ns, from 5V to 0V	100		200	ns
Output Section						
V_{OH}	Output Voltage High	I_O=-100mA, T_A=25°C	9.2	11.0	12.8	V
V_{OL}	Output Voltage Low	I_O=200mA, T_A=25°C		1.0	2.5	V
t_{RISE}	Rising Time[4]	C_{IN}=1nF		50	100	ns
t_{FALL}	Falling Time[4]	C_{IN}=1nF		50	100	ns
$V_{O,MAX}$	Maximum Output Voltage	V_{CC}=20V, I_O=100µA	11.5	13.0	14.5	V
$V_{O,UVLO}$	Output Voltage with UVLO Activated	V_{CC}=5V, I_O=100µA			1	V
Restart / Maximum Switching Frequency Limit Section						
t_{RST}	Restart Timer Delay		50	150	300	µs
f_{MAX}	Maximum Switching Frequency[4]		250	300	350	kHz
RDY Pin						
$I_{RDY,SK}$	Output Sink Current		1	2	4	mA
$V_{RDY,SAT}$	Output Saturation Voltage	$I_{RDY,SK}$=2mA		320	500	mV
$I_{RDY,LK}$	Output Leakage Current	Output High Impedance			1	µA
Soft-Start Timer Section						
t_{SS}	Internal Soft-Soft[4]		3	5	7	ms
UVLO Section						
V_{RDY}	Output Ready Voltage		2.185	2.240	2.295	V
HY_{RDY}	Output Ready Hysteresis			0.600		V
Protections						
V_{OVP}	OVP Threshold Voltage	T_A=25°C	2.620	2.675	2.730	V
HY_{OVP}	OVP Hysteresis	T_A=25°C	0.120	0.175	0.230	V
V_{EN}	Enable Threshold Voltage		0.40	0.45	0.50	V
HY_{EN}	Enable Hysteresis		0.050	0.10	0.15	V
T_{SD}	Thermal Shutdown Temperature[4]		125	140	155	°C
T_{HYS}	Hysteresis Temperature of TSD[4]			60		°C

Note:

4. These parameters, although guaranteed by design, are not production tested.

Comparison of FAN7530 and FAN7930

Function	FAN7530	FAN7930	FAN7930 Advantages
PFC Ready Pin	None	Integrated	▪ No External Circuit for PFC Output UVLO ▪ Reduction of Power Loss and BOM Cost Caused by PFC Out UVLO Circuit ▪ Open-Drain Pin has Versatile Uses
Frequency Limit	None	Integrated	▪ Abnormal CCM Operation Prohibited ▪ Abnormal Inductor Current Accumulation can be Prohibited
AC Absent Detection	None	Integrated	▪ Increase System Reliability with AC On-Off Test ▪ Guarantee Stable Operation at Short Electric Power Failure
Soft-Start and Overshoot-less	None	Integrated	▪ Reduce Voltage and Current Stress at Startup ▪ Eliminate Audible Noise due to Unwanted OVP Triggering
THD Optimizer	External	Internal	▪ No External Resistor is Needed
TSD	None	140°C with 60°C Hysteresis	▪ Stable and Reliable TSD Operation ▪ Converter Temperature Range Limited Range

Typical Performance Characteristics

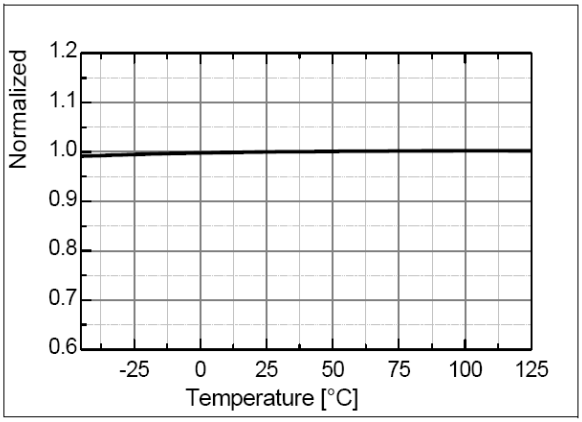

Figure 4. Voltage Feedback Input Threshold 1 (V_{REF1}) vs. T_A

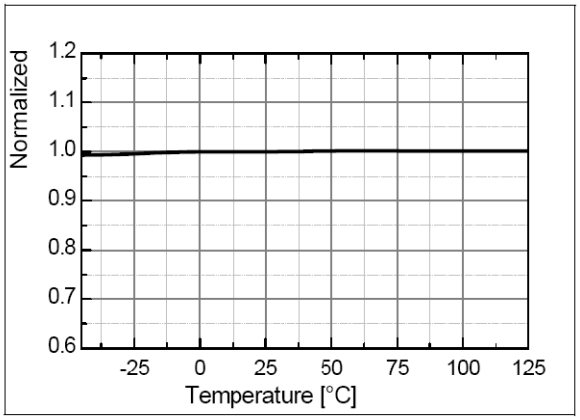

Figure 5. Start Threshold Voltage (V_{START}) vs. T_A

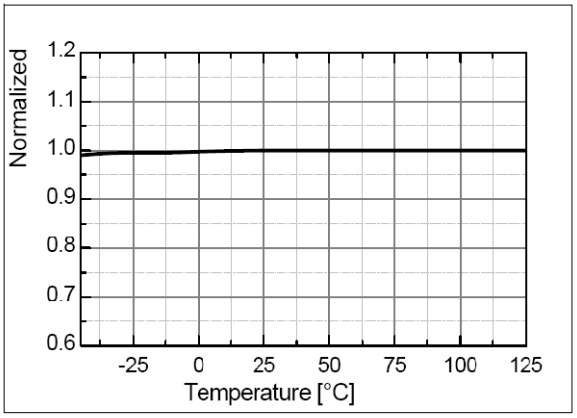

Figure 6. Stop Threshold Voltage (V_{STOP}) vs. T_A

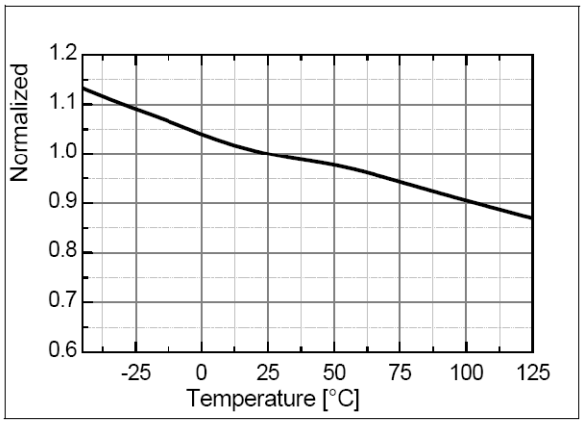

Figure 7. Startup Supply Current (I_{START}) vs. T_A

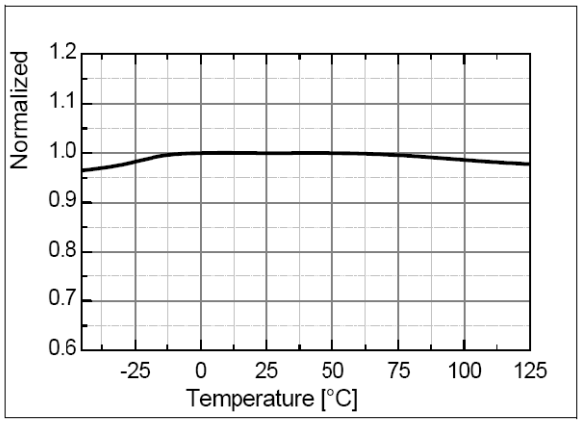

Figure 8. Operating Supply Current (I_{OP}) vs. T_A

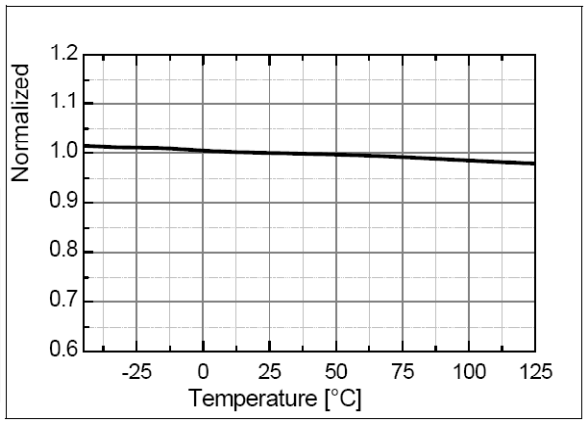

Figure 9. Output Upper Clamp Voltage (V_{EAH}) vs. T_A

Typical Performance Characteristics

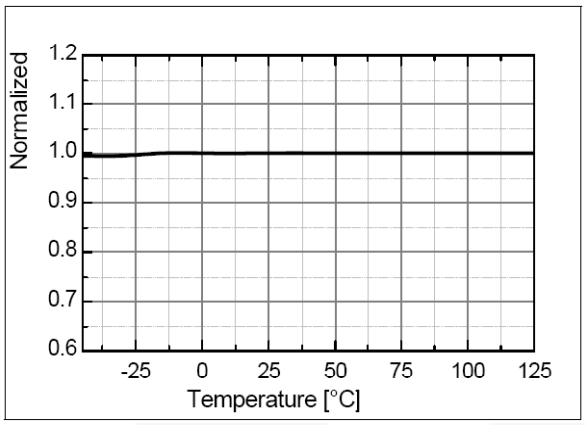

Figure 10. Zero Duty Cycle Output Voltage (V_{EAZ}) vs. T_A

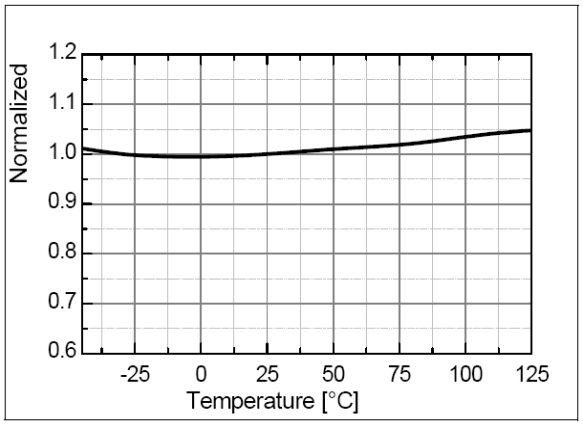

Figure 11. Maximum On-Time Program 1 ($t_{ON,MAX1}$) vs. T_A

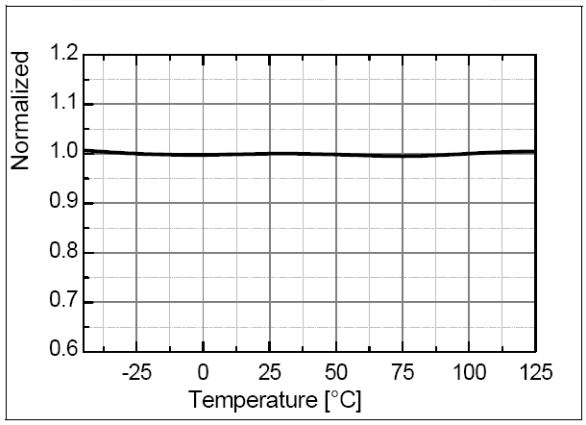

Figure 12. Maximum On-Time Program 2 ($t_{ON,MAX2}$) vs. T_A

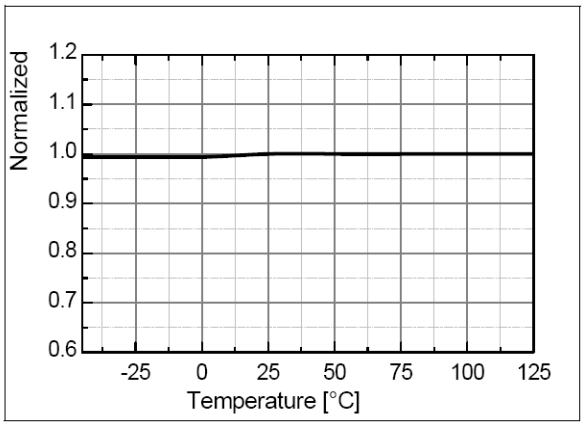

Figure 13. Current Sense Input Threshold Voltage Limit (V_{CS}) vs. T_A

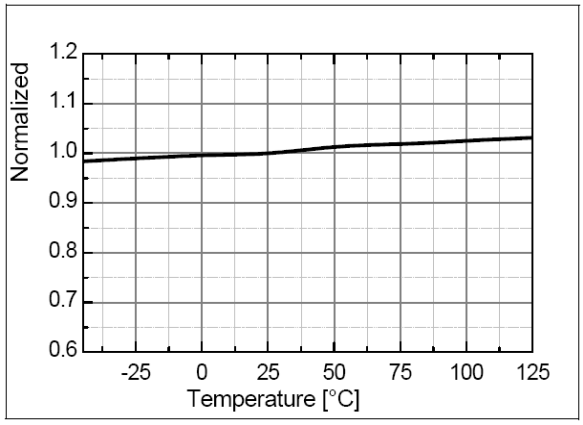

Figure 14. Input High Clamp Voltage (V_{CLAMPH}) vs. T_A

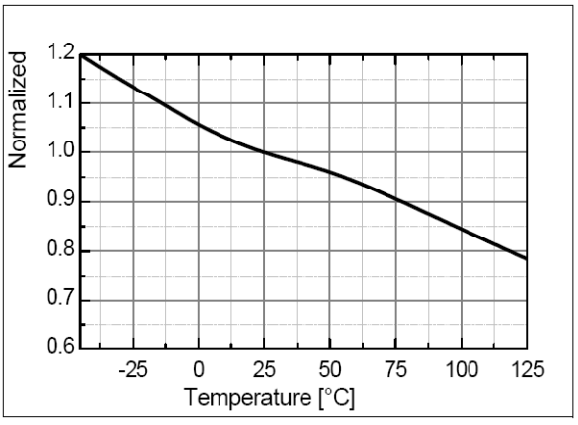

Figure 15. Input Low Clamp Voltage (V_{CLAMPL}) vs. T_A

Typical Performance Characteristics

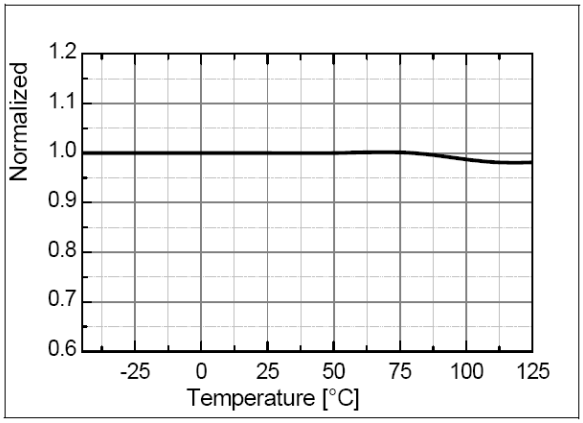

Figure 16. Output Voltage High (V_{OH}) vs. T_A

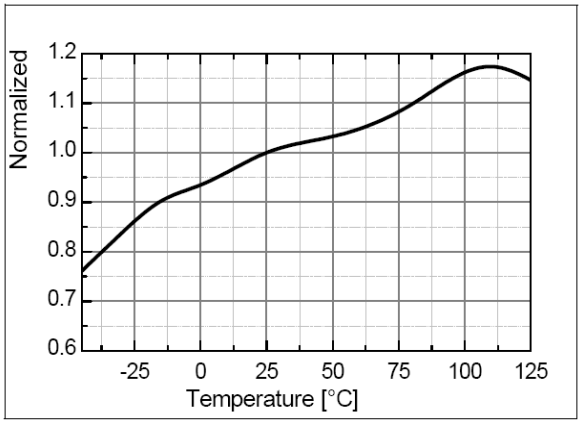

Figure 17. Output Voltage Low (V_{OL}) vs. T_A

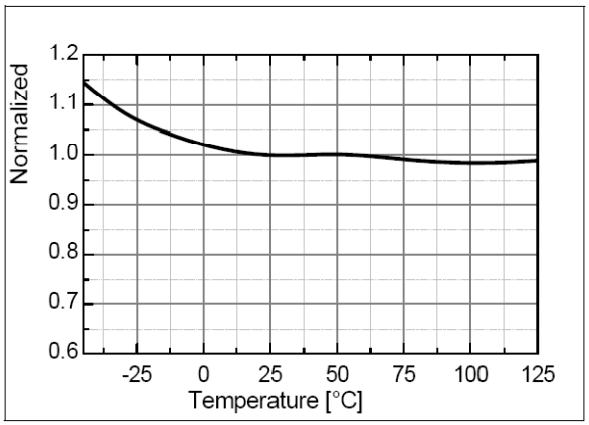

Figure 18. Restart Timer Delay (t_{RST}) vs. T_A

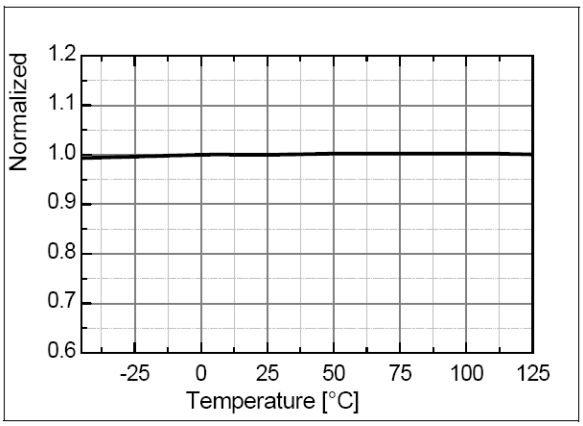

Figure 19. Output Ready Voltage (V_{RDY}) vs. T_A

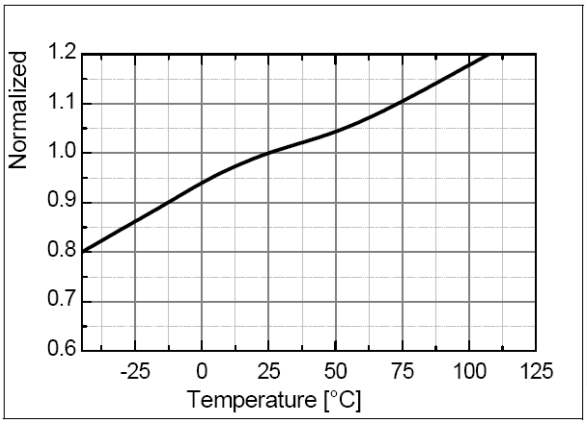

Figure 20. Output Saturation Voltage ($V_{RDY,SAT}$) vs. T_A

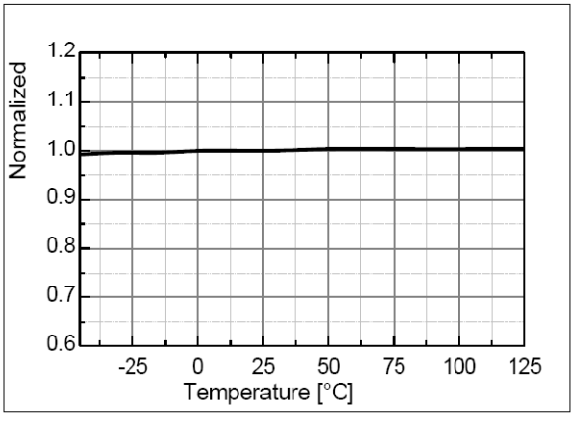

Figure 21. OVP Threshold Voltage (V_{OVP}) vs. T_A

Applications Information

1. Startup: Normally, supply voltage (V_{CC}) of a PFC block is fed from the additional power supply, which can be called standby power. Without this standby power, auxiliary winding to detect zero current detection can be used as a supply source. Once the supply voltage of the PFC block exceeds 12V, internal operation is enabled until the voltage drops to 8.5V. If V_{CC} exceeds V_Z, 20mA current is sinking from V_{CC}.

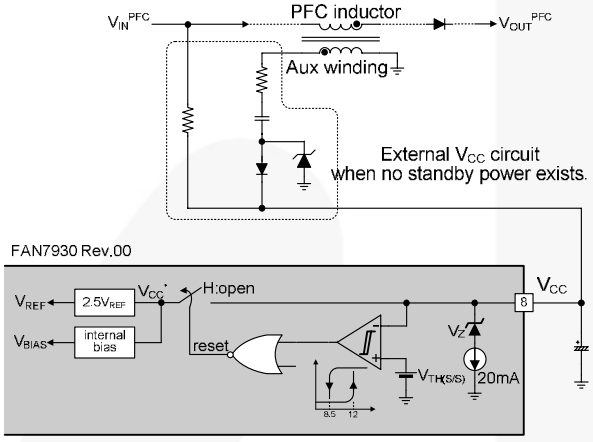

Figure 22. Startup Circuit

2. INV Block: Scaled-down voltage from the output is the input for the INV pin. Many functions are embedded based on the INV pin: transconductance amplifier, output OVP comparator, disable comparator, and output UVLO comparator.

For the output voltage control, a transconductance amplifier is used instead of the conventional voltage amplifier. The transconductance amplifier (voltage-controlled current source) aids the implementation of OVP and disable function. The output current of the amplifier changes according to the voltage difference of the inverting and non-inverting input of the amplifier. To cancel down the line input voltage effect on power factor correction, effective control response of PFC block should be slower than the line frequency and this conflicts with the transient response of controller. Two-pole one-zero type compensation may be used to meet both requirements.

The OVP comparator shuts down the output drive block when the voltage of the INV pin is higher than 2.675V and there is 0.175V hysteresis. The disable comparator disables the operation when the voltage of the inverting input is lower than 0.35V and there is 100mV hysteresis. An external small-signal MOSFET can be used to disable the IC, as shown in Figure 23. The IC operating current decreases to reduce power consumption if the IC is disabled. Figure 24 is the timing chart of the internal circuit near the INV pin when rated PFC output voltage is assumed at $390V_{DC}$ and V_{CC} supply voltage is 15V.

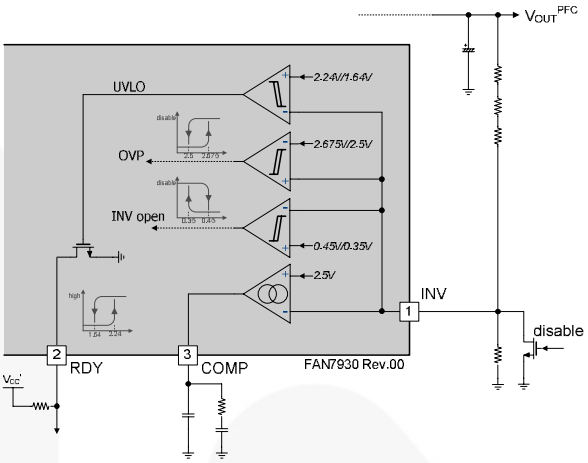

Figure 23. Circuit Around INV Pin

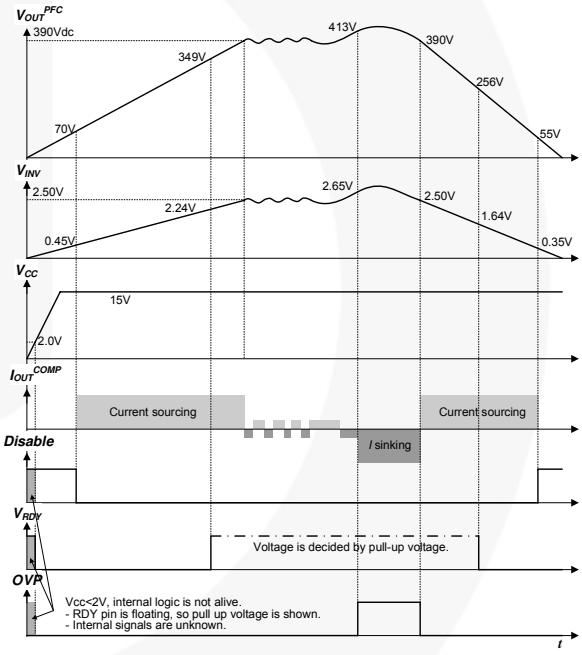

Figure 24. Timing Chart for INV Block

3. RDY Output: When the INV voltage is higher than 2.24V, output UVLO voltage is triggered to high and lasts until the INV voltage is lower than 1.64V. This signal outputs through the RDY pin. RDY pin output is open-drain type, so needs an external pull-up resistor to supply the proper power source. The RDY pin output remains floating until V_{CC} is higher than 2V.

4. Zero-Current Detection: Zero-current detection (ZCD) generates the turn-on signal of the MOSFET when the boost inductor current reaches zero using an auxiliary winding coupled with the inductor. When the power switch turns on, negative voltage is induced at the auxiliary winding due to the opposite winding direction (see equation 1) and positive voltage is induced *(see equation 2)* when the power switch turns off.

$$V_{AUX} = -\frac{T_{AUX}}{T_{IND}} \cdot V_{AC} \quad (1)$$

$$V_{AUX} = \frac{T_{AUX}}{T_{IND}} \cdot (V_{PFCOUT} - V_{AC}) \quad (2)$$

where, V_{AUX} is the auxiliary winding voltage, T_{IND} and T_{AUX} are boost inductor turns and auxiliary winding turns respectively, V_{AC} is input voltage for PFC converter and V_{OUT_PFC} is output voltage from the PFC converter.

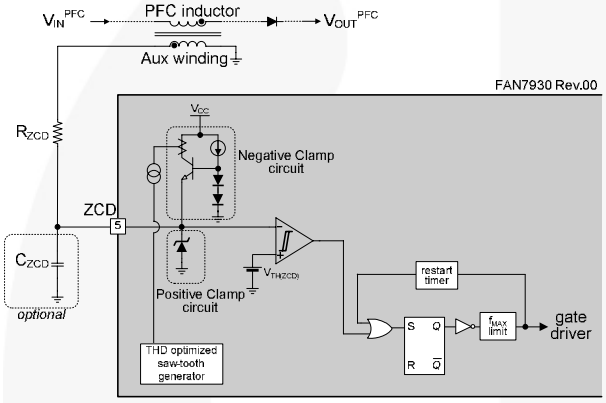

Figure 25. Circuit Near ZCD

Because auxiliary winding voltage can swing from negative voltage to positive voltage, the internal block in ZCD pin has both positive and negative voltage clamping circuits. When the auxiliary voltage is negative, internal circuit clamps the negative voltage at the ZCD pin around 0.65V by sourcing current to the serial resistor between the ZCD pin and the auxiliary winding. When the auxiliary voltage is higher than 6.5V, current is sinked through a resistor from the auxiliary winding to the ZCD pin.

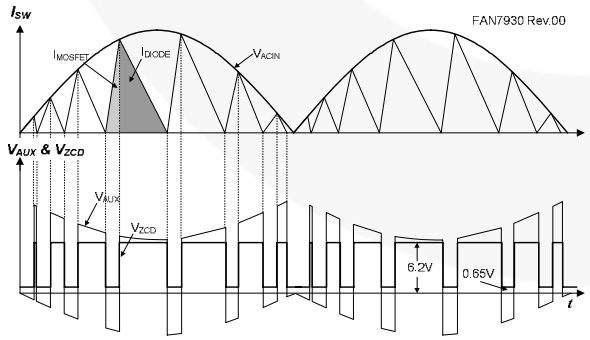

Figure 26. Auxiliary Voltage Depends on MOSFET Switching

To check the boost inductor current zero instance, auxiliary winding voltage is used. When boost inductor current becomes zero, there is a resonance between boost inductor and all capacitors at MOSFET drain pin, including C_{OSS} of the MOSFET; an external capacitor at the D-S pin to reduce the voltage rising and falling slope of the MOSFET; a parasitic capacitor at inductor; and so on to improve performance. Resonated voltage is reflected to the auxiliary winding and can be used as detecting zero current of boost inductor and valley position of MOSFET voltage stress. For valley detection, a minor delay by the resistor and capacitor is needed. A capacitor increases the noise immunity at the ZCD pin. If ZCD voltage is higher than 1.5V, an internal ZCD comparator output becomes HIGH and LOW when the ZCD goes below 1.4V. At the falling edge of comparator output, internal logic turns on the MOSFET.

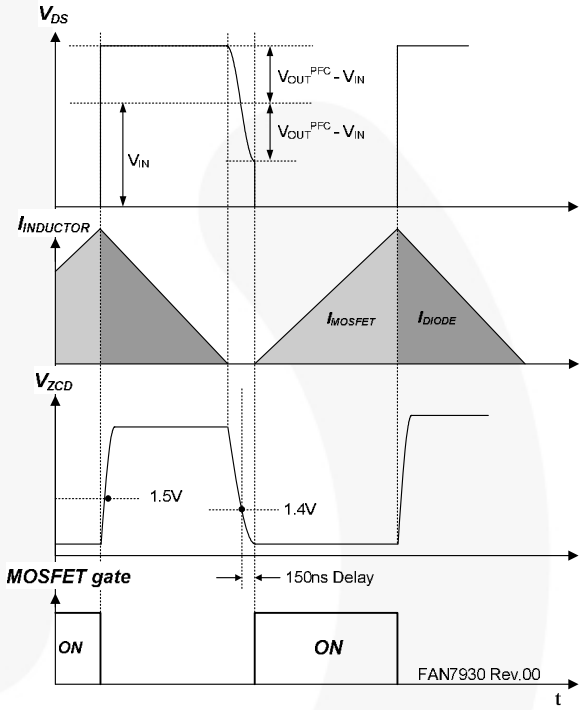

Figure 27. Auxiliary Voltage Threshold

When no ZCD signal is available, the PFC controller cannot turn on MOSFET, so the controller checks every switching off time and forces MOSFET turn on when the off time is longer than 150μs. It is called restart timer. Restart timer triggers MOSFET turn on at startup and may be used at the input voltage zero cross period.

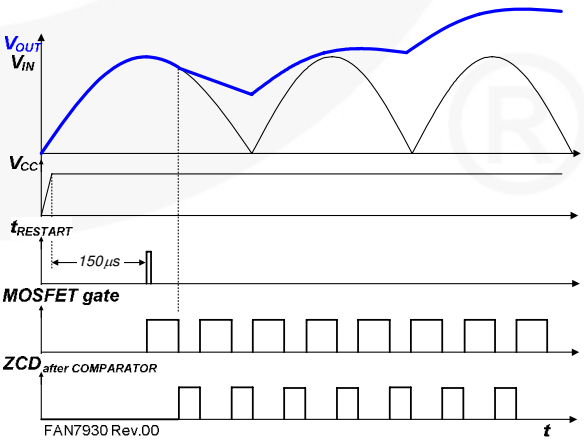

Figure 28. Restart Timer at Startup

Because the MOSFET turn on depends on the ZCD input, switching frequency may increase to higher than several megahertz due to the miss-triggering or noise on the nearby ZCD pin. If the switching frequency is higher than needed for critical conduction mode (CRM), operation mode shifts to continuous conduction mode (CCM). In CCM, unlike CRM where the boost inductor current is reset to zero at the next switch on; inductor current builds up at every switching cycle and can be raised to very high current, that exceeds the current rating of the power switch or diode. This can seriously damage the power switch and result in burn down. To avoid this, maximum switching frequency limitation is embedded. If ZCD signal is applied again within 3.3μs after the previous rising edge of gate signal, this signal is ignored internally and FAN7930 waits for another ZCD signal. This slightly degrades the power factor performance at light load and high input voltage.

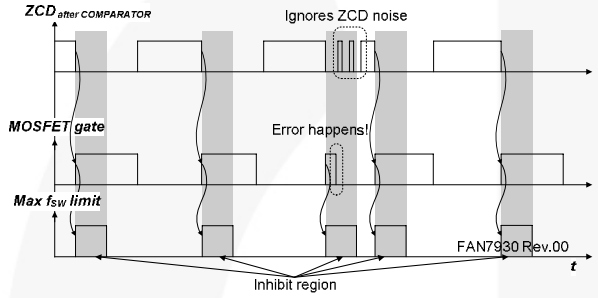

Figure 29. Maximum Switching Frequency Limit Operation

5. Control: The scaled output is compared with the internal reference voltage and sinking or sourcing current is generated from the COMP pin by the transconductance amplifier. The error amplifier output is compared with the internal sawtooth waveform to give proper turn-on time based on the controller.

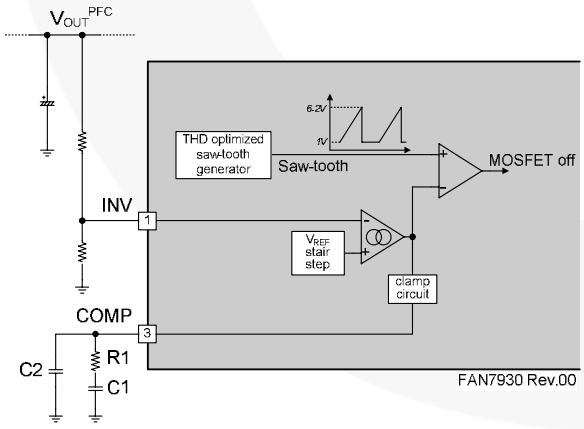

Figure 30. Control Circuit

Unlike a conventional voltage-mode PWM controller, FAN7930 turns on the MOSFET at the falling edge of ZCD signal. On instance is decided by the external signal and the turn-on time lasts until the error amplifier output (V_{COMP}) and sawtooth waveform meet. When load is heavy, output voltage decreases, scaled output decreases, COMP voltage increases to compensate low output, turn-on time lengthens to give more inductor turn-on time, and increased inductor current raises the output voltage. This is how PFC negative feedback controller regulates output.

The maximum of V_{COMP} is limited to 6.5V, which dictates the maximum turn-on time, and switching stops when V_{COMP} is lower than 1.0V.

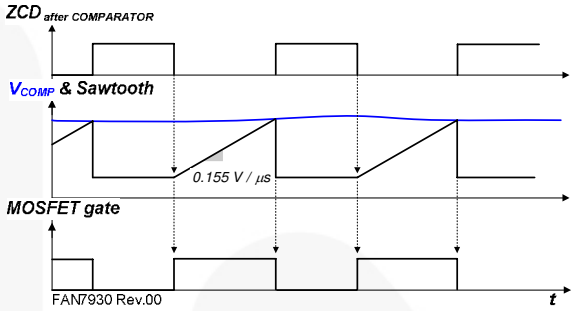

Figure 31. Turn-On Time Determination

The roles of PFC controller are regulating output voltage and input current shaping to increase power factor. Duty control based on the output voltage should be fast enough to compensate output voltage dip or overshoot. For the power factor, however, the control loop must not react to the fluctuating AC input voltage. These two requirements conflict; therefore, when designing a feedback loop, the feedback loop should be least 10 times slower than AC line frequency. That slow response is made by C1 at compensator. R1 makes gain boost around operation region and C2 attenuates gain at higher frequency. Boost gain by R1 helps raise the response time and improves phase margin.

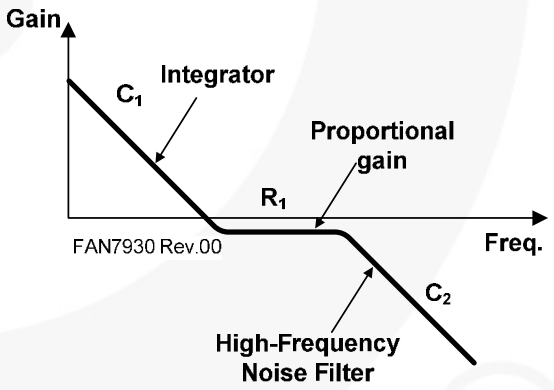

Figure 32. Compensators Gain Curve

For the transconductance error amplifier side, gain changes based on differential input. When the error is large, gain is large to make the output dip or peak to suppress quickly. When the error is small, low gain is used to improve power factor performance.

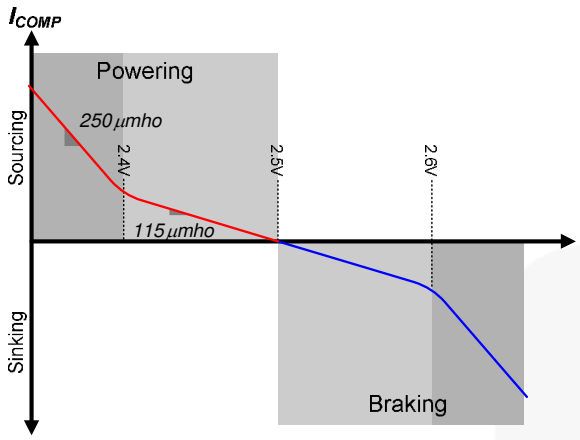

Figure 33. Gain Characteristic

6. Soft-Start: When V_{CC} touches V_{START}, internal reference voltage is increased like a stair step for 5ms. As a result, V_{COMP} is also raised gradually and MOSFET turn-on time increases smoothly. This reduces voltage and current stress on the power switch during startup.

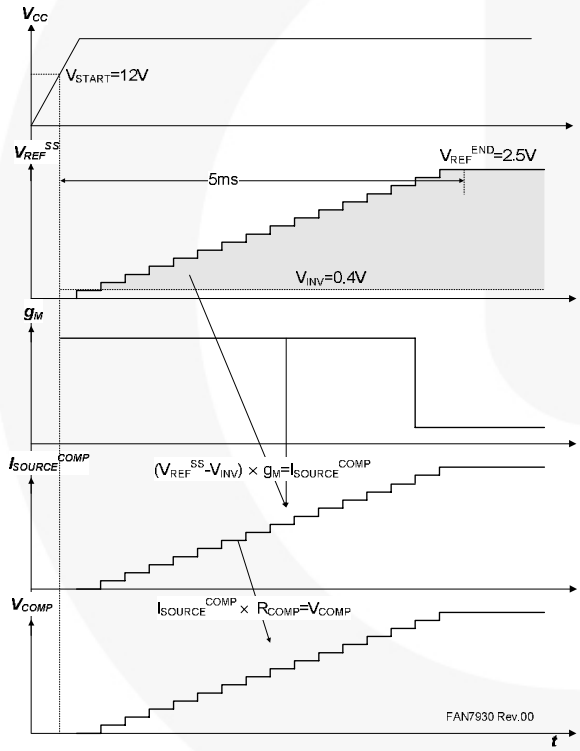

Figure 34. Soft-Start Sequence

7. "Overshoot-less" Startup: Feedback control speed of PFC is quite slow. Due to the slow response, there is a gap between output voltage and feedback control. That is why over-voltage protection (OVP) is critical at the PFC controller and voltage dip caused by fast load changes from light to heavy is diminished by a bulk capacitor. OVP is easily triggered at startup phase. Operation on and off by OVP at startup may cause audible noise and can increase voltage stress at startup, which is normally higher than in normal operation. This operation is better when soft-start time is very long. However, too long startup time enlarges the output voltage building time at light load. FAN7930 has "overshoot-less" control at startup. During startup, the feedback loop is controlled by an internal proportional gain controller and when the output voltage reaches the rated value, it switches to an external compensator after a transition time of 30ms. In short, an internal proportional gain controller eliminates overshoot at startup and an external conventional compensator takes over successfully afterward.

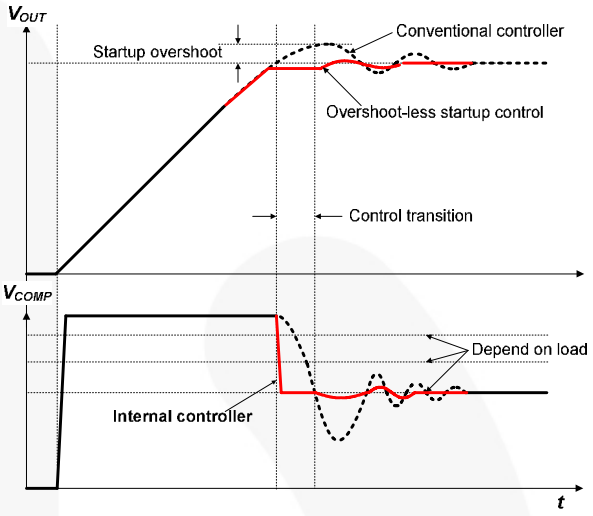

Figure 35. Overshoot-less Startup Control

8. THD Optimization: Total harmonic distortion (THD) is the factor that dictates how closely input current shape matches sinusoidal form. The turn-on time of the PFC controller is almost constant over one AC line period due to the extremely low feedback control response. The turn-off time is decided by the current decrease slope of the boost inductor made by the input voltage and output voltage. Once inductor current becomes zero, resonance between C_{OSS} and the boost inductor makes oscillating waveforms at the drain pin and auxiliary winding. By checking the auxiliary winding voltage through the ZCD pin, the controller can check the zero current of boost inductor. At the same time, a minor delay time is inserted to determine the valley position of drain voltage. The input and output voltage difference is at its maximum at the zero cross point of AC input voltage. The current decrease slope is steep near the zero cross region and more negative inductor current flows during a drain voltage valley detection time. Such a negative inductor current cancels down the positive current flows and input current becomes zero, called "zero-cross distortion" in PFC.

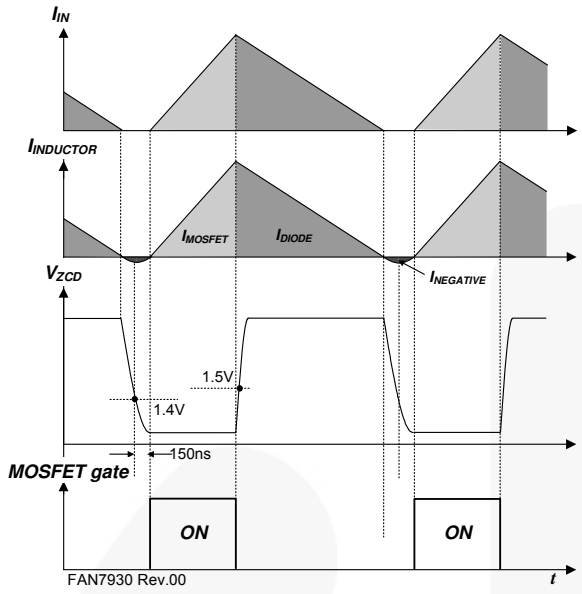

Figure 36. Input and Output Current Near Input Voltage Peak

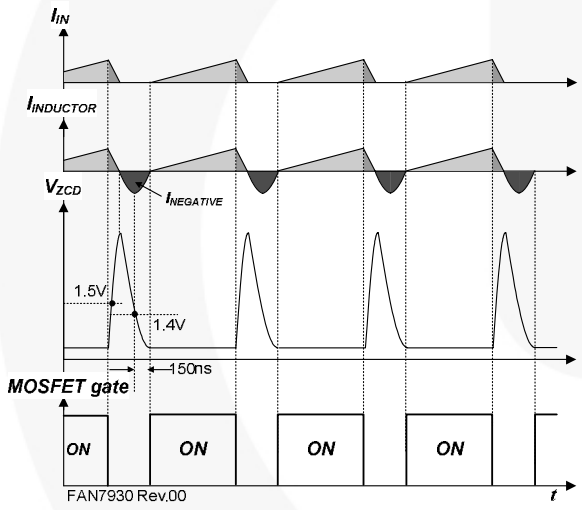

Figure 37. Input and Output Current Near Input Voltage Peak Zero Cross

To improve this, lengthened turn-on time near the zero cross region is a well-known technique, though the method may be different from company to company and may be proprietary. FAN7930 emdodies this by sourcing current through the ZCD pin. Auxiliary winding voltage becomes negative when the MOSFET turns on and is proportional to input voltage. The negative clamping circuit of ZCD outputs the current to maintain the ZCD voltage at a fixed value. The sourcing current from the ZCD is directly proportional to the input voltage. Some portion of this current is applied to the internal sawtooth generator together with a fixed-current source. Theoretically, the fixed-current source and the capacitor at sawtooth generator decide the maximum turn-on time when no current is sourcing at ZCD clamp circuit and available turn-on time gets shorter proportional to the ZCD sourcing current.

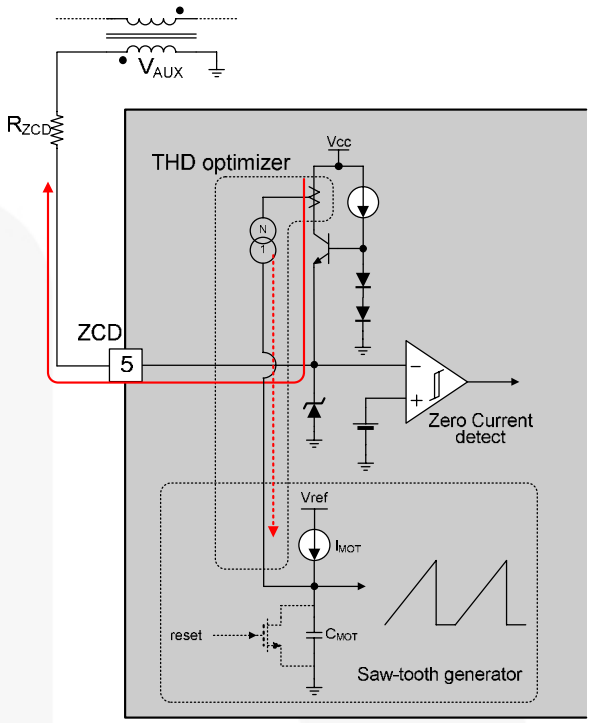

Figure 38. Circuit of THD Optimizer

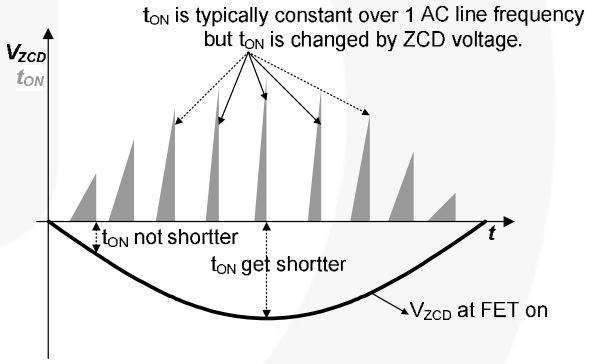

Figure 39. Effect of THD Optimizer

By THD optimizer, turn-on time over one AC line period is proportionally changed, depending on input voltage. Near zero cross, lengthened turn-on time improves THD performance.

9. Input Voltage Absent Detection: To save power loss caused by input voltage sensing resistors and to optimize THD easily, the FAN7930 omits AC input voltage detection. Therefore, no information about AC input is available from the internal controller. In many cases, the V_{CC} of PFC controller is supplied by a independent power source like standby power. In this scheme, some mismatch may exist. For example, when the electric power is suddenly interrupted during two or three AC line periods; V_{CC} is still alive during that time, but output voltage drops because there is no input power source. Consequently, the control loop tries to compensate for the output voltage drop and V_{COMP} reaches its maximum. This lasts until AC input voltage is

live again. When AC input voltage is live again, high V_{COMP} allows high switching current and more stress is put on the MOSFET and diode. To protect against this, FAN7930 internally checks if the input AC voltage exists. If input does not exist, soft-start is reset and waits until AC input is live again. Soft-start manages the turn-on time for smooth operation when it detects AC input is applied again and applies less voltage and current stress on startup.

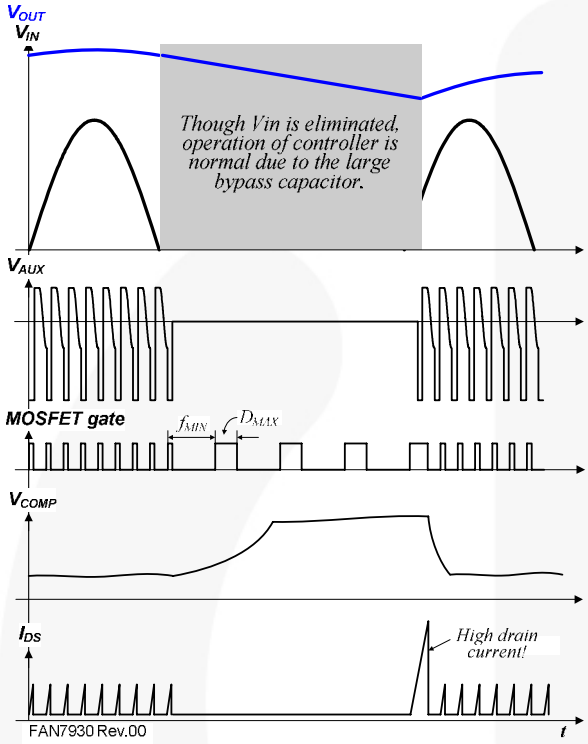

Figure 40. Operation without Input Voltage Absent Circuit

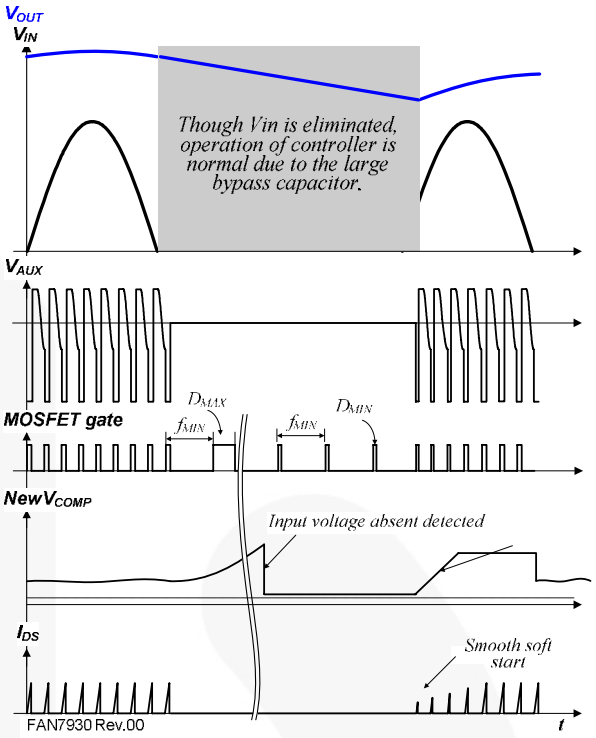

Figure 41. Operation with Input Voltage Absent Circuit

10. Current Sense: The MOSFET current is sensed using an external sensing resistor for the over-current protection. If the CS pin voltage is higher than 0.8V, the over-current protection comparator generates a protection signal. An internal RC filter of 40kΩ and 8pF is included to filter switching noise.

11. Gate Driver Output: FAN7930 contains a single totem-pole output stage designed for a direct drive of the power MOSFET. The drive output is capable of up to +500/-800mA peak current with a typical rise and fall time of 50ns with 1nF load. The output voltage is clamped to 13V to protect the MOSFET gate even if the V_{CC} voltage is higher than 13V.

PCB Layout Guide

PFC block normally handles high switching current and the voltage low energy signal path can be affected by the high energy path. Cautious PCB layout is mandatory for stable operation.

1. The gate drive path should be as short as possible. The closed-loop that starts from the gate driver, MOSFET gate, and MOSFET source to ground of PFC controller is recommended as close as possible. This is also crossing point between power ground and signal ground. Power ground path from the bridge diode to the output bulk capacitor should be short and wide. The sharing position between power ground and signal ground should be only at one position to avoid ground loop noise. Signal path of PFC controller should be short and wide for external components to contact.
2. PFC output voltage sensing resistor is normally high to reduce current consumption. This path can be affected by external noise. To reduce noise possibility at the INV pin, a shorter path for output sensing is recommended. If a shorter path is not possible, place some dividing resistors between PFC output and the INV pin — closer to the INV pin is better. Relative high voltage close to the INV pin can be helpful.
3. ZCD path is recommended close to auxiliary winding from boost inductor and to the ZCD pin. If that is difficult, place a small capacitor (below 50pF) to reduce noise.
4. Switching current sense path should not share with another path to avoid interference. Some additional components may be needed to reduce the noise level applied to the CS pin.
5. A stabilizing capacitor for V_{CC} is recommended as close as possible to the V_{CC} and ground pins. If it is difficult, place the SMD capacitor as close to the corresponding pins as possible.

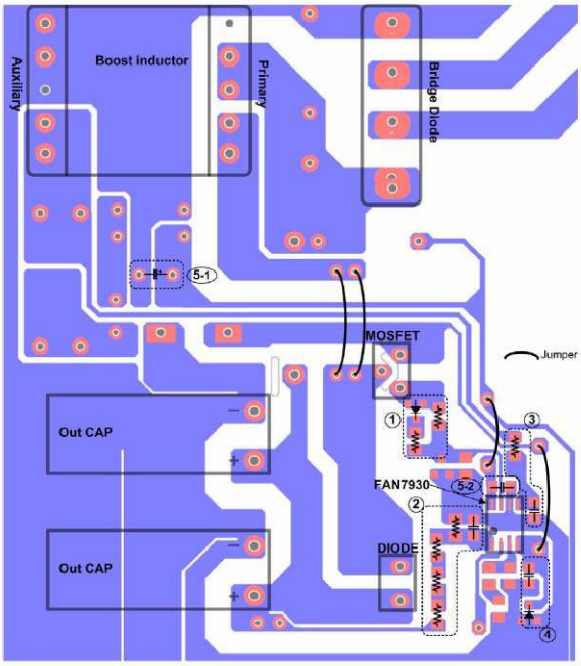

Figure 42. Recommended PCB Layout

Typical Application Circuit

Application	Device	Input Voltage Range	Rated Output Power	Output Voltage (Maximum Current)
LCD TV Power Supply	FAN7930	90-265V_{AC}	195W	390V (0.5A)

Features

- Average efficiency of 25%, 50%, 75%, and 100% load conditions is higher than 95% at universal input.
- Power factor at rated load is higher than 0.98 at universal input.
- Total Harmonic Distortion (THD) at rated load is lower than 15% at universal input.

Key Design Notes

- When auxiliary V_{CC} supply is not available, V_{CC} power can be supplied through Zero Current Detect (ZCD) winding. The power consumption of R103 is quite high, so its power rating needs checking.
- Because the input bias current of INV pin is almost zero, output voltage sensing resistors (R112~R115) as high as possible. However, too-high resistance makes the node easily affected by noise. Thus values need to strike a balance between power consumption and noise immunity.
- Quick charge diode (D106) can be eliminated. Without D106, system operation is normal due to the controller's highly reliable protection features.

1. Schematic

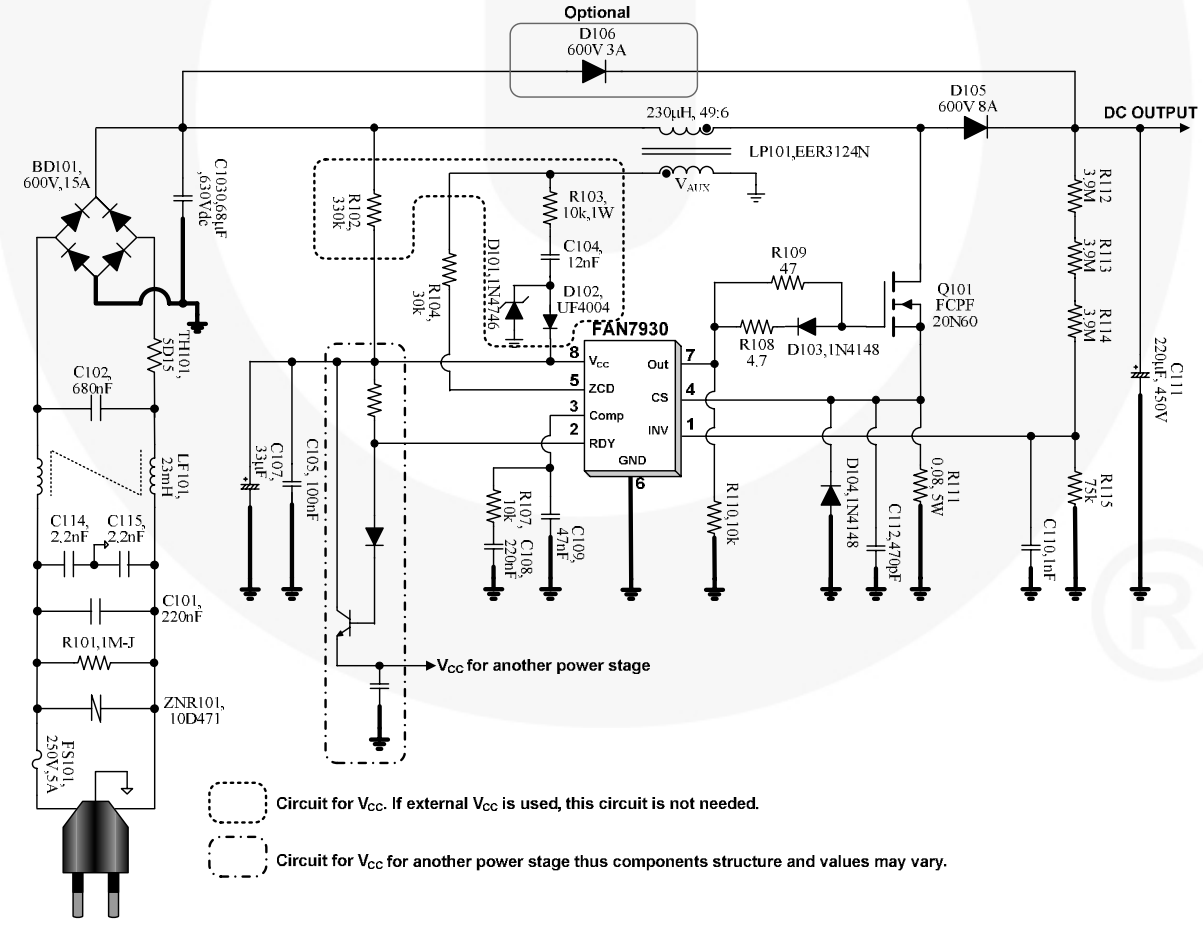

Figure 43. Demonstration Circuit

2. Transformer

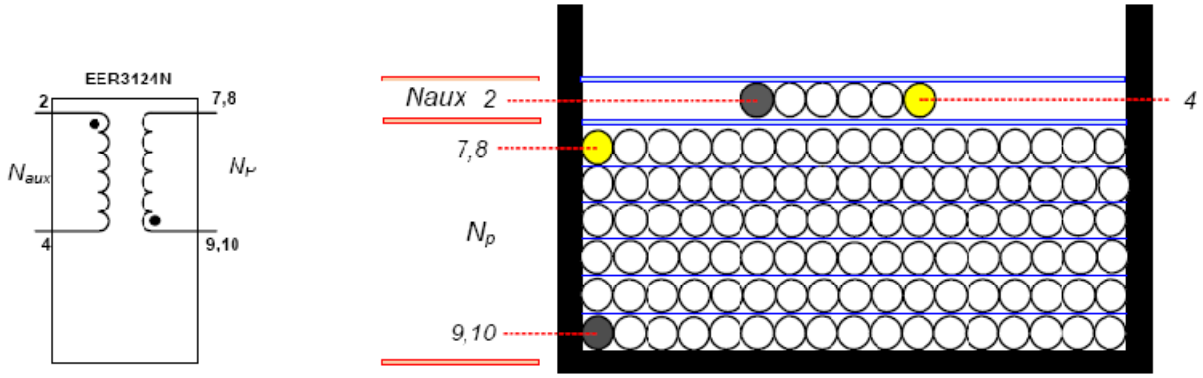

Figure 44. Transformer Schematic Diagram of FAN7930

3. Winding Specification

Position	No	Pin (S → F)	Wire	Turns	Winding Method	Barrier Tape		
						TOP	BOT	Ts
Bottom	N_p	9, 10 → 7, 8	0.1φ×50	49	Solenoid Winding			1
	Insulation: Polyester Tape t = 0.025mm, 3 Layers							
Top	N_{AUX}	2 → 4	0.3φ	6	Solenoid Winding			
	Insulation: Polyester Tape t = 0.025mm, 4 Layers							

4. Electrical Characteristics

	Pin	Specification	Remark
Inductance	9, 10 → 7, 8	230μH ± 7%	100kHz, 1V

5. Core & Bobbin

Core: EER3124, Samhwa (PL-7) (Ae=97.9mm^2)
Bobbin: EER3124

6. Bill of Materials

Part #	Value	Note	Part #	Value	Note
Resister			**Switch**		
R101	1MΩ	1W	Q101	FCPF20N60	20A, 600V, SuperFET
R102	330kΩ	1/2W	**Diode**		
R103	10kΩ	1W	D101	1N4746	1W, 18V, Zener Diode
R104	30kΩ	1/4W	D102	UF4004	1A, 400V Glass Passivated High-Efficiency Rectifier
R107	10kΩ	1/4W	D103	1N4148	1A, 100V Small-Signal Diode
R108	4.7kΩ	1/4W	D104	1N4148	1A, 100V Small-Signal Diode
R109	47kΩ	1/4W	D105		8A, 600V, General-Purpose Rectifier
R110	10kΩ	1/4W	D106		3A, 600V, General-Purpose Rectifier
R111	0.80kΩ	5W			
R112, 113, 114	3.9kΩ	1/4W	IC101	FAN7930	CRM PFC Controller
R115	75kΩ	1/4W			
Capacitor			**Fuse**		
C101	220nF/275V_{AC}	Box Capacitor	FS101	5A/250V	
C102	680nF/275V_{AC}	Box Capacitor	**NTC**		
C103	0.68µF/630V	Box Capacitor	TH101	5D-15	
C104	12nF/50V	Ceramic Capacitor	**Bridge Diode**		
C105	100nF/50V	SMD (1206)	BD101		15A, 600V
C107	33µF/50V	Electrolytic Capacitor	**Line Filter**		
C108	220nF/50V	Ceramic Capacitor	LF101	23mH	
C109	47nF/50V	Ceramic Capacitor	**Transformer**		
C110	1nF/50V	Ceramic Capacitor	T1	EER3124	Ae=97.9mm^2
C112	47nF/50V	Ceramic Capacitor	**ZNR**		
C111	220µF/450V	Electrolytic Capacitor	ZNR101	10D471	
C114	2.2nF/450V	Box Capacitor			
C115	2.2nF/450V	Box Capacitor			

Physical Dimensions

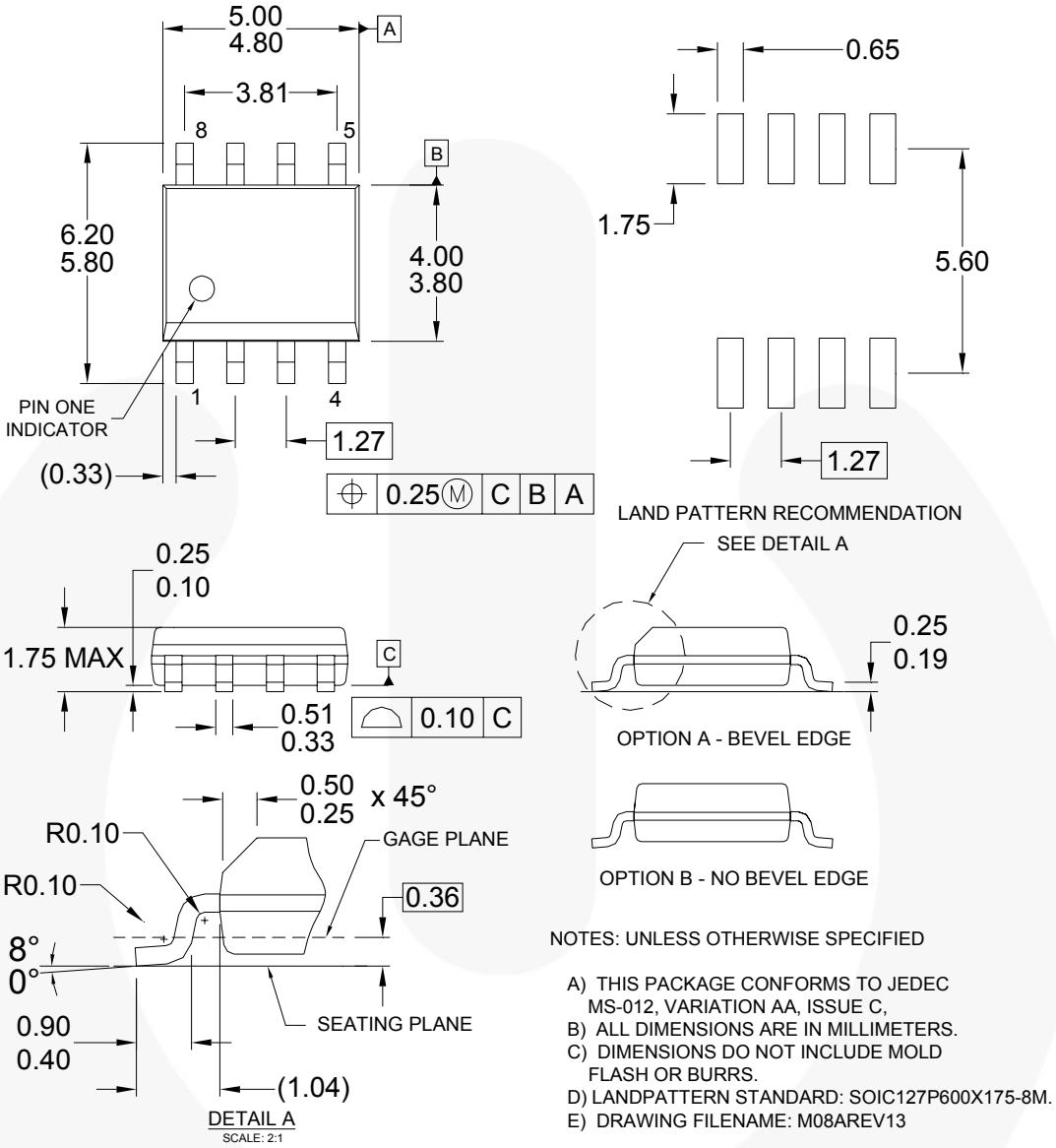

Figure 45. 8-Lead Small Outline Package (SOP)

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings:
http://www.fairchildsemi.com/packaging/.

FAIRCHILD SEMICONDUCTOR®

TRADEMARKS

The following includes registered and unregistered trademarks and service marks, owned by Fairchild Semiconductor and/or its global subsidiaries, and is not intended to be an exhaustive list of all such trademarks.

AccuPower™
Auto-SPM™
Build it Now™
CorePLUS™
CorePOWER™
CROSSVOLT™
CTL™
Current Transfer Logic™
DEUXPEED®
Dual Cool™
EcoSPARK®
EfficientMax™
ESBC™
F®
Fairchild®
Fairchild Semiconductor®
FACT Quiet Series™
FACT®
FAST®
FastvCore™
FETBench™
FlashWriter®*
FPS™
F-PFS™
FRFET®
Global Power Resource℠
Green FPS™
Green FPS™ e-Series™
Gmax™
GTO™
IntelliMAX™
ISOPLANAR™
MegaBuck™
MICROCOUPLER™
MicroFET™
MicroPak™
MicroPak2™
MillerDrive™
MotionMax™
Motion-SPM™
OptoHiT™
OPTOLOGIC®
OPTOPLANAR®
®
PDP SPM™
Power-SPM™
PowerTrench®
PowerXS™
Programmable Active Droop™
QFET®
QS™
Quiet Series™
RapidConfigure™
™
Saving our world, 1mW/W/kW at a time™
SignalWise™
SmartMax™
SMART START™
SPM®
STEALTH™
SuperFET™
SuperSOT™-3
SuperSOT™-6
SuperSOT™-8
SupreMOS®
SyncFET™
Sync-Lock™
SYSTEM GENERAL®*
The Power Franchise®
the power franchise
TinyBoost™
TinyBuck™
TinyCalc™
TinyLogic®
TINYOPTO™
TinyPower™
TinyPWM™
TinyWire™
TriFault Detect™
TRUECURRENT™*
µSerDes™
µ SerDes
UHC®
Ultra FRFET™
UniFET™
VCX™
VisualMax™
XS™

* Trademarks of System General Corporation, used under license by Fairchild Semiconductor.

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION, OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS. THESE SPECIFICATIONS DO NOT EXPAND THE TERMS OF FAIRCHILD'S WORLDWIDE TERMS AND CONDITIONS, SPECIFICALLY THE WARRANTY THEREIN, WHICH COVERS THESE PRODUCTS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.

As used herein:

1. Life support devices or systems are devices or systems which, (a) are
2. A critical component in any component of a life support, device, or