

# 4104B

## QUAD LOW VOLTAGE TO HIGH VOLTAGE TRANSLATOR WITH 3-STATE OUTPUTS

**DESCRIPTION** — The 4104B Quad Low Voltage to High Voltage Translator with 3-State Outputs provides the capability of interfacing low voltage circuits to high voltage circuits, such as low voltage CMOS and TTL to high voltage CMOS. It has four Data Inputs ( $I_0$ - $I_3$ ), an active HIGH Output Enable input (EO), four Data Outputs ( $Z_0$ - $Z_3$ ) and their Complements ( $\bar{Z}_0$ - $\bar{Z}_3$ ). With the Output Enable input HIGH, the Outputs ( $Z_0$ - $Z_3$ ,  $\bar{Z}_0$ - $\bar{Z}_3$ ) are in the low impedance "ON" state, either HIGH or LOW as determined by the Data Inputs; with the Output Enable input LOW, the Outputs are in the high impedance "OFF" state. The voltage level on the Output Enable input may swing between  $V_{DD1}$  and  $V_{SS}$ .

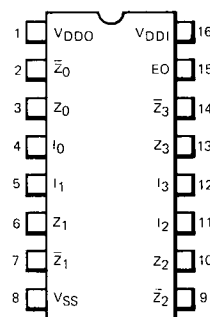
The device uses a common negative supply ( $V_{SS}$ ) and separate positive supplies for inputs ( $V_{DD1}$ ) and outputs ( $V_{DD0}$ ).  $V_{DD1}$  must always be less than or equal to  $V_{DD0}$ , even during power turn-on and turn-off. For the allowable operating range of  $V_{DD1}$  and  $V_{DD0}$  see Figure 1. Each input protection circuit is terminated between  $V_{DD0}$  and  $V_{SS}$ . This allows the input signals to be driven from any potential between  $V_{DD0}$  and  $V_{SS}$ , without regard to current limiting. When driving from potentials greater than  $V_{DD0}$  or less than  $V_{SS}$ , the current at each input must be limited to 10 mA.

When used in a bus organized system, all 4104B devices on the same bus line should be connected to the same  $V_{DD0}$  and  $V_{SS}$  supplies. Otherwise, parasitic diodes from the output to  $V_{DD0}$  and  $V_{SS}$  can become forward biased, even while the device is in the OFF state, causing catastrophic failure if the current is not limited to 10 mA.

- 3-STATE FULLY BUFFERED OUTPUTS
- OUTPUT ENABLE INPUT (ACTIVE HIGH)
- DUAL POWER SUPPLY

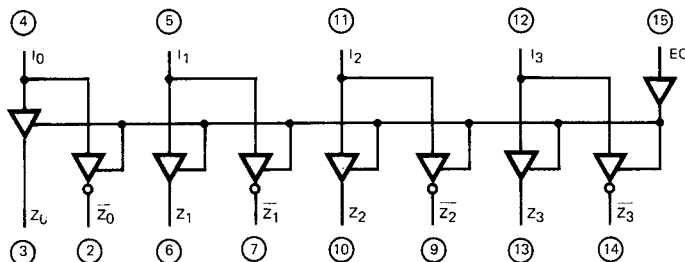
PIN NAMES	FUNCTION
$I_0$ - $I_3$	Data Inputs
EO	Output Enable Input
$Z_0$ - $Z_3$	Data Outputs
$\bar{Z}_0$ - $\bar{Z}_3$	Complimentary Data Outputs

**CONNECTION DIAGRAM  
DIP (TOP VIEW)**



**NOTE:**  
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

### LOGIC SYMBOL



$V_{DD0}$  = Pin 1  
 $V_{DD1}$  = Pin 16  
 $V_{SS}$  = Pin 8  
 ○ = Pin Number

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DC CHARACTERISTICS:  $V_{DDO} = V_{DDI}$  as shown,  $V_{SS} = 0$  V

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS	
			$V_{DDO/I} = 5$ V			$V_{DDO/I} = 10$ V			$V_{DDO/I} = 15$ V						
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX				
$V_{IH}$	Input HIGH Voltage		3.5		Note 1	7		Note 1	11		Note 1	V	All	Guaranteed Input HIGH Voltage	
$V_{IL}$	Input LOW Voltage		Note 2		1.5	Note 2		3		Note 2	4	V	All	Guaranteed Input LOW Voltage	
$V_{OH}$	Output HIGH Voltage		4.95			9.95			14.95			V	MIN, 25°C	$I_{OH} < 1 \mu A$ Note 3	
			4.95			9.95			14.95				MAX		
			4.5			9.0			13.5				All		$I_{OL} < 1 \mu A$ Note 4
$V_{OL}$	Output LOW Voltage				0.05			0.05			0.05	V	MIN, 25°C	$I_{OL} < 1 \mu A$ Note 3	
					0.05			0.05			0.05		MAX		
					0.5			1.0			1.5		All		$I_{OH} < 1 \mu A$ Note 4
$I_{IN}$	Input Current	XC									0.3	$\mu A$	MIN, 25°C	Lead Under Test at 0 V or $V_{DDO}$ . All Other Inputs Simultaneously at 0 V or $V_{DDO}$	
											1.0		MAX		
												0.1	$\mu A$		MIN, 25°C
										1.0	MAX				
$I_{OH}$	Output HIGH Current		-1.5									mA	MIN, 25°C		$V_{OUT} = 2.5$ V for $V_{DDO} = 5$ V Note 3
			-1.0												
			-0.7			-1.4			-2.2					MIN, 25°C	
			-0.4			-0.8			-1.4			MAX	-0.5 V Note 3		
$I_{OL}$	Output LOW Current		1.0			2.6			3.6			mA	MIN, 25°C	$V_{OUT} = 0.4$ V for $V_{DDO} = 5$ V $V_{OUT} = 0.5$ V for $V_{DDO} = 10$ V $V_{OUT} = 0.5$ V for $V_{DDO} = 15$ V Note 3	
			0.8			2.0			3.6				MAX		
			0.4			1.2			2.0						
$I_{OZH}$	Output OFF Current HIGH	XC									1.6	$\mu A$	MIN, 25°C		Output Returned to $V_{DDO}$ , $E_O = V_{SS}$
											12		MAX		
												0.4	$\mu A$		
											12	MAX			
$I_{OZL}$	Output OFF Current LOW	XC									-1.6	$\mu A$	MIN, 25°C	Output Returned to $V_{SS}$ , $E_O = V_{SS}$	
											-12		MAX		
												-0.4	$\mu A$		MIN, 25°C
											-12	MAX			
$I_{DD}$	Quiescent Power Supply Current	XC			20			40			80	$\mu A$	MIN, 25°C	All Inputs at 0 V or $V_{DDI} = V_{DDO}$	
					150			300			600		MAX		
					5			10			20	$\mu A$	MIN, 25°C		
					150			300			600		MAX		

NOTES:

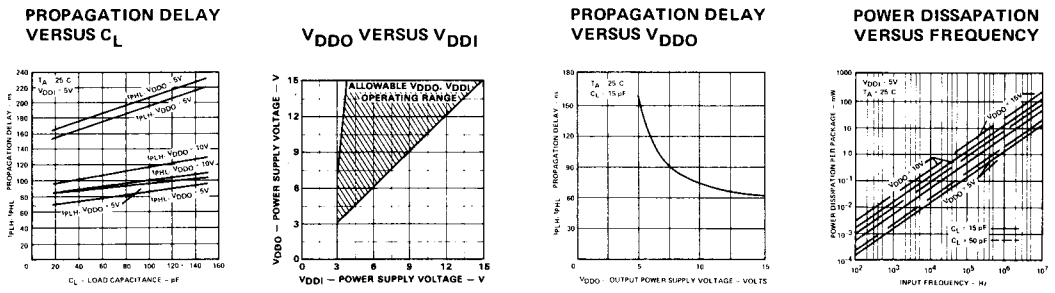
- $V_{IH}$  must be less than or equal to  $V_{DDO}$ . If  $V_{IH}$  is greater than  $V_{DDO}$ , current at each input must be limited to 10 mA.
- $V_{IL}$  must be greater than or equal to  $V_{SS}$ ; if  $V_{IL}$  is less than  $V_{SS}$ , current at each input must be limited to 10 mA.
- Inputs at 0 V or  $V_{DDO}$  per function.
- Inputs at minimum  $V_{IH}$  or maximum  $V_{IL}$  per function.
- Propagation Delays and Output Transition Times are graphically described in this section under 4000B Series CMOS Family Characteristics.

AC CHARACTERISTICS AND SET-UP REQUIREMENTS:  $V_{DD1} = 5\text{ V}$ ,  $V_{DD0}$  as shown,  $V_{SS} = 0\text{ V}$ ,  $T_A = 25^\circ\text{C}$  (See Note 5)

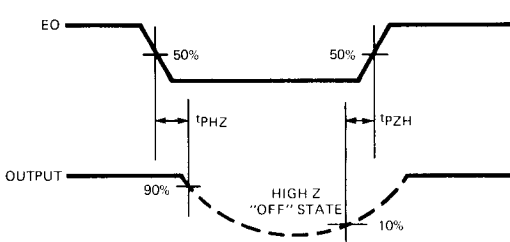
SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		$V_{DD0} = 5\text{ V}$			$V_{DD0} = 10\text{ V}$			$V_{DD0} = 15\text{ V}$				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
$t_{PLH}$	Propagation Delay, $I_n$ to $Z_n$ or $\bar{Z}_n$		160	375		85	180		75	144	ns	$C_L = 50\text{ pF}$ , $R_L = 200\text{ k}\Omega$
$t_{PHL}$			160	375		85	180		75	144		
$t_{PZH}$	Output Enable Time		200	450		80	110		70	88	ns	$(R_L = 1\text{ k}\Omega \text{ to } V_{SS})$ $(R_L = 1\text{ k}\Omega \text{ to } V_{DD0})$
$t_{PZL}$	Output Disable Time		200	450		100	170		80	136		
$t_{PHZ}$	Output Disable Time		75	165		90	170		75	136	ns	$(R_L = 1\text{ k}\Omega \text{ to } V_{SS})$ $(R_L = 1\text{ k}\Omega \text{ to } V_{DD0})$
$t_{PLZ}$	Output Disable Time		50	115		80	110		70	88		
$t_{TLH}$	Output Transition Time		60	135		30	70		25	45	ns	Input Transition Times $\leq 20\text{ ns}$
$t_{THL}$	Output Transition Time		60	135		30	70		25	45		

Notes on previous page.

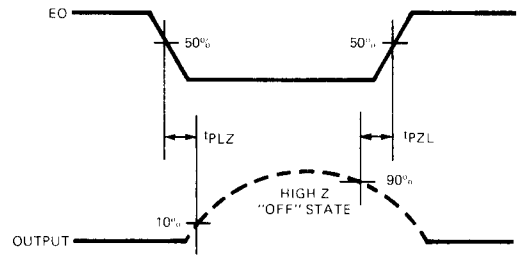
Fig. 1 TYPICAL ELECTRICAL CHARACTERISTICS



SWITCHING WAVEFORMS



OUTPUT ENABLE TIME ( $t_{PHZ}$ ) AND OUTPUT DISABLE TIME ( $t_{PHZ}$ )



OUTPUT ENABLE TIME ( $t_{PLZ}$ ) AND OUTPUT DISABLE TIME ( $t_{PLZ}$ )