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DS91M047

125 MHz Quad M-LVDS Line Driver

General Description

The DS91M047 is a high-speed quad M-LVDS line driver designed for driving clock or data signals to up to four multipoint networks.

M-LVDS (Multipoint LVDS) is a new family of bus interface devices based on LVDS technology specifically designed for multipoint and multidrop cable and backplane applications. It differs from standard LVDS in providing increased drive current to handle double terminations that are required in multipoint applications. Controlled transition times minimize reflections that are common in multipoint configurations due to unterminated stubs.

The DS91M047 accepts LVTTTL/LVCMOS input levels and translates them to M-LVDS signal levels with transition times of greater than 1 ns. The device provides the DE and \overline{DE} inputs that are ANDed together and control the TRI-STATE outputs. The DE and \overline{DE} inputs are common to all four drivers. The DS91M047 has a flow-through pinout for easy PCB layout. The DS91M047 provides a new alternative for high speed multipoint interface applications. It is packaged in a space saving SOIC-16 package.

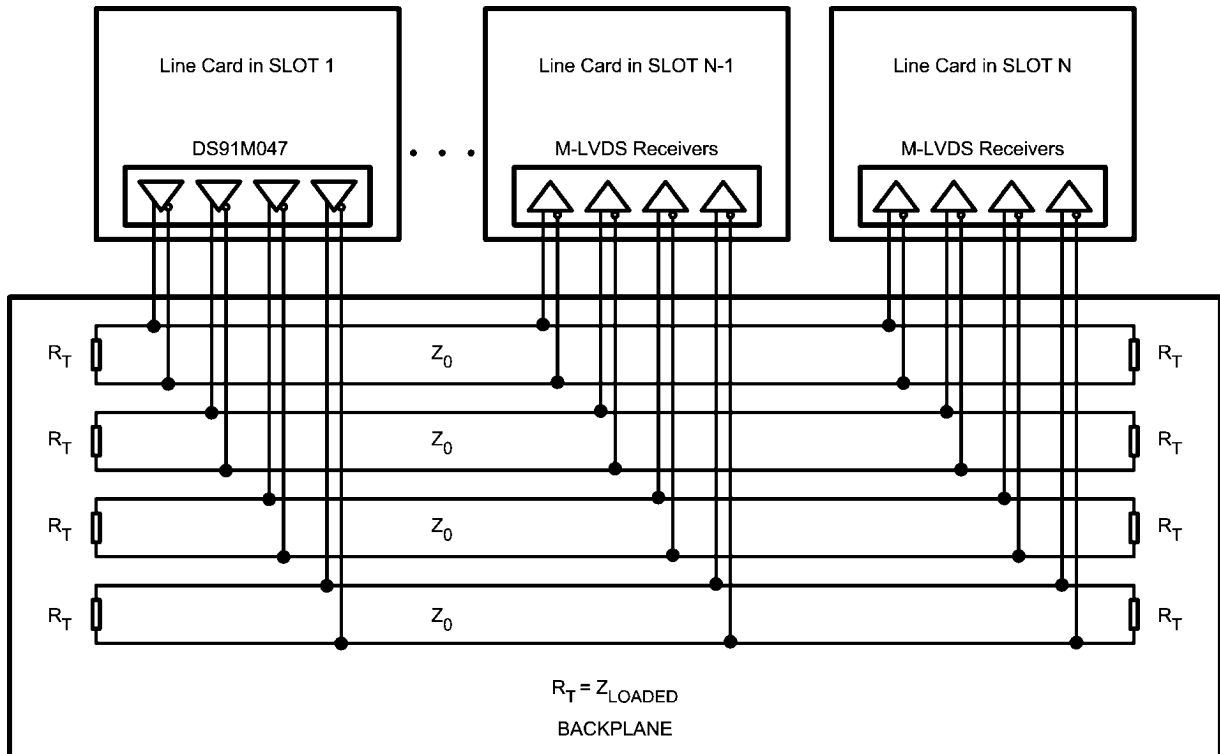
Features

- DC - 125 MHz / 250 Mbps low jitter, low skew, low power operation
- Conforms to TIA/EIA-899 M-LVDS Standard
- Controlled transition times (2 ns typ) minimize reflections
- 8 kV ESD on M-LVDS pins protects adjoining components
- Flow-through pinout simplifies PCB layout
- Industrial operating temperature range (-40°C to $+85^{\circ}\text{C}$)
- Available in a space saving SOIC-16 package

Applications

- Multidrop / Multipoint clock and data distribution
- High-Speed, Low Power, Short-Reach alternative to TIA/EIA-485/422
- Clock distribution in AdvancedTCA (ATCA) and MicroTCA (μTCA , uTCA) backplanes

Typical Application

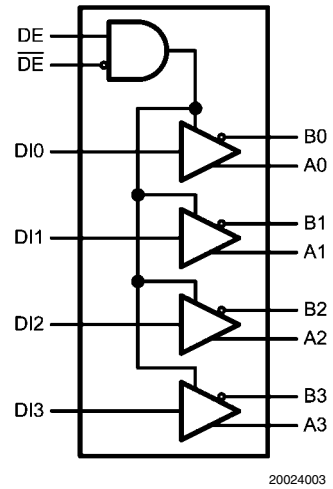
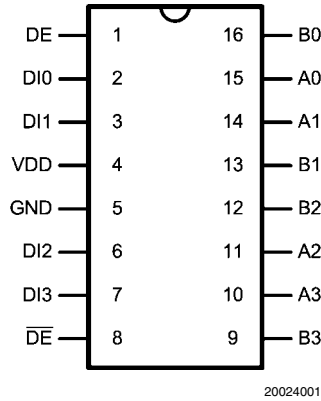


20024002

Ordering Information

Operating Temperature	Package Type / Number	Order Number
-40°C to +85°C	SOIC/M16A	DS91M047TMA

Connection Diagrams



Pin Descriptions

Pin No.	Name	Description
2, 3, 6, 7	DI	Driver input pin, LVCMOS compatible.
10, 11, 14, 15	A	Non-inverting driver output pin, M-LVDS levels.
9, 12, 13, 16	B	Inverting driver output pin, M-LVDS levels.
1	DE	Driver enable pin: When DE is low, the driver is disabled. When DE is high and \overline{DE} is low or open, the driver is enabled. If both DE and \overline{DE} are open circuit, then the driver is disabled.
8	\overline{DE}	Driver enable pin: When \overline{DE} is high, the driver is disabled. When \overline{DE} is low or open and DE is high, the driver is enabled. If both DE and \overline{DE} are open circuit, then the driver is disabled.
4	V _{DD}	Power supply pin, +3.3V ± 0.3V
5	GND	Ground pin

Truth Table

Enables		Input DI	Outputs	
DE	\overline{DE}		A	B
H	L	L	L	H
		H	H	L
All other combinations of ENABLE inputs		X	Z	Z

Absolute Maximum Ratings (Note 4)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Power Supply Voltage	-0.3V to +4V
LVC MOS Input Voltage	-0.3V to ($V_{DD} + 0.3V$)
M-LVDS Output Voltage	-1.9V to +5.5V
M-LVDS Output Short Circuit Current Duration	Continuous
Junction Temperature	+140°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature Range	
Soldering (4 sec.)	+260°C
Maximum Package Power Dissipation @ +25°C	
MA Package	2.21W
Derate MA Package	19.2 mW/°C above +25°C
Package Thermal Resistance (4-Layer, 2 oz. Cu, JEDEC)	
θ_{JA}	+52°C/W
θ_{JC}	+19°C/W

ESD Susceptibility

HBM	≥8 kV
MM	≥250V
CDM	≥1250V

Note 1: Human Body Model, applicable std. JESD22-A114C

Note 2: Machine Model, applicable std. JESD22-A115-A

Note 3: Field Induced Charge Device Model, applicable std. JESD22-C101-C

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage (VDD)	+3.0	+3.3	+3.6	V
Voltage at Any Bus Terminal (Separate or Common-Mode)	-1.4		+3.8	V
High Level Input Voltage (V_{IH})	2.0		V_{DD}	V
Low Level Input Voltage (V_{IL})	0		0.8	V
Operating Free Air Temperature (T_A)	-40	+25	+85	°C

DC Electrical Characteristics (Note 5, Note 6, Note 7, Note 9)

Over supply voltage and operating temperature ranges, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
LVC MOS DC Specifications						
V_{IH}	High-Level Input Voltage		2.0		V_{DD}	V
V_{IL}	Low-Level Input Voltage		GND		0.8	V
I_{IH}	High-Level Input Current	$V_{IH} = 3.6V$	-15	±1	15	μA
I_{IL}	Low-Level Input Current	$V_{IL} = 0V$	-15	±1	15	μA
V_{CL}	Input Clamp Voltage	$I_{IN} = -18 mA$	-1.5			V
M-LVDS DC Specifications						
$ V_{AB} $	Differential Output Voltage Magnitude	$R_L = 50\Omega, C_L = 5 pF$ Figures 1, 3	480		650	mV
ΔV_{AB}	Change in Differential Output Voltage Magnitude Between Logic States		-50		50	mV
$V_{OS(SS)}$	Steady-State Common-Mode Output Voltage	Figures 1, 2 $R_L = 50\Omega$	0.30	1.6	2.10	V
$ \Delta V_{OS(SS)} $	Change in Steady-State Common-Mode Output Voltage Between Logic States		0		50	mV
$V_{A(OC)}$	Maximum Steady-State Open-Circuit Output Voltage	Figure 4	0		2.4	V
$V_{B(OC)}$	Maximum Steady-State Open-Circuit Output Voltage		0		2.4	V
$V_{P(H)}$	Voltage Overshoot, Low-to-High Level Output <small>(Note 10)</small>	$R_L = 50\Omega, C_L = 5 pF$ $C_D = 0.5 pF$, Figures 6, 7			$1.2V_{SS}$	V
$V_{P(L)}$	Voltage Overshoot, High-to-Low Level Output <small>(Note 10)</small>		-0.2 V_{SS}			V
I_{OS}	Output Short-Circuit Current <small>(Note 8)</small>	Figure 5	-43		43	mA
I_A	Driver High-Impedance Output Current	$V_A = 3.8V, V_B = 1.2V$	0		32	μA
		$V_A = 0V$ or $2.4V, V_B = 1.2V$	-20		20	μA
		$V_A = -1.4V, V_B = 1.2V$	-32		0	μA
I_B	Driver High-Impedance Output Current	$V_A = 3.8V, V_B = 1.2V$	0		32	μA
		$V_A = 0V$ or $2.4V, V_B = 1.2V$	-20		20	μA
		$V_A = -1.4V, V_B = 1.2V$	-32		0	μA
I_{AB}	Driver High-Impedance Output Differential Current ($I_A - I_B$)	$V_A = V_B, -1.4V \leq V \leq 3.8V$	-4		4	μA

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$I_{A(OFF)}$	Driver High-Impedance Output Power-Off Current	$V_A = 3.8V, V_B = 1.2V$ $DE = 0V$ $0V \leq V_{DD} \leq 1.5V$	0		32	μA
		$V_A = 0V \text{ or } 2.4V, V_B = 1.2V$ $DE = 0V$ $0V \leq V_{DD} \leq 1.5V$	-20		20	μA
		$V_A = -1.4V, V_B = 1.2V$ $DE = 0V$ $0V \leq V_{DD} \leq 1.5V$	-32		0	μA
$I_{B(OFF)}$	Driver High-Impedance Output Power-Off Current	$V_A = 3.8V, V_B = 1.2V$ $DE = 0V$ $0V \leq V_{DD} \leq 1.5V$	0		32	μA
		$V_A = 0V \text{ or } 2.4V, V_B = 1.2V$ $DE = 0V$ $0V \leq V_{DD} \leq 1.5V$	-20		20	μA
		$V_A = -1.4V, V_B = 1.2V$ $DE = 0V$ $0V \leq V_{DD} \leq 1.5V$	-32		0	μA
$I_{AB(OFF)}$	Driver High-Impedance Output Power-Off Current ($I_{A(OFF)} - I_{B(OFF)}$)	$V_A = V_B, -1.4V \leq V \leq 3.8V$ $DE = 0V$ $0V \leq V_{DD} \leq 1.5V$	-4		4	μA
C_A	Driver Output Capacitance	$V_{DD} = 0V$		7.8		pF
C_B	Driver Output Capacitance			7.8		pF
C_{AB}	Driver Output Differential Capacitance			3		pF
$C_{A/B}$	Driver Output Capacitance Balance (C_A/C_B)			1		
I_{CC}	Power Supply Current	$R_L = 50\Omega$ (All Outputs) $DI = V_{DD}$ or GND (All Inputs) $DE = V_{DD}, \overline{DE} = GND$ $f = 125 \text{ MHz}$		65	75	mA
I_{CCZ}	TRI-STATE Power Supply Current	$R_L = 50\Omega$ (All Outputs) $DI = V_{DD}$ or GND (All Inputs) $DE = GND, \overline{DE} = V_{DD}$		19	24	mA

Note 4: "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The Recommended Operating Conditions indicate conditions at which the device is functional and the device should not be operated beyond such conditions.

Note 5: The Electrical Characteristics tables list guaranteed specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not guaranteed.

Note 6: Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground except V_{OD} and ΔV_{OD} .

Note 7: Typical values represent most likely parametric norms for $V_{DD} = +3.3V$ and $T_A = +25^\circ C$, and at the Recommended Operation Conditions at the time of product characterization and are not guaranteed.

Note 8: Output short circuit current (I_{OS}) is specified as magnitude only, minus sign indicates direction only.

Note 9: C_L includes fixture capacitance and C_D includes probe capacitance.

Note 10: Specification is guaranteed by characterization and is not tested in production.

Switching Characteristics (Note 11, Note 12, Note 18)

Over supply voltage and operating temperature ranges, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHL}	Differential Propagation Delay High to Low	$R_L = 50\Omega$ $C_L = 5\text{ pF}$ $C_D = 0.5\text{ pF}$ Figures 6, 7	1.5	3.1	5.0	ns
t_{PLH}	Differential Propagation Delay Low to High		1.5	3.1	5.0	ns
t_{SKD1}	Differential Pulse Skew $ t_{PHL} - t_{PLH} $ (Note 13, Note 14)		0	70	140	ps
t_{SKD2}	Channel-to-Channel Skew (Note 13, Note 15)		0	70	200	ps
t_{SKD3}	Differential Part-to-Part Skew (Note 13, Note 16) (Constant T_A and V_{DD})		0	0.8	1.5	ns
t_{SKD4}	Differential Part-to-Part Skew (Note 17)		0		3.5	ns
t_{TLH}	Rise Time (Note 13)		1.1	2.0	3.0	ns
t_{THL}	Fall Time (Note 13)	1.1	2.0	3.0	ns	
t_{PHZ}	Disable Time High to Z	$R_L = 50\Omega$ $C_L = 5\text{ pF}$ $C_D = 0.5\text{ pF}$ Figures 8, 9		7	12.5	ns
t_{PLZ}	Disable Time Low to Z			7	12.5	ns
t_{PZH}	Enable Time Z to High			7	12.5	ns
t_{PZL}	Enable Time Z to Low			7	12.5	ns
f_{MAX}	Maximum Operating Frequency		(Note 13)	125		

Note 11: The Electrical Characteristics tables list guaranteed specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not guaranteed.

Note 12: Typical values represent most likely parametric norms for $V_{DD} = +3.3V$ and $T_A = +25^\circ C$, and at the Recommended Operation Conditions at the time of product characterization and are not guaranteed.

Note 13: Specification is guaranteed by characterization and is not tested in production.

Note 14: t_{SKD1} , $|t_{PLHD} - t_{PHLD}|$, Pulse Skew, is the magnitude difference in differential propagation delay time between the positive going edge and the negative going edge of the same channel.

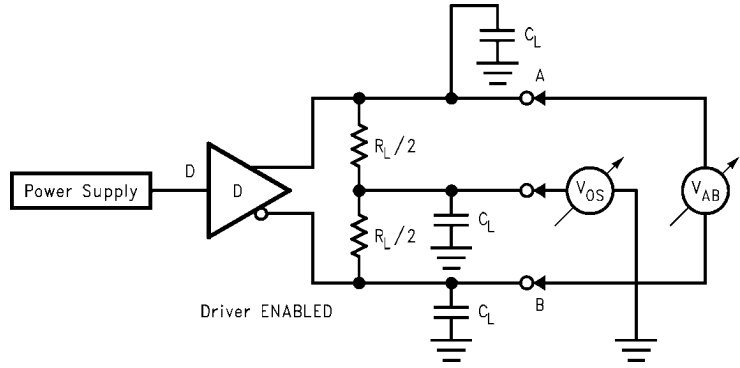
Note 15: t_{SKD2} , Channel-to-Channel Skew, is the difference in propagation delay (t_{PLHD} or t_{PHLD}) among all output channels.

Note 16: t_{SKD3} , Part-to-Part Skew, is defined as the difference between the minimum and maximum differential propagation delays. This specification applies to devices at the same V_{DD} and within $5^\circ C$ of each other within the operating temperature range.

Note 17: t_{SKD4} , Part-to-Part Skew, is the differential channel-to-channel skew of any event between devices. This specification applies to devices over recommended operating temperature and voltage ranges, and across process distribution. t_{SKD4} is defined as $|Max - Min|$ differential propagation delay.

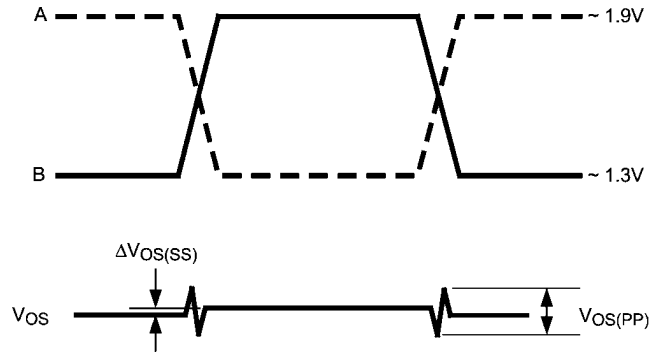
Note 18: C_L includes fixture capacitance and C_D includes probe capacitance.

Parameter Measurement Information



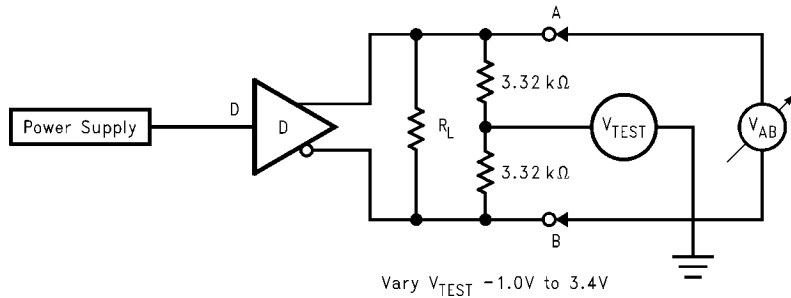
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FIGURE 1. Differential Driver Test Circuit



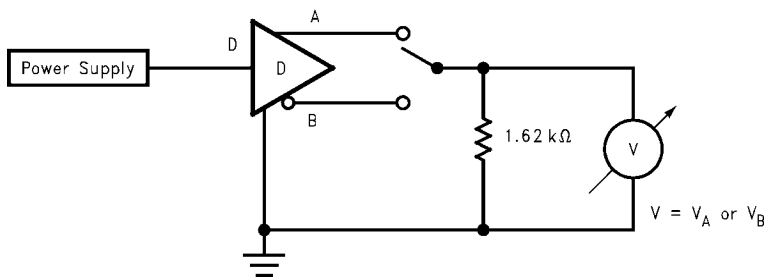
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FIGURE 2. Differential Driver Waveforms



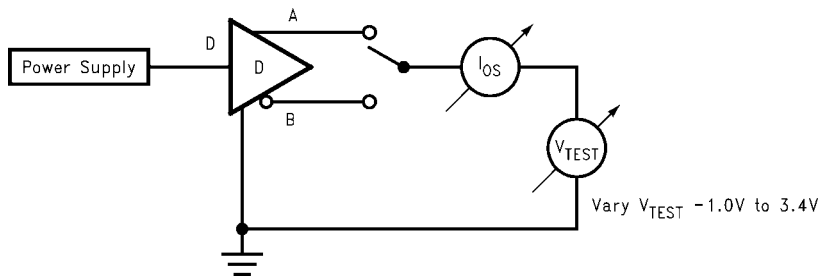
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FIGURE 3. Differential Driver Full Load Test Circuit



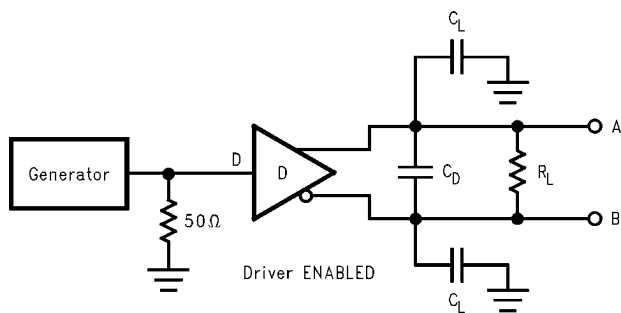
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FIGURE 4. Differential Driver DC Open Test Circuit



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FIGURE 5. Differential Driver Short-Circuit Test Circuit



20024004

FIGURE 6. Driver Propagation Delay and Transition Time Test Circuit

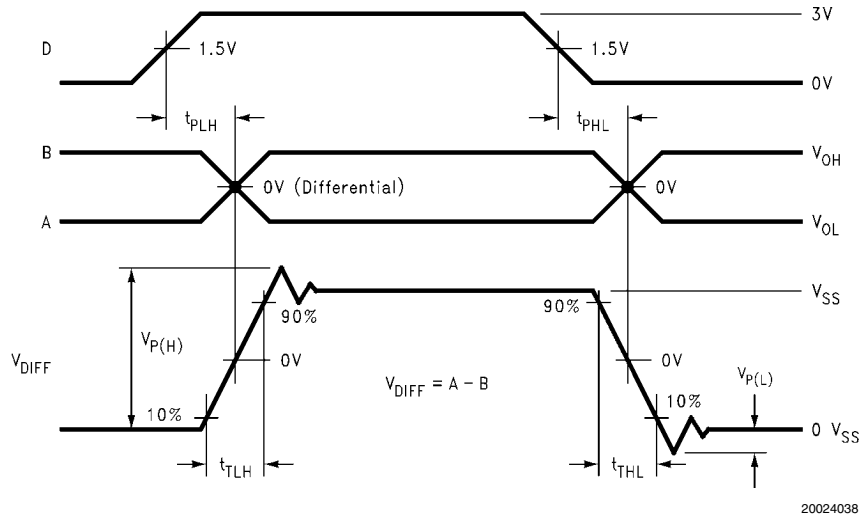


FIGURE 7. Driver Propagation Delay and Transition Time Waveforms

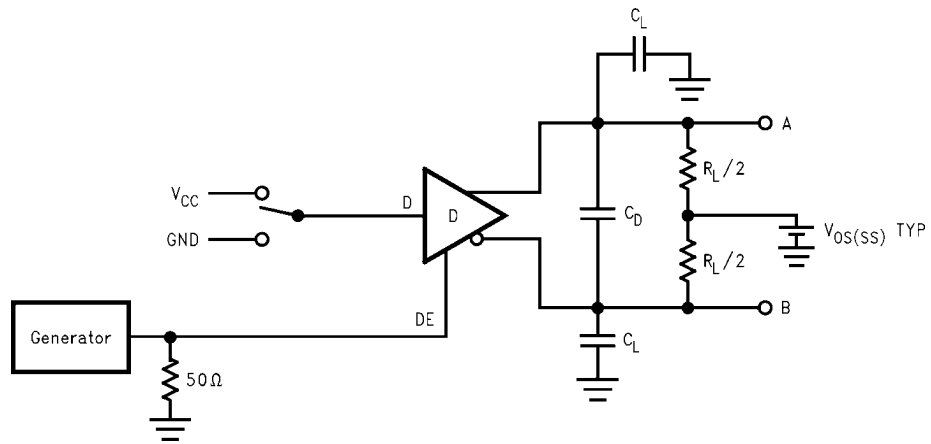


FIGURE 8. Driver TRI-STATE Delay Test Circuit

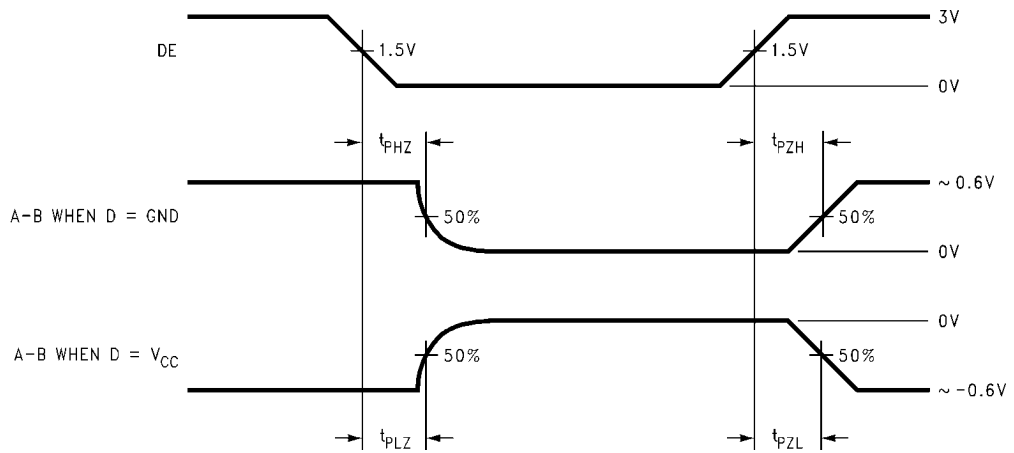
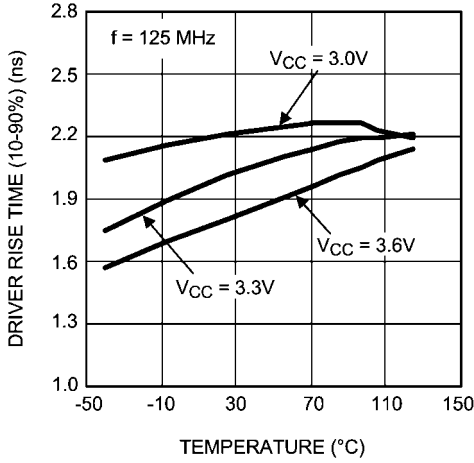
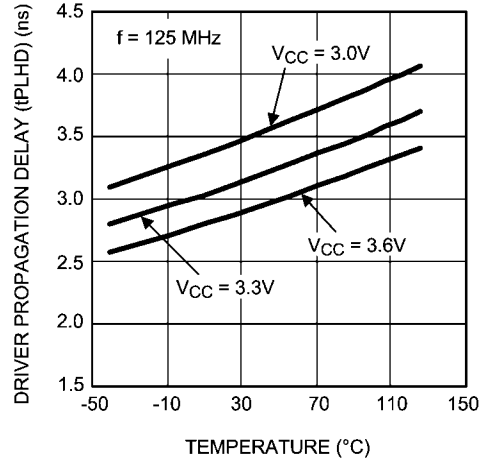


FIGURE 9. Driver TRI-STATE Delay Waveforms

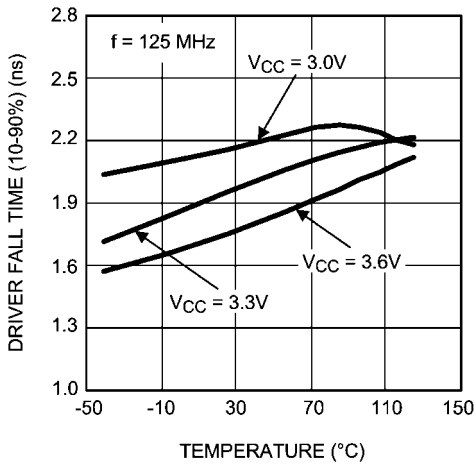
Typical Performance Characteristics



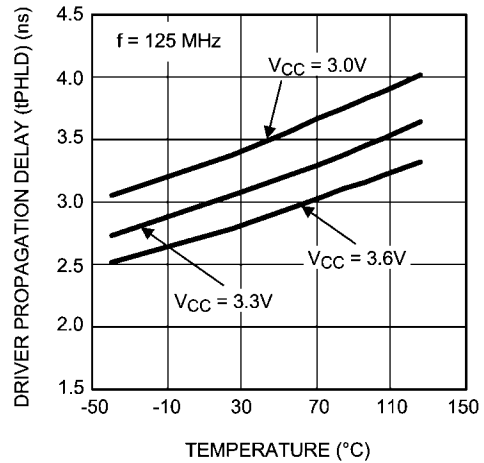
20024050
Driver Rise Time as a Function of Temperature



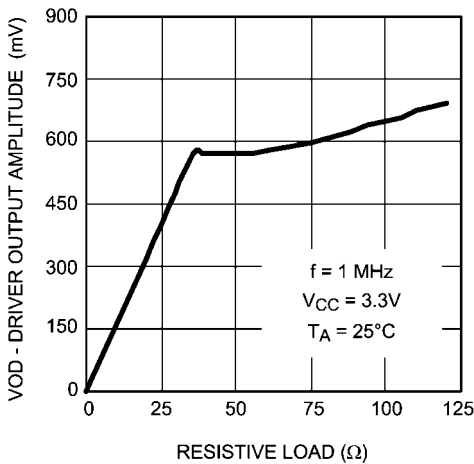
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Driver Propagation Delay (t_{PLHD}) as a Function of Temperature



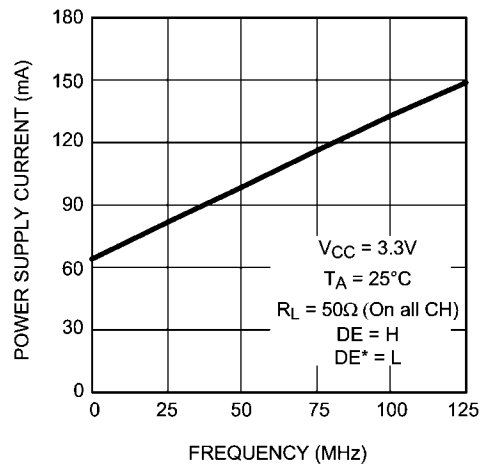
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Driver Fall Time as a Function of Temperature



20024053
Driver Propagation Delay (t_{PLHD}) as a Function of Temperature

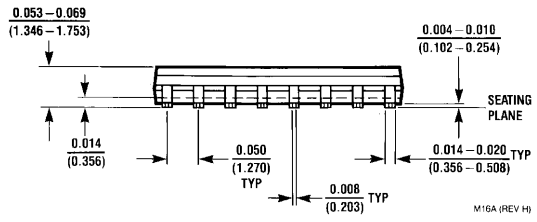
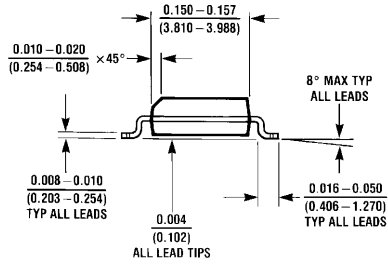
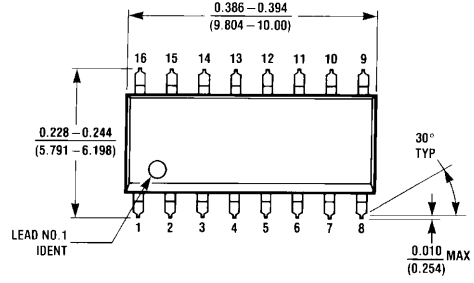


20024058
Driver Output Signal Amplitude as a Function of Resistive Load



20024054
Driver Power Supply Current as a Function of Frequency

Physical Dimensions inches (millimeters) unless otherwise noted



**16-Lead (0.150 Wide) Molded Small Outline Package, JEDEC
Order Number DS91M047TMA
NS Package Number M16A**

M16A (REV H)

Notes

Notes

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