MAX8930

WLED Charge Pump, RGB, OLED Boost, LDOs with ALC and CAI

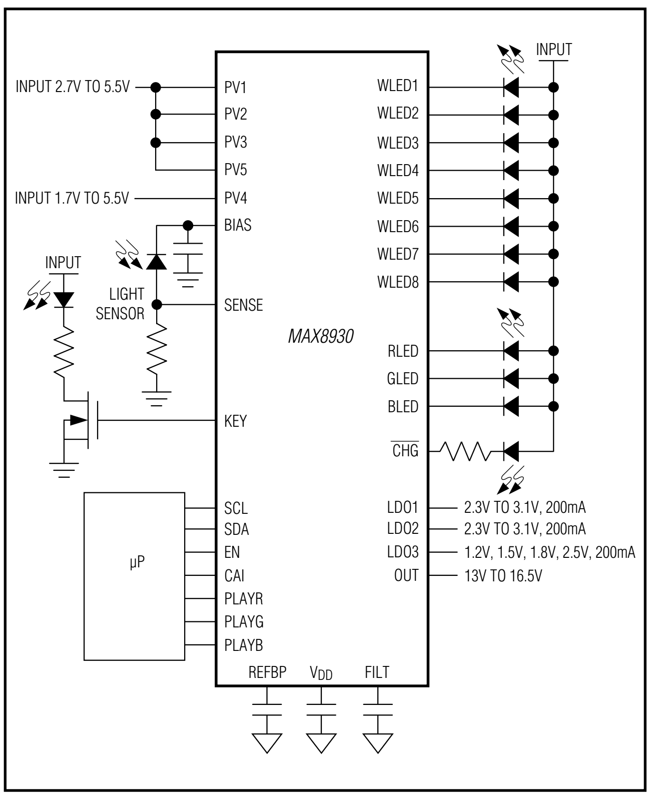
General Description

The MAX8930 integrates a charge pump for white LED display backlighting with ambient light control (ALC) feature. The high-efficiency, adaptive-mode 1x/-0.5x charge pump drives up to 11 LEDs (8 WLEDs + RGB LED) with constant current for uniform brightness. The LED current is adjustable from 0.1mA to 25.6mA in 256 linear steps through I²C. High accuracy and LED-to-LED current matching are maintained throughout the adjustment range. The MAX8930 includes soft-start, thermal shutdown, open-circuit, and short-circuit protection.

Three 200mA LDOs are provided with programmable output voltages to provide power to external circuitry. These three LDOs can also be configured for a GPO function through the I²C. A step-up converter is also available on the MAX8930 for biasing a PMOLED sub-panel.

The MAX8930 is available in the 49-bump, 3.17mm x 3.17mm WLP package.

Simplified Application Circuit



Features

- ♦ White LED Charge Pump
- ♦ Adaptive 1x or -0.5x Negative Modes
- ♦ 11 Low-Dropout LED Current Sinks with 25.6mA to 0.1mA in 256 Dimming Steps
- ♦ Ramp-Up/Down Control for Main White LED
- ♦ Ramp-Up/Down Control for RGB LED
- ♦ Individual Brightness Control for Each White, RGB LED
- ♦ Low 240µA (typ) Quiescent Current
- ♦ Ambient Light Control (ALC) for Any Type of Light Sensor
- ♦ Content Adaptive Interface
- ♦ I²C-Compatible Control Interface
- ♦ Three Programmable LDOs Up to 200mA
- ♦ Step-Up DC-DC Converter with Programmable Output for PMOLED Application
- ♦ Low 0.1µA Shutdown Current
- ♦ 2.7V to 5.5V Supply Voltage Range
- ♦ Thermal Shutdown
- ♦ Open and Short-Circuit Protection

Applications

Cell Phones and Smartphones

PDAs, Digital Cameras, Camcorders, and Other Portable Equipment

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX8930EWJ+	-40°C to +85°C	49 WLP 0.4mm pitch

+Denotes a lead(Pb)-free/RoHS-compliant package.

Typical Operating Circuit appears at end of data sheet.

ABSOLUTE MAXIMUM RATINGS

PV_, V_{DD}, EN, CAI, PLAY_, BIAS,
SENSE, REFBP, ECAGND to AGND.................-0.3V to +6.0V
PV_, V_{DD}, PGND_, AGND to NEG ....-0.3V to +6.0V
ECAGND, PGND_ to AGND................................-0.3V to +0.3V
WLED_, RGB_, C1N, C2N,
C1P, C2P to NEG.........-0.3V to (V_{PV1} + V_{PV2} + V_{PV3} + 0.3V)
FILT to AGND... -0.3V to (V_{PV3} + 0.3V)
SCL, SDA to AGND................................. -0.3V to (V_{DD} + 0.3V)
LDO_ to AGND........................... -0.3V to (V_{PV3} + V_{PV4} + 0.3V)
SW to PGND3... -0.3V to (V_{PV5} + 0.3V)
LX, OUT to PGND3 ....-0.3V to +22V
KEY to AGND ....-0.3V to (V_{PV3} + 0.3V)
Continuous Power Dissipation (T_A = +70°C)
49-Pin WLP 3.17mm x 3.17mm
(derate 20mW/°C above +70°C)...............................1600mW
Operating Temperature Range.......................... -40°C to +85°C
Junction Temperature ....+150°C
Storage Temperature Range........................... -65°C to +150°C
Soldering Temperature (reflow) ....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

($V_{PV\_}$ = V_{EN} = V_{DD} = 3.7V, $V_{PGND\_}$ and V_{AGND} = 0V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
PV1, PV2, PV3, PV5 Operating Voltage			2.7		5.5	V
Undervoltage Lockout Threshold	V_{PV1}, V_{PV2}, V_{PV3}, V_{PV5} rising		2.25	2.45	2.65	V
UVLO Hysteresis				100		mV
PV4 Operating Voltage			1.7		5.5	V
V_{DD} Operating Range	V_{DD} is supply voltage for I²C input block only; all other logic is supplied from PV_		1.7		5.5	V
PV_ Shutdown Supply Current 1 (All Outputs Off, I²C Disabled)	EN = AGND, V_{DD} = 0V	T_A = +25°C		0.1	1	µA
		T_A = +85°C		0.1		
PV_ Shutdown Supply Current 2 (All Outputs Off, I²C Enabled)	V_{DD} = V_{PV3}, EN = AGND	T_A = +25°C		2	10	µA
		T_A = +85°C		2		
V_{DD} Shutdown Threshold	V_{DD} falling, hysteresis = 50mV		1.15	1.4	1.65	V
Supply Current	1x mode, no load, ALC off, step-up off, $I_{LDO\_}$ = 0mA			240	400	µA
	-0.5x mode, 4MHz switching, each $I_{LED\_}$ = 0.1mA, ALC off, I_{LDO} = 0mA, step-up I_o = 0mA at V_{PV3} = 2.7V (Note 2)			6.8		mA
Reference Bypass (REFBP) Output Voltage	0µA ≤ I_{REFBP} ≤ 1µA		1.164	1.200	1.236	V
REFBP Supply Rejection	2.5V ≤ V_{PV3} ≤ 5.5V			0.2	5	mV
Thermal Shutdown				+160		°C
Thermal Shutdown Hysteresis				20		°C

I2C INTERFACE CHARACTERISTICS

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
SDA, SCL Input High Voltage	V_{DD} = 1.7V to 5.5V		0.7 x V_{DD}			V
SDA, SCL Input Low Voltage	V_{DD} = 1.7V to 5.5V				0.3 x V_{DD}	V
SDA, SCL Input Current	V_{IL} = 0V or V_{IH} = 5.5V, V_{DD} = 5.5V	T_A = +25°C		0.01	1	µA
		T_A = +85°C		0.1		
SDA Output Low Voltage	I_{SDA} = 3mA, for acknowledge (Note 3)			0.03	0.4	V
Clock Frequency	(Note 3)		100		400	kHz
Bus-Free Time Between START and STOP	t_{BUF} (Note 3)		1.3			µs
Hold Time Repeated START Condition	$t_{HD,STA}$ (Note 3)		0.6	0.1		µs
SCL Low Period	t_{LOW} (Note 3)		1.3	0.2		µs
SCL High Period	t_{HIGH} (Note 3)		0.6	0.2		µs
Setup Time Repeated START Condition	$t_{SU,STA}$ (Note 3)		0.6	0.1		µs
SDA Hold Time	$t_{HD,DAT}$ (Note 3)		0	0.01		µs
SDA Setup Time	$t_{SU,DAT}$ (Note 3)		100	50		ns
Setup Time for STOP Condition	$t_{SU,STO}$ (Note 3)		0.6	0.1		µs

CHARGE PUMP CHARACTERISTICS

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Switching Frequency			4		MHz
Pump Soft-Start Time			0.5		ms
Charge-Pump Regulation Voltage (and OVP)	V_{PV1}, V_{PV2} - V_{NEG}	4.3	5		V
Open-Loop NEG Output Resistance	(0.5 x (V_{PV1} or V_{PV2}) - V_{NEG})/I_{NEG}		1.3	2.49	Ω
Guaranteed Output Current	LED V_{FMAX} = 3.9V, V_{PV1} = V_{PV2} = 3.2V	281			mA
NEG Discharge Resistance in Shutdown	All LEDs off		10		kΩ

CURRENT SINK DRIVER CHARACTERISTICS

PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
Current Setting Range	WLED1–WLED8, RGB programmable by I^2C			0.1		25.6	mA
WLED_, RGB Ramp-Up/Ramp-Down Time	Main WLED_ and RGB ramp-up/ramp-down in 0.1mA increments; 8 steps are programmable through I^2C; ramp-up and ramp-down times are set separately				0 (default)		ms/ 0.1mA
					0.016		
					0.064		
					0.128		
					0.256		
					0.512		
					1.024		
					2.048		
WLED_, RGB Current Accuracy	25.6mA setting, T_A = +25°C			-2.5		+2.5	%
	0.1mA setting, T_A = +25°C			-50	±10	+50	
WLED_, RGB Current Matching	WLED1–WLED8, RGB (Note 4)				5	10	%
WLED_, RGB R_{DSON}	1x mode				2.68		Ω
	-0.5x mode				4.12		
WLED_, RGB Current Regulator Dropout Voltage	25.6mA setting (Note 5)	1x mode	T_A = 0°C to +85°C		62	120	mV
			T_A = -40°C		62	150	
		-0.5x mode			95	200	
WLED_, RGB Current Regulator Switchover Threshold (1x to -0.5x)	V_{LED} falling			125	150	175	mV
WLED_, RGB Current Regulator Switchover Hysteresis					100		mV
WLED_, RGB Leakage in Shutdown	All LEDs off	T_A = +25°C			0.01	5	µA
		T_A = +85°C			0.1		

LDO1 CHARACTERISTICS

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage V_{LDO1} (Default)	200mA at V_{PV3} = 3.6V	2.522	2.6	2.678	V
Programmable Output Voltage	I_{LDO1} = 50mA	2.231	2.3	2.369	V
		2.425	2.5	2.575	
		2.522	2.6	2.678	
		2.619	2.7	2.781	
		2.716	2.8	2.884	
		2.813	2.9	2.987	
		2.910	3.0	3.090	
		3.007	3.1	3.193	
Output Current		200			mA
Current Limit	V_{LDO1} = 90% of nominal regulation voltage (Note 3)	250	475	750	mA
Dropout Voltage	I_{LDO1} = 200mA, T_A = +25°C		120	300	mV
Line Regulation	3.4V ≤ $V_{PV3\_}$ ≤ 5.5V, I_{LDO1} = 150mA		2.4		mV
Load Regulation	1mA < I_{LDO1} < 200mA		25		mV

LDO1 CHARACTERISTICS (continued)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Power-Supply Rejection $\Delta V_{LDO1}/\Delta V_{PV3}$	f = 10Hz to 10kHz, I_{LDO1} = 10mA, C_{LDO1} = 1µF		60		dB
Output Noise Voltage (RMS)	f = 100Hz to 100kHz, I_{LDO1} = 10mA, C_{LDO1} = 1µF		45		$µV_{RMS}$
Minimum Output Capacitor	I_{LDO1} < 200mA		1		µF
Startup Time from Shutdown	I_{LDO1} = 150mA (Note 3)		40	100	µs
Startup Transient Overshoot	I_{LDO1} = 150mA (Note 3)		3	50	mV
Shutdown Output Impedance	LDO1 disabled through I^2C (default on)		1		kΩ

LDO2 CHARACTERISTICS

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage V_{LDO2} (Default)	200mA at V_{PV3} = 3.6V	2.813	2.9	2.987	V
Programmable Output Voltage	I_{LDO2} = 50mA	2.231	2.3	2.369	V
		2.425	2.5	2.575	
		2.522	2.6	2.678	
		2.619	2.7	2.781	
		2.716	2.8	2.884	
		2.813	2.9	2.987	
		2.910	3.0	3.090	
		3.007	3.1	3.193	
Output Current		200			mA
Current Limit	V_{LDO2} = 90% of nominal regulation voltage (Note 4)	250	475	750	mA
Dropout Voltage	I_{LDO2} = 200mA, T_A = +25°C		120	300	mV
Line Regulation	3.4V ≤ $V_{PV3\_}$ ≤ 5.5V, I_{LDO2} = 150mA		2.4		mV
Load Regulation	1mA < I_{LDO2} < 200mA		25		mV
Power-Supply Rejection $\Delta V_{LDO2}/\Delta V_{PV3}$	f = 10Hz to 10kHz, I_{LDO2} = 10mA, C_{LDO2} = 1µF		60		dB
Output Noise Voltage (RMS)	f = 100Hz to 100kHz, I_{LDO2} = 10mA, C_{LDO2} = 1µF		45		$µV_{RMS}$
Minimum Output Capacitor	I_{LDO2} < 200mA		1		µF
Startup Time from Shutdown	I_{LDO2} = 150mA (Note 3)		40	100	µs
Startup Transient Overshoot	I_{LDO2} = 150mA (Note 3)		3	50	mV
Shutdown Output Impedance	LDO2 disabled through I^2C (default on)		1		kΩ

LDO3 CHARACTERISTICS

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Operating Range	V_{PV4}	1.7		5.5	V
Output Voltage V_{LDO3}	200mA at V_{PV4} = 2.4V	1.764	1.80	1.854	V
Programmable Output Voltage	V_{PV4} = 1.8V, I_{LDO3} = 50mA	1.164	1.2	1.236	V
		1.455	1.5	1.545	
	V_{PV4} = 3.7V, I_{LDO3} = 50mA	1.764	1.80	1.854	
		2.425	2.5	2.575	
Output Current				200	mA
Current Limit	V_{LDO3} = 90% of nominal regulation voltage (Note 4)	250	475	750	mA
Dropout Voltage	I_{LDO3} = 200mA, T_A = +25°C		120	300	mV
Line Regulation	2.4V ≤ V_{PV4} ≤ 5.5V, I_{LDO3} = 150mA		2.4		mV
Load Regulation	1mA < I_{LDO3} < 200mA		25		mV
Power-Supply Rejection $\Delta V_{LDO3}/\Delta V_{PV4}$	f = 10Hz to 10kHz, I_{LDO3} = 10mA, C_{LDO3} = 2.2µF		60		dB
Output Noise Voltage (RMS)	f = 100Hz to 100kHz, I_{LDO3} = 10mA, C_{LDO3} = 2.2µF		75		$µV_{RMS}$
Minimum Output Capacitor	0µA < I_{LDO3} < 200mA (Note 3)	2.2			µF
Startup Time from Shutdown	I_{LDO3} = 150mA (Note 3)		100	250	µs
Startup Transient Overshoot	I_{LDO3} = 150mA (Note 3)		3	50	mV
Shutdown Output Impedance	LDO3 disabled through I^2C (default on)		1		kΩ

STEP-UP CONVERTER CHARACTERISTICS

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Operating Range	V_{PV5}		2.7		5.5	V
Line Regulation	V_{OUT} = 14V, I_{OUT} = 5mA, V_{PV5} = 2.7V to 5.5V			0.1		%/V
Load Regulation	V_{OUT} = 14V, I_{OUT} = 0mA to 5mA, V_{PV5} = 3.7V			0.1		%/mA
LX Voltage Range					20	V
LX Switch Current Limit			192	241	289	mA
LX Leakage Current	V_{LX} = 20V, step-up converter disabled	T_A = +25°C		0.01	2	µA
		T_A = +85°C		0.1		
Isolation pMOS $R_{DS(ON)}$	V_{PV5} = 2.7V, I_{SW} = 100mA			1.5	2.4	Ω
pMOS Rectifier $R_{DS(ON)}$	LX to OUT, V_{PV5} = 3.7V, I_{LX} = 100mA			4.0		Ω
Isolation pMOS Current Limit	V_{PV5} = 3.7V, V_{SW} = 0V		0.15	0.3	0.6	A
Isolation pMOS Leakage Current	SW = PGND3, V_{PV5} = 5.5V	T_A = +25°C		0.01	1	µA
		T_A = +85°C		0.1		
SW Soft-Start Time	V_{PV5} = 2.7V			0.2		ms
nMOS $R_{DS(ON)}$	V_{PV5} = 3.7V, I_{LX} = 100mA			0.9	1.5	Ω
Maximum LX On-Time			8	11	14	µs
Minimum LX Off-Time	V_{OUT} > 12V		1.6	2	2.4	µs
OVP Threshold	No feedback, V_{OUT} rising		17.6	18.5	19.4	V
OVP Threshold Hysteresis				1		V

STEP-UP CONVERTER CHARACTERISTICS (continued)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Current Limit Propagation Delay (LX)				55		ns
Output Voltage Accuracy	V_{PV5} = 3.7V, I_{OUT} = 0mA	T_A = 0°C to +85°C	-2		+2	%
		T_A = -40°C	-2.5		+2.5	
Programmable Output Voltage	V_{PV5} = 3.7V, I_{OUT} = 0mA			13.0		V
				13.5		
				14.0		
				14.5		
				15.0		
				15.5		
				16.0		
				16.5		

AMBIENT LIGHT SENSOR INTERFACE

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
BIAS Output Voltage	I_{BAIS} = 200µA, V_{PV3} = 3.2V to 5.5V		2.85	3.0	3.15	V
BIAS Output Current	V_{BIAS} = 3.0V ±5%				30	mA
BIAS Dropout Voltage	I_{BIAS} = 10mA (Note 3)			125	250	mV
SENSE Input Voltage Range			0		V_{BIAS} x 255/256	V
BIAS Discharge Resistance in Shutdown				1.0	1.5	kΩ
ADC Resolution				8		Bit
ADC Integral Nonlinearity Error			-3		+3	LSB
ADC Differential Nonlinearity Error			-1		+1	LSB
SENSE Input Impedance	T_A = +25°C (Note 3)		1			MΩ
Waiting Time for ADC Movement After ALCEN = 1	V_{BIAS} = 3V	Bit 0 = 0 in 02h register		32		ms
		Bit = 1 in 02h register		64 (default)		ms

KEY CHARACTERISTICS

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Low-Level Output Voltage	I_{SINK} = 1mA				0.4	V
High-Level Output Voltage	I_{SOURCE} = 1mA		1.8			V
nMOS Output Leakage Current	At complementary output, V_{PV3} = 3.7V (Note 6)	T_A = +25°C		0.01	1	µA
		T_A = +85°C		0.1		
pMOS Output Leakage Current	At complementary output, V_{PV3} = 3.7V (Note 6)	T_A = +25°C		0.01	1	µA
		T_A = +85°C		0.1		

CAI CHARACTERISTICS

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
PWM Low-Level Input Voltage					0.4	V
PWM High-Level Input Voltage			1.4			V
PWM Dimming Frequency	C_{FILT} = 0.1µF (Note 3)		0.1	0.2	15	kHz
Current Dimming Range	Duty cycle = 0% to 100% (Note 3)		0		25.6	mA
PWM Dimming Resolution	1% ≤ duty cycle ≤ 100% (Note 3)			0.256		mA/%
CAI Enable Blanking Time (t_B)	Time from CAI enable until dimming control switches to CAI input (Note 4)			10		ms
Input Leakage Current	CAI = GND or V_{CAI} = 3.7V	T_A = +25°C		0.1	1	µA
		T_A = +85°C		1		

GPO (OPEN-DRAIN OUTPUT) CHARACTERISTICS

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Low-Level Output Voltage	I_{SINK} = 1mA				0.2	V
Output Leakage Current	$V_{LDO\_\_}$ = 2.6V	T_A = +25°C		0.1		µA
		T_A = +85°C		1		

EN CHARACTERISTICS

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Low-Level Input Voltage					0.4	V
High-Level Input Voltage			1.4			V
Input Leakage Current	V_{EN} = 0V or 3.7V	T_A = +25°C		0.1	1	µA
		T_A = +85°C		1		

PLAYR/PLAYG/PLAYB CHARACTERISTICS

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Low-Level Input Voltage				0.4	V
High-Level Input Voltage		1.4			V
ON/OFF PWM Frequency	(Note 3)	2		200	Hz
PLAY_ Minimum High Time	PLAY_ active high (Bit 1 = low in Register 20h) (Note 3)	80			µs
PLAY_ Minimum Low Time	PLAY_ active low (Bit 1= high in Register 20h) (Note 3)	80			µs
Pulldown Resistor to AGND			800		kΩ

$\overline{CHG}$ PIN CHARACTERISTICS

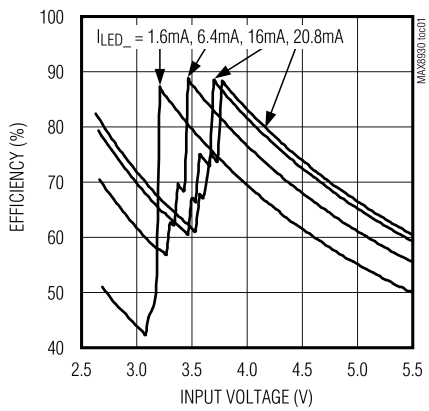
PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Low-Level Voltage	$I_{\overline{CHG}}$ = 5mA			0.05	0.2	V
Leakage Current	$V_{\overline{CHG}}$ = 3.7V	T_A = +25°C		0.1	1	µA
		T_A = +85°C		1		

Note 1: Limits are 100% production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design.
Note 2: 0.1mA LED load current is not included.
Note 3: Guaranteed by design. Not production tested.
Note 4: LED current matching is defined as: (I_{MAX} - I_{MAX})/25.6mA. Matching is for LEDs within the RGB group (RLED, GLED, BLED) or the white LED group (WLED1–WLED8).
Note 5: Dropout voltage is defined as the LED_ to AGND voltage at which current into LED_ drops 10% from the value at $V_{LED\_}$ = 0.5V at 1x mode.
Note 6: V_{KEY} = 0V when pulling low, leakage current from PV3. V_{KEY} = 3.7V when pulling high, leakage current is to GND.

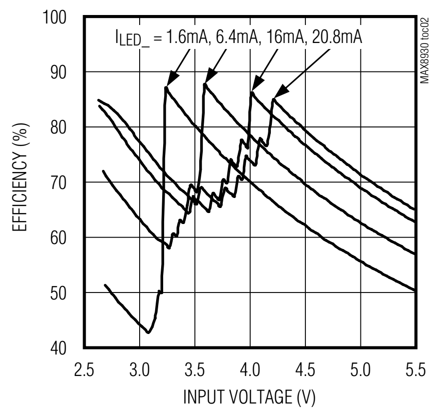
Typical Operating Characteristics

($V_{PV\_}$ = V_{EN} = 3.7V, circuit of Figure 1, T_A = +25°C, unless otherwise noted.)

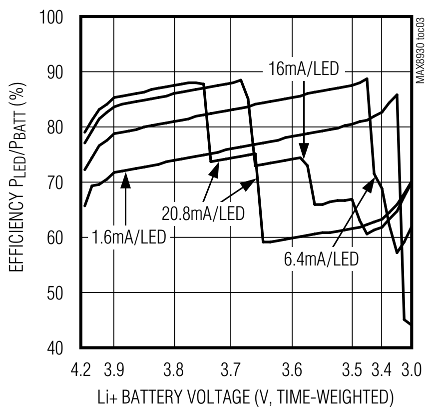
WLED EFFICIENCY vs. INPUT VOLTAGE, 6 MATCHED WLEDS



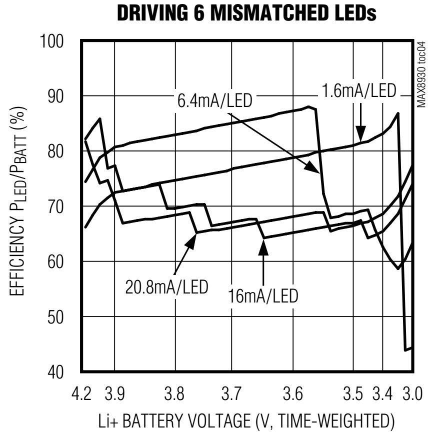
WLED EFFICIENCY vs. INPUT VOLTAGE, 6 MISMATCHED WLEDS



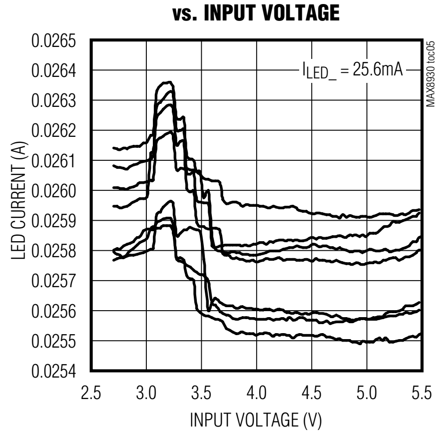
EFFICIENCY vs. Li+ BATTERY VOLTAGE DRIVING 6 MATCHED LEDs



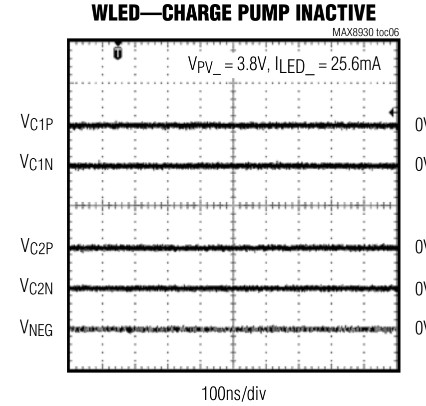
EFFICIENCY vs. Li+ BATTERY VOLTAGE DRIVING 6 MISMATCHED LEDs



WLED CURRENT MATCHING vs. INPUT VOLTAGE



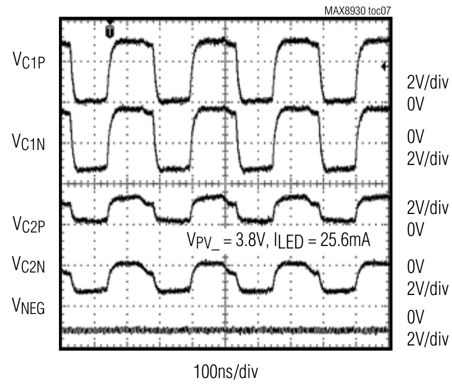
WLED—CHARGE PUMP INACTIVE



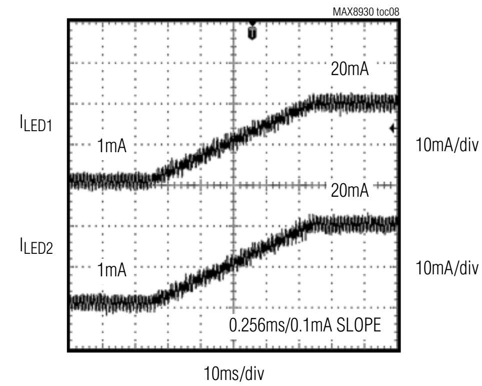
Typical Operating Characteristics (continued)

($V_{PV\_} = V_{EN} = 3.7V$, circuit of Figure 1, $T_A = +25°C$, unless otherwise noted.)

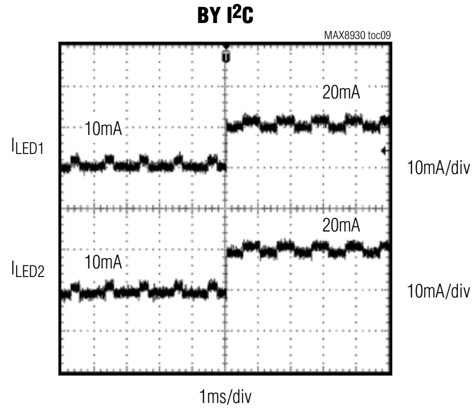
WLED—CHARGE PUMP ACTIVE



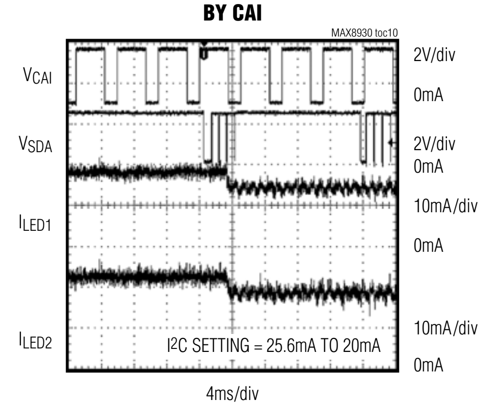
WLED—DIMMING CURRENT TRANSIENT WITH SLOPE CONTROL



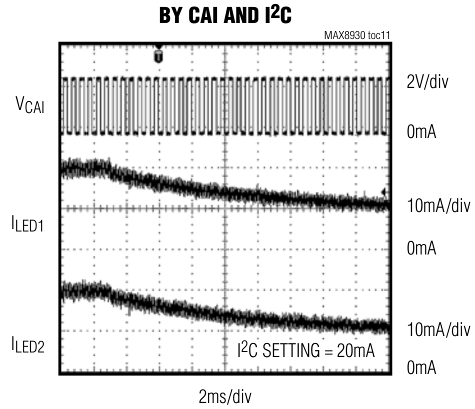
WLED—DIMMING CURRENT TRANSIENT BY I²C



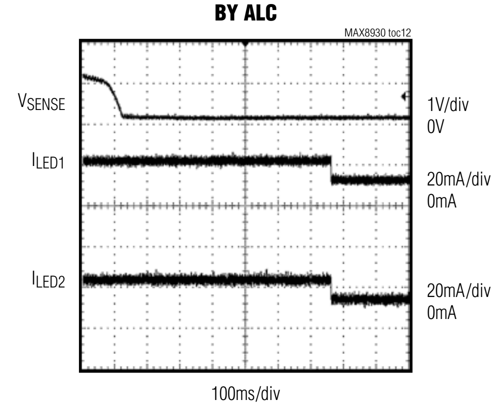
WLED—DIMMING CURRENT TRANSIENT BY CAI



WLED—DIMMING CURRENT TRANSIENT BY CAI AND I²C



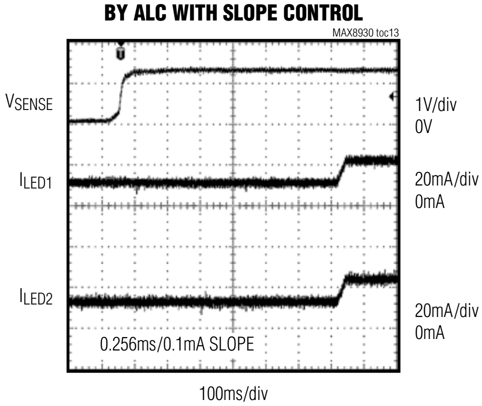
WLED—DIMMING CURRENT TRANSIENT BY ALC



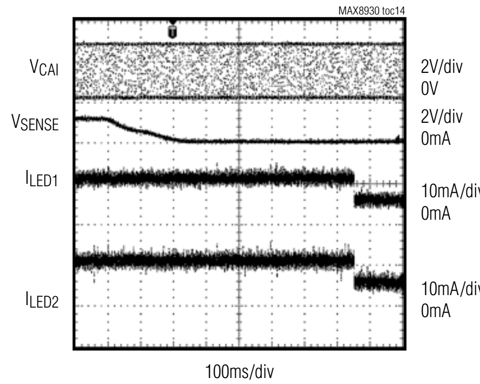
Typical Operating Characteristics (continued)

($V_{PV\_} = V_{EN} = 3.7V$, circuit of Figure 1, $T_A = +25°C$, unless otherwise noted.)

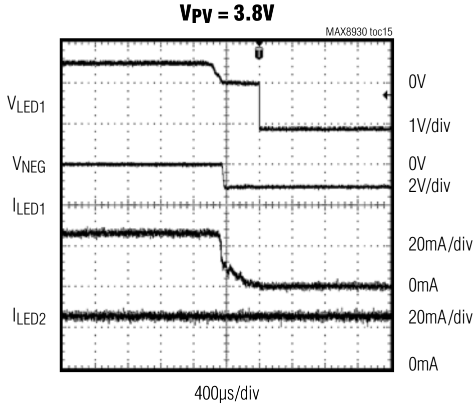
WLED—DIMMING CURRENT TRANSIENT BY ALC WITH SLOPE CONTROL



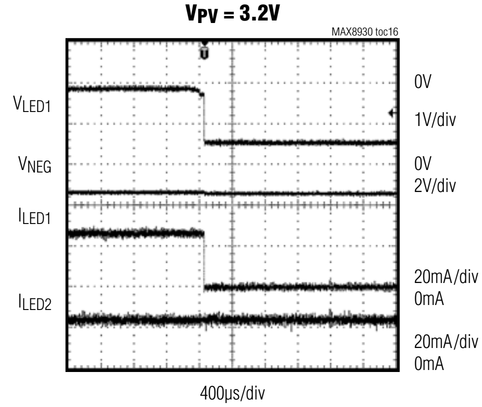
WLED—DIMMING CURRENT TRANSIENT BY ALC AND CAI



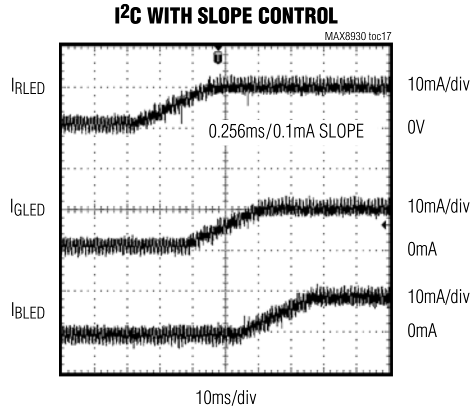
WLED—LED1 OPEN CIRCUIT, V_{PV} = 3.8V



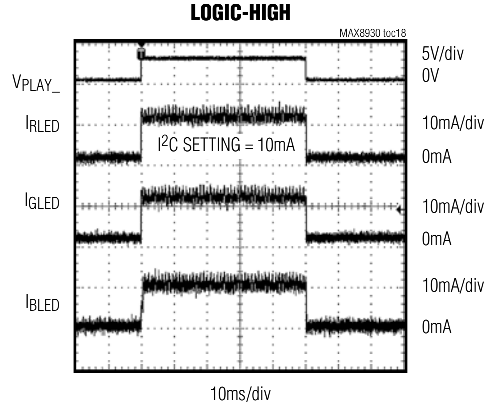
WLED—LED1 OPEN CIRCUIT, V_{PV} = 3.2V



RGB—CURRENT TRANSIENT BY I^2C WITH SLOPE CONTROL



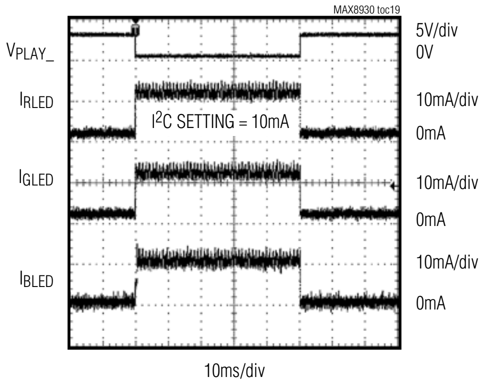
RGB—PLAY_ ON/OFF TRANSITION, LOGIC-HIGH



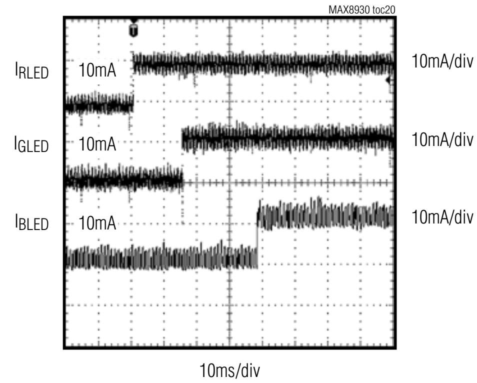
Typical Operating Characteristics (continued)

($V_{PV\_}$ = V_{EN} = 3.7V, circuit of Figure 1, T_A = +25°C, unless otherwise noted.)

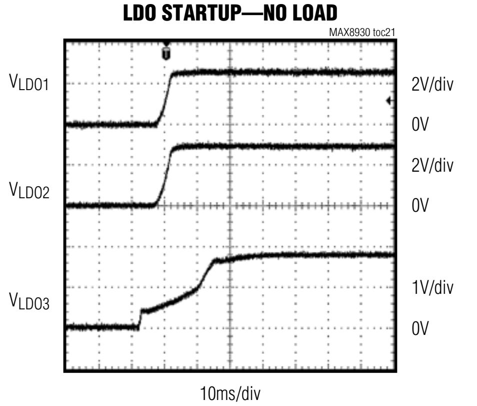
RGB—PLAY_ ON/OFF TRANSITION, LOGIC-LOW



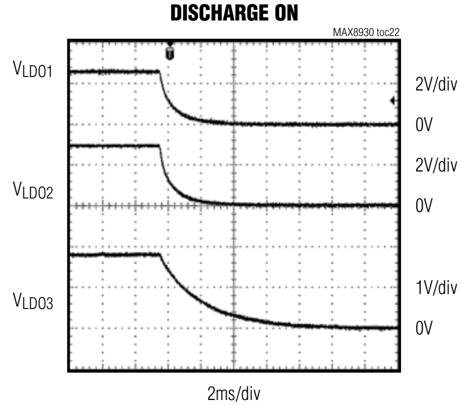
RGB—PLAY_ ON/OFF TRANSITION AND I²C COMING



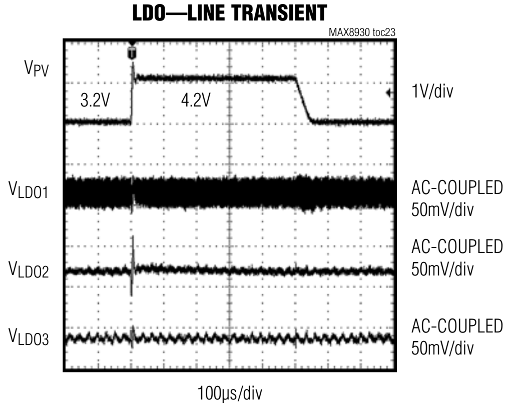
LDO STARTUP—NO LOAD



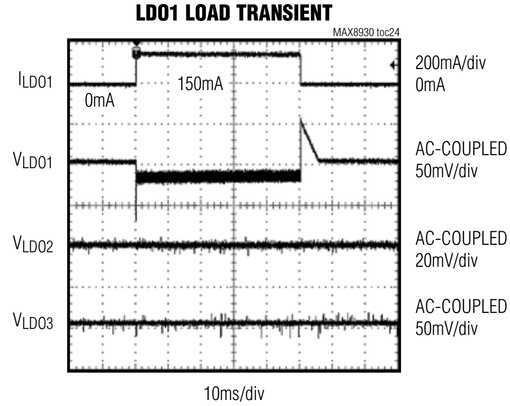
LDO SHUTDOWN—DEFAULT ACTIVE DISCHARGE ON



LDO—LINE TRANSIENT



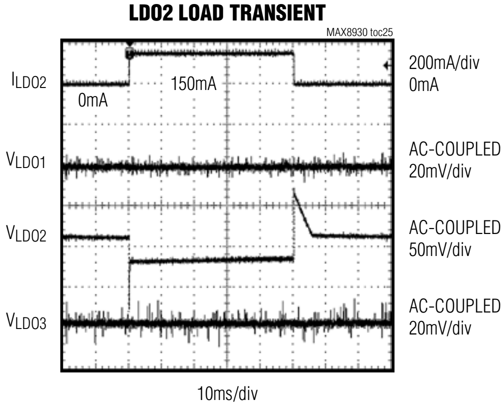
LDO1 LOAD TRANSIENT



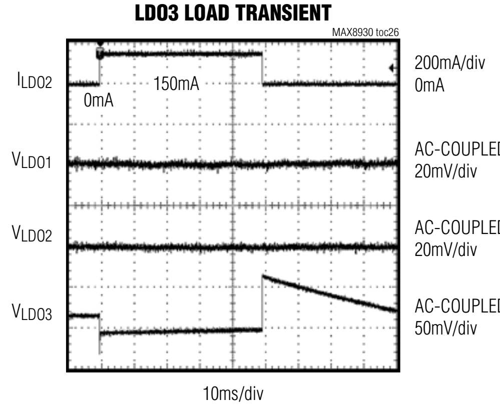
Typical Operating Characteristics (continued)

($V_{PV\_} = V_{EN} = 3.7V$, circuit of Figure 1, $T_A = +25°C$, unless otherwise noted.)

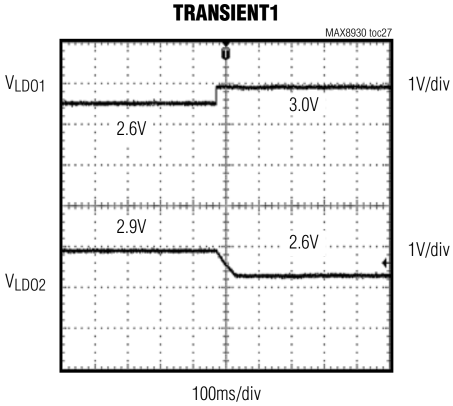
LDO2 LOAD TRANSIENT



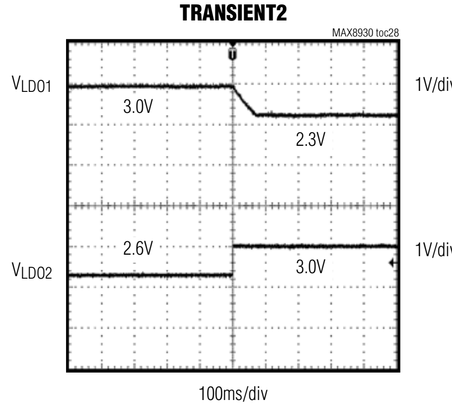
LDO3 LOAD TRANSIENT



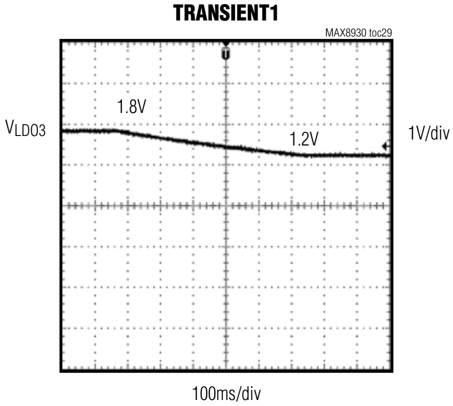
LDO1 AND LDO2—OUTPUT VOLTAGE TRANSIENT1



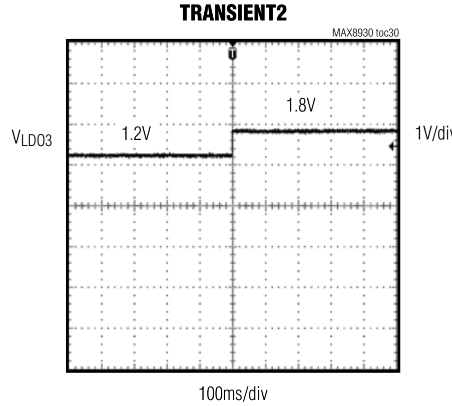
LDO1 AND LDO2—OUTPUT VOLTAGE TRANSIENT2



LDO3—OUTPUT VOLTAGE TRANSIENT1



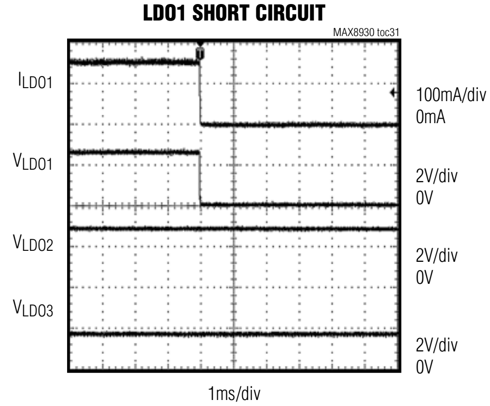
LDO3—OUTPUT VOLTAGE TRANSIENT2



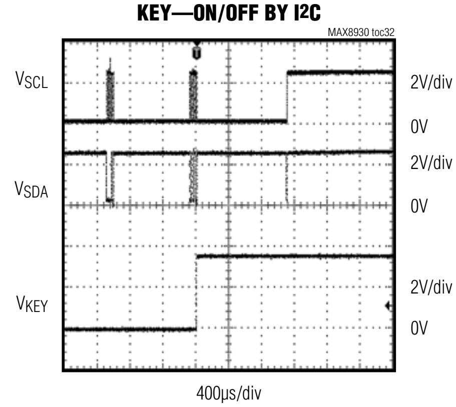
Typical Operating Characteristics (continued)

($V_{PV\_} = V_{EN} = 3.7V$, circuit of Figure 1, $T_A = +25°C$, unless otherwise noted.)

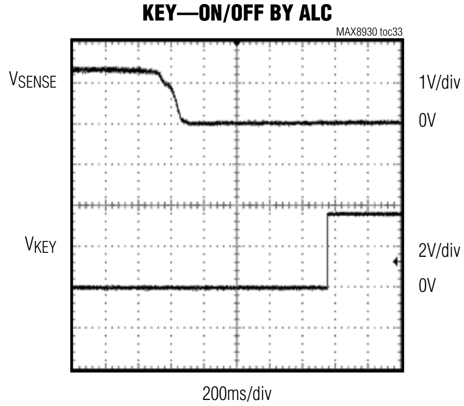
LDO1 SHORT CIRCUIT



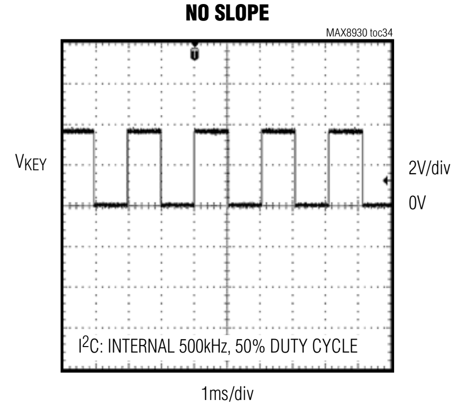
KEY—ON/OFF BY I2C



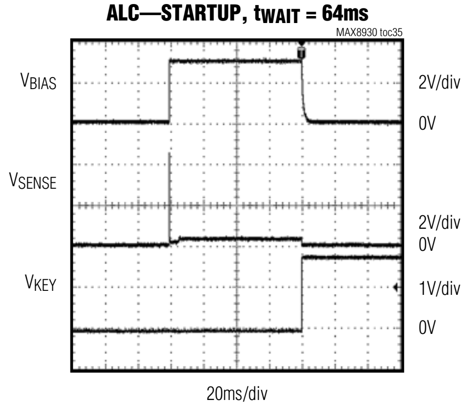
KEY—ON/OFF BY ALC



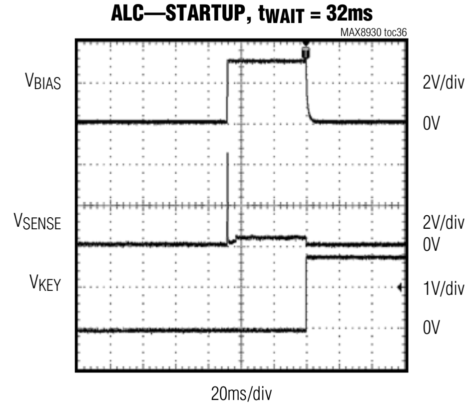
KEY—ON/OFF BY INTERNAL PWM, NO SLOPE



ALC—STARTUP, t_{WAIT} = 64ms



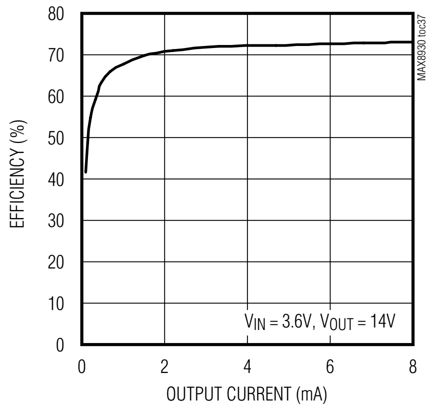
ALC—STARTUP, t_{WAIT} = 32ms



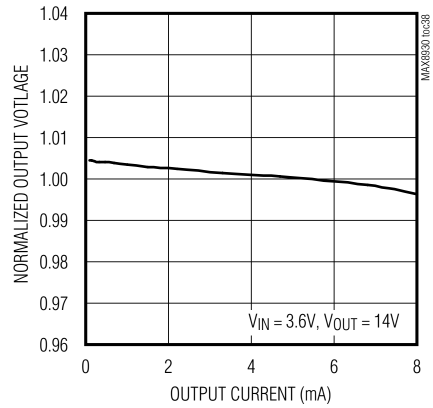
Typical Operating Characteristics (continued)

($V_{PV\_} = V_{EN} = 3.7V$, circuit of Figure 1, $T_A = +25°C$, unless otherwise noted.)

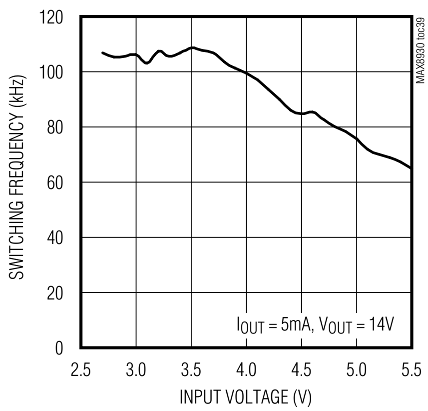
STEP-UP EFFICIENCY vs. LOAD CURRENT



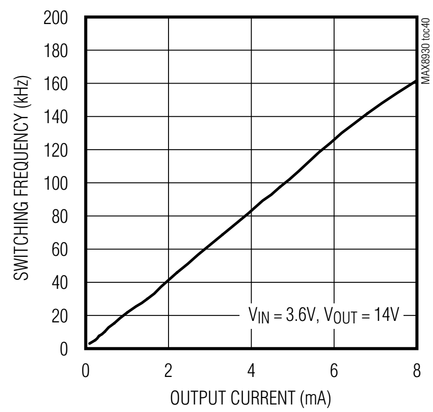
STEP-UP LOAD REGULATION vs. OUTPUT CURRENT



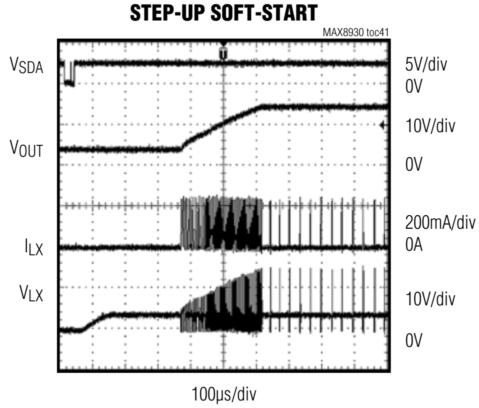
STEP-UP SWITCHING FREQUENCY vs. INPUT VOLTAGE



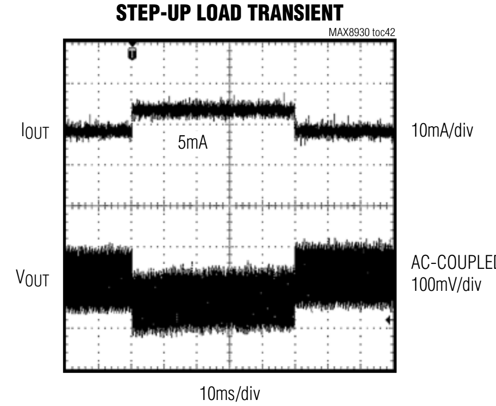
STEP-UP SWITCHING FREQUENCY vs OUTPUT CURRENT



STEP-UP SOFT-START



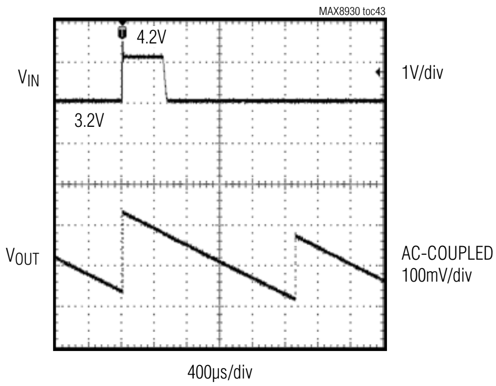
STEP-UP LOAD TRANSIENT



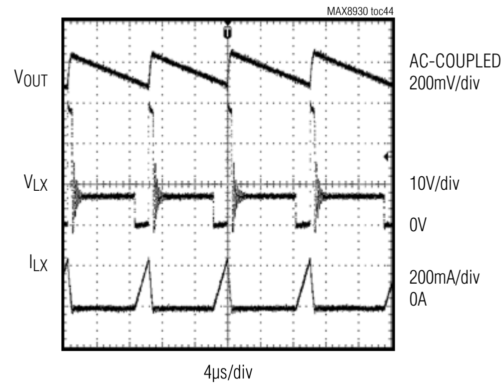
Typical Operating Characteristics (continued)

($V_{PV\_}$ = V_{EN} = 3.7V, circuit of Figure 1, T_A = +25°C, unless otherwise noted.)

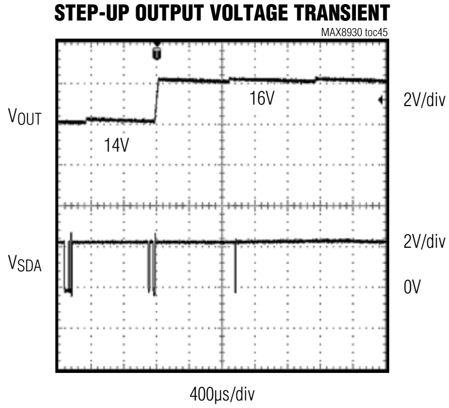
STEP-UP LINE TRANSIENT



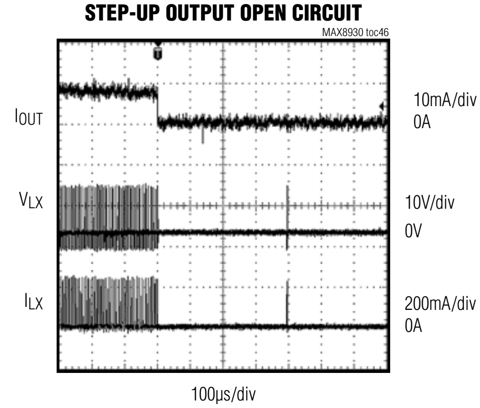
STEP-UP SWITCHING WAVEFORMS



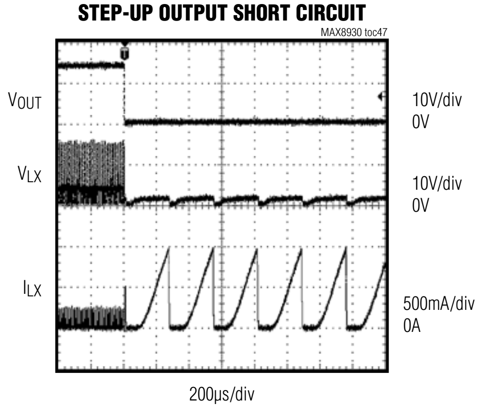
STEP-UP OUTPUT VOLTAGE TRANSIENT



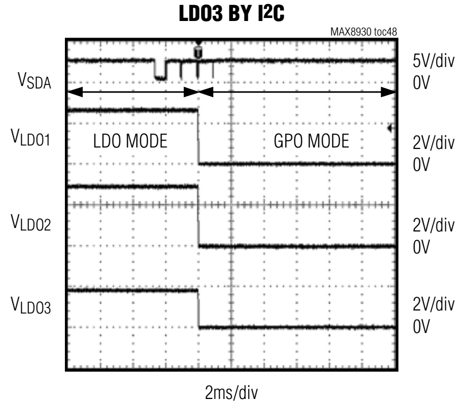
STEP-UP OUTPUT OPEN CIRCUIT



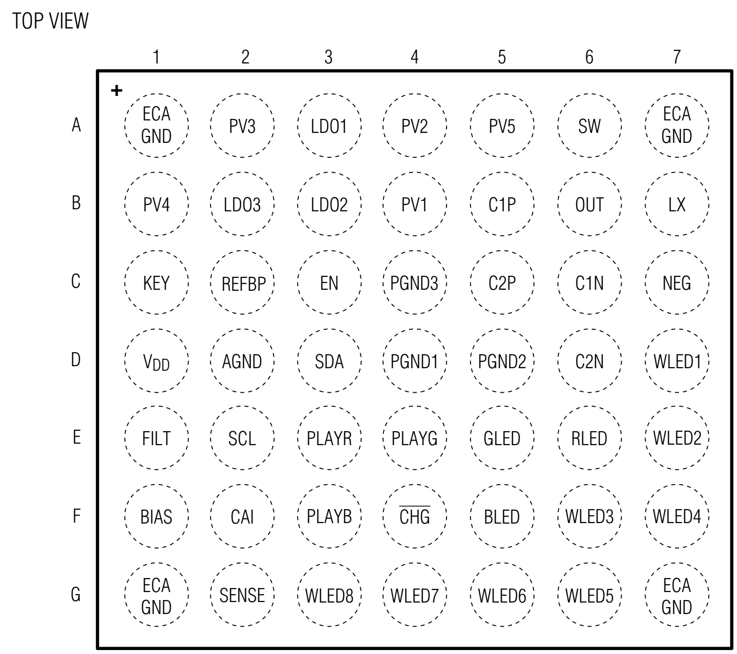
STEP-UP OUTPUT SHORT CIRCUIT



GPO—ON/OFF MODE LDO1, LDO2, LDO3 BY I2C



Pin Configuration



Pin Description

PIN	NAME	FUNCTION
EXTERNALLY CONNECTED TO PGND		
A1, A7, G1, G7	ECAGND	Connect to AGND
POWER INPUT SUPPLY AND POWER GROUND		
A2	PV3	Supply Voltage Input for Ref, Bias, LDO1, and LDO2. The input voltage range is 2.7V to 5.5V. Bypass PV3 to AGND with a 2.2µF ceramic capacitor as close as possible to the IC. PV3 is high impedance during shutdown. Connect PV3 to PV1, PV2, and PV5.
A4	PV2	Supply Voltage Input. Connect PV2 to PV1.
A5	PV5	Supply Voltage Input for the Step-Up Converter. The input voltage range is 2.7V to 5.5V. Bypass PV5 to PGND3 with a 1µF ceramic capacitor as close as possible to the IC. PV5 is high impedance during shutdown. Connect PV5 to PV1, PV2, and PV3.
B1	PV4	Supply Voltage Input for LDO3. The input voltage range is 1.7V to 5.5V. Bypass PV4 to AGND with a 2.2µF ceramic capacitor as close as possible to the IC. PV4 is high impedance during shutdown. If PV4 is not used separately, connect PV4 to PV1.
B4	PV1	Supply Voltage Input for Charge-Pump Circuitry. The input voltage range is 2.7V to 5.5V. Bypass PV1 to PGND1 and PGND2 with a 4.7µF to 10µF ceramic capacitor as close as possible to the IC. PV1 is high impedance during shutdown. Connect PV1 to PV2, PV3, and PV5.
C4	PGND3	Power Ground for the Step-Up Converter
D4	PGND1	Power Ground for the Charge-Pump Block
D5	PGND2	Power Ground for the Charge-Pump Block

Pin Description (continued)

PIN	NAME	FUNCTION
LDO FUNCTION		
A3	LDO1	Output of LDO1. The default value is 2.6V. Bypass LDO1 to AGND with a 1µF ceramic capacitor as close as possible to the IC.
B3	LDO2	Output of LDO2. The default value is 2.9V. Bypass LDO2 to AGND with a 1µF ceramic capacitor as close as possible to the IC.
B2	LDO3	Output of LDO3. The default value is 1.80V. Bypass LDO3 to AGND with a minimum 2.2µF ceramic capacitor as close as possible to the IC.
LOGIC AND ENABLE FUNCTION		
D1	V_{DD}	Logic-Supply Voltage Input. Bypass V_{DD} to AGND with a 0.1µF ceramic capacitor as close as possible to the IC. The input range is 1.7V to 5.5V.
D3	SDA	I^2C Data Input. Data is read on the rising edge of SCL. Connect a 1.5kΩ resistor from SDA to V_{DD}.
E2	SCL	I^2C Clock Input. Data is read on the rising edge of SCL. Connect a 1.5kΩ resistor from SCL to V_{DD}.
D2	AGND	Analog Ground. Connect AGND to the system ground plane.
C3	EN	Hardware Enable Input for the IC. Drive EN high to activate the IC. Drive EN low to disable the IC.
WLED AND RGB DIMMING RELATED FUNCTION		
F2	CAI	Brightness Control Input by Contents Adaptive Interface (DPWM signal). CAI varies the brightness of main WLEDs from 0% to 100%. The dimming frequency is typically 200Hz. When CAI is used as the main control method for main white LEDs, the ramp-up/ramp-down is automatically disabled.
E3	PLAYR	On/Off Input for the Red LED Current Regulator. The PLAYR signal can be either active high or active low. Program either active high or active low through the 20h register.
E4	PLAYG	On/Off Input for the Green LED Current Regulator. The PLAYG signal can be either active high or active low. Program either active high or active low through the 20h register.
F3	PLAYB	On/Off Input for the Blue LED Current Regulator. The PLAYB signal can be either active high or active low. Program either active high or active low through the 20h register.
E1	FILT	PWM Filter Capacitor. Connect a 0.1µF ceramic capacitor between FILT and AGND as close as possible to FILT.
C1	KEY	Key Backlight Control Output. Two threshold values for ON/OFF are available and programmable through the I^2C serial interface. KEY on/off function is controlled by the I^2C, ALC, or the internal 500Hz PWM signal. Program the settings for KEY through the I^2C interface.
C2	REFBP	1.20V Reference output. Bypass REFBP to AGND with 0.1µF ceramic capacitor as close as possible to the IC. Do not load REFBP.
AUTOMATIC LUMINANCE CONTROL		
F1	BIAS	Bias Output for an External Light Sensor. Bypass BIAS to AGND with a 1µF ceramic capacitor as close as possible to the IC. The BIAS output is 3.0V.
G2	SENSE	Input from Ambient Light Sensor. Connect a 5.1kΩ resistor from SENSE to AGND.
CHARGE-PUMP BLOCK		
B5	C1P	Transfer Capacitor 1 Positive Connection. Connect a 1µF ceramic capacitor from C1P to C1N.
C6	C1N	Transfer Capacitor 1 Negative Connection. Connect a 1µF ceramic capacitor from C1P to C1N.
C5	C2P	Transfer Capacitor 2 Positive Connection. Connect a 1µF ceramic capacitor from C2P to C2N.
C7	NEG	Charge-Pump Negative Output. Connect a 1µF to 2.2µF ceramic capacitor from NEG to PGND1. In shutdown, an internal 10kΩ resistor pulls NEG to PGND.
D6	C2N	Transfer Capacitor 2 Negative Connection. Connect a 1µF ceramic capacitor from C2P to C2N.

Pin Description (continued)

PIN	NAME	FUNCTION
WLED AND RGB		
D7	WLED1	WLED Current Sink Regulator. Current into WLED1 is based upon the programmed internal I^2C registers. Connect WLED1 to the cathodes of external LEDs. WLED1 is high impedance during shutdown. If unused, short WLED1 to PV3.
E7	WLED2	WLED Current Sink Regulator. Current into WLED2 is based upon the programmed internal I^2C registers. Connect WLED2 to the cathodes of external LEDs. WLED2 is high impedance during shutdown. If unused, short WLED2 to PV3.
F6	WLED3	WLED Current Sink Regulator. Current into WLED3 is based upon the programmed internal I^2C registers. Connect WLED3 to the cathode of an external WLED. WLED3 is high impedance during shutdown. If unused, short WLED3 to PV3.
F7	WLED4	WLED Current Sink Regulator. Current into WLED4 is based upon the programmed internal I^2C registers. Connect WLED4 to the cathode of an external LED. WLED4 is high impedance during shutdown. If unused, short WLED4 to P3.
G6	WLED5	WLED Current Sink Regulator. Current into WLED5 is based upon the programmed internal I^2C registers. Connect WLED5 to the cathode of an external WLED. WLED5 is high impedance during shutdown. If unused, short WLED5 to either PV3 or disable the regulator.
G5	WLED6	WLED Current Sink Regulator. Current into WLED6 is based upon the programmed internal I^2C registers. Connect WLED6 to the cathode of an external WLED. WLED6 is high impedance during shutdown. If unused, short WLED6 to either PV3 or disable the regulator.
G4	WLED7	WLED Current Sink Regulator. Current into WLED7 is based upon the programmed internal I^2C registers. Connect WLED7 to the cathode of an external WLED. WLED7 is high impedance during shutdown. If unused, short WLED7 to either PV3 or disable the regulator.
G3	WLED8	WLED Current Sink Regulator. Current into WLED8 is based upon the programmed internal I^2C registers. Connect WLED8 to the cathode of an external WLED. WLED8 is high impedance during shutdown. If unused, short WLED8 to either PV3 or disable the regulator.
E6	RLED	Red LED Connection. The brightness is set up by I^2C. ON/OFF is synchronized with the PWM signal applied to PLAYR pin. RLED maximum brightness is enabled/disabled through the serial interface.
E5	GLED	Green LED Connection. The brightness is set up by I^2C. ON/OFF is synchronized with the PWM signal applied to PLAYG pin. GLED maximum brightness is enabled/disabled through the serial interface.
F5	BLED	Blue LED Connection. The brightness is set up by I^2C. ON/OFF is synchronized with the PWM signal applied to PLAYB pin. BLED maximum brightness is enabled/disabled through the serial interface.
BOOST CONVERTER		
B6	OUT	Step-Up Converter Output. Bypass OUT to GND with a 1µF ceramic capacitor. During shutdown, OUT is pulled to PGND3 by an internal 1MΩ resistor.
A6	SW	Isolation Switch Output for the Step-Up Converter. SW is internally connected to the drain of a p-channel MOSFET and used to isolate the output of the step-up from the input during shutdown. If true shutdown is not required, SW can be left open with the input supply connected directly to the inductor.
B7	LX	Inductor Switching Connection. Connect the inductor between LX and SW. For most applications, use a 22µH inductor.
STATUS INDICATOR		
F4	$\overline{CHG}$	Charging Status Output. $\overline{CHG}$ is an open-drain output that goes low when the battery is charging. On/off is operated by I^2C. $\overline{CHG}$ is high impedance when the IC is in shutdown mode. Enable $\overline{CHG}$ through the I^2C interface.

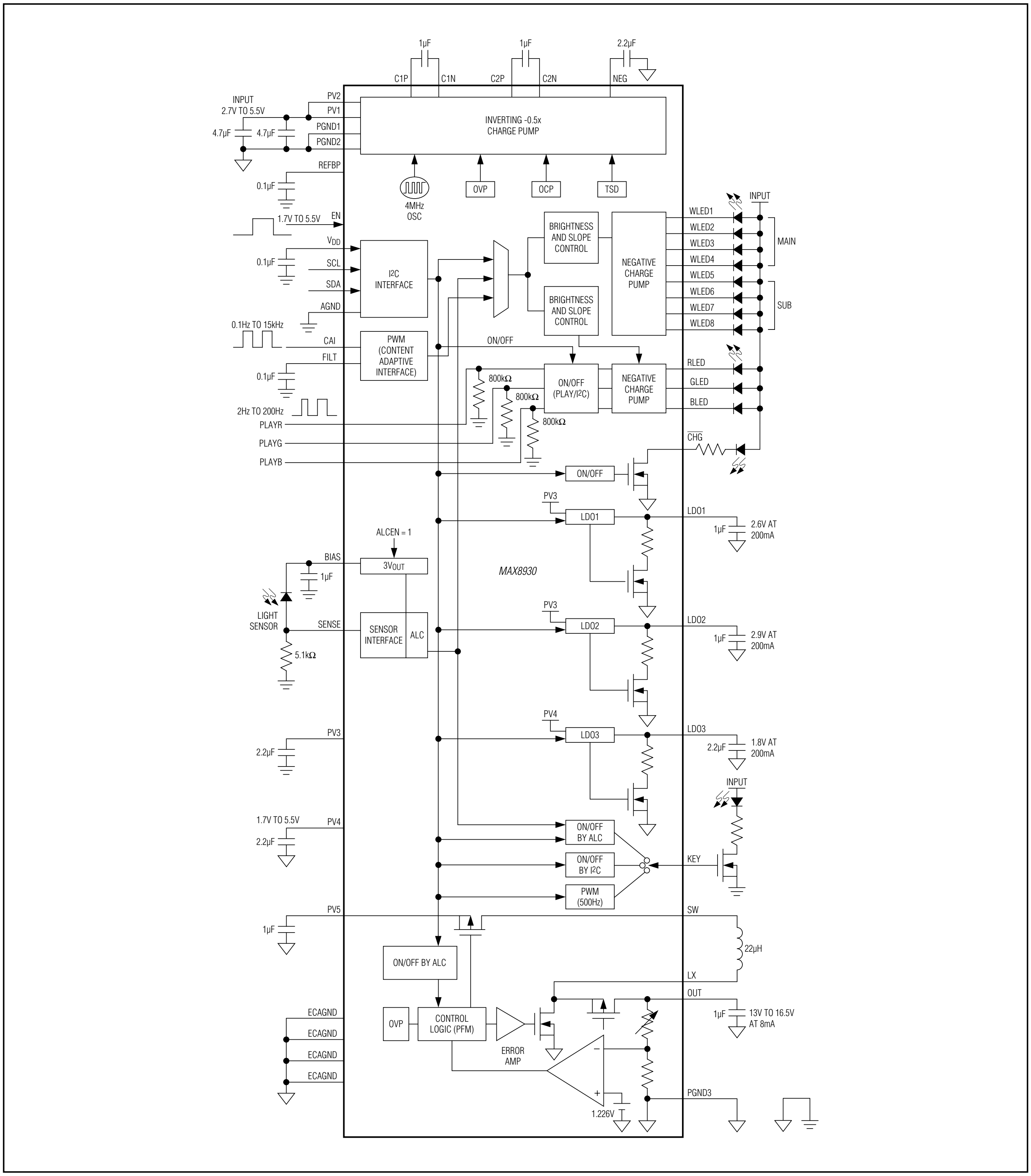


Figure 1. Typical Application and Block Diagram

External Components

PIN	EXTERNAL COMPONENTS	NOTES
PV1, PV2, PV3, PV5	10µF Total capacitance ≥ total LDO, boost, and charge-pump capacitance	System stability
PV4	2.2µF	LDO stability
V_{DD}	0.1µF	Decoupling
BIAS	1µF	LDO compensation
LDO1	1µF	LDO compensation
LDO2	1µF	LDO compensation
LDO3	2.2µF	LDO compensation
FILT	0.1µF	Noise filter
REFBP	0.1µF	Noise filter
C1P, C1N	1µF	Charge pump
C2P, C2N	1µF	Charge pump
NEG	2.2µF	Charge pump
WLED1–WLED8	White LED	—
RLED, GLED, BLED	Red, green, blue LED	—
$\overline{\text{CHG}}$	A resister, for example 10kΩ	Current limit
SW, LX	22µH	Boost converter
OUT	1µF	Boost stability
SENSE	5.1kΩ	Converter ambient light to a voltage
ALC	Toshiba TPS852	Any type (linear/log) of photo IC

Note: *All output capacitors are ceramic and X7R/X5R type.*

Detailed Description

The MAX8930 integrates a negative charge pump for both white LED display backlighting with ambient light control (ALC) function, content adaptive interface (CAI) function, and R/G/B LED. There is one step-up converter for passive matrix OLED (PMOLED) oriented application and three LDOs with programmable output voltage. The three LDO outputs are able to convert to GPO (general-purpose output) status through an I2C command. The MAX8930 includes soft-start, thermal shutdown, open-circuit, and short-circuit protection in the charge-pump circuitry.

Reset Control

The MAX8930 uses two different methods of reset: software and hardware.

Software Reset: All the registers are initiated by RESET = 1 at Register 00h. After that, the values in all registers come back to POR (power-on-reset) state. The bit of RESET in 00h is automatically returned to 0. Auto return to 0.

Hardware Reset: Hardware reset is done by toggling EN from logic-high to logic-low. All the registers under hardware reset conditions are returned to their initial values (POR) and stop receiving any commands.

Open-Circuit and Short-Circuit Protection

If any WLED/RGB fails as an open circuit, that LED pin pulls to ground, and the IC is forced into -0.5X mode. Therefore, connect any unused WLED_/RGB pins to PV1, PV2, or PV3 to disable the corresponding current regulator. The MAX8930 contains special circuitry to detect this condition and disables the corresponding current regulator to avoid wasting battery current.

Thermal Shutdown

The MAX8930 includes a thermal-limit circuit that shuts down the IC at about +160°C. The part turns on after the IC cools by approximately 20°C.

Thermal shutdown is applied to the following blocks:

- White and RGB LED driver
- Step-up converter
- LDO1, LDO2, LDO3
- SBIAS

LED Charge Pump

The charge pump drives up to 8 white LEDs (4 WLEDs for main and 4 WLEDs for sub) and 3 RGB LEDs with regulated constant current for both display backlight and fun light applications. By utilizing individually adaptive 1x/-0.5x negative charge-pump modes and extremely low-dropout current regulators, it is able to achieve high efficiency over the full 1-cell lithium battery input voltage range. High-frequency switching of 4MHz allows for tiny external components. The regulation scheme is optimized to ensure low EMI and low input ripple. Each channel for WLED and RGB LED has the capability of delivering 25.6mA with 256 dimming steps (0.1mA per step). The current-level adjustment is programmed by an I2C command. Figure 2 is the flow chart of the startup and mode-change algorithm.

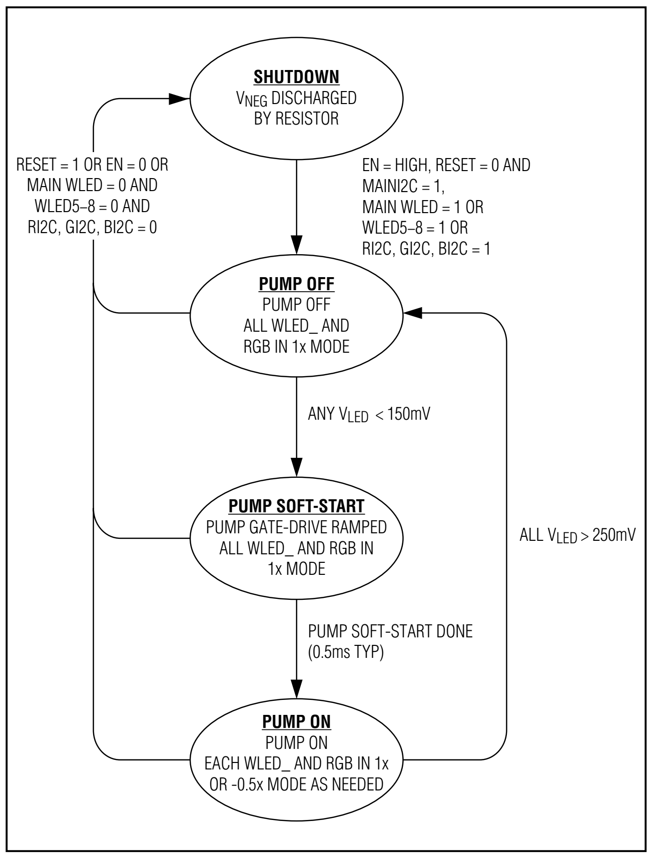


Figure 2. Startup and Mode Change Algorithm

WLED1–WLED8 Driver Operation

The white LED current regulators are composed of 4 main-group drivers (WLED1–WLED4) and 4 subgroup drivers (WLED5–WLED8). The current of the main-group LEDs can be selected by an I^2C register. Both ambient light control (ALC) mode and ramp-up/ramp-down control are applied to only the main-group white LEDs.

The subgroup LEDs can choose either individual control or can belong to the main group based on the status of a bit in the register (01h and 02h). In this function, combinations can be adjusted as required. For example, main 4ch + sub 4ch or main 5ch + sub 3ch.

The CAI (PWM) signal from either the LCD driver module or baseband chipset controls only the main-group WLEDS. The up/down slope control can be programmed by the setting of the 0Ah register when the main LEDs are controlled by either I^2C or ALC.

For main LEDs, there are three different dimming control methods, I^2C, ALC, and CAI. The dimming range for main LEDs and sub LEDs is from 0.1mA to 25.6mA in 0.1mA increments.

RGB Driver Operation

The brightness for each color LED has 256 different steps (0.1mA to 25.6mA). The RGB LED can be activated by either the high/low status of the PLAY_ PWM signal or by I^2C ON/OFF command. The default dimming control is I^2C command. An I^2C command for dimming can adjust the current of each RGB individually. The operation of ON/OFF by I^2C command also allows individual control. However, the operation of ON/OFF by PWM to PLAY_ RGB is group control. To operate with either an active-high or active-low signal coming from the microprocessor such as audio processor, the register related to active high or active low should be selected first (the bit 1 in 20h). When a call comes in or music plays, all RGB LEDs are allowed to be activated by either a PWM signal applied to PLAY_ or a designated register by I^2C.

The main purpose for the PLAY_ is for ON/OFF control function and not for dimming control. If the dimming current is set to 10mA on each RGB LED, the PWM signal to PLAY_ RGB turns all of the current regulators on or off at the same time. However, the dimming current for RGB can be set by I^2C command during ON/OFF operation. When the PLAY_ is in active-high period, the RGB current regulator is on with 10mA current. When the PLAY_ is in the opposite state (active-low period), the RGB regulator is off with 0mA current. The default method to turn the RGB LED on is to pull the PLAY_ input high with a minimum on-time of 80µs in active-high mode. If bit 1 in 20h is set to 1, then all current regulators for RGB are activated by active-low signal with a minimum off-time of 80µs. The up/down slope control can be programmed by the setting of the 0Bh register when the RGB LEDs are controlled by I^2C only.

If bit 7 in 20h is set to logic-low, then slope up/down is automatically deactivated.

CAI (Contents Adaptive Interface) Operation

A 200Hz PWM signal is applied to the CAI pin. The CAI signal can be from either the LCD driver module with gamma correction information or from the baseband chipset. The main WLED can be activated by either the high/low status of the CAI PWM signal or with either an active-high or active-low signal coming from either a LCD driver module or baseband chipset. The corresponding register bit (bit 0 in 02h) should be set to either, 1 or 0 by I^2C command.

Depending on the duty cycle, the brightness varies from 0mA to 25.6mA with the resolution of 0.256mA per 1% duty variation. In control of CAI (PWM) independently, the existing brightness setting from either I^2C or ALC is overwritten because CAI has the priority over I^2C and ALC.

See the *Dimming by Digital PWM on CAI Only* and *Dimming by Both Digital PWM on CAI and Either I^2C or ALC at the Same Time* sections for details on the CAI dimming control.

Dimming by Digital PWM on CAI Only

When the digital PWM (DPWM) signal (100Hz ~15kHz) is provided by either the baseband or CPU for dimming the brightness, the MAX8930 DPWM function takes over the responsibility of dimming the main WLEDs. The dimming by CAI is initiated by setting CAI (bit 7 of Register 02h) to 1. After the set-up, both I^2C register dimming settings and ALC no longer control the dimming current for the main WLEDs. The frequency range on the CAI pin is from 100Hz to 15kHz, where 0% duty cycle corresponds to 0mA and 100% duty cycle corresponds to full current, 25.6mA.

When CAI is set to 1, the ramp-up/down slope for main WLED_ is automatically disabled by the MAX8930 control logic. Figure 3 is the timing diagram on initiating CAI. The MAX8930 maintains its previous dimming setting for t_B (10ms typ) to allow the PWM filter time to settle to its average value before activating CAI dimming. This is done automatically inside the IC. The bit of MAINI2C

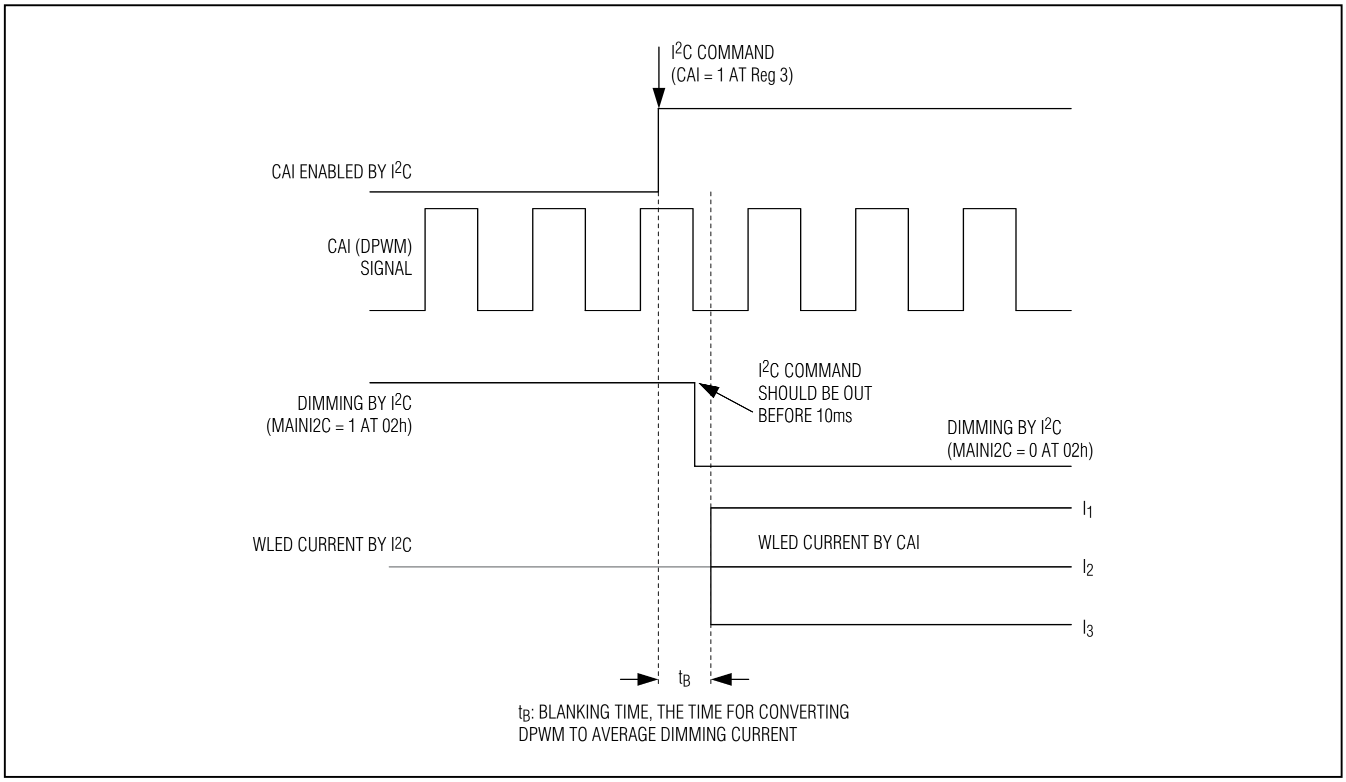


Figure 3. Timing Diagram of Stand-Alone CAI Dimming Operation

should be set to 0 in less than t_B, 10ms (typ) for CAI dimming to be exclusively through DPWM.

If this setup fails, the previous dimming current is still effective even though bit 7 in 02h (CAI) has been set to 1.

The current of I1, I2, and I3 of Figure 3 is different depending on the duty cycle of DPWM.

t_B is the settling time for the CAI input filter to calculate an average value for the dimming current.

Dimming by Both Digital PWM on CAI and Either I2C or ALC at the Same Time

If an end-user wants to see either TV or a movie, the LCD driver module may take care of dimming control independently. In this situation, the output signal from the LCD module has some color information. For example, (16mA/LED) + gamma correction can make the user feel the same brightness of the LCD screen compared to (20mA/LED) + no gamma correction.

In this combined dimming control, any dimming current set earlier by either the I2C register or the ALC register is the value corresponding with 100% duty cycle of the CAI signal.

Ambient Light Control Operation

Dimming of the LCD backlight and ON/OFF control of the keypad backlight are possible on the basis of the data detected by an external ambient light sensor. The ALC consists of the following segments:

- Bias function (3V output)
- 8-bit ADC with an average filter
- A slope process function
- A LOG scale conversion function

A wide range of ambient light sensors can be used with the MAX8930, including photo diode, photo transistor, photo IC (a linear output/LOG output), etc. The detected amount of ambient light is changed into digital data by

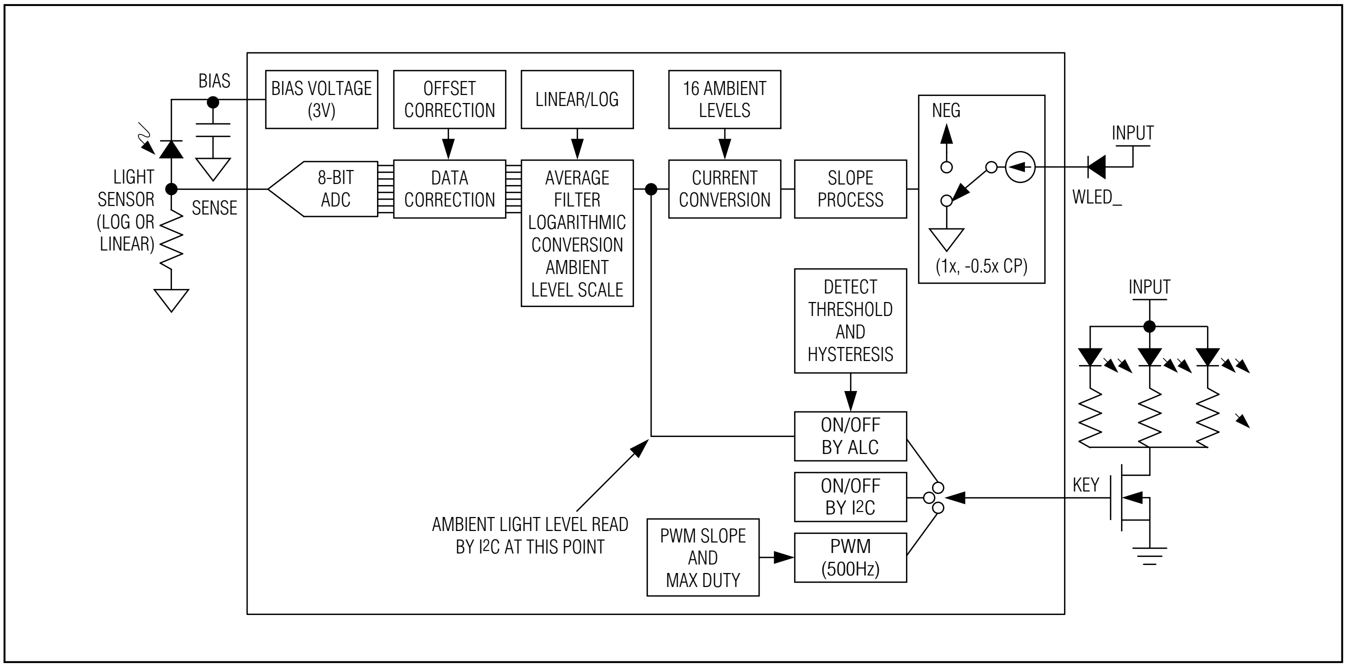


Figure 4. ALC Block Diagram

the embedded digital processing. This data can be read through the I2C (0Dh).

The conversion to LED current can be accomplished either through a built-in initial lookup table or a built-in user settable lookup table.

When ALC is activated, the brightness settings of the main LEDs are controlled through the ALC control circuitry and not by the baseband processor. The default setting on power-on reset is for control by the baseband processor.

ON/OFF of ALC Block for Main WLEDs

ALC operation can be activated independently for the main LED and the keypad backlight. The ALCEN bit in register 00h activates ambient light control. The KBALC bit in register 00h activates ON/OFF for the keypad backlight in ALC mode. For keypad backlight, the output is simple logic-high/logic-low.

Bias Voltage for a Sensor

An embedded LDO with a nominal 3V output provides the bias voltage for the ambient light sensor. This bias output is enabled as soon as the ALCEN bit is set to 1.

The operation of the bias output voltage has two options based on the value of the SBIAS bit (bit 7 in Register 0Ch). When this bit is set to 1, the bias output is synchronized with the measurement cycle. This means that the bias voltage generator is active only when a measurement cycle is being performed. The measurement cycle has four different times, 0.52s, 1.05s, 1.57s, and 2.10s. When this bit is set to 0, the bias output is always on as long as the ALCEN bit is set to 1.

Brightness Data Conversion

16 different dimming steps are available depending on the ambient light condition. The selection of the log or linear conversion is possible by the setting of the LSTY bit (bit 6 of register 0Ch).

Linear type sensor: LOG conversion

Log type sensor: Data bypass

The brightness data can be read through I2C (Register at 0Dh).

LED Current Conversion

The following is the initial current value to each level of ambient light. This value can be overwritten by I2C command.

Table 1. Brightness Data Conversion Settings

AMBIENT LEVEL	WITH LOG CONVERSION (LINEAR TYPE OF SENSOR)	WITHOUT LOG CONVERSION (LOG TYPE OF SENSOR)
0h	V_{SBIAS} x 0/256	V_{SBIAS} x 0/256 ~ V_{SBIAS} x 17/256
1h	V_{SBIAS} x 1/256	V_{SBIAS} x18/256 ~ V_{SBIAS} x 26/256
2h	V_{SBIAS} x 2/256	V_{SBIAS} x 27/256 ~ V_{SBIAS} x 36/256
3h	V_{SBIAS} x 3/256 ~ V_{SBIAS} x 4/256	V_{SBIAS} x 37/256 ~ V_{SBIAS} x 47/256
4h	V_{SBIAS} x 5/256 ~ V_{SBIAS} x 6/256	V_{SBIAS} x 48/256 ~ V_{SBIAS} x 59/256
5h	V_{SBIAS} x 7/256 ~ V_{SBIAS} x 9/256	V_{SBIAS} x 60/256 ~ V_{SBIAS} x 71/256
6h	V_{SBIAS} x 10/256 ~ V_{SBIAS} x 13/256	V_{SBIAS} x 72/256 ~ V_{SBIAS} x 83/256
7h	V_{SBIAS} x 14/256 ~ V_{SBIAS} x 19/256	V_{SBIAS} x 84/256 ~ V_{SBIAS} x 95/256
8h	V_{SBIAS} x 20/256 ~ V_{SBIAS} x 27/256	V_{SBIAS} x 96/256 ~ V_{SBIAS} x 107/256
9h	V_{SBIAS} x 28/256 ~ V_{SBIAS} x 38/256	V_{SBIAS} x 108/256 ~ V_{SBIAS} x 119/256
Ah	V_{SBIAS} x 39/256 ~ V_{SBIAS} x 53/256	V_{SBIAS} x 120/256 ~ V_{SBIAS} x 131/256
Bh	V_{SBIAS} x 54/256 ~ V_{SBIAS} x 74/256	V_{SBIAS} x 132/256 ~ V_{SBIAS} x 143/256
Ch	V_{SBIAS} x 75/256 ~ V_{SBIAS} x 104/256	V_{SBIAS} x 144/256 ~ V_{SBIAS} x 155/256
Dh	V_{SBIAS} x 105/256 ~ V_{SBIAS} x 144/256	V_{SBIAS} x 156/256 ~ V_{SBIAS} x 168/256
Eh	V_{SBIAS} x 145/256 ~ V_{SBIAS} x 199/256	V_{SBIAS} x 169/256 ~ V_{SBIAS} x 181/256
Fh	V_{SBIAS} x 200/256 ~ V_{SBIAS} x 255/256	V_{SBIAS} x 182/256 ~ V_{SBIAS} x 255/256

Table 2. LED Current Conversion

BRIGHTNESS	INITIAL	CURRENT (mA)	BRIGHTNESS	INITIAL	CURRENT (mA)
0	0Fh	1.6	8	89h	13.8
1	1Eh	3.1	9	98h	15.3
2	2Dh	4.6	A	A7h	16.8
3	3Ch	6.1	B	B6h	18.3
4	4Ch	7.7	C	C6h	19.9
5	5Bh	9.2	D	D5h	21.4
6	6Ah	10.7	E	E4h	22.9
7	79h	12.2	F	F9h	25.0

The Operation of ALC Function

Table 3 shows the various conditions on the main WLED_ current for LCD backlight.

Sensor Interface

As a default value, 3V is applied from the BIAS pin. The sensed voltage at the SENSE pin is transformed into digital data by the embedded 8-bit ADC.

A/D Conversion

The detection of ambient light condition is performed in periodic time steps (4 options). BIAS and ADC are turned off except when reading the ambient light condition. The sensor is also turned off in between measurements. This leads to lower power consumption. For the first 64ms, the ambient light data is discarded because the data might be inaccurate information in startup period. For

Table 3. ALC Function

ALC ON/OFF	MAIN WLED_ ON/OFF	ALC BLOCK	LCD BACKLIGHT CURRENT
0	0	OFF	OFF
0	1		Setup by main LED current*
1	0	ON	OFF
1	1		Setup by ambient light data†

**The ALC for WLED backlight is disabled in this mode. It means the current for the LCD backlight is set up by the main LED current value using either I²C or CAI.*

†*The ALC for WLED backlight is enabled in this mode. It means the current for the LCD backlight is set up by the ambient light data from 0h to Fh.*

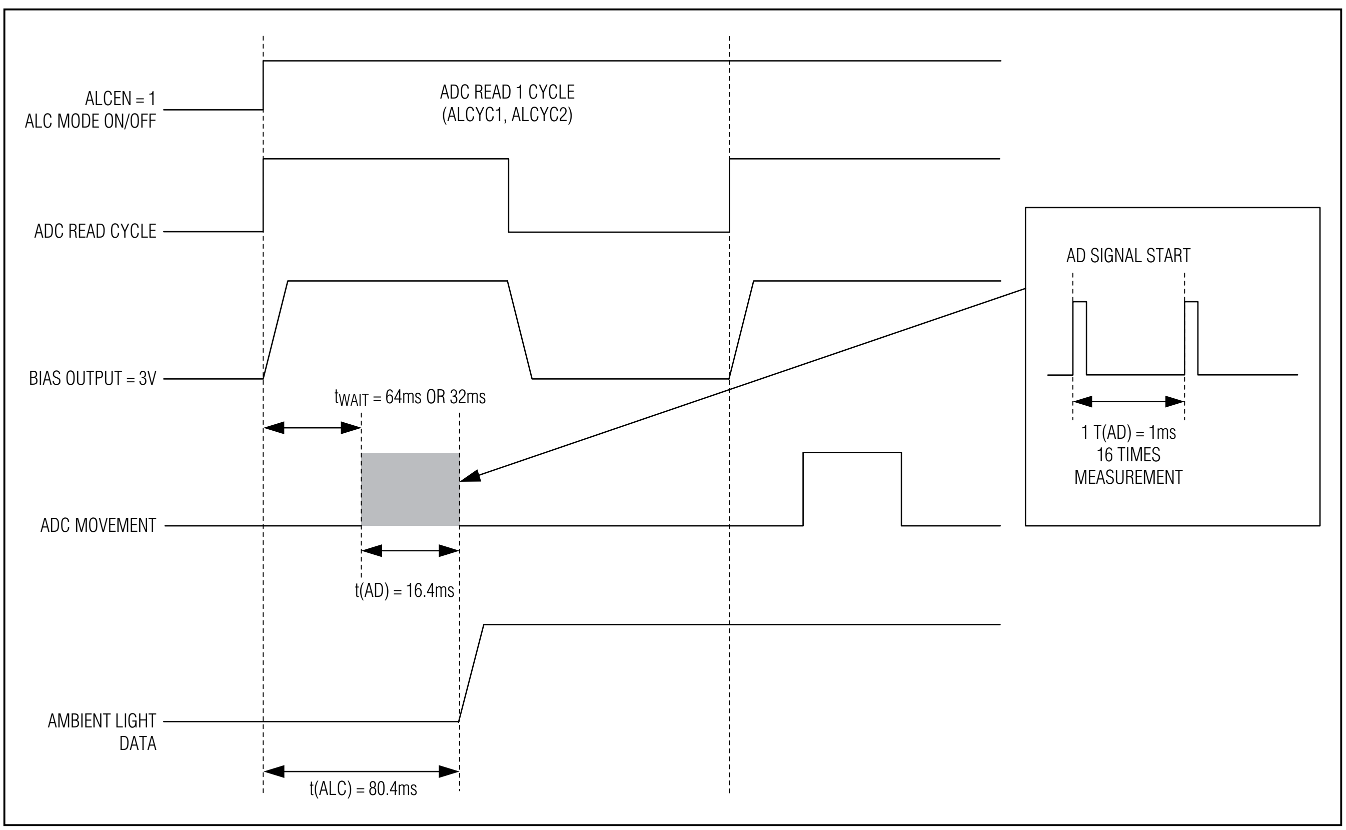


Figure 5. ALC A/D Conversion

the next 16.4ms, the internal digital logic block tries to read the ambient light condition 16 times and calculate the average data. This read data is automatically saved in Register 0Dh.

Up/Down Slope Control

The up/down slope control is sometimes necessary for dimming the main WLED_ in a natural way. The up (dark to bright), down (bright to dark) main WLED current transition speeds are set individually.

The default value of the up/down slope is 0s. It is programmable by the settings of control bits in Register 0Ah. The up/down slope time is per 0.1mA increment; for example, if the I_{LED1} current is 0mA and the up slope time is set to 2.048ms. After reading the ambient light condition and getting I_{LED2} with 20mA, the total time from I_{LED1} to I_{LED2} is 0.4096s [(20mA/0.1mA) x 2.048ms = 0.4096s].

ADC Data Offset Adjustment

The accuracy of the ALC control circuitry can be calibrated in each IC using the ADC data offset adjustment register. This offset adjustment can correct for parameter variation in the IC and in the external light sensor. This adjustment is performed with bits 3–0 in Register 0Ch.

Table 4 shows all possibilities of dimming control for both main WLEDs and KEY.

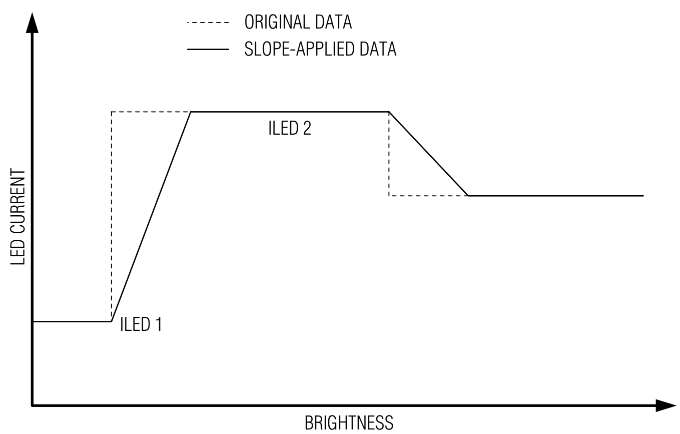


Figure 6. LED Current vs. Brightness

Table 4. Summary of Dimming Control for Main WLEDs and KEY

		I^2C	ALC	CAI (PWM)	PWM (500Hz)	I^2C + ALC	I^2C + CAI	ALC + CAI	I^2C + CAI + ALC
MAIN WHITE LEDS	**DIMMING**	Yes (default)	Yes	Yes	No	No	Yes	Yes	No
	UP/ DOWN SLOPE CONTROL	Available	Available	Not available	Not available	Not available	Not available	Not available	Not available
KEY	**ON/OFF**	Yes (default)	Yes	No	Yes	No	No	No	No
	DUTY TRANSITION CONTROL TIME	Not available	Not available	Not available	Available	Not available	Not available	Not available	Not available

KEY (Keypad Backlight) ON/OFF Control Operation

The keypad lighting is controlled by 3 methods, which are all exclusive of each other.

These are:

- ALC
- PWM
- I^2C command

If KBALC (bit 1 of 00h) is set to 1, then ALC for keypad is ON, otherwise, it is off.

If KYPWM (bit 0 of 03h) is set to 1, PWM for keypad is ON, otherwise, it is off.

If KYI2C (bit 5 of 02h) is set to 1, I^2C for keypad is ON, otherwise, it is off.

The ambient light level at which the key backlight is turned off can be set in register 0Fh. The default ambient light is Ah. There is also a programmable hysteresis level, accessed through I^2C in the 0Fh register. The default hysteresis width is 3h. See Figure 7.

There is a built in PWM that has a 500Hz operation frequency. The dimming can be adjusted by duty ratio (set KYDT_ bit in register 0Eh).

The KEY output is simply a 1 bit value representing ON or OFF function.

Keypad Backlight ON/OFF Operation by ALC

To link the keypad backlight ON/OFF control to the ALC, the register bit, KBALC, at register 00h, should be set to 1 (see Table 5).

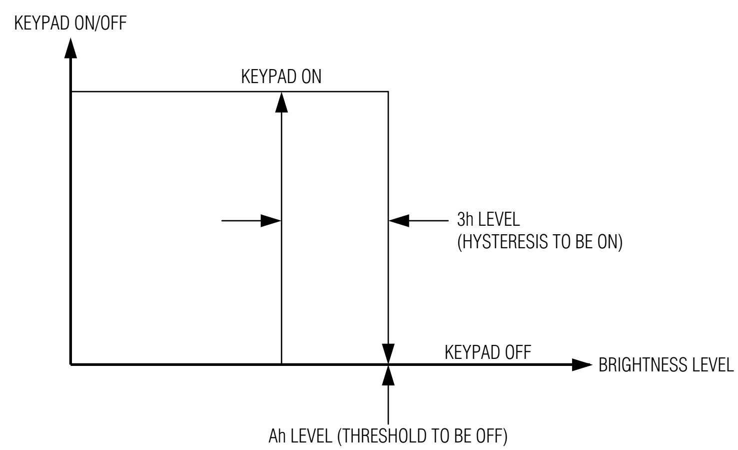


Figure 7. KEY On/Off Hysteresis

Table 5. Keypad Backlight On/Off by ALC

ALCEN	KBALC	MAIN WLEDs IN ALC MODE	ALC BLOCK	KEY BACKLIGHT
0	0	No	OFF	OFF
0	1			ON/OFF by I^2C or PWM*
1	0	Yes	ON	ON/OFF by I^2C or PWM**
1	1	Yes	ON	ON/OFF depends on ALC data level***

**The ALC block is disabled in this mode. In this condition, keypad backlight is activated and controlled by either internal PWM operation (500Hz) or I^2C.*

***The ALC block is enabled in this mode. However KBALC bit is still set to 0. Therefore, the on/off control should be either I^2C or internal 500Hz PWM.*

****The ALC block is enabled in this mode. ALC has priority over both internal PWM and I^2C in case KBALC bit is set to 1. This means that the activation of the key backlight depends on the preprogrammed on/off threshold and hysteresis width.*

The ambient light level at which the key backlight is turned off can be set in register 0Fh. The default ambient light level is Ah, which is bright enough for the user to recognize the numbers on the keypad. At this time, the key output is held off. There is also a programmable hysteresis level, accessed through I2C in the 0Fh register. The default hysteresis width is 3h. The key output is held high on any hysteresis value minus 1h. For example, if the hysteresis is set to 3h, in this default condition, the key output is held low at Ah level and then high at 6h level.

Keypad Backlight ON/OFF Operation by PWM

There is a built-in PWM signal operating at a frequency of 500Hz. The on/off can be adjusted by duty cycle ratio (set KYDT_ bit in Register 0Eh). 16 different duty values of PWM are available in register 0Eh. In addition, fade-in and fade-out can also be set up with the KYSL_ bits in the 0Eh register.

Keypad Backlight ON/OFF Operation by I2C Command

There is a dedicated register bit (KYI2C at 02h, see Table 15) to both enable and disable the KEY function. This I2C on/off is the default for KEY.

Control of Duty Transition Time Control in Internal PWM Mode (500Hz)

The internal 500Hz PWM can set up the duty transition control time by the register (KYSL1 and KYSL2 at 0Eh).

Figure 8 shows the duty transition in slope-applied mode.

Low-Drop Output (LDO) Operation

The linear regulators are designed for low-input, low-dropout, low quiescent current to maximize battery life. All LDOs are controlled through the serial interface, minimizing the requirements of control lines to the MAX8930.

Each of the LDOs are turned on or off through the setting of the control bits in the On/Off Control register, 00h. For each LDO, it is possible to set the output voltage and enable/disable the active pulldown resistor (1kΩ typ) during power-off. This is done in the 03h and 04h registers. For optimized battery life, there are two external supply voltage inputs, PV3 for LDO1 and LDO2 and PV4 for LDO3. This allows the input voltage of the LDO to be supplied from a lower voltage power rail, resulting in higher efficiency operation and longer battery life. LDO3 is a low V_{IN} LDO (V_{IN} = 1.7V to 5.5V). The input voltage, V_{PV3} and V_{PV4} must be greater than the selected LDO1 to LDO3 voltages.

GPO Operation

Three LDO outputs have the option of being converted to GPO outputs through an I2C command. Figure 9 shows the external connections. The register, 24h, is responsible for this setup. In GPO mode, the output capacitors should be removed in advance, otherwise, there is some delay in both turn-on and turn-off mode.

Component Selection

Use only ceramic capacitors with an X5R, X7R, or better dielectric. See the Table 6 for a list of recommended parts. Connect a 1µF and 2.2µF ceramic capacitor between LDO1, LDO2, and LDO3 and PGND3, respectively, for 200mA applications. The LDO output capacitor's equivalent series resistance (ESR) affects stability and output noise. Use output capacitors with an ESR of 0.1Ω or less to ensure stability and optimum transient

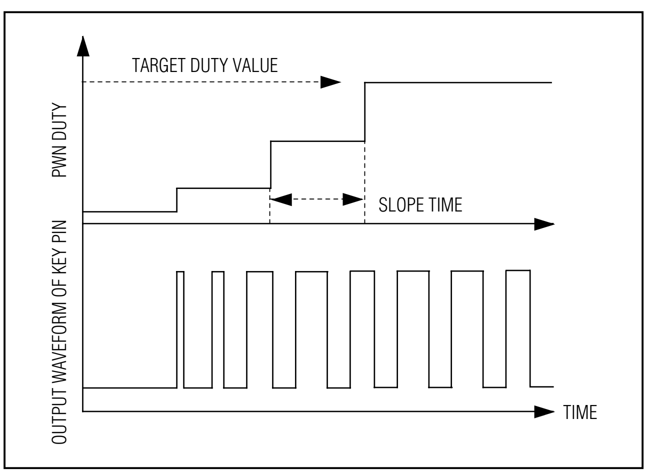


Figure 8. Slope Time-In Internal PWM Mode (500Hz)

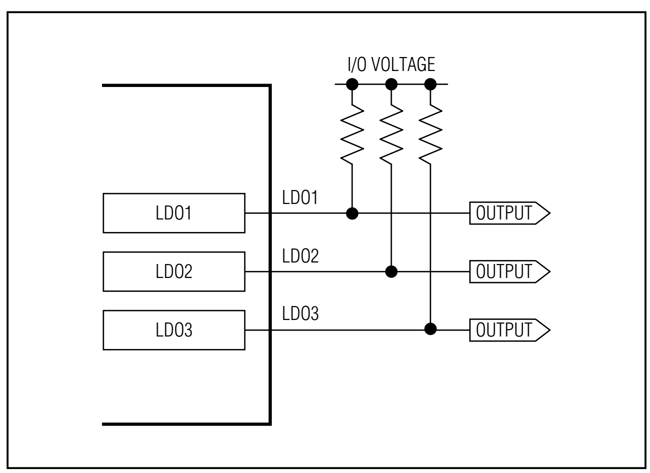


Figure 9. LDO GPO Configuration

Table 6. Recommended Capacitors

DESIGNATION	VALUE (µF)	MANUFACTURER	PART NUMBER	DESCRIPTION
C_{PV3}	2.2	TDK	C2012X5R0J225M	2.2µF ±20%, 6.3V X5R ceramic capacitor
C_{PV4} (in case of external supply)	2.2	TDK	C2012X5R0J225M	2.2µF ±20%, 6.3V X5R ceramic capacitor
C_{LDO1}	1	TDK	C1005X5R0J105M	1µF ±20%, 6.3V X5R ceramic capacitor
C_{LDO2}	1	TDK	C1005X5R0J105M	1µF ±20%, 6.3V X5R ceramic capacitor
C_{LDO3}	2.2	TDK	C1005X5R0J225M	2.2µF ±20%, 6.3V X5R ceramic capacitor

response. Connect C_{LDO} as close as possible to the MAX8930 to minimize the impact of PCB trace inductance.

Step-Up DC-DC Converter Operation

The step-up DC-DC converter operates from a 2.7V to 5.5V supply. The MAX8930 includes an internal high-voltage nMOSFET switch with low on-resistance and a synchronous rectifier to reduce losses and achieve higher efficiency. A true-shutdown feature disconnects the battery from the load and reduces the supply current to 0.05µA. This DC-DC converter provides adjustable output voltage from 13.0V to 16.5V with 0.5V steps. The adjustment bits are located in the 04h register.

Control Scheme

The step-up DC-DC features a minimum off-time, current-limited control scheme operating in discontinuous conduction mode. An internal p-channel MOSFET switch connects PV5 to SW to provide power to the inductor when the converter is operating. When the converter is shut down, this switch disconnects the input supply from the inductor. To boost the output voltage, an n-channel MOSFET switch turns on and allows the inductor current to ramp up to the current limit. Once the inductor current reaches the current limit, the switch turns off and the inductor current flows through synchronous rectifier (pMOS) to supply the output voltage. The switching frequency varies depending on the load and input and output voltage and can be up to 750kHz.

Setting the Output Voltage

The output voltage of the step-up converter is set by bit, boost1 to boost3, in Register 04h. The output voltage can be adjusted from 13.0V to 16.5V in 0.5V increments.

Shutdown

If Bit 6, SUEN, in Register 00h is set to 0, the step-up converter enters shutdown. During shutdown, the output is disconnected from the input, and LX enters a high-impedance state. The capacitance and load at the output determine the rate at which V_{OUT} decays.

Soft-Start

The step-up converter uses two soft-start mechanisms. When the true-shutdown feature is used, the gate of the internal synchronous turns on slowly to prevent inrush current. This takes approximately 0.04ms (typ). When SW is fully turned on, the internal n-channel switch begins boosting the input to set the output voltage.

Protection Features

The step-up converter has protection features designed to make it extremely robust to application errors. If the output capacitor in the application is missing, the converter protects the internal switch from being damaged.

Table 7. Protection Features

APPLICATION FAULTS	PROTECTION
Output Shorted to Ground	True off-switch detects short, opens when current reaches the synchronous rectifier current limit, and restarts soft-start. This protects the inductor and the synchronous rectifier.
Output Capacitor Missing	LX may boost one or two times before the internal FB voltage exceeds the trip point. In the rare case where the capacitive loading and external loading on OUT is small enough that the energy in one cycle can slew it more than 22V, the internal OVP operates at the typical threshold value, 18.5V.

Inductor Selection

Smaller inductance values typically offer smaller physical size for a given series resistance or saturation current. The inductor's saturation current rating should be greater than the peak switching current. Recommended inductor values range from 10µH to 100µH (e.g., 22µH, VLF3010AT-220MR33-1, TDK).

Capacitor Selection

Small, ceramic surface-mount capacitors with X7R or X5R temperature characteristics are recommended due to their small size, low cost, low equivalent series resistance (ESR), and low equivalent series inductance (ESL). If nonceramic capacitors are used, it is important that they have low ESR to reduce the output ripple voltage and peak-to-peak load transient voltage.

$\overline{CHG}$ Charge-Indicator Output

$\overline{CHG}$ is an open-drain output that indicates charger status and can be used with an LED. $\overline{CHG}$ goes low during charging when the bit of $\overline{CHG}$ at 02h is 1. $\overline{CHG}$ goes high impedance when the bit of $\overline{CHG}$ at 02h is 0. When this function is used in conjunction with a microprocessor (µP), connect a pullup resistor between $\overline{CHG}$ and the logic I/O voltage to indicate charge status to the µP.

I²C Interface

The slave address for MAX8930 is EC/Dh in write/read mode.

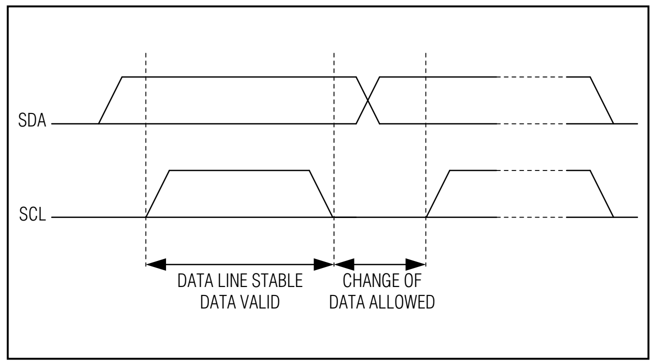


Figure 10. SDA and SCL Bit Transfer

Table 8. Recommended Inductors

DESIGNATION	VALUE (µH)	DCR (Ω)	MANUFACTURER	PART	CURRENT (mA)
L_{SW}	22	1.5	TDK	VLF3010AT-220MR33-1	330
	22	4.0	Panasonic	ELJPC220KF	160
	22	1.0	Taiyo Yuden	LB2016-220	105
	22	5.0	Taiyo Yuden	LEM2520-220	125
	47	2.2	Sumida	CMD4D11-47	180
	68	3.3	Taiyo Yuden	LEMC3225-680	120

Table 9. Recommended Capacitors

DESIGNATION	VALUE (µF)	MANUFACTURER	PART	DESCRIPTION
C_{PV5}	1	TDK	C2012X5R0J105M	1µF ±20%, 6.3V X5R ceramic capacitor
C_{OUT}	1	Taiyo Yuden	TMK316BJ105KL	1µF ±20%, 25V X7R ceramic capacitor

Table 10. Slave Address

A7	A6	A5	A4	A3	A2	A1	R/W
1	1	1	0	1	1	0	1/0

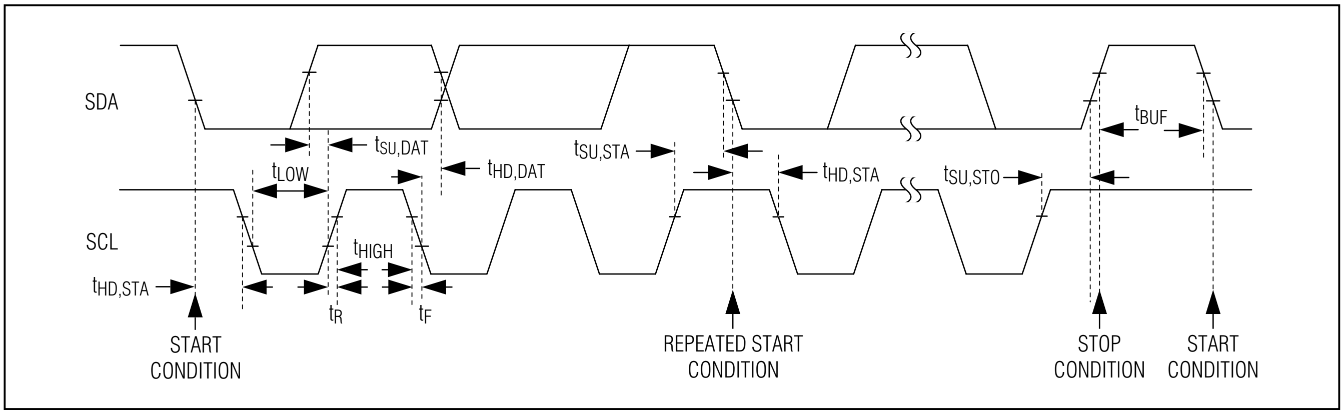


Figure 11. START and STOP Conditions

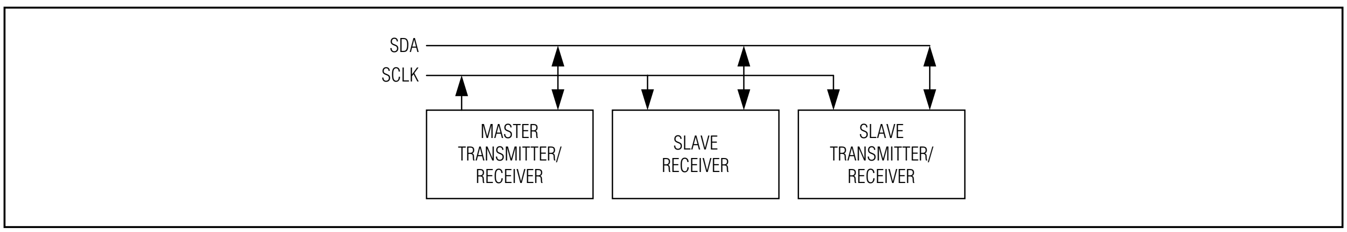


Figure 12. I²C Master and Slave Configuration

I²C Bit Transfer

One data bit is transferred for each clock pulse. The data on SDA must remain stable during the high portion of the clock pulse as changes in data during this time are interpreted as a control signal.

I²C START and STOP Conditions

Both SDA and SCL remain high when the bus is not busy. A high-to-low transition of SDA, while SCL is high is defined as the START (S) condition. A low-to-high transition of the data line while SCL is high is defined as the STOP (P) condition.

I²C System Configuration

A device on the I²C bus that generates a message is called a transmitter and a device that receives the message is a receiver. The device that controls the message is the master and the devices that are controlled by the master are called slaves.

I²C Acknowledge

The number of data bytes between the START and STOP conditions for the transmitter and receiver are unlimited. Each 8-bit byte is followed by an acknowledge bit. The acknowledge bit is a high-level signal put on DATA by the transmitter during which time the master generates an extra acknowledge related clock pulse. A slave receiver that is addressed must generate an acknowledge after each byte it receives. Also, a master receiver must generate an acknowledge after each byte it receives that has been clocked out of the slave transmitter.

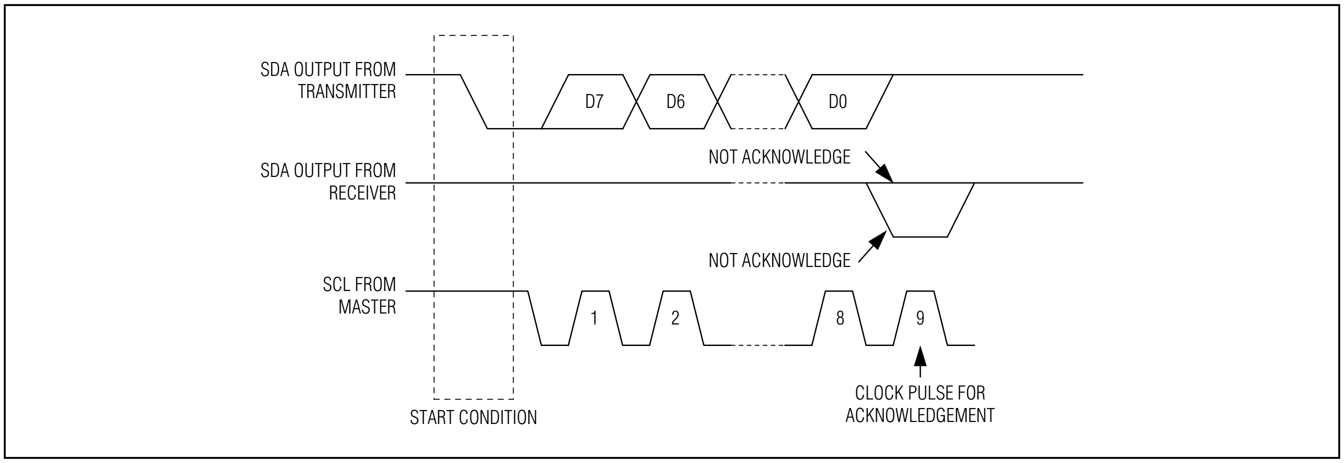


Figure 13. I²C Acknowledge

The device that acknowledges must pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable low during the high period of the acknowledge clock pulse (setup and hold times must also be met). A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this case, the transmitter must leave SDA high to enable the master to generate a STOP condition.

Current Level for 8 WLEDs and 3 RGB LEDs

The total 11 LEDs (8 WLEDs and 3 RGB LEDs) have linear scale current dimming by 0.1mA step as follows.

Table 11. LED Current Levels

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	LED CURRENT (mA)
0	0	0	0	0	0	0	0	0.1
0	0	0	0	0	0	0	1	0.2
0	0	0	0	0	0	1	0	0.3
0	0	0	0	0	0	1	1	0.4
0	0	0	0	0	1	0	0	0.5
0	0	0	0	0	1	0	1	0.6
0	0	0	0	0	1	1	0	0.7
—	—	—	—	—	—	—	—	—
—	—	—	—	—	—	—	—	—
1	1	1	1	1	1	1	0	25.5
1	1	1	1	1	1	1	1	25.6

Table 12. Register Map

ADDRESS (HEX)	POR (HEX)	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	FUNCTION
00h	00	RESET	SUEN	LDO1	LDO2	LDO3	Main WLED	KBALC	ALCEN	On/off control for boost, LDO1, LDO2, LDO3, main WLED_, ALC
01h	00	WLED7	WLED6	WLED5	Sub7	Sub6	Sub5	RGB slope	LED slope	On/off control for backlight-related LEDs
02h	26	CAI	$\overline{CHG}$	KYI2C	WLED8	Sub8	x	MAIN I2C	HLCAI	On/off control for dimming-related signal, bias output
03h	6C	LDO10	LDO11	LDO12	x	LDO20	LDO21	LDO22	KYPWM	Output program for LDO1 and LDO2
04h	BA	LDO 30	LDO 31	LDO1ADIS	LDO2ADIS	LDO3ADIS	Boost1	Boost2	Boost3	Output program for LDO3 and boost
05h	01	IMLED7	IMLED6	IMLED5	IMLED4	IMLED3	IMLED2	IMLED1	IMLED0	256 steps current scale for main WLEDs
06h	01	ISLED7	ISLED6	ISLED5	ISLED4	ISLED3	ISLED2	ISLED1	ISLED0	256 steps current scale for sub WLED5
07h	01	ISLED7	ISLED6	ISLED5	ISLED4	ISLED3	ISLED2	ISLED1	ISLED0	256 steps current scale for sub WLED6
08h	01	ISLED7	ISLED6	ISLED5	ISLED4	ISLED3	ISLED2	ISLED1	ISLED0	256 steps current scale for sub WLED7

Table 12. Register Map (continued)

ADDRESS (HEX)	POR (HEX)	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	FUNCTION
09h	01	ISLED7	ISLED6	ISLED5	ISLED4	ISLED3	ISLED2	ISLED1	ISLED0	256 steps current scale for sub WLED8
0Ah	00	x	DSLP3	DSLP2	DSLP1	x	USLP3	USLP2	USLP1	Slope control for main WLEDs in step-up/down
0Bh	00	x	DSLP3	DSLP2	DSLP1	x	USLP3	USLP2	USLP1	Slope control for RGB in step-up/down
0Ch	10	SBIAS	LSTY	ALCYC1	ALCYC2	OST1	OST2	OST3	OST4	Control for ALC-related functions
0Dh	—	ALDA1	ALDA2	ALDA3	ALDA4	x	x	x	TWAIT	Read the ADC data based on ambient condition
0Eh	00	KYSL1	KYSL2	x	KYDT0	KYDT1	KYDT2	KYDT3	KYDT4	Control for PWM slope and duty
0Fh	A8	KYHS1	KYHS2	KYTH1	KYTH2	KYTH3	KYTH4	x	x	Control for hysteresis width and on/off
10h	0F	CADA07	CADA06	CADA05	CADA04	CADA03	CADA02	CADA01	CADA00	Current level of 0h
11h	1E	CADA17	CADA16	CADA15	CADA14	CADA13	CADA12	CADA11	CADA10	Current level of 1h
12h	2D	CADA27	CADA26	CADA25	CADA24	CADA23	CADA22	CADA21	CADA20	Current level of 2h
13h	3C	CADA37	CADA36	CADA35	CADA34	CADA33	CADA32	CADA31	CADA30	Current level of 3h
14h	4C	CADA47	CADA46	CADA45	CADA44	CADA43	CADA42	CADA41	CADA40	Current level of 4h
15h	5B	CADA57	CADA56	CADA55	CADA54	CADA53	CADA52	CADA51	CADA50	Current level of 5h

Table 12. Register Map (continued)

ADDRESS (HEX)	POR (HEX)	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	FUNCTION
16h	6A	CADA67	CADA66	CADA65	CADA64	CADA63	CADA62	CADA61	CADA60	Current level of 6h
17h	79	CADA77	CADA76	CADA75	CADA74	CADA73	CADA72	CADA71	CADA70	Current level of 7h
18h	89	CADA87	CADA86	CADA85	CADA84	CADA83	CADA82	CADA81	CADA80	Current level of 8h
19h	98	CADA97	CADA96	CADA95	CADA94	CADA93	CADA92	CADA91	CADA90	Current level of 9h
1Ah	A7	CADAA7	CADAA6	CADAA5	CADAA4	CADAA3	CADAA2	CADAA1	CADAA0	Current level of Ah
1Bh	B6	CADAB7	CADAB6	CADAB5	CADAB4	CADAB3	CADAB2	CADAB1	CADAB0	Current level of Bh
1Ch	C6	CADAC7	CADAC6	CADAC5	CADAC4	CADAC3	CADAC2	CADAC1	CADAC0	Current level of Ch
1Dh	D5	CADAD7	CADAD6	CADAD5	CADAD4	CADAD3	CADAD2	CADAD1	CADAD0	Current level of Dh
1Eh	E4	CADAE7	CADAE6	CADAE5	CADAE4	CADAE3	CADAE2	CADAE1	CADAE0	Current level of Eh
1Fh	F9	CADAF7	CADAF6	CADAF5	CADAF4	CADAF3	CADAF2	CADAF1	CADAF0	Current level of Fh
20h	00	RGBEN	x	x	RI2C	GI2C	BI2C	HLRGB	x	Control for on/off of RGB
21h	01	RLED7	RLED6	RLED5	RLED4	RLED3	RLED2	RLED1	RLED0	Current level for Red
22h	01	GLED7	GLED6	GLED5	GLED4	GLED3	GLED2	GLED1	GLED0	Current level for Green
23h	01	BLED7	BLED6	BLED5	BLED4	BLED3	BLED2	BLED1	BLED0	Current level for Blue
24h	00	GPO1	GPO2	x	GPLD1	GPLD2	GPLD3	GPWD8	x	On/off for GPO

x = Don't care.

POR = Default state at reset and initial startup condition.

Table 13. On/Off Register 1 for Boost, LDO1, LDO2, LDO3, Main WLED, and ALC

ADDRESS (HEX)	POR (HEX)	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
00	00	RESET	SUEN	LDO1	LDO2	LDO3	Main WLED	KB ALC	ALC EN
NAME	**POR**	**R/W**	**DESCRIPTION**						
RESET	0	R/W	1: IC is reset, back to POR status 0: Reset is off						
SUEN	0	R/W	1: Boost output is on 0: Boost output is off						
LDO1	0	R/W	1: LDO1 output is on 0: LDO1 output is off						
LDO2	0	R/W	1: LDO2 output is on 0: LDO2 output is off						
LDO3	0	R/W	1: LDO3 output is on 0: LDO3 output is off						
Main WLED	0	R/W	1: Main WLEDs are on 0: Main WLEDs are off						
KBALC	0	R/W	1: ALC for keypad is on 0: ALC for keypad is off						
ALCEN	0	R/W	1: ALC function for main WLEDs is on 0: ALC function is off						

Table 14. On/Off Register 2 for Backlight-Related WLED5, WLED6, WLED7 and RGB

ADDRESS (HEX)	POR (HEX)	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
01	00	WLED7	WLED6	WLED5	Sub7	Sub6	Sub5	RGB Slope	LED Slope
NAME	**POR**	**R/W**	**DESCRIPTION**						
WLED7	0	R/W	1: WLED7 output is on 0: WLED7 output is off						
WLED6	0	R/W	1: WLED6 output is on 0: WLED6 output is off						
WLED5	0	R/W	1: WLED5 output is on 0: WLED5 output is off						
SUB7	0	R/W	1: WLED7 belongs to main group 0: WLED7 belongs to subgroup						
SUB6	0	R/W	1: WLED6 belongs to main group 0: WLED6 belongs to subgroup						
SUB5	0	R/W	1: WLED5 belongs to main group 0: WLED5 belongs to subgroup						
RGB Slope	0	R/W	1: Dimming slope for RGB LED is on 0: Dimming slope is off						
LED Slope	0	R/W	1: Dimming slope for main WLED_ is on 0: Dimming slope is off						

Table 15. On/Off Register 3

ADDRESS (HEX)	POR (HEX)	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
02	26	CAI	CHG	KYI2C	WLED8	SUB8	TWAIT	MAIN I^2C	HLCAI

NAME	POR	R/W	DESCRIPTION
CAI	0	R/W	1: CAI Dimming for main WLEDs is on 0: Off
CHG	0	R/W	1: nMOS for charging indicator is on 0: Off
KYI2C	1	R/W	1: I^2C for keypad is on 0: I^2C for keypad is off
WLED8	0	R/W	1: WLED8 output is on 0: WLED8 output is off
SUB8	0	R/W	1: WLED8 belongs to main group 0: WLED8 belongs to subgroup
TWAIT	1	R/W	1: 64ms waiting time for ALC calculation 0: 32ms
MAINI2C	1	R/W	1: I^2C dimming for main WLEDs is ON 0: I^2C dimming for main WLEDs is OFF
HLCAI	0	R/W	1: Active low for main WLED_ activated 0: Active high to be ON

Table 16. LDO1 and LDO2 Register

ADDRESS (HEX)	POR (HEX)	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
03	4A	R/W	LDO10	LDO11	LDO12	Reserved	LDO20	LDO21	LDO22	KYPWM

DESCRIPTION

LDO10	LDO11	LDO12	LDO1 VOLTAGE (V)
0	0	0	2.3
0	0	1	2.5
0	1	0	2.6 (default)
0	1	1	2.7
1	0	0	2.8
1	0	1	2.9
1	1	0	3.0
1	1	1	3.1
LDO20	**LDO21**	**LDO22**	**LDO2 VOLTAGE (V)**
0	0	0	2.3
0	0	1	2.5
0	1	0	2.6
0	1	1	2.7
1	0	0	2.8
1	0	1	2.9 (default)
1	1	0	3.0
1	1	1	3.1

NAME	POR	DESCRIPTION
KYPWM	0	1: PWM for keypad is on. 0: PWM for keypad is off

Table 17. LDO3, Step-Up, LDO1, LDO2, and LDO3 Active Discharge Function Register

ADDRESS (HEX)	POR (HEX)	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
04	BA	R/W	LDO30	LDO31	LDO1 ADIS	LDO2 ADIS	LDO3 ADIS	Boost1	Boost2	Boost3

DESCRIPTION

LDO30	LDO31	LDO3 voltage
0	0	1.2V
0	1	1.5V
1	0	1.8V (default)
1	1	2.5V

NAME	POR	DESCRIPTION
LDO1ADIS	1	1: Enable LDO1 active discharge 0: Disable LDO1 active discharge
LDO2ADIS	1	1: Enable LDO2 active discharge 0: Disable LDO2 active discharge
LDO3ADIS	1	1: Enable LDO3 active discharge 0: Disable LDO3 active discharge

BOOST1	BOOST2	BOOST3	OUTPUT (V)
0	0	0	13.0
0	0	1	13.5
0	1	0	14.0 (default)
0	1	1	14.5
1	0	0	15.0
1	0	1	15.5
1	1	0	16.0
1	1	1	16.5

Table 18. Dimming Current Register for Main WLEDs

ADDRESS (HEX)	POR (HEX)	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
05	01	IMLED7	IMLED6	IMLED5	IMLED4	IMLED3	IMLED2	IMLED1	IMLED0

NAME	POR	R/W	DESCRIPTION								
IMLED7	0	R/W	BIT								COMMENTS
IMLED6	0	R/W	7	6	5	4	3	2	1	0	
IMLED5	0	R/W	0	0	0	0	0	0	0	0	Minimum current = 0.1mA
IMLED4	0	R/W	0	0	0	0	0	0	0	1	0.2mA set as default
IMLED3	0	R/W	•	•	•	•	•	•	•	•	•
IMLED2	0	R/W	1	1	1	1	1	1	1	1	Maximum LED current = 25.6mA
IMLED1	0	R/W	256 steps from 0.1 to 25.6mA by 0.1mA step by binary value increment								
IMLED0	1	R/W									

Table 19. Dimming Current Register for Sub WLED5

ADDRESS (HEX)	POR (HEX)		BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
06	01		ISLED7	ISLED6	ISLED5	ISLED4	ISLED3	ISLED2	ISLED1	ISLED0

NAME	POR	R/W	DESCRIPTION								
ISLED7	0	R/W	BIT								COMMENTS
ISLED6	0	R/W	7	6	5	4	3	2	1	0	
ISLED5	0	R/W	0	0	0	0	0	0	0	0	Minimum current = 0.1mA
ISLED4	0	R/W	0	0	0	0	0	0	0	1	0.2mA set as default
ISLED3	0	R/W	•	•	•	•	•	•	•	•	•
ISLED2	0	R/W	1	1	1	1	1	1	1	1	Maximum LED current = 25.6mA
ISLED1	0	R/W	256 steps from 0.1 to 25.6mA by 0.1mA step by binary value increment								
ISLED0	1	R/W									

Table 20. Dimming Current Register for Sub WLED6

ADDRESS (HEX)	POR (HEX)		BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
07	01		ISLED7	ISLED6	ISLED5	ISLED4	ISLED3	ISLED2	ISLED1	ISLED0

NAME	POR	R/W	DESCRIPTION								
ISLED7	0	R/W	BIT								COMMENTS
ISLED6	0	R/W	7	6	5	4	3	2	1	0	
ISLED5	0	R/W	0	0	0	0	0	0	0	0	Minimum current = 0.1mA
ISLED4	0	R/W	0	0	0	0	0	0	0	1	0.2mA set as default
ISLED3	0	R/W	•	•	•	•	•	•	•	•	•
ISLED2	0	R/W	1	1	1	1	1	1	1	1	Maximum LED current = 25.6mA
ISLED1	0	R/W	256 steps from 0.1 to 25.6mA by 0.1mA step by binary value increment								
ISLED0	1	R/W									

Table 21. Dimming Current Register for Sub WLED7

ADDRESS (HEX)	POR (HEX)	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
08	01	ISLED7	ISLED6	ISLED5	ISLED4	ISLED3	ISLED2	ISLED1	ISLED0

NAME	POR	R/W	DESCRIPTION								
ISLED7	0	R/W	BIT								COMMENTS
ISLED6	0	R/W	7	6	5	4	3	2	1	0	
ISLED5	0	R/W	0	0	0	0	0	0	0	0	Minimum current = 0.1mA
ISLED4	0	R/W	0	0	0	0	0	0	0	1	0.2mA set as default
ISLED3	0	R/W	•	•	•	•	•	•	•	•	•
ISLED2	0	R/W	1	1	1	1	1	1	1	1	Maximum LED current = 25.6mA
ISLED1	0	R/W	256 steps from 0.1 to 25.6mA by 0.1mA step by binary value increment								
ISLED0	1	R/W									

Table 22. Dimming Current Register for Sub WLED8

ADDRESS (HEX)	POR (HEX)	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
09	01	ISLED7	ISLED6	ISLED5	ISLED4	ISLED3	ISLED2	ISLED1	ISLED0

NAME	POR	R/W	DESCRIPTION								
ISLED7	0	R/W	BIT								COMMENTS
ISLED6	0	R/W	7	6	5	4	3	2	1	0	
ISLED5	0	R/W	0	0	0	0	0	0	0	0	Minimum current = 0.1mA
ISLED4	0	R/W	0	0	0	0	0	0	0	1	0.2mA set as default
ISLED3	0	R/W	•	•	•	•	•	•	•	•	•
ISLED2	0	R/W	1	1	1	1	1	1	1	1	Maximum LED current = 25.6mA
ISLED1	0	R/W	256 steps from 0.1 to 25.6mA by 0.1mA step by binary value increment								
ISLED0	1	R/W									

Table 23. Slope Control Register for Main WLEDs

ADDRESS (HEX)	POR (HEX)		BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0A	00		Reserved	DSLP3	DSLP2	DSLP1	Reserved	USLP3	USLP2	USLP1
NAME	**POR**	**R/W**	**DESCRIPTION**							
DSLP3	0	R/W	Slope control for ramp down and up has 8 steps, respectively (see details in Table 25)							
DSLP2	0	R/W								
DSLP1	0	R/W								
USLP4	0	R/W								
USLP4	0	R/W								
USLP3	0	R/W								

Table 24. Slope Control Register for RGB LED

ADDRESS (HEX)	POR (HEX)		BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0B	00		Reserved	DSLP3	DSLP2	DSLP1	Reserved	USLP3	USLP2	USLP1
NAME	**POR**	**R/W**	**DESCRIPTION**							
DSLP3	0	R/W	Slope control for ramp down and up has 8 steps, respectively (see details in Table 25)							
DSLP2	0	R/W								
DSLP1	0	R/W								
USLP4	0	R/W								
USLP4	0	R/W								
USLP3	0	R/W								

Table 25. Ramp-Up/Down Transition Time in 0.1mA Step

BIT							COMMENTS
6	5	4	3	2	1	0	
0	0	0	—	•	•	•	0 seconds (default)
0	0	1	—	•	•	•	0.016ms (2^4 x 1Fs)
0	1	0	—	•	•	•	0.068ms (2^6 x 1Fs)
0	1	1	—	•	•	•	0.128ms (2^7 x 1Fs)
1	0	0	—	•	•	•	0.256ms (2^8 x 1Fs)
1	0	1	—	•	•	•	0.512ms (2^9 x 1Fs)
1	1	0	—	•	•	•	1.024ms (2^{10} x 1Fs)
1	1	1	—	•	•	•	2.048ms (2^{11} x 1Fs)
•	•	•	—	0	0	0	0 seconds (default)
•	•	•	—	0	0	1	0.016ms (2^4 x 1Fs)
•	•	•	—	0	1	0	0.068ms (2^6 x 1µs)
•	•	•	—	0	1	1	0.128ms (2^7 x 1µs)
•	•	•	—	1	0	0	0.256ms (2^8 x 1µs)
•	•	•	—	1	0	1	0.512ms (2^9 x 1µs)
•	•	•	—	1	1	0	1.024ms (2^{10} x 1µs)
•	•	•	—	1	1	1	2.048ms (2^{11} x 1µs)

Table 26. ALC Control Register 1

ADDRESS (HEX)	POR (HEX)	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0C	10	SBIAS	LSTY	ALCYC1	ALCYC2	OST1	OST2	OST3	OST4

NAME	POR	R/W	DESCRIPTION
SBIAS	0	R/W	1: Measurement cycle is synchronized 0: Always on
LSTY	0	R/W	1: LOG type of light sensor is connected 0: Linear type sensor
ALCYC1	0	R/W	The measurement cycle 00: 0.52s; 01: 1.05s 10: 1.57s; 11: 2.10s
ALCYC2	1		
OST_	0	R/W	Optimize the offset of ADC data

OST1	OST2	OST3	OST4	OFFSET VALUE
0	0	0	0	Non-offset (default)
0	0	0	1	+1 LSB
0	0	1	0	+2 LSB
0	0	1	1	+3 LSB
0	1	0	0	+4 LSB
0	1	0	1	+5 LSB
0	1	1	0	+6 LSB
0	1	1	1	+7 LSB
1	0	0	0	-8 LSB
1	0	0	1	-7 LSB
1	0	1	0	-6 LSB
1	0	1	1	-5 LSB
1	1	0	0	-4 LSB
1	1	0	1	-3 LSB
1	1	1	0	-2 LSB
1	1	1	1	-1 LSB

Table 27. ALC Control Register 2

ADDRESS (HEX)	POR (HEX)	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0D	00	ALDA1	ALDA2	ALDA3	ALDA4	Reserved	Reserved	Reserved	Reserved

NAME	POR	R/W	DESCRIPTION
ALDA_		R	16 different levels based on ambient light conditions

ALDA1	ALDA2	ALDA3	ALDA4	AMBIENT LIGHT CONDITION
0	0	0	0	0h level
0	0	0	1	1h level
0	0	1	0	2h level
0	0	1	1	3h level
0	1	0	0	4h level
0	1	0	1	5h level
0	1	1	0	6h level
0	1	1	1	7h level
1	0	0	0	8h level
1	0	0	1	9h level
1	0	1	0	Ah level
1	0	1	1	Bh level
1	1	0	0	Ch level
1	1	0	1	Dh level
1	1	1	0	Eh level
1	1	1	1	Fh level

Table 28. Keypad Control Register

ADDRESS (HEX)	POR (HEX)		BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0E	00		KYSL1	KYSL2	Reserved	KYDT0	KYDT1	KYDT2	KYDT3	KYDT4
NAME	**POR**	**R/W**	**DESCRIPTION**							
KYSL_	0	R/W	PWM slope time is the transition time for stepping to the next duty ratio (both up and down)							
KYSL1	**KYSL2**		**PWM SLOPE RISING TIME (ms)**							
0	0		0 (default)							
0	1		32							
1	0		64							
1	1		128							
NAME	**POR**	**R/W**	**DESCRIPTION**							
KYDT_	0	R/W	Duty is set by the active-high period							
KYDT0	KYDT0		KYDT2	KYDT3	KYDT4	Duty ratio				
0	0		0	0	0	0% (default)				
0	0		0	0	1	6.25%				
0	0		0	1	0	12.5%				
0	0		0	1	1	18.75%				
0	0		1	0	0	25.0%				
0	0		1	0	1	31.25%				
0	0		1	1	0	37.5%				
0	0		1	1	1	43.75%				
0	1		0	0	0	50.0%				
0	1		0	0	1	56.25%				
0	1		0	1	0	62.5%				
0	1		0	1	1	68.75%				
0	1		1	0	0	75.0%				
0	1		1	0	1	81.25%				
0	1		1	1	0	87.5%				
0	1		1	1	1	93.75%				
1	0		0	0	0	100%				

Table 29. Keypad Control Register for ALC

ADDRESS (HEX)	POR (HEX)	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0F	A8	KYHS1	KYHS2	KYTH1	KYTH2	KYTH3	KYTH4	Reserved	Reserved

NAME	POR	R/W	DESCRIPTION
KYHS_	10	R/W	The hysteresis values between ON and OFF. The value should meet the following equation. The value of KYTH_ - the value of KYHS_ > 1

KYHS1	KYHS2	Hysteresis values
0	0	No hysteresis
0	1	2h
1	0	3h
1	1	4h

NAME	POR	R/W	DESCRIPTION
KYTH_	—	R/W	Determine the OFF time based on ambient light condition

KYTH1	KYTH2	KYTH3	KYTH4	Keypad off	KYTH1
0	0	0	0	0h off	0
0	0	0	1	1h off	0
0	0	1	0	2h off	0
0	0	1	1	3h off	0
0	1	0	0	4h off	0
0	1	0	1	5h off	0
0	1	1	0	6h off	0
0	1	1	1	7h off	0
1	0	0	0	8h off	1
1	0	0	1	9h off	1
1	0	1	0	Ah off	1
1	0	1	1	Bh off	1
1	1	0	0	Ch off	1
1	1	0	1	Dh off	1
1	1	1	0	Eh off	1
1	1	1	1	Fh off	1

Table 30. Control Register in ACL 1–16

ADDRESS (HEX)	POR (HEX)		BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	
10~1F	—		CADA*7	CADA*6	CADA*5	CADA*4	CADA*3	CADA*2	CADA*1	CADA*0	
NAME	**POR**	**R/W**	**DESCRIPTION**								
			BIT								**COMMENTS**
			7	6	5	4	3	2	1	0	
CADA*	—	R/W	0	0	0	0	0	0	0	0	Minimum current = 0.1mA
			0	0	0	0	0	0	0	1	0.2mA set as default
			•	•	•	•	•	•	•	•	•
			1	1	1	1	1	1	1	1	Maximum LED current = 25.6mA
			256 steps from 0.1 to 25.6mA by 0.1mA step by binary value increment								

Refers to 0~F

Table 31. RGB LED On/Off Control Register

ADDRESS (HEX)	POR (HEX)		BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
20	00		RGBEN	Reserved	Reserved	RI2C	GI2C	BI2C	HLRGB	Reserved
NAME	**POR**	**R/W**	**DESCRIPTION**							
RGBEN	0	R/W	1: RGB LED is on by I2C 0: RGB LED is ON by play pin							
RI2C	0	R/W	1: RED LED is ON by I2C 0: Off							
GI2C	0	R/W	1: Green LED is ON by I2C 0: Off							
BI2C	0	R/W	1: Blue LED is ON by I2C 0: Off							
HLRGB	0	R/W	1: Active low for RGB LED activated 0: Active high for RGB LED ON							

Table 32. Red LED Dimming Current Control Register

ADDRESS (HEX)	POR (HEX)		BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	
21	01		RLED7	RLED6	RLED5	RLED4	RLED3	RLED2	RLED1	RLED0	
NAME	**POR**	**R/W**	**DESCRIPTION**								
RLED7	0	R/W	**BIT**								**COMMENTS**
RLED6	0	R/W	7	6	5	4	3	2	1	0	
RLED5	0	R/W	0	0	0	0	0	0	0	0	Minimum current = 0.1mA
RLED4	0	R/W	0	0	0	0	0	0	0	1	0.2mA set as default
RLED3	0	R/W	•	•	•	•	•	•	•	•	•
RLED2	0	R/W	1	1	1	1	1	1	1	1	Maximum LED current = 25.6mA
RLED1	0	R/W	256 steps from 0.1 to 25.6mA by 0.1mA step by binary value increment								
RLED0	1	R/W									

Table 33. Green LED Dimming Current Control Register

ADDRESS (HEX)	POR (HEX)	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
22	01	GLED7	GLED6	GLED5	GLED4	GLED3	GLED2	GLED1	GLED0

NAME	POR	R/W	DESCRIPTION								
GLED7	0	R/W	BIT								COMMENTS
GLED6	0	R/W	7	6	5	4	3	2	1	0	
GLED5	0	R/W	0	0	0	0	0	0	0	0	Minimum current = 0.1mA
GLED4	0	R/W	0	0	0	0	0	0	0	1	0.2mA set as default
GLED3	0	R/W	•	•	•	•	•	•	•	•	•
GLED2	0	R/W	1	1	1	1	1	1	1	1	Maximum LED current = 25.6mA
GLED1	0	R/W	256 steps from 0.1 to 25.6mA by 0.1mA step by binary value increment								
GLED0	1	R/W									

Table 34. Blue LED Dimming Current Control Register

ADDRESS (HEX)	POR (HEX)	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
23	01	BLED7	BLED6	BLED5	BLED4	BLED3	BLED2	BLED1	BLED0

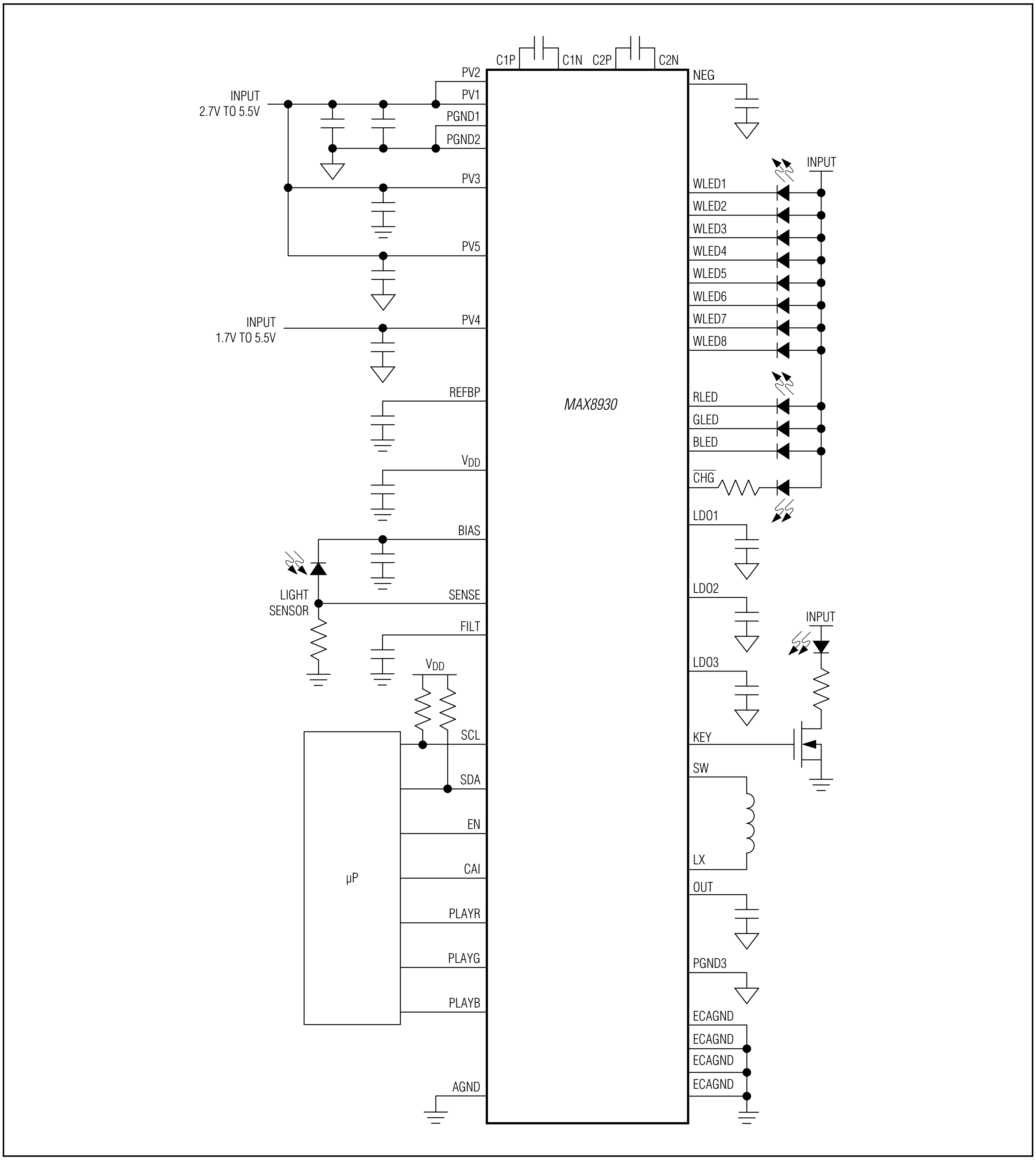
NAME	POR	R/W	DESCRIPTION								
BLED7	0	R/W	BIT								COMMENTS
BLED6	0	R/W	7	6	5	4	3	2	1	0	
BLED5	0	R/W	0	0	0	0	0	0	0	0	Minimum current = 0.1mA
BLED4	0	R/W	0	0	0	0	0	0	0	1	0.2mA set as default
BLED3	0	R/W	•	•	•	•	•	•	•	•	•
BLED2	0	R/W	1	1	1	1	1	1	1	1	Maximum LED current = 25.6mA
BLED1	0	R/W	256 steps from 0.1 to 25.6mA by 0.1mA step by binary value increment								
BLED0	1	R/W									

Table 35. On/Off Control Register

ADDRESS (HEX)	POR (HEX)	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
24	00	GPO1	Reserved	Reserved	GPLD1	GPLD2	GPLD3	Reserved	Reserved

NAME	POR	R/W	DESCRIPTION
GPO1	0	R/W	1: GPO mode 0: LDO Mode for LDO1, LDO2, LDO3
GPLD1	0	R/W	1: Output low for LDO1 (power SW on) 0: Output high (power SW off)
GPLD2	0	R/W	1: Output low for LDO2 (power SW on) 0: Output high (Power SW off)
GPLD3	0	R/W	1: Output low for LDO3 (power SW on) 0: Output high (power SW off)

Typical Operating Circuit



PCB Layout

Good PCB layout is essential for optimizing performance. Use large traces for the power-supply inputs to minimize losses due to parasitic trace resistance and route heat away from the device. Good design minimizes excessive EMI on the switching paths and voltage gradients in the ground plane, resulting in a stable and well regulated charge pump. Connect all capacitors as close as possible to the IC and keep their traces short, direct, and wide. Keep noisy traces, as short as possible. Connect AGND, PGND1, PGND2, and PGND3 to the common ground plane.

Chip Information

PROCESS: BiCMOS

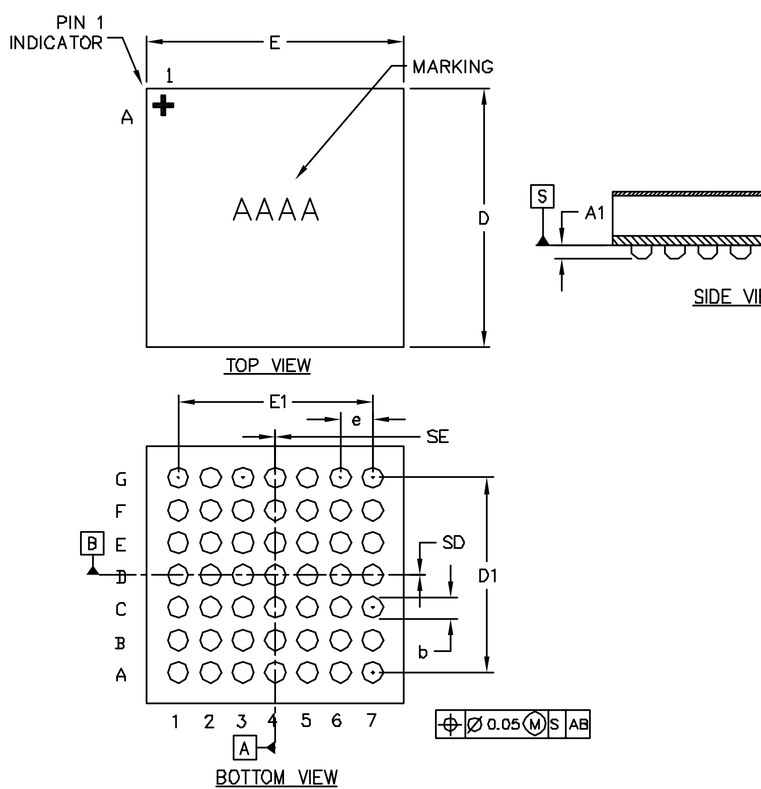
MAX8930

WLED Charge Pump, RGB, OLED Boost, LDOs with ALC and CAI

Package Information

For the latest package outline information and land patterns, go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
49 WLP	W493B3+2	21-0441



COMMON DIMENSIONS	
A	0.64±0.05
A1	0.21±0.03
A2	0.43 REF
A3	0.025 BASIC
A4	0.07 BASIC
b	ø0.26±0.03
D1	2.40
E1	2.40
e	0.40 BASIC
SD	0.00 BASIC
SE	0.00 BASIC

PKG. CODE	E		D		DEPOPULATED BUMPS
	MIN	MAX	MIN	MAX	
W493B3+2	3.05	3.25	3.05	3.25	NONE

NOTES:
1. Terminal pitch is defined by terminal center to center value.
2. Outer dimension is defined by center lines between scribe lines.
3. All dimensions in millimeters.
4. Marking shown is for package orientation reference only.
5. Tolerance is ± 0.02mm unless specified otherwise.
6. All dimensions apply to PbFree (+) package codes only.

-DRAWING NOT TO SCALE-

TITLE: PACKAGE OUTLINE 49 BUMPS, WLP PKG. 0.4mm PITCH

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0443	A	1/1