# MOSFET - N-Channel, Small Signal, SOT-23 60 V, 115 mA

# 2N7002L, 2V7002L

#### **Features**

- 2V Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable (2V7002L)
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

## **MAXIMUM RATINGS**

Rating	Symbol	Value	Unit
Drain-Source Voltage	$V_{DSS}$	60	Vdc
Drain-Gate Voltage ( $R_{GS}$ = 1.0 $M\Omega$ )	$V_{DGR}$	60	Vdc
Drain Current  - Continuous $T_C = 25^{\circ}C$ (Note 1) $T_C = 100^{\circ}C$ (Note 1)  - Pulsed (Note 2)	I <sub>D</sub> I <sub>D</sub> I <sub>DM</sub>	±115 ±75 ±800	mAdc
Gate–Source Voltage  – Continuous  – Non–repetitive (t <sub>p</sub> ≤ 50 μs)	V <sub>GS</sub> V <sub>GSM</sub>	±20 ±40	Vdc Vpk

## THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Total Device Dissipation FR-5 Board (Note 3) T <sub>A</sub> = 25°C Derate above 25°C Thermal Resistance, Junction-to-Ambient	$P_D$	225 1.8 556	mW mW/°C °C/W
Total Device Dissipation (Note 4) Alumina Substrate, T <sub>A</sub> = 25°C Derate above 25°C Thermal Resistance, Junction–to–Ambient	P <sub>D</sub>	300 2.4 417	mW mW/°C °C/W
Junction and Storage Temperature	T <sub>J</sub> , T <sub>stg</sub>	-55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- The Power Dissipation of the package may result in a lower continuous drain current.
- 2. Pulse Test: Pulse Width  $\leq$  300  $\mu$ s, Duty Cycle  $\leq$  2.0%.
- 3.  $FR-5 = 1.0 \times 0.75 \times 0.062$  in.
- 4. Alumina = 0.4 x 0.3 x 0.025 in 99.5% alumina.

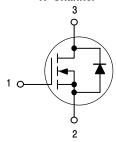


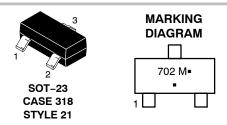
## ON Semiconductor®

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V <sub>(BR)DSS</sub>	R <sub>DS(on)</sub> MAX	I <sub>D</sub> MAX
60 V	7.5 Ω @ 10 V, 500 mA	115 mA

#### N-Channel





702 = Device Code M = Date Code\* • Pb-Free Package

(Note: Microdot may be in either location)
\*Date Code orientation and/or position may vary depending upon manufacturing location.

### **ORDERING INFORMATION**

Device	Package	Shipping <sup>†</sup>
2N7002LT1G		3,000 Tape & Reel
2N7002LT3G	SOT-23 (Pb-Free)	10,000 Tape & Reel
2N7002LT7G	]`	3,500 Tape & Reel
2V7002LT1G		3,000 Tape & Reel
2V7002LT3G	SOT-23 (Pb-Free)	10,000 Tape & Reel
2N7002LT1H*		3,000 Tape & Reel
2N7002LT7H*		3,500 Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

<sup>\*</sup>Not for new design.

## 2N7002L, 2V7002L

## **ELECTRICAL CHARACTERISTICS** ( $T_A = 25^{\circ}C$ unless otherwise noted)

Characteristic	Symbol	Min	Тур	Max	Unit
OFF CHARACTERISTICS					•
Drain-Source Breakdown Voltage $(V_{GS} = 0, I_D = 10 \mu Adc)$	V <sub>(BR)DSS</sub>	60	-	-	Vdc
Zero Gate Voltage Drain Current $T_J = 25^{\circ}C$ $(V_{GS} = 0, V_{DS} = 60 \text{ Vdc})$ $T_J = 125^{\circ}C$	I <sub>DSS</sub>	- -	- -	1.0 500	μAdc
Gate-Body Leakage Current, Forward (V <sub>GS</sub> = 20 Vdc)	I <sub>GSSF</sub>	-	-	100	nAdc
Gate-Body Leakage Current, Reverse (V <sub>GS</sub> = -20 Vdc)	I <sub>GSSR</sub>	-	-	-100	nAdc
ON CHARACTERISTICS (Note 5)					
Gate Threshold Voltage $(V_{DS} = V_{GS}, I_D = 250 \mu Adc)$	V <sub>GS(th)</sub>	1.0	_	2.5	Vdc
On–State Drain Current $(V_{DS} \ge 2.0 \ V_{DS(on)}, \ V_{GS} = 10 \ Vdc)$	I <sub>D(on)</sub>	500	-	-	mA
Static Drain-Source On-State Voltage ( $V_{GS}$ = 10 Vdc, $I_D$ = 500 mAdc) ( $V_{GS}$ = 5.0 Vdc, $I_D$ = 50 mAdc)	V <sub>DS(on)</sub>	- -	- -	3.75 0.375	Vdc
$ \begin{array}{lll} \text{Static Drain-Source On-State Resistance} & & & & & & \\ \text{($V_{GS}$ = 10 V, $I_{D}$ = 500 mAdc)} & & & & & & \\ \text{$T_{C}$ = 25°C} & & & & & \\ \text{$T_{C}$ = 125°C} & & & & \\ \text{($V_{GS}$ = 5.0 Vdc, $I_{D}$ = 50 mAdc)} & & & & & \\ \text{$T_{C}$ = 25°C} & & & & \\ \end{array} $	r <sub>DS(on)</sub>	- - -	- - -	7.5 13.5 7.5	Ohms
$T_{C} = 125^{\circ}C$ Forward Transconductance $(V_{DS} \ge 2.0 \ V_{DS(on)}, \ I_{D} = 200 \ \text{mAdc})$	9FS	80	_	13.5	mS
DYNAMIC CHARACTERISTICS	1			1	
Input Capacitance (V <sub>DS</sub> = 25 Vdc, V <sub>GS</sub> = 0, f = 1.0 MHz)	C <sub>iss</sub>	-	-	50	pF
Output Capacitance (V <sub>DS</sub> = 25 Vdc, V <sub>GS</sub> = 0, f = 1.0 MHz)	C <sub>oss</sub>	-	-	25	pF
Reverse Transfer Capacitance (V <sub>DS</sub> = 25 Vdc, V <sub>GS</sub> = 0, f = 1.0 MHz)	C <sub>rss</sub>	-	-	5.0	pF
SWITCHING CHARACTERISTICS (Note 5)			•	•	•
Turn–On Delay Time $(V_{DD} = 25 \text{ Vdc}, I_D \cong 500 \text{ mAdc},$	t <sub>d(on)</sub>	-	-	20	ns
Turn–Off Delay Time $R_G = 25 \Omega$ , $R_L = 50 \Omega$ , $V_{gen} = 10 V$ )	t <sub>d(off)</sub>	-	-	40	ns
BODY-DRAIN DIODE RATINGS					
Diode Forward On-Voltage (I <sub>S</sub> = 115 mAdc, V <sub>GS</sub> = 0 V)	V <sub>SD</sub>	-	-	-1.5	Vdc
Source Current Continuous (Body Diode)	I <sub>S</sub>	-	-	-115	mAdc
Source Current Pulsed	I <sub>SM</sub>	_	_	-800	mAdc

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Pulse Test: Pulse Width  $\leq$  300  $\mu$ s, Duty Cycle  $\leq$  2.0%.

## 2N7002L, 2V7002L

## TYPICAL ELECTRICAL CHARACTERISTICS

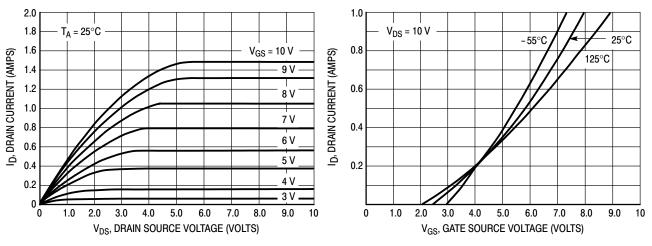


Figure 1. Ohmic Region

Figure 2. Transfer Characteristics

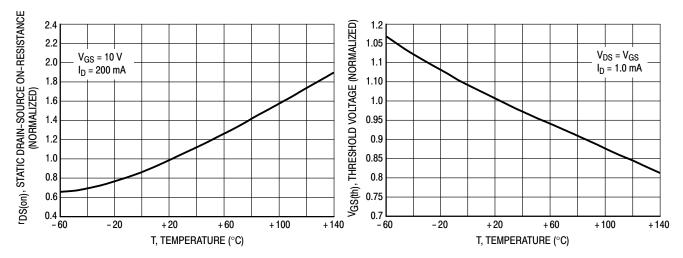


Figure 3. Temperature versus Static Drain-Source On-Resistance

Figure 4. Temperature versus Gate Threshold Voltage

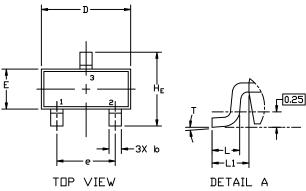




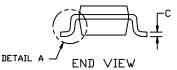
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**DATE 01 MAR 2023** 









#### NOTES:

- DIMENSIONING AND TOLERANCING PER ASME Y14.5M,1994.
- 2. CONTROLLING DIMENSION: MILLIMETERS
- 3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL.
- 4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

	MILLIM	ETERS		INCHES		
DIM	MIN.	N□M.	MAX.	MIN.	N□M.	MAX.
Α	0.89	1.00	1.11	0.035	0.039	0.044
A1	0.01	0.06	0.10	0.000	0.002	0.004
b	0.37	0.44	0.50	0.015	0.017	0.020
С	0.08	0.14	0.20	0.003	0.006	0.008
D	2.80	2.90	3.04	0.110	0.114	0.120
Ε	1.20	1.30	1.40	0.047	0.051	0.055
e	1.78	1.90	2.04	0.070	0.075	0.080
L	0.30	0.43	0.55	0.012	0.017	0.022
L1	0.35	0.54	0.69	0.014	0.021	0.027
HE	2.10	2.40	2.64	0.083	0.094	0.104
Т	0*		10°	0*		10°



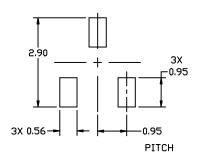


XXX = Specific Device Code

M = Date Code

■ = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.



RECOMMENDED MOUNTING FOOTPRINT

For additional information on our Pb-Free strategy and soldering details, please download the DN Semiconductor Soldering and Mounting Techniques Reference Manual, SDLDERRM/D.

## **STYLES ON PAGE 2**

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# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



## **SOT-23 (TO-236)** CASE 318 ISSUE AT

**DATE 01 MAR 2023** 

STYLE 1 THRU 5: CANCELLED	STYLE 6: PIN 1. BASE 2. EMITTER 3. COLLECTOR	STYLE 7: PIN 1. EMITTER 2. BASE 3. COLLECTOR	STYLE 8: PIN 1. ANODE 2. NO CONNECTION 3. CATHODE	1	
STYLE 9: PIN 1. ANODE 2. ANODE 3. CATHODE	STYLE 10: PIN 1. DRAIN 2. SOURCE 3. GATE	STYLE 11: PIN 1. ANODE 2. CATHODE 3. CATHODE-ANODE	STYLE 12: PIN 1. CATHODE 2. CATHODE 3. ANODE	STYLE 13: PIN 1. SOURCE 2. DRAIN 3. GATE	STYLE 14: PIN 1. CATHODE 2. GATE 3. ANODE
STYLE 15: PIN 1. GATE 2. CATHODE 3. ANODE	STYLE 16: PIN 1. ANODE 2. CATHODE 3. CATHODE	STYLE 17: PIN 1. NO CONNECTION 2. ANODE 3. CATHODE	STYLE 18: PIN 1. NO CONNECTION 2. CATHODE 3. ANODE	STYLE 19: I PIN 1. CATHODE 2. ANODE 3. CATHODE-ANODE	STYLE 20: PIN 1. CATHODE 2. ANODE 3. GATE
STYLE 21: PIN 1. GATE 2. SOURCE 3. DRAIN	STYLE 22: PIN 1. RETURN 2. OUTPUT 3. INPUT	STYLE 23: PIN 1. ANODE 2. ANODE 3. CATHODE	STYLE 24: PIN 1. GATE 2. DRAIN 3. SOURCE	STYLE 25: PIN 1. ANODE 2. CATHODE 3. GATE	STYLE 26: PIN 1. CATHODE 2. ANODE 3. NO CONNECTION
STYLE 27: PIN 1. CATHODE 2. CATHODE 3. CATHODE	STYLE 28: PIN 1. ANODE 2. ANODE 3. ANODE				

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