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AS3693B–16 Channel high precision LED driver for LCD Backlight

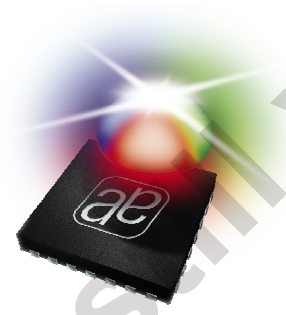
1 General Description

The AS3693B is a 16 channels high precision LED controller with built in PWM generators for driving external FETs in LCD-backlight panels.

External clock and synchronizing inputs allow the synchronization of the LCD backlight with the TV picture. Local dimming and scan dimming is supported by 16 independent PWM generators with programmable delay, period and duty cycle. Three free configurable dynamic power feedback circuits make the device usable for white LED as well as RGB backlights. Built in safety features include thermal shutdown as well as open and short LED detection. All circuit parameters are programmable via I2C or SPI interface.

2 Key Features

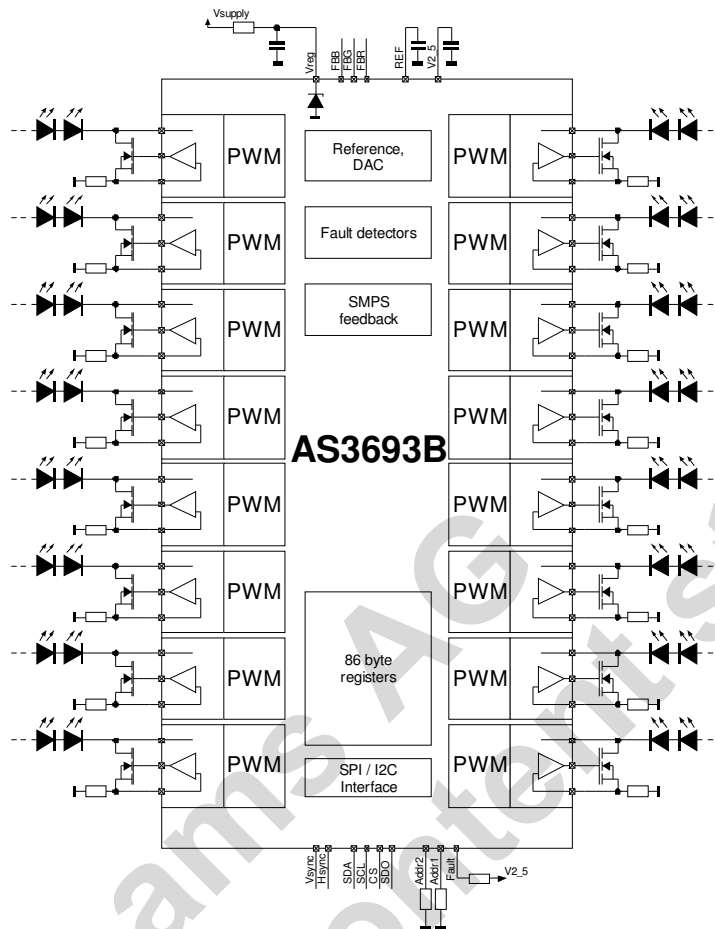
- 16 Channel LED driver
- Output current only limited by external transistor
- Output voltage 0.4V to 50V
- Absolute current accuracy +/- 0.5%
- Output slew rate programmable
- Current programmable with external resistor
- Linear current control with 8 - bit DAC
- Linear current control with external analog voltage
- Digital current control with 16 independent PWM generators

- 
- Free programmable 12 bit resolution (period, high time and delay)
 - Overvoltage detection (short LED)
 - Undervoltage detection (open LED)
 - Temperature shutdown
 - Fault interrupt output
 - H-Sync, V-Sync inputs to synchronize with TV-set
 - Internal or external PWM – clock
 - I2C interface
 - SPI interface
 - 5 bit device - address (sets device address and interface mode)
 - Automatic supply regulation feedback
 - Each output can be assigned to red, green or blue feedback.
 - Package epTQFP64 and QFN64

3 Applications

- LED backlighting for LCD – TV sets and monitors

4 Block Diagram



Typical application

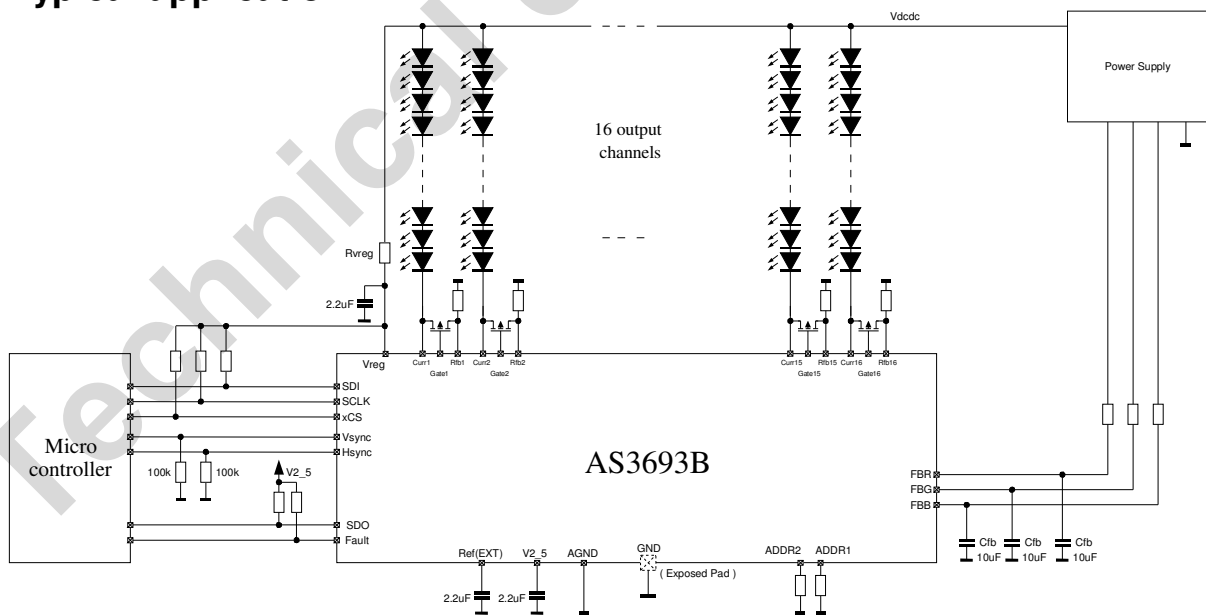


Table of Contents

| | | |
|-------|---|----|
| 1 | General Description | 1 |
| 2 | Key Features..... | 1 |
| 3 | Applications..... | 1 |
| 4 | Block Diagram..... | 2 |
| 5 | Characteristics | 4 |
| 5.1 | Absolute Maximum Ratings | 4 |
| 5.2 | Operating Conditions..... | 5 |
| 5.3 | Electrical Characteristics..... | 6 |
| 6 | Typical Operation Characteristics | 8 |
| 6.1 | Output current vs Output Voltage | 8 |
| 6.2 | Vsupply vs VREG and V2.5 at startup | 8 |
| 6.3 | 9us Slew Rate..... | 9 |
| 6.4 | Supply Regulation..... | 9 |
| 7 | Block Description | 10 |
| 7.1 | Feedback Circuit..... | 10 |
| 7.1.1 | Feedback Selection | 11 |
| 7.1.2 | Voltage fault registers..... | 12 |
| 7.2 | Curreg 1-16..... | 12 |
| 7.3 | PWM – modes | 14 |
| 7.3.1 | SYNC mode (PWM_MODE = 00)..... | 14 |
| 7.3.2 | ASYN – mode (PWM_MODE = 01) | 16 |
| 7.4 | PWM – high time, period and delay registers | 17 |
| 7.5 | Shunt Regulator | 18 |
| 7.5.1 | Undervoltage lockout..... | 18 |
| 7.6 | Over temperature control..... | 18 |
| 7.7 | Device address setup | 19 |
| 7.7.1 | I2C Device Address setup | 19 |
| 7.7.2 | SPI Device Address setup..... | 19 |
| 7.8 | Digital interface | 20 |
| 7.8.1 | I2C interface | 20 |
| 7.8.2 | SPI interface | 22 |
| 8 | Register map..... | 24 |
| 9 | Pinout and Packaging..... | 27 |
| 9.1 | Pinout..... | 27 |
| 9.2 | Package drawing epTQFP64..... | 29 |
| 9.3 | Package drawing QFN64..... | 30 |
| 10 | Ordering Information | 31 |
| | Copyright..... | 32 |
| | Disclaimer | 32 |
| | Contact Information..... | 32 |

5 Characteristics

5.1 Absolute Maximum Ratings

Stresses beyond those listed in Table 1 may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in Section 5 Electrical Characteristics is not implied.

Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 1 – Absolute Maximum Ratings

| Symbol | Parameter | Min | Max | Unit | Note |
|---------|---|-------|-----------|-----------|--|
| VDDMAX | Supply for LED's | -0.3 | >50 | V | See notes ¹ |
| VINVREG | VREG supply voltage | -0.3 | 7.0 | V | Applicable for pin VREG |
| IINVREG | Maximum Vreg current | | 100 | mA | Maximum Current flowing into Vreg |
| VIN2.5V | 2.5 V Pins | -0.3 | V2_5+0.3V | V | Applicable for 2.5V pins ⁴ |
| VIN5V | 5V Pins | -0.3 | VREG+0.3V | V | Applicable for 5V pins ² |
| VIN50V | 50V Pins | -0.3 | 55 | V | Applicable for CURRE1, CURRE2, CURRE3 up to CURRE16 |
| IIN | Input Pin Current | -25 | +25 | mA | At 25°C, Norm: Jedec 17 |
| TSTRG | Storage Temperature Range | -55 | 150 | °C | |
| | Humidity | 5 | 85 | % | Non condensing |
| VESD | Electrostatic Discharge on Pins Curr1 – Curr16 | -4000 | 4000 | V | Norm: MIL 883 E Method 3015 |
| VESD | Electrostatic Discharge on all Pins | -2000 | 2000 | V | Norm: MIL 883 E Method 3015 |
| PT | Total Power Dissipation | | 3.8W | W | At Ta = 25°C, no airflow for ePTQFP64 on two layer FR4-Cu PCB ³ |
| PDERATE | PT Derating Factor | | 40 | mW/ °C | See notes ³ |
| TBODY | Body Temperature during Soldering | | 260 | °C | according to IPC/JEDEC J-STD-020C |

Notes:

- 1, As the AS3693B is not directly connected to this supply. Only the parameters VINVREG, VIN5V and VIN50V have to be guaranteed by the application
- 2, All pins except CURRE1 to CURRE16 and 2.5V
- 3, Copper area > 9 cm², thermal vias
- 4, 2.5V Pins are Fault, SDO, ADDR1 and ADDR2

5.2 Operating Conditions

Test circuit

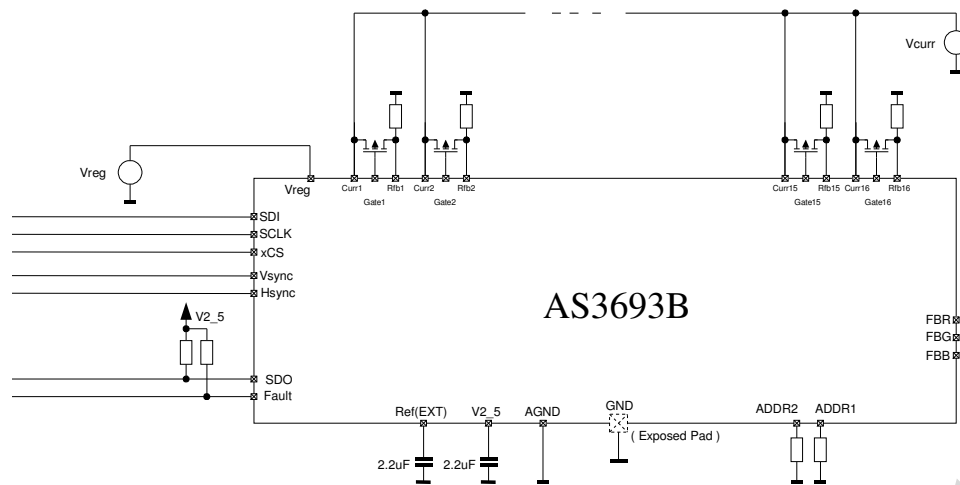


Table 2 – Operating Conditions

| Symbol | Parameter | Min | Typ | Max | Unit | Note |
|---------------|---|-----|-----|-------------|------|---|
| VDD | Main Supply | | | Not Limited | V | Supply is not directly connected to the AS3693B – see section ‘Shunt Regulator’ |
| VDDTOL | Main Supply Voltage Tolerance | -20 | | +20 | % | Applies only for supply VREG is connected via Rvdd |
| VREGINT | Supply (shunt regulated by AS3693B) | 5.0 | 5.2 | 5.4 | V | If internally (shunt-)regulated by ZD1 |
| VREGEXT | | 3 | 4.5 | 4.9 | V | If externally supplied |
| VUVL | Undervoltage lockout voltage | 2.4 | 2.7 | 3 | V | If Vreg < UVUL current sources are turned off (Addr 0x01, Addr 0x02 = 0x00) |
| IVREG | Supply Current (Chip current consumption) | | | 20 | mA | Excluding current through shunt regulator (ZD1) – see section ‘Shunt Regulator’. Note: Take care of the Power dissipation of the external Resistor. |
| IVREG_MAX | Maximum Supply current | | | 30 | mA | Maximum Current Into VREG – PIN (Supply current + shunt regulator current). |
| IVREG_EXT_OFF | | | | 350 | uA | Condition: externally supplied Curr_reg1-16 off (register 01h = 00h, register 02h = 00h) |
| Igate | Gate driving capability | 0.5 | 1 | 2 | mA | Gate1 – Gate16 output current |

5.3 Electrical Characteristics

Table 3 – Analog Electrical Characteristics

| Symbol | Parameter | Min | Typ | Max | Unit | Note |
|---------------|--|------|-----|------|------|---|
| VCURR | Voltage at CURR1 to CURR16 | | | 50.0 | V | |
| ICURR, TOL | Current Source Tolerance | -0.5 | | +0.5 | % | Using 250mV reference @25°C T _{JUNCTION} , excluding variation of external resistors |
| | | -1.5 | | +1.5 | % | Using 250mV reference -20°C to +100°C ⁽¹⁾ T _{JUNCTION} , -20°C to +85°C T _{AMB} , excluding variation of external resistors; V(CURR _X) <= 4.0V |
| | | -1.6 | | +1.6 | % | Using DAC reference VDAC =250mV (Data = 0x80) @25°C T _{JUNCTION} , excluding variation of external resistors |
| DAC_INL | DAC INL | -4 | | +4 | LSB | DAC integral nonlinearity |
| VC | Automatic Supply Regulation trip point | 0.5 | | 1 | V | See section 'Feedback Circuit (DCDC_Regulation_Trip_Point)' |
| VC,GAIN | Automatic Supply Regulation gain | | 2.0 | | mA/V | Voltage to current ratio; output current range typ. 0 to 200uA |
| TOVTEMP | Over temperature Limit | 130 | 140 | 150 | °C | Maximum junction temperature ⁽²⁾ |
| Thyst | Over temperature hysteresis | | 10 | | °C | |
| CLK | Internal Clock for PWM | 400 | 500 | 600 | KHz | Clock for internal PWM generation |

Notes:

- 1, Accuracy at +100°C guaranteed by design and verified by laboratory characterization
- 2, If the temperature exceeds the over temperature limit, the PWM will be turned off. If the temperature decreases, the PWM is activated again. The register settings are not reset.

Table 4 – Digital Input pins characteristics (SDI,VSYN,HSYN,SCL,CS)

| Symbol | Parameter | Min | Typ | Max | Unit | Note |
|-----------------------|--|------|-----|------|------|---|
| V _{IH} | High Level Input voltage | 1.3 | | VREG | V | |
| V _{IL} | Low Level Input voltage | -0.3 | | 0.4 | V | |
| f _{SCL} | Maximum SCL Frequency | | | 10 | MHz | |
| f _{HSYN} | Maximum HSYNC Frequency | | | 10 | MHz | Output driver is slew rate limited (Register: Curreg_Control 0x0D) |
| t _{s_VH} | Vsync setup time before rising edge of Hsync | 15 | | | ns | SYNC-mode: PWM values are updated with first rising edge of Hsync while Vsync = 1 (see 7.3.1.1) |
| t _{h_VH} | Vsync hold time after rising edge of Hsync | 15 | | | ns | |
| t _{s_SCISCL} | Setup time SDI,SCL | 15 | | | ns | SPI interface mode |
| t _{h_SCLSCI} | Hold time SCL,SDI | 15 | | | ns | SPI interface mode |
| t _{s_CSSCL} | Setup time CS,SCL | 15 | | | ns | SPI interface mode |

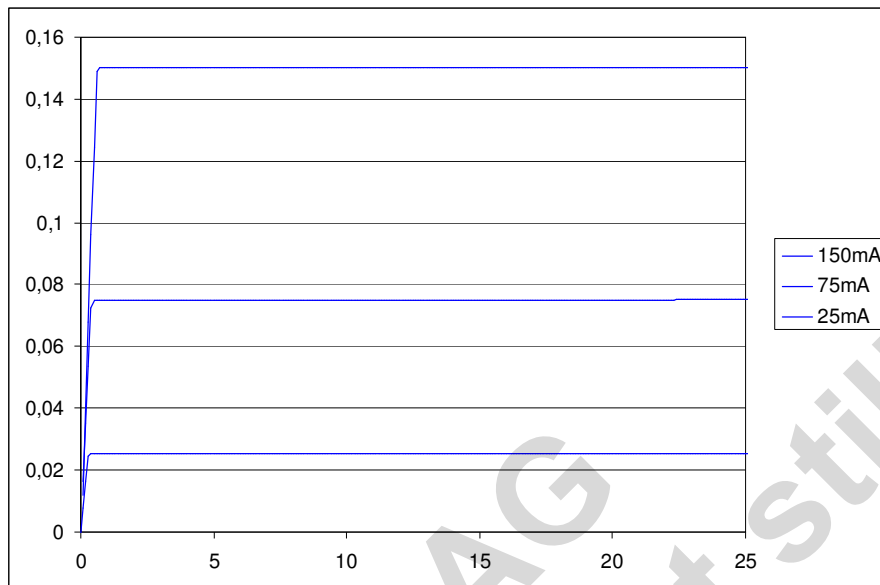
| Symbol | Parameter | Min | Typ | Max | Unit | Note |
|-------------|---|-----|-----|-----|------|--------------------|
| th_SCLCS | Hold time SCL, CS | 15 | | | ns | SPI interface mode |
| tBUF | Bus free time between Stop and Start conditions | 1.3 | | | us | I2C interface mode |
| Tsetupstart | Setup time for repeated Start condition | 100 | | | ns | I2C interface mode |
| Tholdstart | Hold time for repeated Start condition | 160 | | | ns | I2C interface mode |
| Tsetupstop | Setup time for Stop condition | 160 | | | ns | I2C interface mode |

Table 5 – Digital output pins characteristics (SDO)

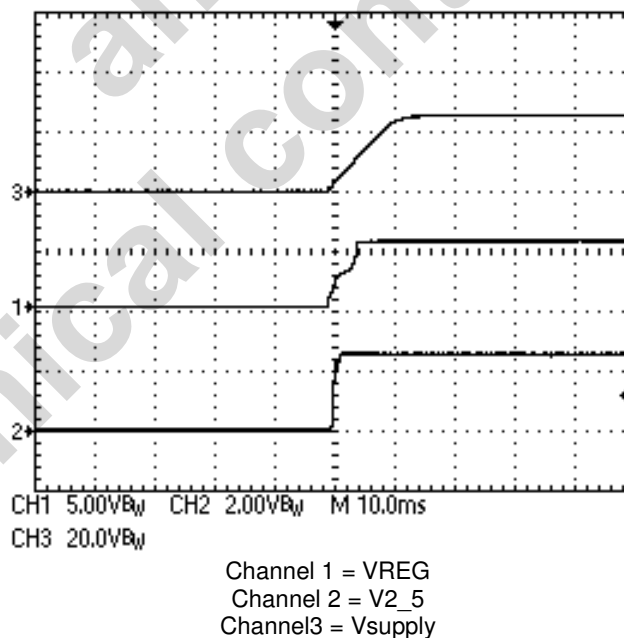
| Symbol | Parameter | Min | Typ | Max | Unit | Note |
|--------|---------------------------|------|-----|-----|------|------|
| VOH | High Level Output voltage | 2.4 | | 2.5 | V | |
| VOL | Low Level Output voltage | -0.3 | | 0.4 | V | |

6 Typical Operation Characteristics

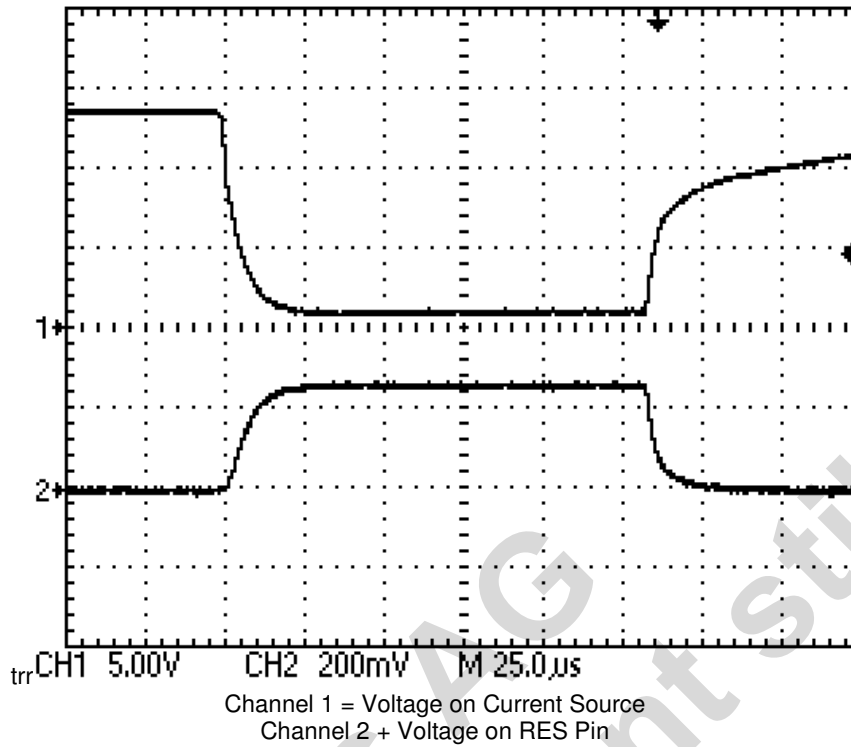
6.1 Output current vs Output Voltage



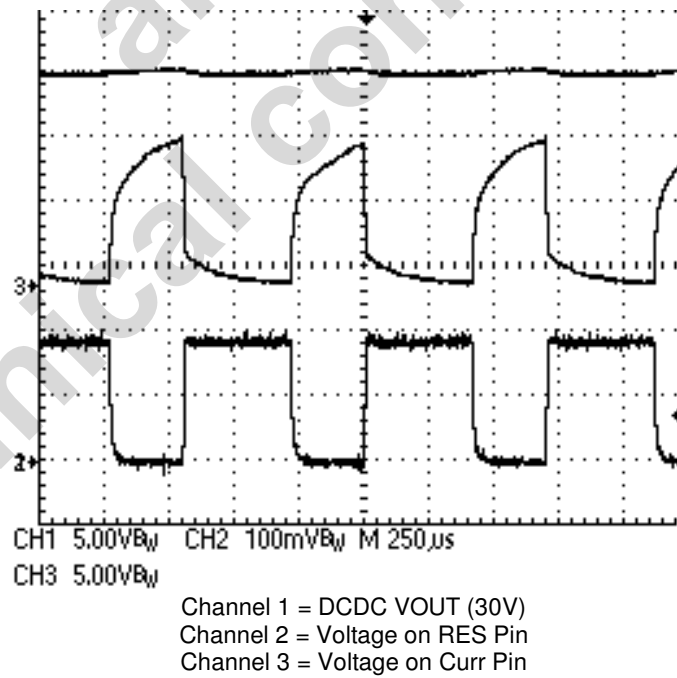
6.2 Vsupply vs VREG and V2.5 at startup



6.3 9 μ s Slew Rate



6.4 Supply Regulation



7 Block Description

7.1 Feedback Circuit

The AS3693B supports a flexible feedback selection for external DCDC – supplies. Beside the default setup for RRGB lighting, each channel can be assigned to an external DCDC feedback loop. This feedback circuit is important to reduce power dissipation of the device.

Table 6 – Feedback Control

| Addr: 04h | | Feedback control | | |
|---|---------------------------------|------------------|--------|--|
| Enables and Disables the Different Feedback modes | | | | |
| Bit | Bit Name | Default | Access | Description |
| 0 | Feedback on | 1 | R/W | 1 = Feedback Circuit is active 0 = The entire Feedback Loop is disabled |
| 1 | Feedback on PWM | 0 | R/W | 0 = The Feedback Regulator is always active 1 = The Feedback Regulator is only active, if PWM = 1 |
| 2 | Open_Led_Det_on | 0 | R/W | Enables open Led Detection Comparators 0 = Open Led Detection Disabled 1 = Open Led Detection Enabled, Level: Ucurrx = 50mV |
| 3 | Short_det_on | 0 | R/W | Enables Short detection 0 = Short detection off 1 = Sort detection on. |
| 5:4 | Short Led Detect Voltage(VSL) | | R/W | Short led Detection Trip Voltage (debounced 3mS) 00 = 2V 01 = 3V |
| 7:6 | DCDC_Regulation_trip Point (VC) | 00 | R/W | Trip Point voltage of the DCDC-Feedback Regulation Circuit. (NOTE: This value has to be adjusted if Analog Ref select Bit is changed.) 00 = 0.5V (Note use for Currents up to 70 mA) 01 = 0.6V (Note use for Currents up to 80 mA) 10 = 0.8V (Note use for Currents up to 110 mA) 11 = 1.0V (Note use for Currents up to 150 mA) |

7.1.1 Feedback Selection

In the AS3693B, each led – string feedback can be assigned to the specific led-supply, to minimize the power consumption in the system. It can be chosen in between FBR, FBG and FBB.

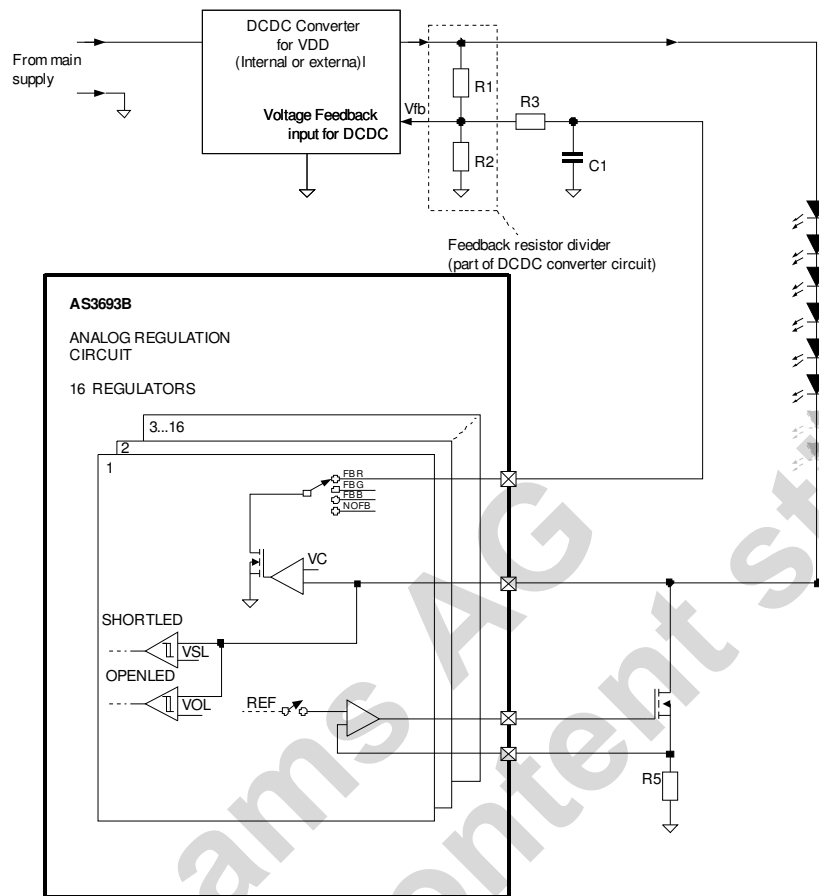


Table 7 – Feedback Selection

| Addr: 05h,06h,07h,08h | | Feedback Select 1-4 | | |
|--|--|---------------------|--------|---|
| This register controls the Feedback of the Automatic feedback loop | | | | |
| Bit | Bit Name | Default | Access | Description |
| 1:0 | FB1_Select FB5_Select FB9_Select FB13_Select | 00 | R/W | Selects the feedback of the voltage regulators 00= regulator on FBR 01= regulator on FBG 10= regulator on FBB 11= regulator not connected to FB |
| 3:2 | FB2_Select FB6_Select FB10_Select FB14_Select | 01 | R/W | Selects the feedback of the voltage regulators 00= regulator on FBR 01= regulator on FBG 10= regulator on FBB 11= regulator not connected to FB |
| 5:4 | FB3_Select FB7_Select FB11_Select FB15_Select | 01 | R/W | Selects the feedback of the voltage regulators 00= regulator on FBR 01= regulator on FBG 10= regulator on FBB 11= regulator not connected to FB |
| 7:6 | FB4_Select FB8_Select FB12_Select FB16_Select | 10 | R/W | Selects the feedback of the voltage regulators 00= regulator on FBR 01= regulator on FBG 10= regulator on FBB 11= regulator not connected to FB |

7.1.2 Voltage fault registers

In this registers an open or short led fault can be detected. If an open or short led error occurs, pin fault is pulled to 0 (3 ms debounced).

Remark: At 100% PWM duty cycle, short led fault detection is not available. Please set PWM to 99% duty cycle. Open led fault detection is available at 100% PWM duty cycle.

Table 8 – Fault Registers

| Addr: 09h-0ch | | Voltage Fault 1,2,3,4 | | |
|---|--|-----------------------|--------|---|
| This register shows a fault on any led string | | | | |
| Bit | Bit Name | Default | Access | Description |
| 1:0 | Fault_Reg 1 Fault_Reg 5 Fault_Reg 9 Fault_Reg 13 | 00 | R | Shows a error on any led string 00 = no fault 01 = open led 10 = short led |
| 3:2 | Fault_Reg 2 Fault_Reg 6 Fault_Reg 10 Fault_Reg 14 | 00 | R | Shows a error on any led string 00 = no fault 01 = open led 10 = short led |
| 5:4 | Fault_Reg 3 Fault_Reg 7 Fault_Reg 11 Fault_Reg 15 | 00 | R | Shows a error on any led string 00 = no fault 01 = open led 10 = short led |
| 7:6 | Fault_Reg 4 Fault_Reg 8 Fault_Reg 12 Fault_Reg 16 | 00 | R | Shows a error on any Led string 00 = no Fault 01 = open Led 10 = short Led |

7.2 Curreg 1-16

Each current source can be turned on and off separately.

Table 9 –Reg. Control 1

| Addr: 01h | | Reg. Control1 | | |
|--|---------------|---------------|--------|---|
| This register enables or disables the curreg 1 - 8 | | | | |
| Bit | Bit Name | Default | Access | Description |
| 7:0 | Curreg 1-8_ON | 00000000 | R/W | Enables or disables the current regulators 0 = regulator off 1 = regulator on |

Table 10– Reg.Control 2

| Addr: 02h | | Reg. Control2 | | |
|---|-----------------|---------------|--------|---|
| This Register enables or disables the curreg 9-16 | | | | |
| Bit | Bit Name | Default | Access | Description |
| 7:0 | Curreg 9 -16_ON | 00000000 | R/W | Enables or disables the current regulators 0 = regulator off 1 = regulator on |

Table 11 – CURREG_CONTROL

| Addr: 0dh | | Curreg Control | | | |
|-----------|-------------------|---|--------|--|--|
| | | Controls Rise, Fall times and References of the Curreg. | | | |
| Bit | Bit Name | Default | Access | Description | |
| 1:0 | Analog Ref Select | 00 | R/W | Voltage reference for the current regulators can be chosen with these options. 00 = 250mV reference 01 = external reference 10 = DAC reference 11 = do not use | |
| 3:2 | SLEW_RATE_CONTROL | 00 | R/W | SLEW – RATE – Control. Adjusts the rise and fall time of the current switching 00 = typ. 9us 01 = typ. 6us 10 = typ. 3us 11 = typ. 1us | |
| 5:4 | PWM_LOW_LEVEL | 00 | R/W | Note: Test bits for internal use only | |
| 7 | boost mode | 0 | R/W | Gives +30% current. only available in internal reference mode. | |

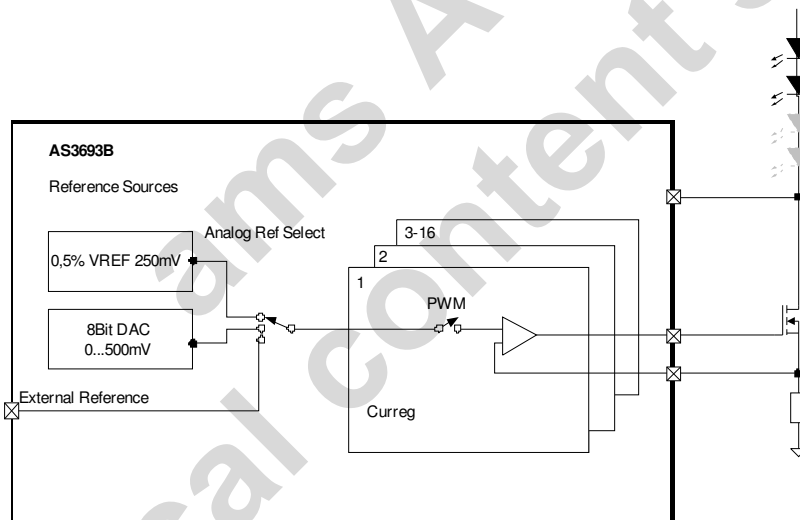


Table 12 – Ref_DAC_Voltage

| Addr: 0eh | | Ref_DAC_Voltage | | | |
|-----------|-----------------|---|--------|--|--|
| | | The Regulation Voltage can be chosen in this register | | | |
| Bit | Bit Name | Default | Access | Description | |
| 7...0 | Ref_DAC_Voltage | 00 | R/W | Reference voltage for current regulators. (Note: If Analog Ref Select = 10, the regulation voltage can be adjusted here. 00000000 = 0mV 00000001 ... 01111111 = 250 mV .. 11111111 = 500mV | |

7.3 PWM – modes

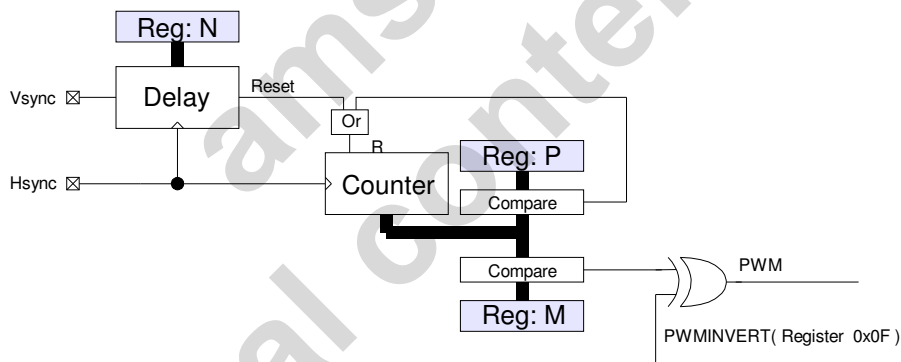
Table 14– PWM CONTROL

| Addr: 0fh | | PWM_MODE | | |
|---|--------------|----------|--------|---|
| Controls the different PWM modes and Internal or external PWM | | | | |
| Bit | Bit Name | Default | Access | Description |
| 1:0 | PWM_MODE | 01 | R/W | 00 Sync mode 01 Async - mode 10 not used 11 not used NOTE: Sync mode can only be used with PWM INT = 0. |
| 2 | PWM INT/EXT | 1 | R/W | 0 PWM generator uses external H and Vsync clock 1 PWM generator uses internal 500kHz clock. |
| 3 | VSYNC_INVERT | 0 | R/W | 0 VSYNC active high (PWM triggers on rising edge) 1 VSYNC active low (PWM triggers on falling edge) |
| 4 | PWMINVERT | 0 | R/W | 0 PWM normal (PWM starts with “1” after delay) 1 PWM inverted(PWM starts with “0” after delay) |

Note: If Vsync or Hsync is not used, connect it to GND.

7.3.1 SYNC mode (PWM_MODE = 00)

In this mode the PWM is synchronized with VSYNC and HSYNC.

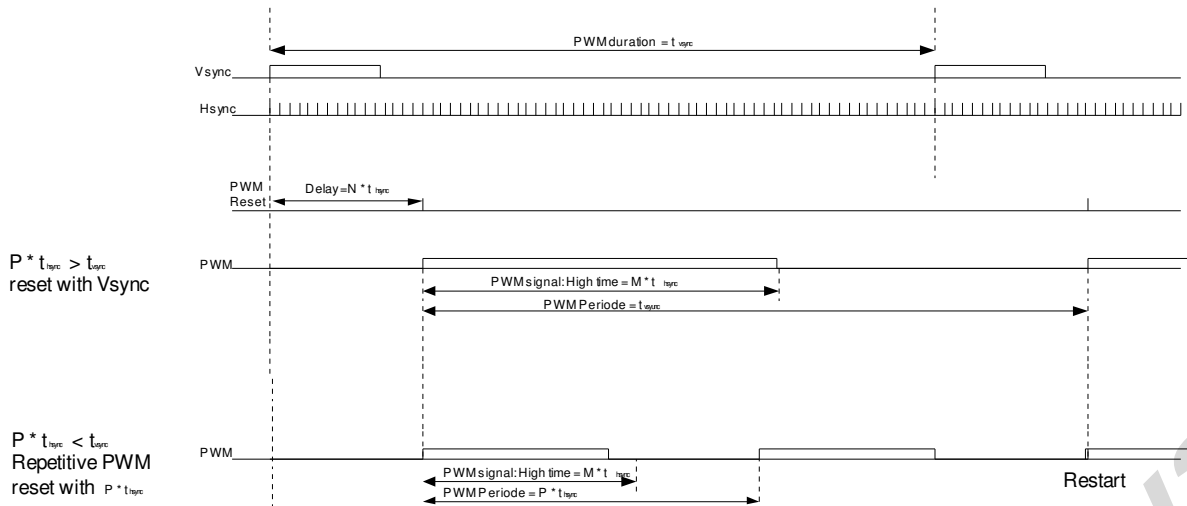


Setup options:

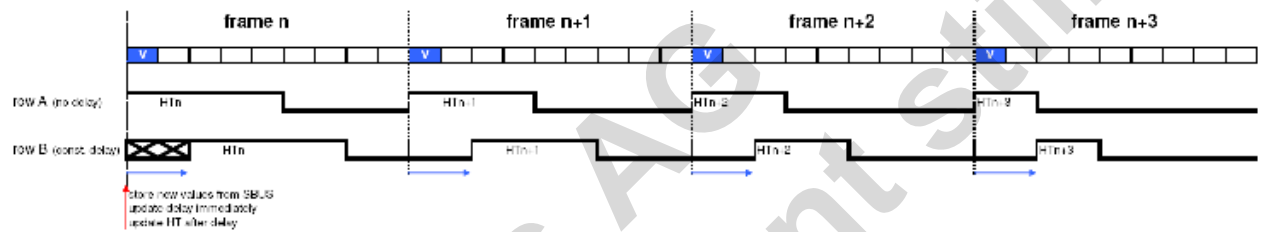
Delay (N) = registers 0h32 to 0h51

High Time (M) = registers 0h12 to 0h31

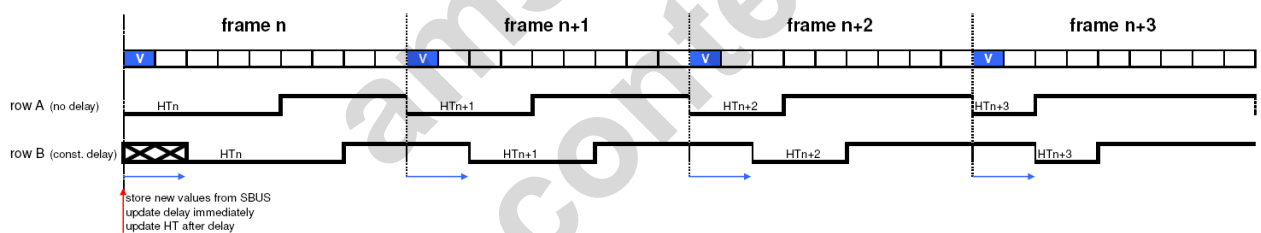
PWM Period (P) = register 0h10



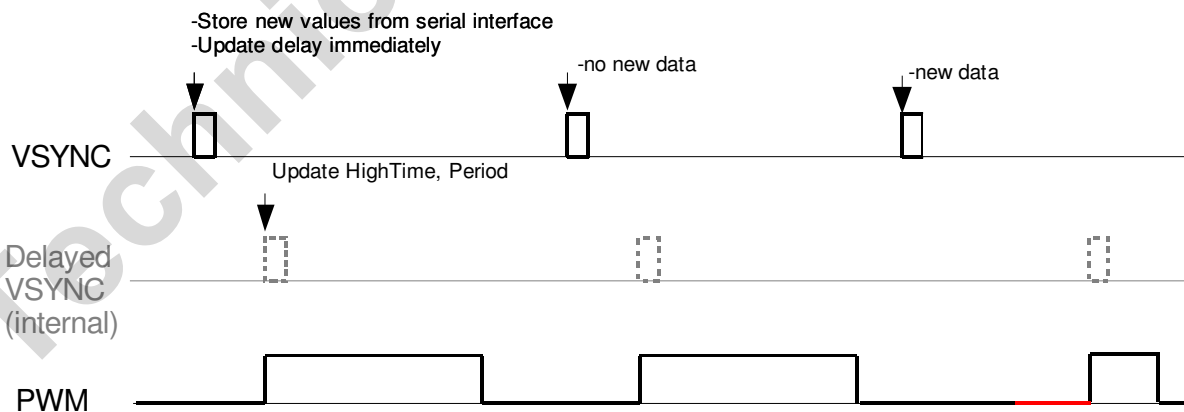
Example: Two PWM output channels with fixed delays and variable high times (HT)
PWMINVERT = 0

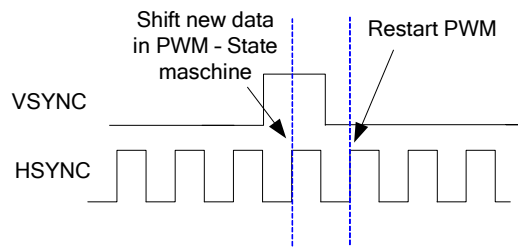


PWMINVERT = 1



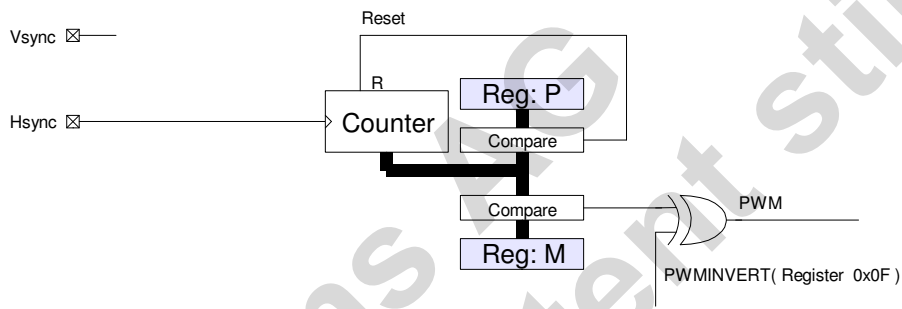
7.3.1.1 SYNC – mode PWM – generator update cycle.





7.3.2 ASYNC – mode (PWM_MODE = 01)

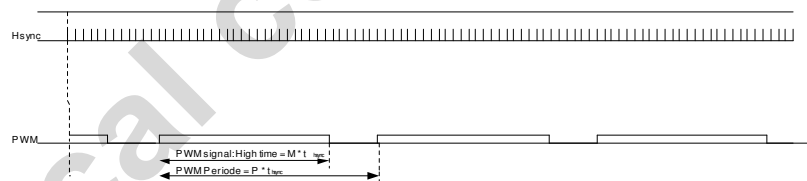
This PWM is synchronized with Hsync or internal 500KHz clock. The registers are updated with each serial data.



High time (M) = registers 0h12 to 0h 31
 PWM period (P) = register 0h10

AsyncMode

Repetitive PWM
 no Reset
 Synchronized on Hsync or internal Clock



7.4 PWM – high time, period and delay registers

Table 15 – Curreg1-16_DELAY_LSB

| Addr: 32h – 50h | | CURREGX_DELAY_LSB | | |
|-----------------|-------------------|--------------------------------------|--------|-----------------------------------|
| | | Defines delay of the different PWM's | | |
| Bit | Bit Name | Default | Access | Description |
| 7:0 | CurregX_DELAY_LSB | 00000000 | R/W | Defines the delay time of the PWM |

Table 16 – Curreg1-16_DELAY_MSB

| Addr: 32h-51h | | CURREGX_DELAY_LSB | | |
|---------------|-------------------|--------------------------------------|--------|-----------------------------------|
| | | Defines delay of the different PWM's | | |
| Bit | Bit Name | Default | Access | Description |
| 3:0 | CurregX_DELAY_MSB | 0000 | R/W | Defines the delay time of the PWM |

Table 17– PWM_PERIOD_LSB

| Addr: 10h | | PWM – Period – LSB | | |
|-----------|----------------|-----------------------|--------|-------------------------------|
| | | Defines PWM – Periode | | |
| Bit | Bit Name | Default | Access | Description |
| 7:0 | PWM_PERIOD_LSB | 11111111 | R/W | Defines the period of the PWM |

Table 18– PWM_PERIOD_MSB

| Addr: 11h | | PWM – Period – MSB | | |
|-----------|----------------|-----------------------|--------|-------------------------------|
| | | Defines PWM – Periode | | |
| Bit | Bit Name | Default | Access | Description |
| 3:0 | PWM_PERIOD_MSB | 0000 | R/W | Defines the period of the PWM |

Table 19– Curreg1-16_HT_LSB

| Addr: 12h-30h | | CURREGX_HT_LSB | | |
|---------------|----------------|--------------------------|--------|-----------------------|
| | | Defines High Time of PWM | | |
| Bit | Bit Name | Default | Access | Description |
| 7:0 | Curreg1_HT_LSB | 0 | R/W | Defines PWM high time |

Table 20– Curreg1-16_HT_MSB

| Addr: 13h-31h | | CURREGX_HT_MSB | | |
|---------------|----------------|--------------------------|--------|-----------------------|
| | | Defines High Time of PWM | | |
| Bit | Bit Name | Default | Access | Description |
| 3:0 | Curreg1_HT_MSB | 0000 | R/W | Defines PWM high time |

7.5 Shunt Regulator

The supply of the AS3693B is generated from the high voltage supply. To obtain a 5V regulated supply, a series resistor R_{vdd} is used together with an internal zener diode (ZD1). An external capacitor C_{vdd} is used to filter the supply on the pin VREG.

The external resistor R_{vdd} has to be chosen according to the following formula:

$$R_{vdd} = \frac{VDD_{MIN} - 5,4V}{20mA}$$

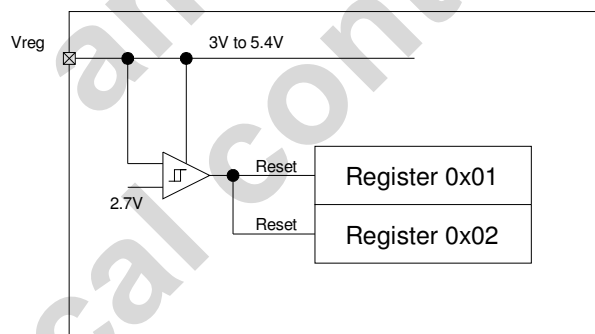
VDD_{MIN} is the minimum voltage of the supply, where R_{vdd} is connected

This ensures enough supply current ($I_{VREGMAX}$) for the AS3693B under minimum supply voltage VDD_{MIN} .

If a stable 5V supply within the operating conditions limits of V_{REGEXT} is already existing in the system it is possible to supply the AS3693B directly. In this case remove the resistor R_{vdd} and connected this supply directly to VREG.

7.5.1 Undervoltage lockout

The undervoltage lockout is an additional safety feature to prevent LED-current under abnormal Vreg conditions. If the supply voltage Vreg is below 2.7V (e.g. device is supplied only by the voltage of the serial interface) the registers Reg.Control1 and RegControl2 (0x01 and 0x02) are reset. This turns off all current sinks.



7.6 Over temperature control

Table 14– Overtemp Control

| Addr:55h | | Over temperature Control | | |
|----------|-------------|------------------------------------|--------|--|
| | | Controls the temperature functions | | |
| Bit | Bit Name | Default | Access | Description |
| 0 | overtemp_on | 1 | R/W | Enables the over temperature protection 0 = Protection off 1 = Protection on |
| 1 | ov_temp | 0 | R/W | Displays temperature status 0 = Normal operation 1 = Over temperature shutdown |

7.7 Device address setup

The I2C and SPI – Device address can be set via PIN ADDR1 and ADDR2. The AS3693B offers 31 I2C or 32 SPI addresses, which can be set via external resistor. ADDR2 bit 2 decides if I2C or SPI interface is used.

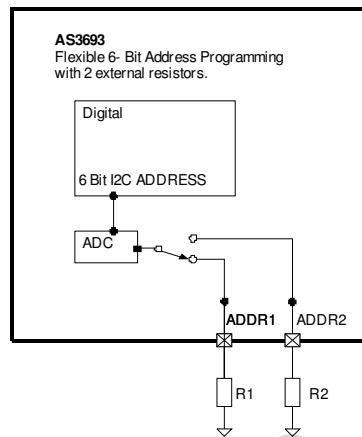


Table 13– Device Address

| Device Address Setup: | | I2C ADDRESS | | |
|-----------------------|--------------|---------------------|--------|--|
| | | I2C ADDRESS Options | | |
| Bit | Bit Name | Default | Access | Description |
| 2:0 | Device ADDR1 | 000 | R | Lower 3 bits of device address 000 open Note: don't use address 00h 001 320kΩ 010 160kΩ 011 80kΩ 100 40kΩ 101 20kΩ 110 10kΩ 111 0Ω |
| 5:3 | Device ADDR2 | 000 | R | Upper 3 bits of device address 000 open Note: activates I2C - mode 001 320kΩ Note: activates I2C - mode 010 160kΩ Note: activates I2C - mode 011 80kΩ Note: activates I2C - mode 100 40kΩ Note: activates SPI - mode 101 20kΩ Note: activates SPI - mode 110 10kΩ Note: activates SPI - mode 111 0Ω Note: activates SPI - mode |

7.7.1 I2C Device Address setup

| BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|-------|--------------|----------|----------|----------|----------|----------|-------|
| 0 | 0 (ADDR2<2>) | ADDR2<1> | ADDR2<0> | ADDR1<2> | ADDR1<1> | ADDR1<0> | R/W |

7.7.2 SPI Device Address setup

| BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|-------|-------|--------------|----------|----------|----------|----------|----------|
| 0 | 0 | 1 (ADDR2<2>) | ADDR2<1> | ADDR2<0> | ADDR1<2> | ADDR1<1> | ADDR1<0> |

7.8 Digital interface

The AS3693B can be controlled with two types of interfaces.

7.8.1 I2C interface

7.8.1.1 Feature List

- Fast-mode capability (max. SCL-frequency is 400 kHz)
- Write formats: Single-Byte-Write, Page-Write
- Read formats: Current-Address-Read, Random-Read, Sequential-Read
- SDA input delay and SCL spike filtering by integrated RC-components

7.8.1.2 Transfer Formats

Figure 1 – I²C Byte-Write:

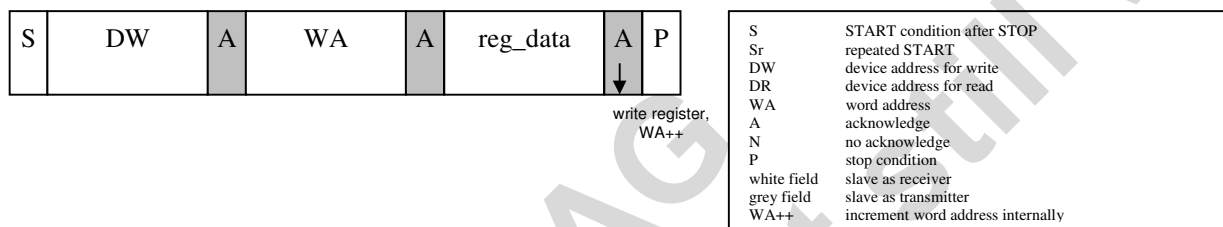
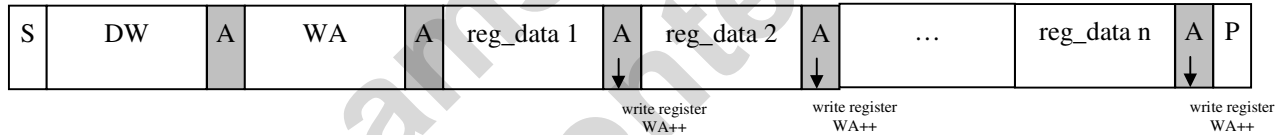


Figure 2 – I²C Page-Write:



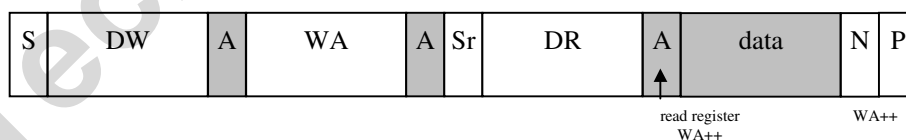
Byte-Write and Page-Write are used to write data to the slave.

The transmission begins with the START condition, which is generated by the master when the bus is in IDLE state (the bus is free). The device-write address is followed by the word address. After the word address any number of data bytes can be send to the slave. The word address is incremented internally, in order to write subsequent data bytes on subsequent address locations.

For reading data from the slave device, the master has to change the transfer direction. This can be done either with a repeated START condition followed by the device-read address, or simply with a new transmission START followed by the device-read address, when the bus is in IDLE state. The device-read address is always followed by the 1st register byte transmitted from the slave. In Read-Mode any number of subsequent register bytes can be read from the slave. The word address is incremented internally.

The diagrams below show various read formats available:

Figure 3 – I²C Random-Read:

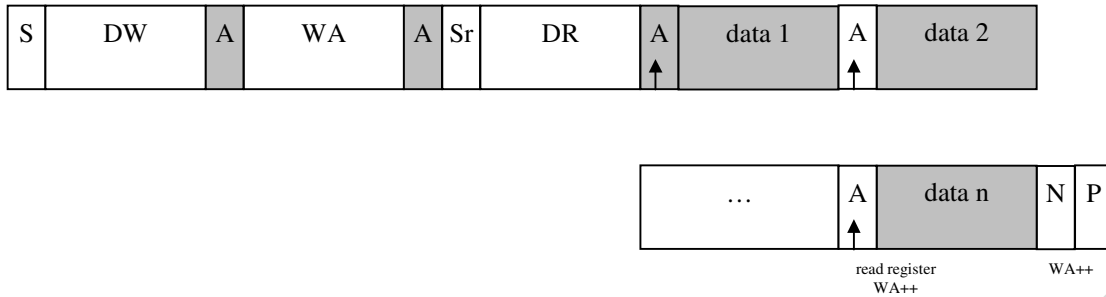


Random-Read and Sequential-Read are combined formats. The repeated START condition is used to change the direction after the data transfer from the master.

The word address transfer is initiated with a START condition issued by the master while the bus is idle. The START condition is followed by the device-write address and the word address.

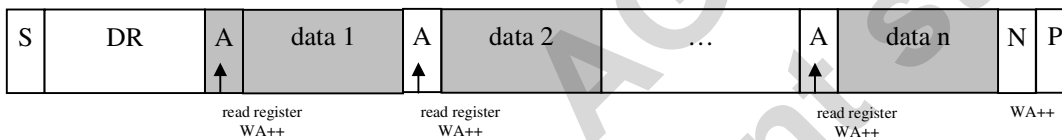
In order to change the data direction a repeated START condition is issued on the 1st SCL pulse after the acknowledge bit of the word address transfer. After the reception of the device-read address, the slave becomes the transmitter. In this state the slave transmits register data located by the previous received word address vector. The master responds to the data byte with a not-acknowledge, and issues a STOP condition on the bus.

Figure 4 – I²C Sequential-Read:



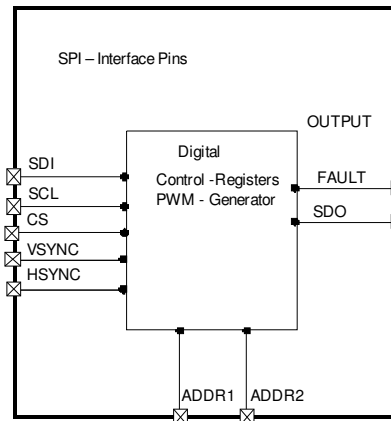
Sequential-Read is the extended form of Random-Read, as more than one register-data bytes are transferred subsequently. In difference to the Random-Read, for a sequential read the transferred register-data bytes are responded by an acknowledge from the master. The number of data bytes transferred in one sequence is unlimited (consider the behavior of the word-address counter). To terminate the transmission the master has to send a not-acknowledge following the last data byte and generate the STOP condition subsequently.

Figure 5 – I²C Current-Address-Read:



To keep the access time as small as possible, this format allows a read access without the word address transfer in advance to the data transfer. The bus is idle and the master issues a START condition followed by the Device-Read address. Analogous to Random-Read, a single byte transfer is terminated with a not-acknowledge after the 1st register byte. Analogous to Sequential-Read an unlimited number of data bytes can be transferred, where the data bytes has to be responded with an acknowledge from the master. For termination of the transmission the master sends a not-acknowledge following the last data byte and a subsequent STOP condition.

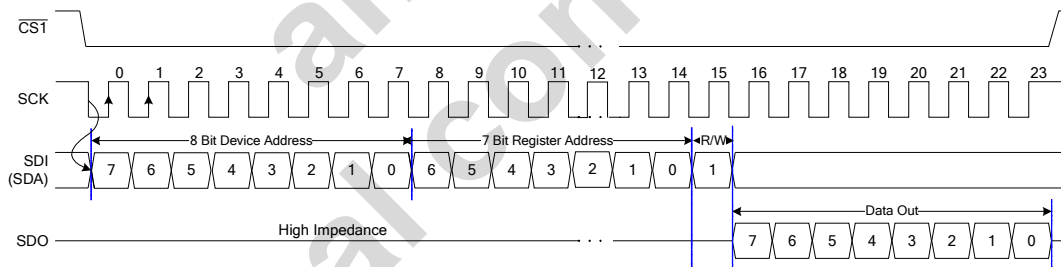
7.8.2 SPI interface



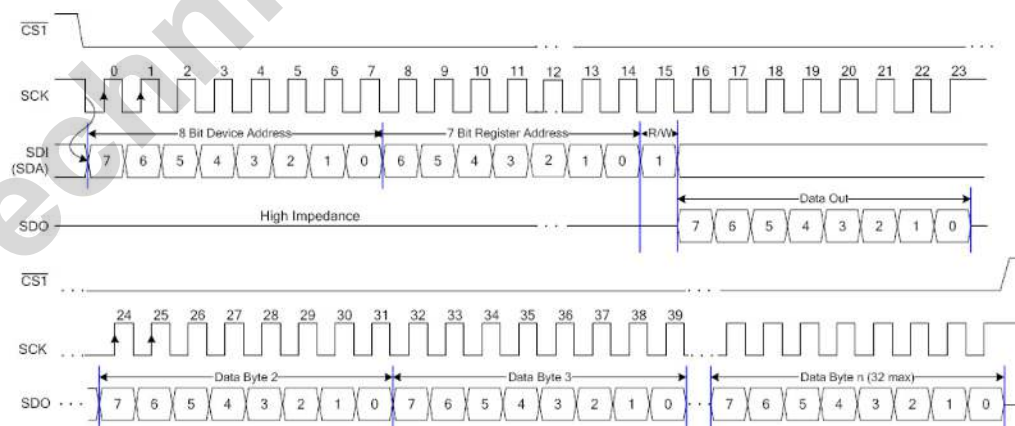
SPI Mode – Digital Interface Pins:

| | |
|-------|--|
| CS(N) | Chip Select input |
| SDO | Serial Data output |
| SDI | Serial Data input |
| SCL | Serial Clock input |
| VSYNC | Video Sync signal input |
| HSYNC | Video Sync signal input |
| ADDR1 | Device Address pins (can be set via resistor). |
| ADDR2 | |

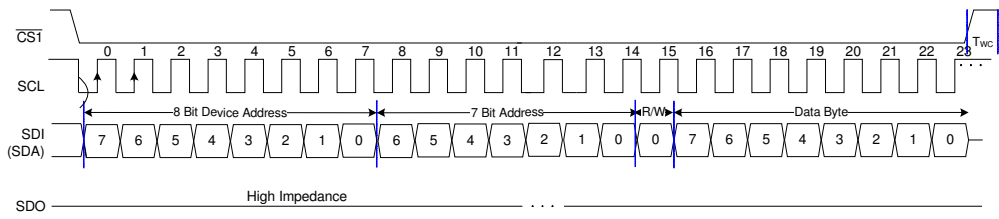
7.8.2.1 Read Sequence



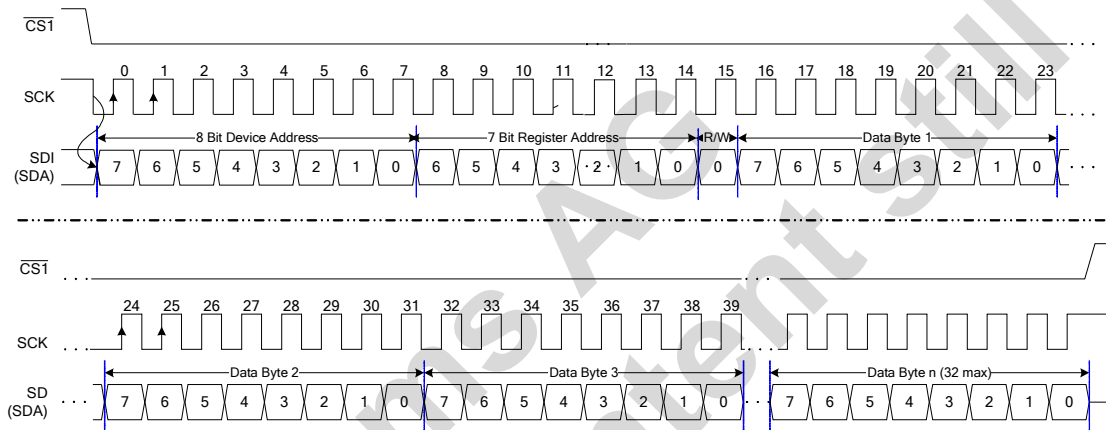
7.8.2.2 Page Read Sequence



7.8.2.3 Write Sequence



7.8.2.4 Page Write Sequence



8 Register map

| Name | Addr | Default | B7 | b6 | b5 | B4 | b3 | b2 | b1 | b0 |
|-------------------|------|---------|----------------------------|----------------------|--------------------------|-------------|--------------------|-----------------|-----------------|-------------|
| Reg. Control1 | 01h | 00h | Curreg8_ON | Curreg7_ON | Curreg6_ON | Curreg5_ON | Curreg4_ON | Curreg3_ON | Curreg2_ON | Curreg1_ON |
| Reg Control 2 | 02h | 00h | Curreg16_ON | Curreg15_ON | Curreg14_ON | Curreg13_ON | Curreg12_ON | Curreg11_ON | Curreg10_ON | Curreg9_ON |
| Feedback Control | 04h | 01h | DCDC_REGULATION_TRIP_POINT | | Short_Led Detect Voltage | | SHORT_DET_ON | OPEN_LED_DET_ON | Feedback_on_PWM | FEEDBACK_ON |
| Feedback Select 1 | 05h | 94h | FB4_Select | | FB3_Select | | FB2_Select | | FB1_Select | |
| Feedback Select 2 | 06h | 94h | FB8_Select | | FB7_Select | | FB6_Select | | FB5_Select | |
| Feedback Select 3 | 07h | 94h | FB12_Select | | FB11_Select | | FB10_Select | | FB9_Select | |
| Feedback Select 4 | 08h | 94h | FB16_Select | | FB15_Select | | FB14_Select | | FB13_Select | |
| Voltage_Fault 1 | 09h | 00h | Fault_Reg4 | | Fault_Reg3 | | Fault_Reg2 | | Fault_Reg1 | |
| Voltage_Fault 2 | 0Ah | 00h | Fault_Reg8 | | Fault_Reg7 | | Fault_Reg6 | | Fault_Reg5 | |
| Voltage_Fault 3 | 0Bh | 00h | Fault_Reg12 | | Fault_Reg11 | | Fault_Reg10 | | Fault_Reg9 | |
| Voltage_Fault 4 | 0Ch | 00h | Fault_Reg16 | | Fault_Reg15 | | Fault_Reg14 | | Fault_Reg13 | |
| CURREG_CONTROL | 0Dh | 00h | boost mode | switch_output_driver | PWM_LOW_LEVEL | | RC_SEL | | Select Ref | |
| Ref_DAC_Voltage | 0Eh | 00h | Vref_DAC | | | | | | | |
| PWM_CONTROL | 0Fh | 04h | | | | PWM_INVERT | VSYNC_INVERT | PWM-INT/EXT | PWM - MODE | |
| PWM-PERIOD_LSB | 10h | FFh | PWM -PERIOD - LSB | | | | | | | |
| PWM-PERIOD-MSB | 11h | 00h | | | | | PWM - period - MSB | | | |
| Curreg1_HT_LSB | 12h | 00h | Curreg1_HT_LSB | | | | | | | |
| Curreg1_HT_MSB | 13h | 00h | | | | | Curreg1_HT_MSB | | | |
| Curreg2_HT_LSB | 14h | 00h | Curreg2_HT_LSB | | | | | | | |
| Curreg2_HT_MSB | 15h | 00h | | | | | Curreg2_HT_MSB | | | |
| Curreg3_HT_LSB | 16h | 00h | Curreg3_HT_LSB | | | | | | | |
| Curreg3_HT_MSB | 17h | 00h | | | | | Curreg3_HT_MSB | | | |
| Curreg4_HT_LSB | 18h | 00h | Curreg4_HT_LSB | | | | | | | |
| Curreg4_HT_MSB | 19h | 00h | | | | | Curreg4_HT_MSB | | | |
| Curreg5_HT_LSB | 1Ah | 00h | Curreg5_HT_LSB | | | | | | | |
| Curreg5_HT_MSB | 1Bh | 00h | | | | | Curreg5_HT_MSB | | | |
| Curreg6_HT_LSB | 1Ch | 00h | Curreg6_HT_LSB | | | | | | | |
| Curreg6_HT_MSB | 1Dh | 00h | | | | | Curreg6_HT_MSB | | | |
| Curreg7_HT_LSB | 1Eh | 00h | Curreg7_HT_LSB | | | | | | | |
| Curreg7_HT_MSB | 1Fh | 00h | | | | | Curreg7_HT_MSB | | | |
| Curreg8_HT_LSB | 20h | 00h | Curreg8_HT_LSB | | | | | | | |

| Name | Addr | Default | B7 | b6 | b5 | B4 | b3 | b2 | b1 | b0 |
|-------------------|------|---------|-------------------|----|----|----|-------------------|----|----|----|
| Curreg8_HT_MSB | 21h | 00h | | | | | Curreg8_HT_MSB | | | |
| Curreg9_HT_LSB | 22h | 00h | Curreg9_HT_LSB | | | | | | | |
| Curreg9_HT_MSB | 23h | 00h | | | | | Curreg9_HT_MSB | | | |
| Curreg10_HT_LSB | 24h | 00h | Curreg10_HT_LSB | | | | | | | |
| Curreg10_HT_MSB | 25h | 00h | | | | | Curreg10_HT_MSB | | | |
| Curreg11_HT_LSB | 26h | 00h | Curreg11_HT_LSB | | | | | | | |
| Curreg11_HT_MSB | 27h | 00h | | | | | Curreg11_HT_MSB | | | |
| Curreg12_HT_LSB | 28h | 00h | Curreg12_HT_LSB | | | | | | | |
| Curreg12_HT_MSB | 29h | 00h | | | | | Curreg12_HT_MSB | | | |
| Curreg13_HT_LSB | 2Ah | 00h | Curreg13_HT_LSB | | | | | | | |
| Curreg13_HT_MSB | 2Bh | 00h | | | | | Curreg13_HT_MSB | | | |
| Curreg14_HT_LSB | 2Ch | 00h | Curreg14_HT_LSB | | | | | | | |
| Curreg14_HT_MSB | 2Dh | 00h | | | | | Curreg14_HT_MSB | | | |
| Curreg15_HT_LSB | 2Eh | 00h | Curreg15_HT_LSB | | | | | | | |
| Curreg15_HT_MSB | 2Fh | 00h | | | | | Curreg15_HT_MSB | | | |
| Curreg16_HT_LSB | 30h | 00h | Curreg16_HT_LSB | | | | | | | |
| Curreg16_HT_MSB | 31h | 00h | | | | | Curreg16_HT_MSB | | | |
| Curreg1_DELAY_LSB | 32h | 00h | Curreg1_DELAY_LSB | | | | | | | |
| Curreg1_DELAY_MSB | 33h | 00h | | | | | Curreg1_DELAY_MSB | | | |
| Curreg2_DELAY_LSB | 34h | 00h | Curreg2_DELAY_LSB | | | | | | | |
| Curreg2_DELAY_MSB | 35h | 00h | | | | | Curreg2_DELAY_MSB | | | |
| Curreg3_DELAY_LSB | 36h | 00h | Curreg3_DELAY_LSB | | | | | | | |
| Curreg3_DELAY_MSB | 37h | 00h | | | | | Curreg3_DELAY_MSB | | | |
| Curreg4_DELAY_LSB | 38h | 00h | Curreg4_DELAY_LSB | | | | | | | |
| Curreg4_DELAY_MSB | 39h | 00h | | | | | Curreg4_DELAY_MSB | | | |
| Curreg5_DELAY_LSB | 3Ah | 00h | Curreg5_DELAY_LSB | | | | | | | |
| Curreg5_DELAY_MSB | 3Bh | 00h | | | | | Curreg5_DELAY_MSB | | | |
| Curreg6_DELAY_LSB | 3Ch | 00h | Curreg6_DELAY_LSB | | | | | | | |
| Curreg6_DELAY_MSB | 3Dh | 00h | | | | | Curreg6_DELAY_MSB | | | |
| Curreg7_DELAY_LSB | 3Eh | 00h | Curreg7_DELAY_LSB | | | | | | | |
| Curreg7_DELAY_MSB | 3Fh | 00h | | | | | Curreg7_DELAY_MSB | | | |
| Curreg8_DELAY_LSB | 40h | 00h | Curreg8_DELAY_LSB | | | | | | | |

| Name | Addr | Default | B7 | b6 | b5 | B4 | b3 | b2 | b1 | b0 |
|--------------------|------|---------|--------------------|----|----|----|--------------------|----|---------|------------|
| Curreg8_DELAY_MSB | 41h | 00h | | | | | Curreg8_DELAY_MSB | | | |
| Curreg9_DELAY_LSB | 42h | 00h | Curreg9_DELAY_LSB | | | | | | | |
| Curreg9_DELAY_MSB | 43h | 00h | | | | | Curreg9_DELAY_MSB | | | |
| Curreg10_DELAY_LSB | 44h | 00h | Curreg10_DELAY_LSB | | | | | | | |
| Curreg10_DELAY_MSB | 45h | 00h | | | | | Curreg10_DELAY_MSB | | | |
| Curreg11_DELAY_LSB | 46h | 00h | Curreg11_DELAY_LSB | | | | | | | |
| Curreg11_DELAY_MSB | 47h | 00h | | | | | Curreg11_DELAY_MSB | | | |
| Curreg12_DELAY_LSB | 48h | 00h | Curreg12_DELAY_LSB | | | | | | | |
| Curreg12_DELAY_MSB | 49h | 00h | | | | | Curreg12_DELAY_MSB | | | |
| Curreg13_DELAY_LSB | 4Ah | 00h | Curreg13_DELAY_LSB | | | | | | | |
| Curreg13_DELAY_MSB | 4Bh | 00h | | | | | Curreg13_DELAY_MSB | | | |
| Curreg14_DELAY_LSB | 4Ch | 00h | Curreg14_DELAY_LSB | | | | | | | |
| Curreg14_DELAY_MSB | 4Dh | 00h | | | | | Curreg14_DELAY_MSB | | | |
| Curreg15_DELAY_LSB | 4Eh | 00h | Curreg15_DELAY_LSB | | | | | | | |
| Curreg15_DELAY_MSB | 4Fh | 00h | | | | | Curreg15_DELAY_MSB | | | |
| Curreg16_DELAY_LSB | 50h | 00h | Curreg16_DELAY_LSB | | | | | | | |
| Curreg16_DELAY_MSB | 51h | 00h | | | | | Curreg16_DELAY_LSB | | | |
| Overtemp control | 55h | 01h | | | | | | | ov_temp | ov_temp_on |
| ASIC ID1 | 5Ch | CAh | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0 |
| ASIC ID2 | 5Dh | 5Xh | 0 | 1 | 0 | 1 | REVISION | | | |

Revision code:
0x8... initial version November 2008

9 Pinout and Packaging

9.1 Pinout

Table 5 – Pinlist

| Pin | Name | Type | Description |
|-----|-------------|------|--|
| 1 | GATE16 | AIO | Connect to Gate of External Transistor |
| 2 | RFB1 | AIO | Connect to Source of External Transistor and to Resistor RSET |
| 3 | GATE1 | AIO | Connect to Gate of External Transistor |
| 4 | CURR_sense1 | AIO | Connect to Drain of external Transistor (input for Open and Short led detection) |
| 5 | FBG | AIO | Automatic supply regulation for GREEN led strings; if not used, leave open |
| 6 | FBB | AIO | Automatic supply regulation for BLUE led strings; if not used, leave open |
| 7 | REF(EXT) | AI | Reference pin for PWM = 1 voltage, if not used leave open |
| 8 | GND(SENSE) | AIO | GND supply connection (sense) |
| 9 | VREG | AIO | Shunt regulator supply; connect to Rvdd and Cvdd |
| 10 | V2_5 | AIO | Digital supply, connect 1uF blocking capacitor |
| 11 | ADDR2 | AIO | Connect to external resistor for serial interface address selection, |
| 12 | ADDR1 | AIO | Connect to external resistor for serial interface address selection. |
| 13 | CURR_sense2 | AIO | Connect to Drain of external Transistor (input for Open and Short led detection) |
| 14 | GATE2 | AIO | Connect to Gate of External Transistor |
| 15 | RFB2 | AIO | Connect to Source of External Transistor and to Resistor RSET |
| 16 | GATE3 | AIO | Connect to Gate of External Transistor |
| 17 | RFB3 | AIO | Connect to Source of External Transistor and to Resistor RSET |
| 18 | CURR_sense3 | AIO | Connect to Drain of external Transistor (input for Open and Short led detection) |
| 19 | GATE4 | AIO | Connect to Gate of External Transistor |
| 20 | RFB4 | AIO | Connect to Source of External Transistor and to Resistor RSET |
| 21 | CURR_sense4 | AIO | Connect to Drain of external Transistor (input for Open and Short led detection) |
| 22 | GATE5 | AIO | Connect to Gate of External Transistor |
| 23 | RFB5 | AIO | Connect to Source of External Transistor and to Resistor RSET |
| 24 | CURR_sense5 | AIO | Connect to Drain of external Transistor (input for Open and Short led detection) |
| 25 | CURR_sense6 | AIO | Connect to Drain of external Transistor (input for Open and Short led detection) |
| 26 | RFB6 | AIO | Connect to Source of External Transistor and to Resistor RSET |
| 27 | GATE6 | AIO | Connect to Gate of External Transistor |
| 28 | CURR_sense7 | AIO | Connect to Drain of external Transistor (input for Open and Short led detection) |
| 29 | RFB7 | AIO | Connect to Source of External Transistor and to Resistor RSET |
| 30 | GATE7 | AIO | Connect to Gate of External Transistor |
| 31 | CURR_sense8 | AIO | Connect to Drain of external Transistor (input for Open and Short led detection) |
| 32 | RFB8 | AIO | Connect to Source of External Transistor and to Resistor RSET |
| 33 | GATE8 | AIO | Connect to Gate of External Transistor |
| 34 | RFB9 | AIO | Connect to Source of External Transistor and to Resistor RSET |
| 35 | GATE9 | AIO | Connect to Gate of External Transistor |

Table 5 – Pinlist

| Pin | Name | Type | Description |
|------------|--------------|------|--|
| 36 | CURR_sense9 | AIO | Connect to Drain of external Transistor (input for Open and Short led detection) |
| 37 | FBR | AIO | Automatic supply regulation for RED led strings; if not used, leave open |
| 38 | VSYNC | DI | Video sync signal , NOTE: Connect to GND in ASYNC MODE |
| 39 | HSYNC | DI | Video sync signal or external clock input in ASYNC mode |
| 40 | CS | DI | SPI : CS – function, I2C: connect to GND |
| 41 | SCL | DI | SPI/ I2C: Serial interface clock input. |
| 42 | SDA | DI | SPI/ I2C: Serial interface data I/O. |
| 43 | SDO | DO | SPI: digital data output, I2C: leave open |
| 44 | FAULT | DO | FAULT PIN, open drain output. Connect pull up resistor to V2_5 |
| 45 | CURR_sense10 | AIO | Connect to Drain of external Transistor (input for Open and Short led detection) |
| 46 | GATE10 | AIO | Connect to Gate of External Transistor |
| 47 | RFB10 | AIO | Connect to Source of External Transistor and to Resistor RSET |
| 48 | GATE11 | AIO | Connect to Gate of External Transistor |
| 49 | RFB11 | AIO | Connect to Source of External Transistor and to Resistor RSET |
| 50 | CURR_sense11 | AIO | Connect to Drain of external Transistor (input for Open and Short led detection) |
| 51 | GATE12 | AIO | Connect to Gate of External Transistor |
| 52 | RFB12 | AIO | Connect to Source of External Transistor and to Resistor RSET |
| 53 | CURR_sense12 | AIO | Connect to Drain of external Transistor (input for Open and Short led detection) |
| 54 | GATE13 | AIO | Connect to Gate of External Transistor |
| 55 | RFB13 | AIO | Connect to Source of External Transistor and to Resistor RSET |
| 56 | CURR_sense13 | AIO | Connect to Drain of external Transistor (input for Open and Short led detection) |
| 57 | CURR_sense14 | AIO | Connect to Drain of external Transistor (input for Open and Short led detection) |
| 58 | RFB14 | AIO | Connect to Source of External Transistor and to Resistor RSET |
| 59 | GATE14 | AIO | Connect to Gate of External Transistor |
| 60 | CURR_sense15 | AIO | Connect to Drain of external Transistor (input for Open and Short led detection) |
| 61 | RFB15 | AIO | Connect to Source of External Transistor and to Resistor RSET |
| 62 | GATE15 | AIO | Connect to Gate of External Transistor |
| 63 | CURR_sense16 | AIO | Connect to Drain of external Transistor (input for Open and Short led detection) |
| 64 | RFB16 | AIO | Connect to Source of External Transistor and to Resistor RSET |
| 65 (EP) | GND | S | VSS Supply connection; add as many vias to ground plane as possible. |

AIO...Analog pin

DI...Digital input. Protected with clamp to 2.5V

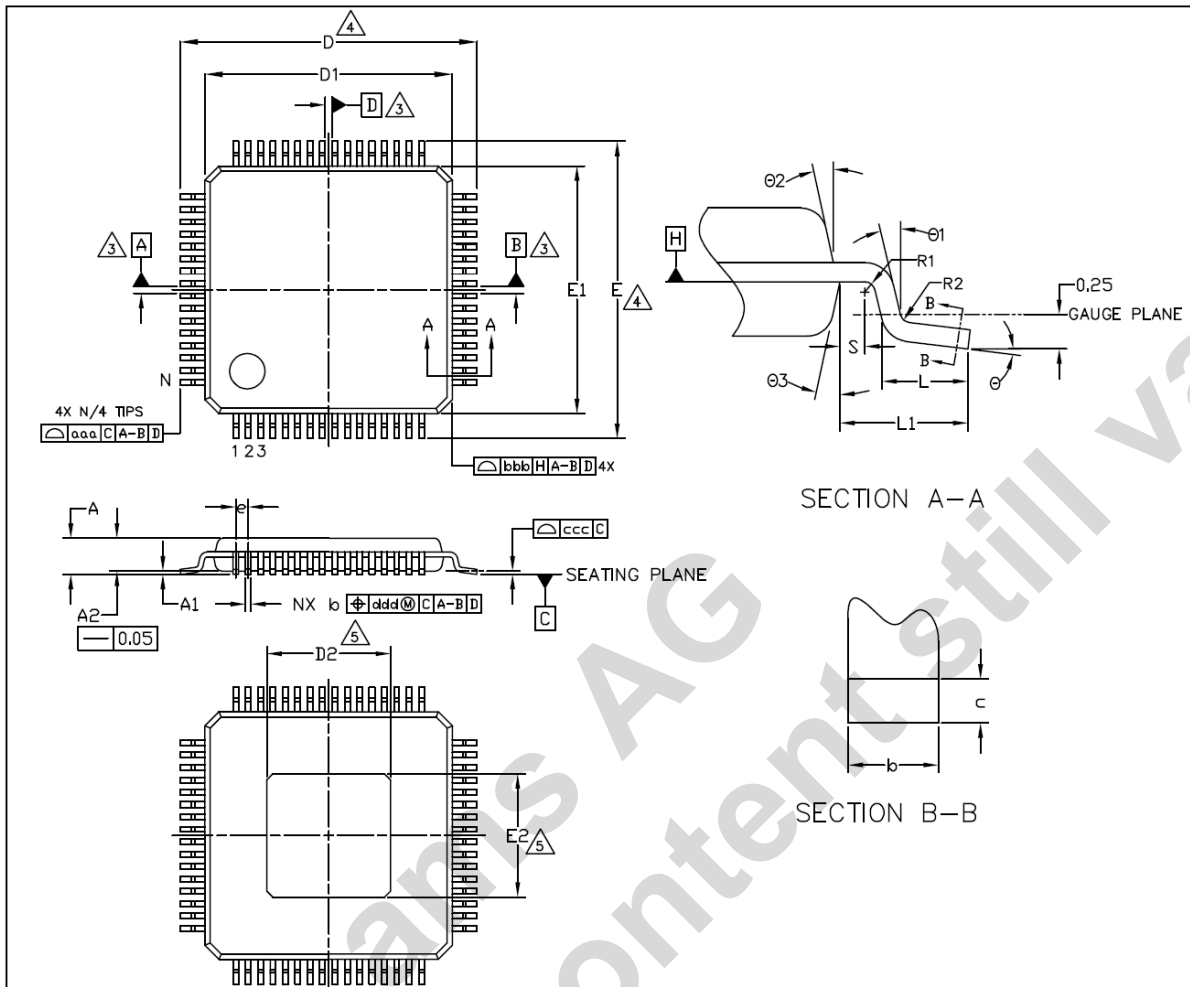
DO...Digital output. Protected with clamp to 2.5V

S... VSS supply

Note: Connect any unused output channel as follows:

- GATE_x = open, RFB_x = CURR_sense_X = GND

9.2 Package drawing epTQFP64



| REF. | MIN | NOM | MAX |
|------------|------|-----------|------|
| A | — | — | 1.20 |
| A1 | 0.05 | — | 0.15 |
| A2 | 0.95 | 1.00 | 1.05 |
| b | 0.17 | 0.22 | 0.27 |
| c | 0.09 | — | 0.20 |
| D | — | 12.00 BSC | — |
| D1 | — | 10.00 BSC | — |
| E | — | 12.00 BSC | — |
| E1 | — | 10.00 BSC | — |
| e | — | 0.50 BSC | — |
| L | 0.45 | 0.60 | 0.75 |
| L1 | — | 1.00 REF | — |
| R1 | 0.08 | — | — |
| R2 | 0.08 | — | 0.20 |
| S | 0.20 | — | — |
| θ | 0° | 3.5° | 7° |
| $\theta 1$ | 0° | — | — |
| $\theta 2$ | 11° | 12° | 13° |
| $\theta 3$ | 11° | 12° | 13° |
| aaa | — | 0.20 | — |
| bbb | — | 0.20 | — |
| ccc | — | 0.08 | — |
| ddd | — | 0.08 | — |
| N | — | 64 | — |

NOTE:

1. DIMENSIONS & TOLERANCEING CONFIRM TO ASME Y14.5M-1994.
 2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGELS ARE IN DEGREES.
- ⊲ 3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
- ⊲ 4. TO BE DETERMINED AT SEATING DATUM PLANE C.
- ⊲ 5. DIMENSION D2 AND E2 SHOW THE MINIMUM ALLOWED FOR THE OPTIONAL EXPOSED HEAT SLUG. THE MAXIMUM ALLOWED IS EQUAL TO THE PACKAGE BODY SIZE (D1 & E1). HOWEVER, THE SIZE OF THE EXPOSED HEAT SLUG IS VARIABLE DEPENDING ON DIE SIZE.

| | | | | |
|-------------------------------|------------|--------|-----------------------------|--------------------|
| | | | ASSEMBLY ENGINEERING | |
| <i>a leap ahead in analog</i> | | | TITLE | REFERENCE DOCUMENT |
| | | | ePTQFP 10x10x1.0mm, 64 LEAD | JEDEC MS - 026 |
| DRAWN | DATE | REV. | DRAWING NO. | LATEST REVISION |
| RH8 | 2011.09.28 | N/C | BBC | |
| CHECKED | DATE | | | UNIT |
| GBO | 2011.09.28 | | | |
| APPROVED | DATE | SHEET | DIMENSION AND TOLERANCE | SCALE |
| MKR | 2011.09.28 | 1 OF 1 | | NOT IN SCALE |

9.3 Package drawing QFN64

The drawing includes the following views and features:

- Top View:** Shows dimensions D (width), E (height), and PIN #1 I.D. (lead diameter). Datum A and B are indicated.
- Side View:** Shows dimensions L (lead length), L1 (lead full back), and e (terminal width). Datum A or B is shown.
- Detail B:** Shows the terminal tip with dimensions b (terminal width) and ddd (lead thickness).
- Bottom View:** Shows dimensions D2 (pitch), E2 (height), and NX L (lead length). Datum A and B are indicated. Pin numbers 1 through 64 are shown.
- Seating Plane:** Indicated by a triangle symbol.

| REF. | MIN | NOM | MAX |
|------|------|----------|------|
| A | 0.80 | 0.90 | 1.00 |
| A1 | 0 | 0.02 | 0.05 |
| A3 | - | 0.20 REF | - |
| L | 0.35 | 0.40 | 0.45 |
| L1 | 0 | - | 0.15 |
| b | 0.18 | 0.25 | 0.30 |
| D | - | 9.00 BSC | - |
| E | - | 9.00 BSC | - |
| e | - | 0.50 BSC | - |
| D2 | 5.90 | 6.00 | 6.10 |
| E2 | 5.90 | 6.00 | 6.10 |
| aaa | - | 0.15 | - |
| bbb | - | 0.10 | - |
| ccc | - | 0.10 | - |
| ddd | - | 0.05 | - |
| eee | - | 0.08 | - |
| fff | - | 0.10 | - |
| N | - | 64 | - |

NOTE:

- DIMENSIONS & TOLERANCEING CONFIRM TO ASME Y14.5M-1994.
- ALL DIMENSIONS ARE IN MILLIMETERS. ANGELS ARE IN DEGREES.
- DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25mm AND 0.30mm FROM TERMINAL TIP. DIMENSION L1 REPRESENTS TERMINAL FULL BACK FROM PACKAGE EDGE UP TO 0.15mm IS ACCEPTABLE.
- COPLANARITY APPLIES TO THE EXPOSED HEAT SLUG AS WELL AS THE TERMINAL.
- RADIUS ON TERMINAL IS OPTIONAL.
- N IS THE TOTAL NUMBER OF TERMINALS.

| | | | | |
|------------------------|--------------------|-----------------|--|---|
| | | | ASSEMBLY ENGINEERING | |
| a leap ahead in analog | | | TITLE SAWN QFN, PULL BACK, 9x9x0.9mm, 64 LEAD, 6.00mm SQ. ePAD | REFERENCE DOCUMENT JEDEC MO - 220 LATEST REVISION |
| DRAWN RH8 | DATE 2010.10.30 | REV. N/C | DRAWING NO. QXK | UNIT |
| CHECKED GBO | DATE 2010.10.30 | | DIMENSION AND TOLERANCE | SCALE NOT IN SCALE |
| APPROVED MKR | DATE 2010.10.30 | SHEET 1 OF 1 | | |

10 Ordering Information

Table 6 – Ordering Information

| Part Number | Marking | Package Type | Delivery Form | Description |
|--------------|---------|--------------|------------------------------|--|
| AS3693B-ZTQT | AS3693B | epTQFP64 | Tape and Reel in Dry Pack | Package size = 10x10mm, Exposed pad size = 4.5x4.5mm, Pitch = 0.5mm, Pb-free; |
| AS3693B-ZQFT | AS3693B | QFN64 | Tape and Reel in Dry Pack | Package size = 9x9mm, Pitch = 0.5mm, Pb-free; |
| AS3693B-ZMFT | AS3693B | MLF64 | Tape and Reel in Dry Pack | Package size = 9x9mm, Pitch = 0.5mm, Pb-free; |

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