To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

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HM628100I Series

Wide Temperature Range Version
8 M SRAM (1024-kword × 8-bit)

ADE-203-1302B (Z)
Rev. 1.0
Sep. 25, 2002

Description

The Hitachi HM628100I Series is 8-Mbit static RAM organized 1,048,576-word × 8-bit. HM628100I Series has realized higher density, higher performance and low power consumption by employing CMOS process technology (6-transistor memory cell). It offers low power standby power dissipation; therefore, it is suitable for battery backup systems. It is packaged in standard 44-pin TSOP II for high density surface mounting.

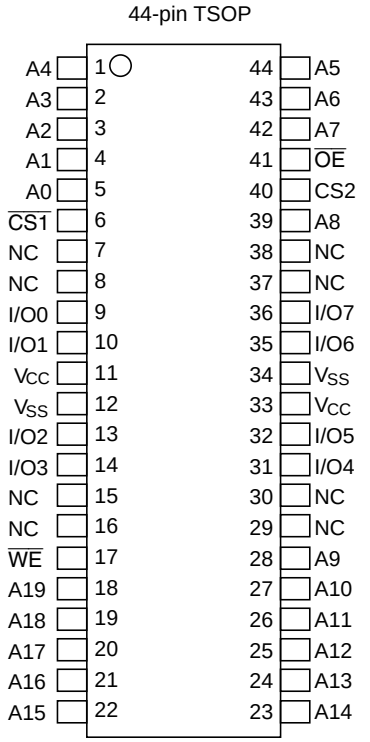
Features

- Single 5.0 V supply: 5.0 V ± 10 %
- Fast access time: 55 ns (max)
- Power dissipation:
  - Active: 10 mW/MHz (typ)
  - Standby: 7.5 µW (typ)
- Completely static memory.
  - No clock or timing strobe required
- Equal access and cycle times
- Common data input and output.
  - Three state output
- Battery backup operation.
  - 2 chip selection for battery backup
- Temperature range: –40 to +85°C

Ordering Information

Type No.	Access time	Package
HM628100LTTI-5SL	55 ns	400-mil 44pin plastic TSOP II (normal-bend type) (TTP-44DE)

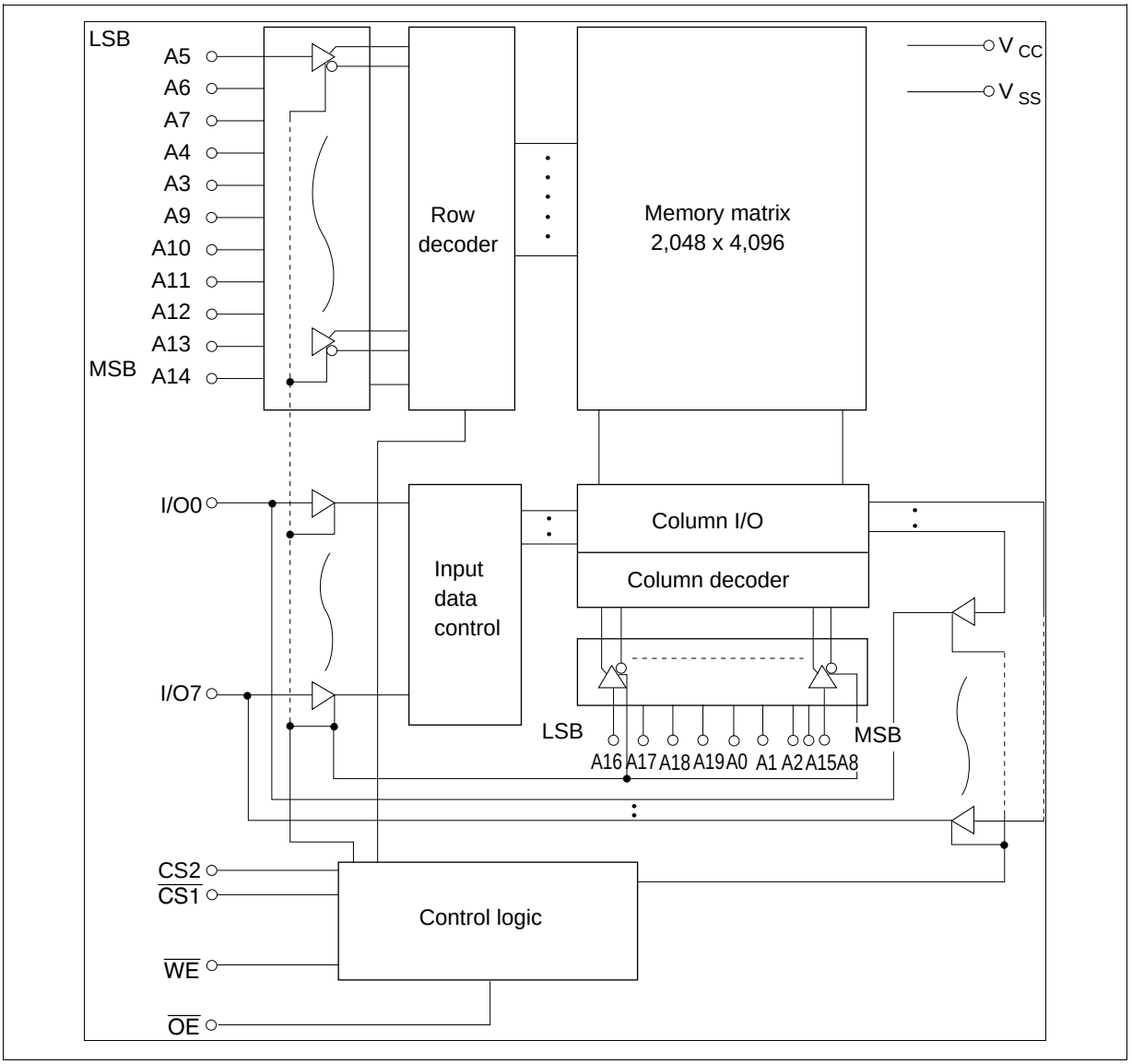
Pin Arrangement



Pin Description (TSOP)

Pin name	Function
A0 to A19	Address input
I/O0 to I/O7	Data input/output
$\overline{CS1}$	Chip select 1
CS2	Chip select 2
$\overline{WE}$	Write enable
$\overline{OE}$	Output enable
V_{CC}	Power supply
V_{SS}	Ground
NC	No connection

Block Diagram (TSOP)



Operation Table

$\overline{CS1}$	CS2	$\overline{WE}$	$\overline{OE}$	I/O0 to I/O7	Operation
H	×	×	×	High-Z	Standby
×	L	×	×	High-Z	Standby
L	H	H	L	Dout	Read
L	H	L	×	Din	Write
L	H	H	H	High-Z	Output disable

Note: H: V_{IH}, L: V_{IL}, ×: V_{IH} or V_{IL}

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Power supply voltage relative to V_{SS}	V_{CC}	–0.5 to + 7.0	V
Terminal voltage on any pin relative to V_{SS}	V_T	–0.5*[1] to V_{CC} + 0.3*[2]	V
Power dissipation	P_T	1.0	W
Storage temperature range	Tstg	–55 to +125	°C
Storage temperature range under bias	Tbias	–40 to +85	°C

Notes: 1. V_T min: –3.0 V for pulse half-width ≤ 30 ns.
2. Maximum voltage is +7.0 V.

DC Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{CC}	4.5	5.0	5.5	V	
	V_{SS}	0	0	0	V	
Input high voltage	V_{IH}	2.2	—	V_{CC} + 0.3	V	
Input low voltage	V_{IL}	–0.3	—	0.8	V	1
Ambient temperature range	Ta	–40	—	85	°C	

Note: 1. V_{IL} min: –3.0 V for pulse half-width ≤ 30 ns.

DC Characteristics

Parameter	Symbol	Min	Typ*[1]	Max	Unit	Test conditions
Input leakage current	$\|I_{LI}\|$	—	—	1	µA	Vin = V_{SS} to V_{CC}
Output leakage current	$\|I_{LO}\|$	—	—	1	µA	$\overline{CS1}$ = V_{IH} or CS2 = V_{IL} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL}, or $V_{I/O}$ = V_{SS} to V_{CC}
Operating current	I_{CC}	—	—	20	mA	$\overline{CS1}$ = V_{IL}, CS2 = V_{IH}, Others = V_{IH}/V_{IL}, $I_{I/O}$ = 0 mA
Average operating current	I_{CC1}	—	14	25	mA	Min. cycle, duty = 100%, $I_{I/O}$ = 0 mA, $\overline{CS1}$ = V_{IL}, CS2 = V_{IH}, Others = V_{IH}/V_{IL}
	I_{CC2}	—	2	4	mA	Cycle time = 1 µs, duty = 100%, $I_{I/O}$ = 0 mA, $\overline{CS1}$ ≤ 0.2 V, CS2 ≥ V_{CC} – 0.2 V V_{IH} ≥ V_{CC} – 0.2 V, V_{IL} ≤ 0.2 V
Standby current	I_{SB}	—	0.1	0.3	mA	CS2 = V_{IL}
Standby current	I_{SB1}	—	0.8	10	µA	0 V ≤ Vin (1) 0 V ≤ CS2 ≤ 0.2 V or (2) $\overline{CS1}$ ≥ V_{CC} – 0.2 V, CS2 ≥ V_{CC} – 0.2 V
Output high voltage	V_{OH}	2.4	—	—	V	I_{OH} = –1 mA
Output low voltage	V_{OL}	—	—	0.4	V	I_{OL} = 2.1 mA

Note: 1. Typical values are at V_{CC} = 5.0 V, Ta = +25°C and not guaranteed.

Capacitance (Ta = +25°C, f = 1.0 MHz)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions	Note
Input capacitance	Cin	—	—	8	pF	Vin = 0 V	1
Input/output capacitance	$C_{I/O}$	—	—	10	pF	$V_{I/O}$ = 0 V	1

Note: 1. This parameter is sampled and not 100% tested.

AC Characteristics (Ta = –40 to +85°C, V_{CC} = 5.0 V ± 10 %, unless otherwise noted.)

Test Conditions

- Input pulse levels: V_{IL} = 0.4 V, V_{IH} = 2.2 V
- Input rise and fall time: 5 ns
- Input and output timing reference levels: 1.5 V
- Output load: 1 TTL Gate + C_L (50 pF) (Including scope and jig)

Read Cycle

		HM628100I			
		-5			
Parameter	**Symbol**	**Min**	**Max**	**Unit**	**Notes**
Read cycle time	t_{RC}	55	—	ns	
Address access time	t_{AA}	—	55	ns	
Chip select access time	t_{ACS1}	—	55	ns	
	t_{ACS2}	—	55	ns	
Output enable to output valid	t_{OE}	—	35	ns	
Output hold from address change	t_{OH}	10	—	ns	
Chip select to output in low-Z	t_{CLZ1}	10	—	ns	2, 3
	t_{CLZ2}	10	—	ns	2, 3
Output enable to output in low-Z	t_{OLZ}	5	—	ns	2, 3
Chip deselect to output in high-Z	t_{CHZ1}	0	20	ns	1, 2, 3
	t_{CHZ2}	0	20	ns	1, 2, 3
Output disable to output in high-Z	t_{OHZ}	0	20	ns	1, 2, 3

Write Cycle

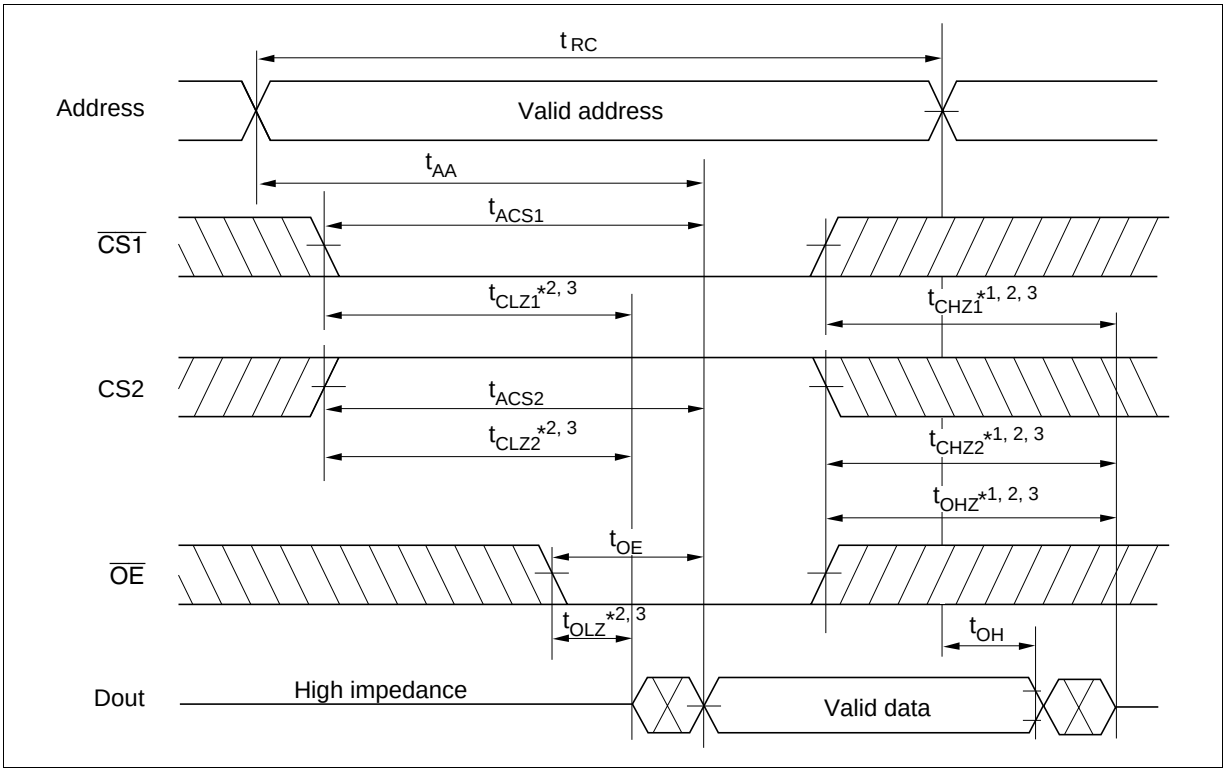
		HM628100I			
		-5			
Parameter	**Symbol**	**Min**	**Max**	**Unit**	**Notes**
Write cycle time	t_{WC}	55	—	ns	
Address valid to end of write	t_{AW}	50	—	ns	
Chip selection to end of write	t_{CW}	50	—	ns	5
Write pulse width	t_{WP}	40	—	ns	4
Address setup time	t_{AS}	0	—	ns	6
Write recovery time	t_{WR}	0	—	ns	7
Data to write time overlap	t_{DW}	25	—	ns	
Data hold from write time	t_{DH}	0	—	ns	
Output active from end of write	t_{OW}	5	—	ns	2
Output disable to output in high-Z	t_{OHZ}	0	20	ns	1, 2
Write to output in high-Z	t_{WHZ}	0	20	ns	1, 2

Notes: 1. t_{CHZ}, t_{OHZ} and t_{WHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referred to output voltage levels.

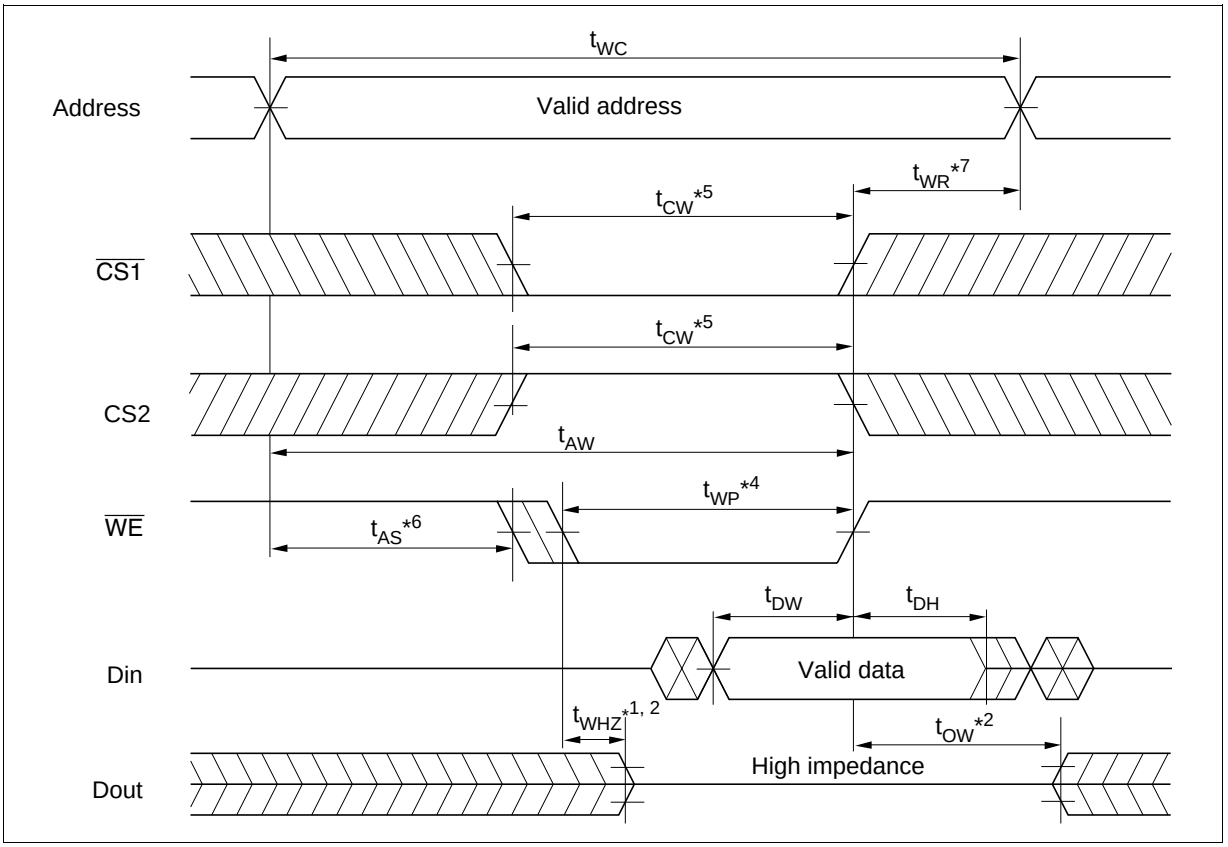
2. This parameter is sampled and not 100% tested.
3. At any given temperature and voltage condition, t_{HZ} max is less than t_{LZ} min both for a given device and from device to device.
4. A write occures during the overlap of a low $\overline{CS1}$, a high CS2, a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS1}$ going low, CS2 going high, $\overline{WE}$ going low. A write ends at the earliest transition among $\overline{CS1}$ going high, CS2 going low, $\overline{WE}$ going high. t_{WP} is measured from the beginning of write to the end of write.
5. t_{CW} is measured from the later of $\overline{CS1}$ going low or CS2 going high to the end of write.
6. t_{AS} is measured from the address valid to the beginning of write.
7. t_{WR} is measured from the earliest of $\overline{CS1}$ or $\overline{WE}$ going high or CS2 going low to the end of write cycle.

Timing Waveform

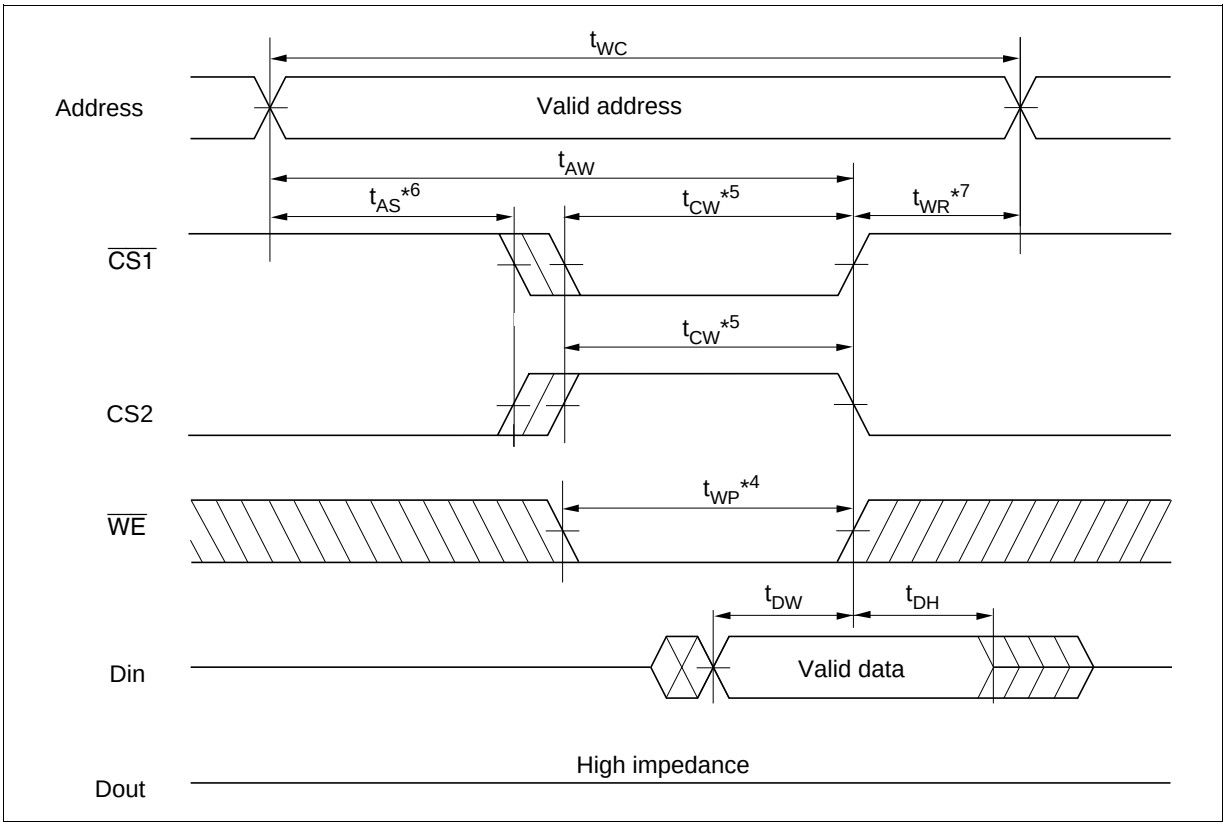
Read Cycle



Write Cycle (1) ($\overline{WE}$ Clock)



Write Cycle (2) ($\overline{CS}$ Clock, $\overline{OE}$ = V_{IH})



Low V_{CC} Data Retention Characteristics (Ta = –40 to +85°C)

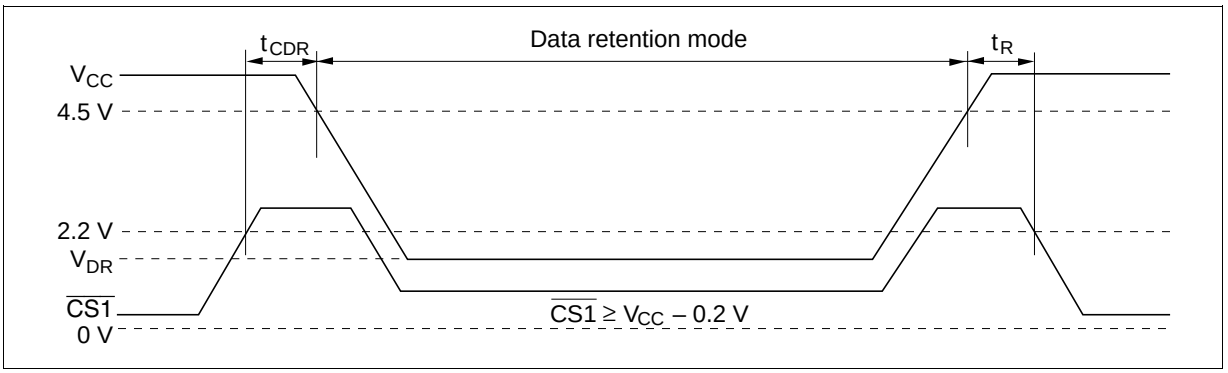
Parameter	Symbol	Min	Typ*[2]	Max	Unit	Test conditions*[1]
V_{CC} for data retention	V_{DR}	2.0	—	—	V	Vin ≥ 0 V (1) 0 V ≤ CS2 ≤ 0.2 V or (2) CS2 ≥ V_{CC} – 0.2 V $\overline{CS1}$ ≥ V_{CC} – 0.2 V
Data retention current	I_{CCDR}	—	0.8	10	µA	V_{CC} = 3.0 V, Vin ≥ 0 V (1) 0 V ≤ CS2 ≤ 0.2 V or (2) CS2 ≥ V_{CC} – 0.2 V, $\overline{CS1}$ ≥ V_{CC} – 0.2 V
Chip deselect to data retention time	t_{CDR}	0	—	—	ns	See retention waveform
Operation recovery time	t_R	t_{RC}*[3]	—	—	ns	

Notes: 1. CS2 controls address buffer, $\overline{WE}$ buffer, $\overline{CS1}$ buffer, $\overline{OE}$ buffer and Din buffer. If CS2 controls data retention mode, Vin levels (address, $\overline{WE}$, $\overline{OE}$, $\overline{CS1}$, I/O) can be in the high impedance state. If $\overline{CS1}$ controls data retention mode, CS2 must be CS2 ≥ V_{CC} – 0.2 V or 0 V ≤ CS2 ≤ 0.2 V. The other input levels (address, $\overline{WE}$, $\overline{OE}$, I/O) can be in the high impedance state.

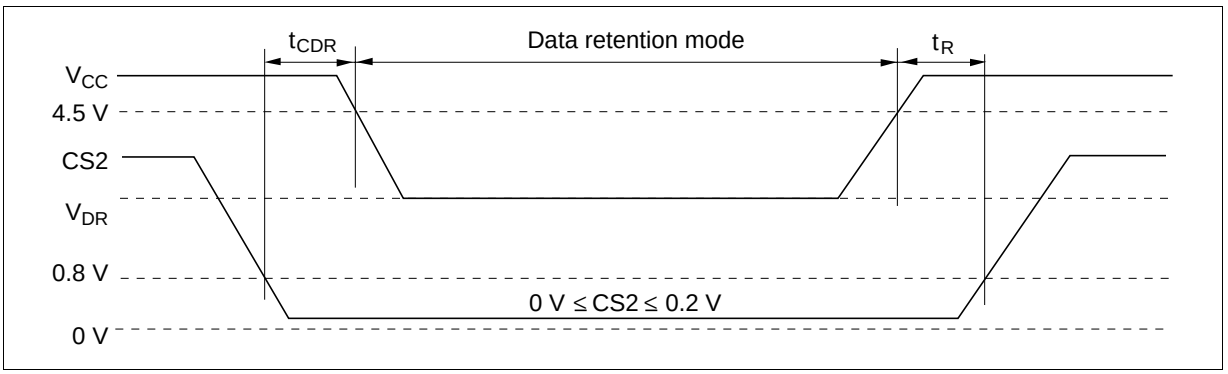
2. Typical values are at V_{CC} = 3.0 V, Ta = +25˚C and not guaranteed.

3. t_{RC} = read cycle time.

Low V_{CC} Data Retention Timing Waveform (1) ($\overline{CS1}$ Controlled)



Low V_{CC} Data Retention Timing Waveform (2) (CS2 Controlled)

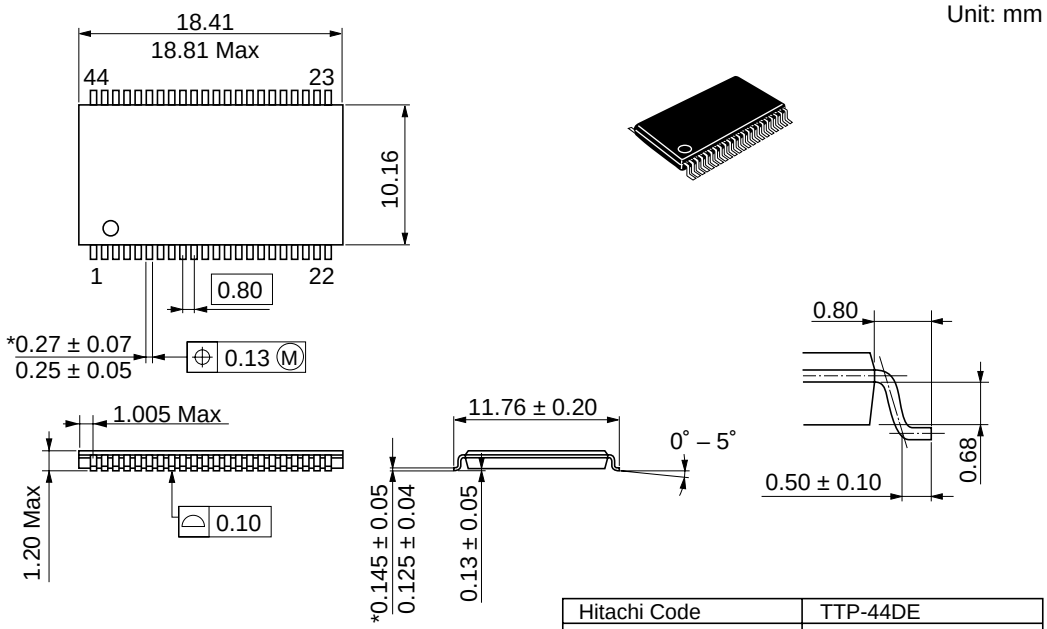


Package Dimensions

HM628100LTTI Series (TTP-44DE)

As of January, 2002

Unit: mm



*Dimension including the plating thickness
Base material dimension

Hitachi Code	TTP-44DE
JEDEC	—
JEITA	—
Mass (reference value)	0.43 g

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