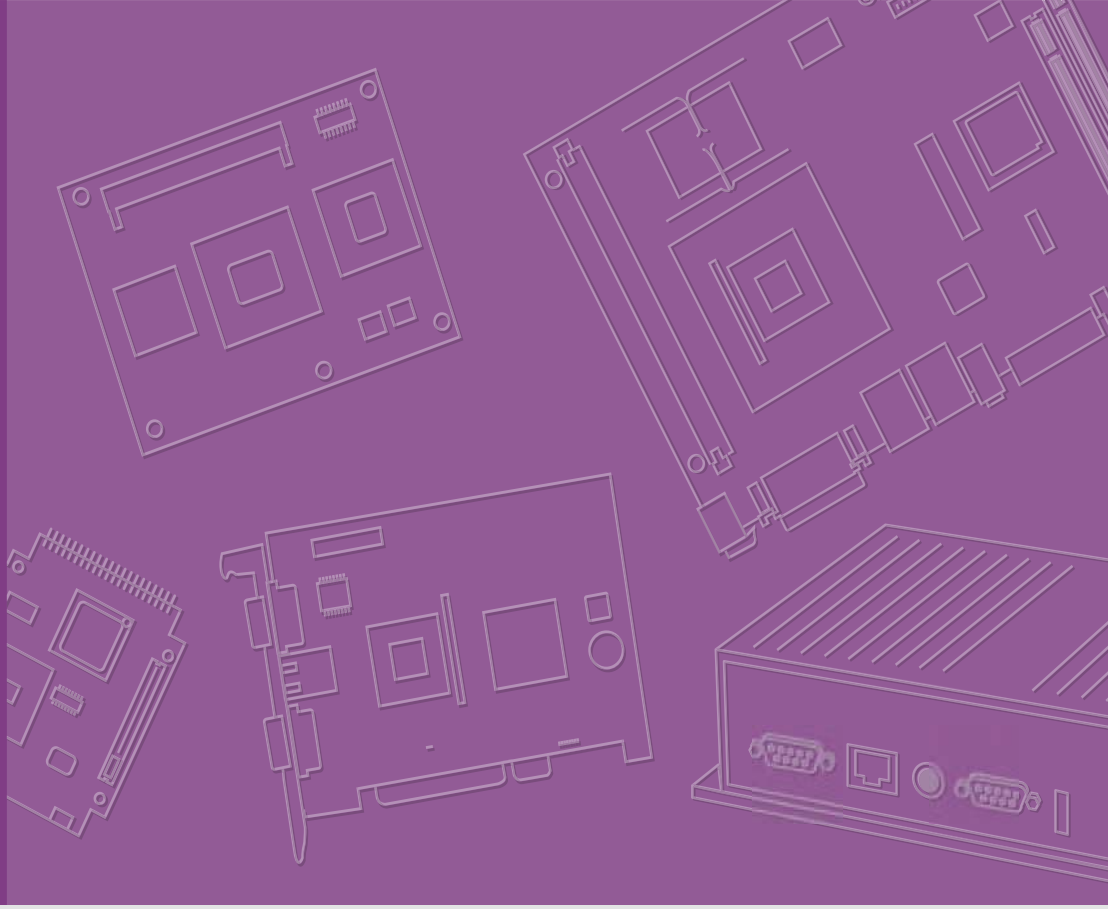


User Manual

ARK-5420 Series

Intel® 3rd Generation Core™ i Processor Based Fanless System with PCIE x 4 & PCI Slot

ADVANTECH

Enabling an Intelligent Planet

Attention!

This package contains a hard-copy user manual in Chinese for China CCC certification purposes, and there is an English user manual included as a PDF file on the CD. Please disregard the Chinese hard copy user manual if the product is not to be sold and/or installed in China.

Copyright

Acknowledgements

The ARK-5420 is trademark of Advantech Co., Ltd.

All other product names or trademarks are properties of their respective owners.

Product Warranty (2 years)

Advantech warrants to you, the original purchaser, that each of its products will be free from defects in materials and workmanship for two years from the date of purchase.

This warranty does not apply to any products which have been repaired or altered by persons other than repair personnel authorized by Advantech, or which have been subject to misuse, abuse, accident or improper installation. Advantech assumes no liability under the terms of this warranty as a consequence of such events.

Because of Advantech's high quality-control standards and rigorous testing, most of our customers never need to use our repair service. If an Advantech product is defective, it will be repaired or replaced at no charge during the warranty period. For out-of-warranty repairs, you will be billed according to the cost of replacement materials, service time and freight. Please consult your dealer for more details.

If you think you have a defective product, follow these steps:

1. Collect all the information about the problem encountered. (For example, CPU speed, Advantech products used, other hardware and software used, etc.) Note anything abnormal and list any onscreen messages you get when the problem occurs.
2. Call your dealer and describe the problem. Please have your manual, product, and any helpful information readily available.
3. If your product is diagnosed as defective, obtain an RMA (return merchandise authorization) number from your dealer. This allows us to process your return more quickly.
4. Carefully pack the defective product, a fully-completed Repair and Replacement Order Card and a photocopy proof of purchase date (such as your sales receipt) in a shippable container. A product returned without proof of the purchase date is not eligible for warranty service.
5. Write the RMA number visibly on the outside of the package and ship it prepaid to your dealer.

Part No. 2001542010 Edition 1

Printed in China August 2015

Technical Support and Assistance

1. Visit the Advantech web site at www.advantech.com/support where you can find the latest information about the product.
2. Contact your distributor, sales representative, or Advantech's customer service center for technical support if you need additional assistance. Please have the following information ready before you call:
   - Product name and serial number
   - Description of your peripheral attachments
   - Description of your software (operating system, version, application software, etc.)
   - A complete description of the problem
   - The exact wording of any error messages

Warnings, Cautions and Notes

Warning! *Warnings indicate conditions, which if not observed, can cause personal injury!*

Caution! *Cautions are included to help you avoid damaging hardware or losing data.*

Note! *Notes provide optional additional information.*

A Message to the Customer

Advantech Customer Services

Each and every Advantech product is built to the most exacting specifications to ensure reliable performance in the harsh and demanding conditions typical of industrial environments. Whether your new Advantech equipment is destined for the laboratory, factory floor, or any of a myriad of other uses, you can be assured that your product will provide the reliability and ease of operation for which the name Advantech has come to be known. Your satisfaction is our primary concern. Here is a guide to Advantech's customer services.

To ensure you get the full benefit of our services, please follow the instructions below carefully.

Technical Support

We want you to get the best performance possible from your products. If you run into technical difficulties, we are here to help. For the most frequently asked questions, you can easily find answers in your product documentation. These answers are normally a lot more detailed than the ones we can give over the phone.

So please consult this manual first. If you still cannot find the answer, gather all the information or questions that apply to your problem, and with the product close at hand, call your dealer. Our dealers are well trained and ready to give you the support you need to get the most from your Advantech products. In fact, most problems reported are minor and are easily solved over the phone.

In addition, free technical support is available from Advantech engineers every business day. We are always ready to give advice about application requirements or specific information on the installation and operation of any of our products.

Initial Inspection

Before setting up the system, check that the items listed below are included and in good condition. If any item does not accord with the table, please contact your dealer immediately.

- 1 x ARK-5420 series industrial computer
- 1 x ARK-5420 accessory box
- 1 x Warranty card

If any of these items are missing or damaged, contact your distributor or sales representative immediately. We have carefully inspected the ARK-5420 mechanically and electrically before shipment. It should be free of marks and scratches and in perfect working order upon receipt. As you unpack the ARK-5420, check it for signs of shipping damage. (For examples: box damage, scratches, dents, etc.) If it is damaged or it fails to meet the specifications, notify our service department or your local sales representative immediately. Also, please notify the carrier. Retain the shipping carton and packing material for inspection by the carrier. After inspection, we will make arrangements to repair or replace the unit.

Safety Instructions

1. Read these safety instructions carefully.
2. Keep this User Manual for later reference.
3. Disconnect this equipment from any AC outlet before cleaning. Use a damp cloth. Do not use liquid or spray detergents for cleaning.
4. For plug-in equipment, the power outlet socket must be located near the equipment and must be easily accessible.
5. Keep this equipment away from humidity.
6. Put this equipment on a reliable surface during installation. Dropping it or letting it fall may cause damage.
7. The openings on the enclosure are for air convection. Protect the equipment from overheating. DO NOT COVER THE OPENINGS.
8. Make sure the voltage of the power source is correct before connecting the equipment to the power outlet.
9. Position the power cord so that people cannot step on it. Do not place anything over the power cord.
10. All cautions and warnings on the equipment should be noted.
11. If the equipment is not used for a long time, disconnect it from the power source to avoid damage by transient overvoltage.
12. Never pour any liquid into an opening. This may cause fire or electrical shock.
13. Never open the equipment. For safety reasons, the equipment should be opened only by qualified service personnel.
14. If one of the following situations arises, get the equipment checked by service personnel:
    - The power cord or plug is damaged.
    - Liquid has penetrated into the equipment.
    - The equipment has been exposed to moisture.
    - The equipment does not work well, or you cannot get it to work according to the user's manual.
    - The equipment has been dropped and damaged.
    - The equipment has obvious signs of breakage.
15. DO NOT LEAVE THIS EQUIPMENT IN AN ENVIRONMENT WHERE THE STORAGE TEMPERATURE MAY GO BELOW -20° C (-4° F) OR ABOVE 60° C (140° F). THIS COULD DAMAGE THE EQUIPMENT. THE EQUIPMENT SHOULD BE IN A CONTROLLED ENVIRONMENT.
16. CAUTION: DANGER OF EXPLOSION IF BATTERY IS INCORRECTLY REPLACED. REPLACE ONLY WITH THE SAME OR EQUIVALENT TYPE RECOMMENDED BY THE MANUFACTURER, DISCARD USED BATTERIES ACCORDING TO THE MANUFACTURER'S INSTRUCTIONS.

The sound pressure level at the operator's position according to IEC 704-1:1982 is no more than 70 dB (A).

DISCLAIMER: This set of instructions is given according to IEC 704-1. Advantech disclaims all responsibility for the accuracy of any statements contained herein.

Safety Precaution - Static Electricity

Follow these simple precautions to protect yourself from harm and the products from damage.

- To avoid electrical shock, always disconnect the power from your PC chassis before you work on it. Don't touch any components on the CPU card or other cards while the PC is on.
- ESD (electrostatic discharge) can cause either catastrophic or latent damage in sensitive electronic components. Take appropriate measures to ensure that any accumulated body charge is removed before accessing electronic devices. A static-safe workbench is ideal.

Battery Information

Batteries, battery packs, and accumulators should not be disposed of as unsorted household waste. Please use the public collection system to return, recycle, or treat them in compliance with the local regulations.

Contents

Chapter 1

Overview

Sections include:

- Introduction
- Specifications
- Power Information
- Environment Specifications
- Dimension Diagram

1.1 Introduction

The ARK-5420 is a fanless, compact embedded industrial computer chassis with Core™ dual core processor and wide voltage input range. This powerful computing platform supports 24-hour-a-day, 7-day-a-week operation.

1.2 Specifications

- **Processor and Chipset:** Core™ processor + Intel® HM76 chipset
- **BIOS:** AMI SPI 64 Mb Flash
- **Memory:** On-board 4 GB DDR3 1333/1600 MHz
- **Display:** Integrated graphics HD4000, with up to 256 MB SDRAM shared system memory
- **Dual Display:**
  - Single display resolution up to 2048 x 1536 @ 60 Hz
  - Dual Display resolution up to 1920 x 1200 @ 60 Hz
- **Storage:** Supports 1 x 2.5” SSD Tray, 1 x Easy-swap CF Tray, 1 x mSATA socket on board
- **Expansion Slot:** 1 x Mini PCIe slot, 1 x PCI slot, 1 PCIE x 4 slot
- **Ethernet:** 2 x 10/100/1000M Ethernet (Controller chip: Intel i210-IT)
- **USB:**
  - 3 x USB2.0 with Type A
  - 2 x USB3.0 with Type A
- **VGA:** 1 x VGA
- **HDMI:** 1 x HDMI
- **Serial I/O:** 2 x DB9, RS232/422/485 with automatic flow control
- **Digital I/O:** 1 x 8-ch GPIO
- **Audio:** 1 x Speaker out with 2 x 4 w amplifer,1 Mic input; DB9 type Reserved Zone (Real I/O panel):
  - 1 x PCI expansion slot
  - 1 x PCIE x 4 slot
  - 1 x LVDS
- **Dimensions (W x H x D):**
  - 210 x 129 x 240 mm (without ears)
  - 253 x 133 x 240 mm (with ears)
- **Weight:** 4.5 kg

1.3 Power Information

ARK-5420 supports 9 V ~ 36 VDC input.

Table 1.1: Power		
DC voltage input	9 V - 36 V	7.2 A - 1.8 A
DC power interface	2-pin terminal block	

1.4 Environmental Specifications

- **Operating Temperature:** -20 ~ 60° C with 0.7 m/sec air flow: with 1 x Industrial SSD without PC expansion boards (Advantech Lab test specification)
- **Safety Certificate:** UL, CCC, BSMI, CE and FCC compliant
- **Temperature:** 0 ~ 50° C
- **Storage Temperature:** -40 ~ 85° C
- **Humidity:** 95% @ 40° C, non-condensing
- **Vibration:**
  - With Compact Flash: 2 Grms @ 5 ~ 500 Hz, random, 1 hr/axis;
  - With 2.5” HDD: 0.5 Grms @ 5 ~ 500 Hz, random, 1 hr/axis; IEC60068-2-6 Sine 2 G @ 5 ~ 500 Hz, 1 hr/axis
- **Shock:**
  - With Compact Flash: 20 G, IEC-68-2-27, half-sine wave, 11 ms duration
  - With 2.5” HDD: 10 G, IEC-68-2-27, half-sine wave, 11 ms duration

1.5 Dimension Diagram

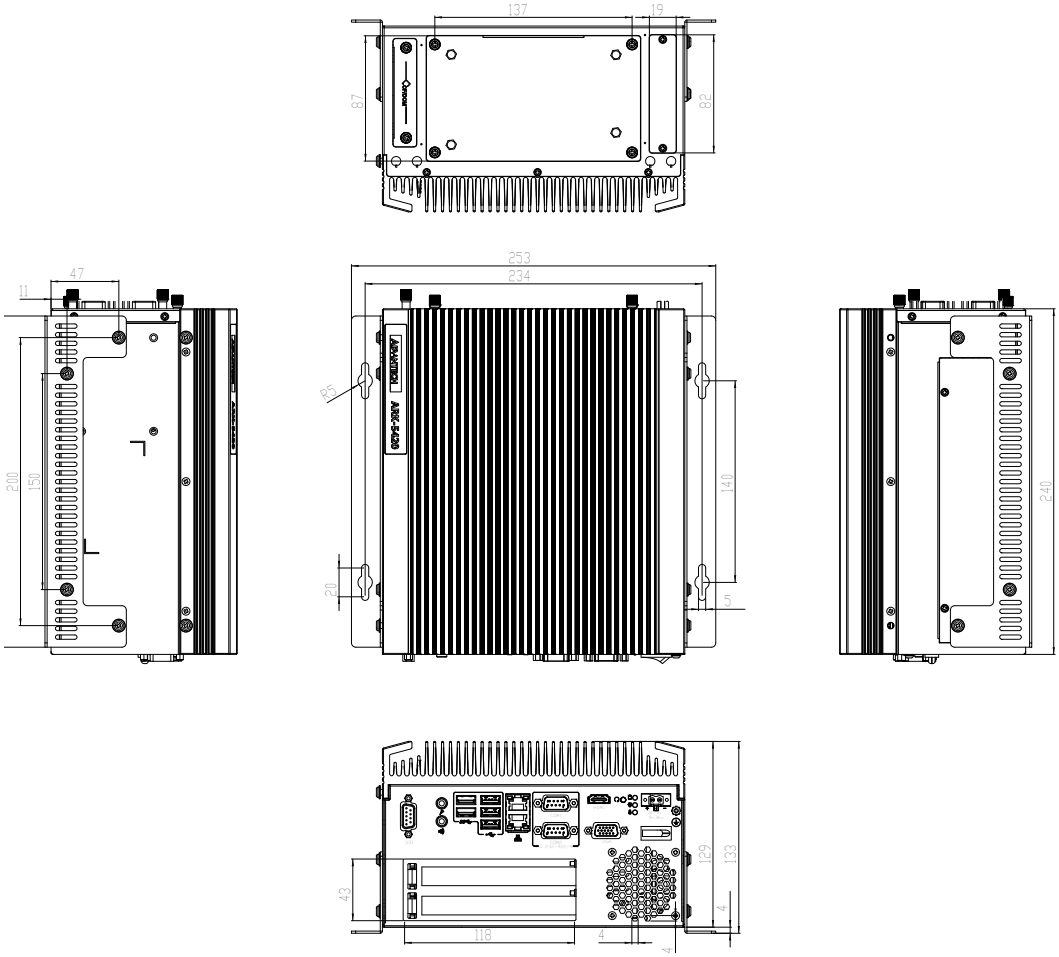


Figure 1.1 Dimension Diagram of ARK-5420

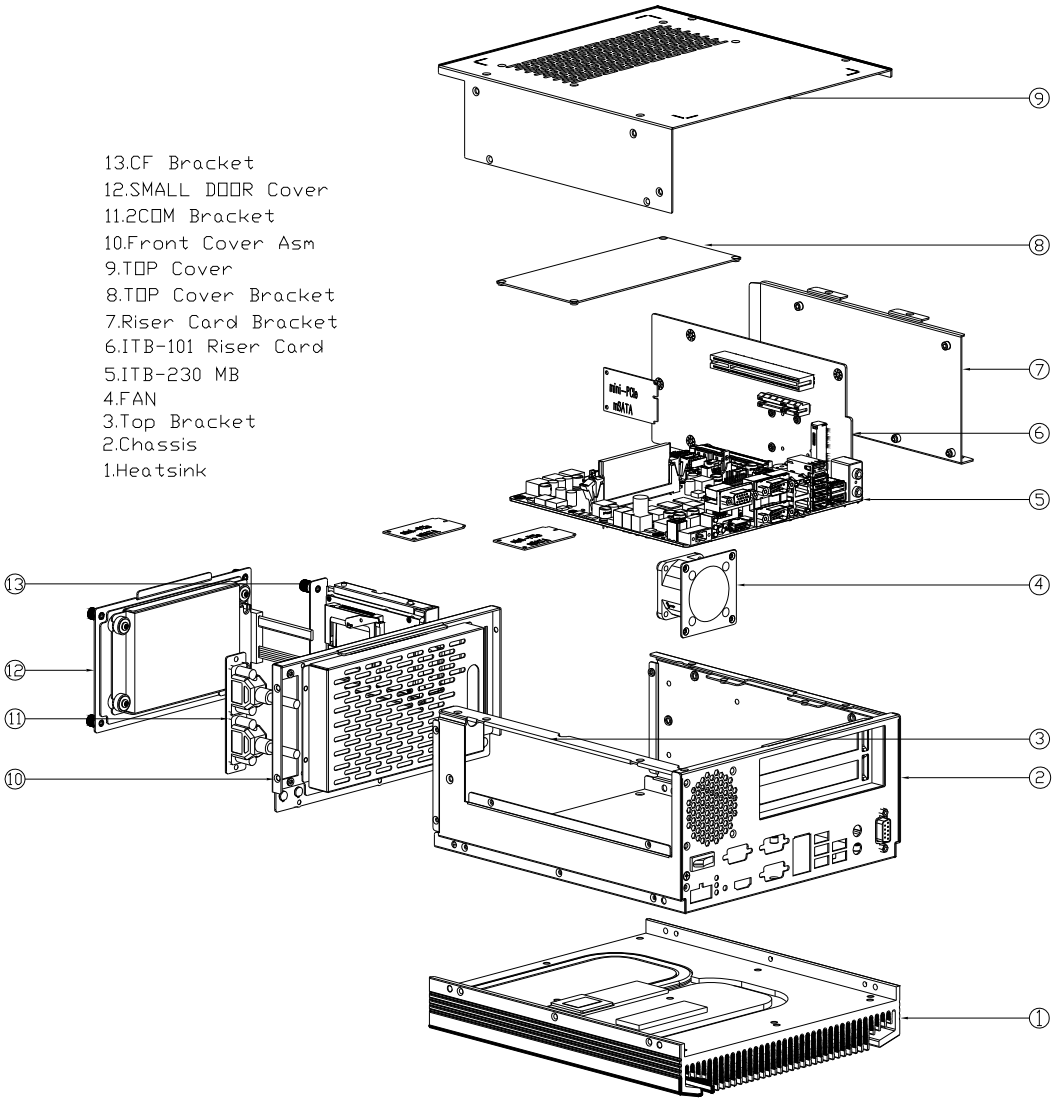


Figure 1.2 Exploded Diagram of ARK-5420

1	Heat sink
2	Chassis
3	Top Bracket
4	FAN
5	ITB-230 MB
6	ITB-102 Riser Card
7	Riser Card Bracket
8	Top Cover Bracket
9	Top Cover
10	Front Cover Asm
11	2 COM Bracket
12	Small Door Cover
13	CF Bracket

Chapter 2

Hardware installation

Sections include:

- Introduction
- Jumpers and Connectors
- I/O Connectors

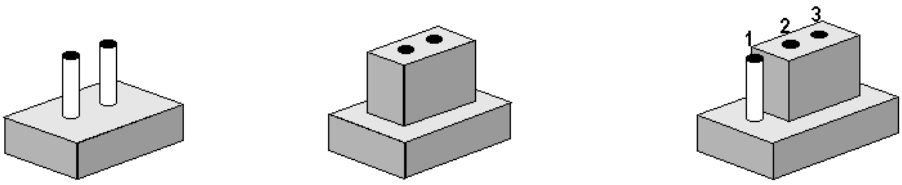
2.1 Introduction

The following sections show the internal jumper settings and the external connectors and pins assignment for applications.

2.2 Jumpers and Connectors

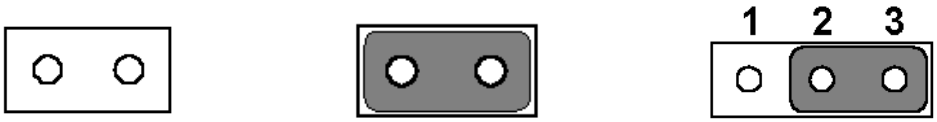
2.2.1 Jumper Description

You may configure the ARK-5420 to match the needs of your application by setting jumpers. A jumper is a metal bridge used to close an electric circuit. It consists of two metal pins and a small metal clip (often protected by a plastic cover) that slides over the pins to connect them. To close a jumper, you connect the pins with the clip. To open a jumper, you remove the clip. Sometimes a jumper will have three pins, labeled 1, 2 and 3. In this case you would connect either pins 1 and 2, or 2 and 3.



Open Closed 2-3 Closed

The jumper settings are schematically depicted in this manual as follows.



Open Closed 2-3 Closed

A pair of needle-nose pliers may be helpful when working with jumpers. If you have any doubts about the best hardware configuration for your application, contact your local distributor or sales representative before you make any changes. Generally, you simply need a standard cable to make most connections.

2.2.2 Jumper and Connector Location

The board has a number of connectors and jumpers that allow you to configure your system to suit your application. The table below lists the function of each of the connectors and jumpers.The locations of jumpers and connector on the board are shown in Figure 2.1.

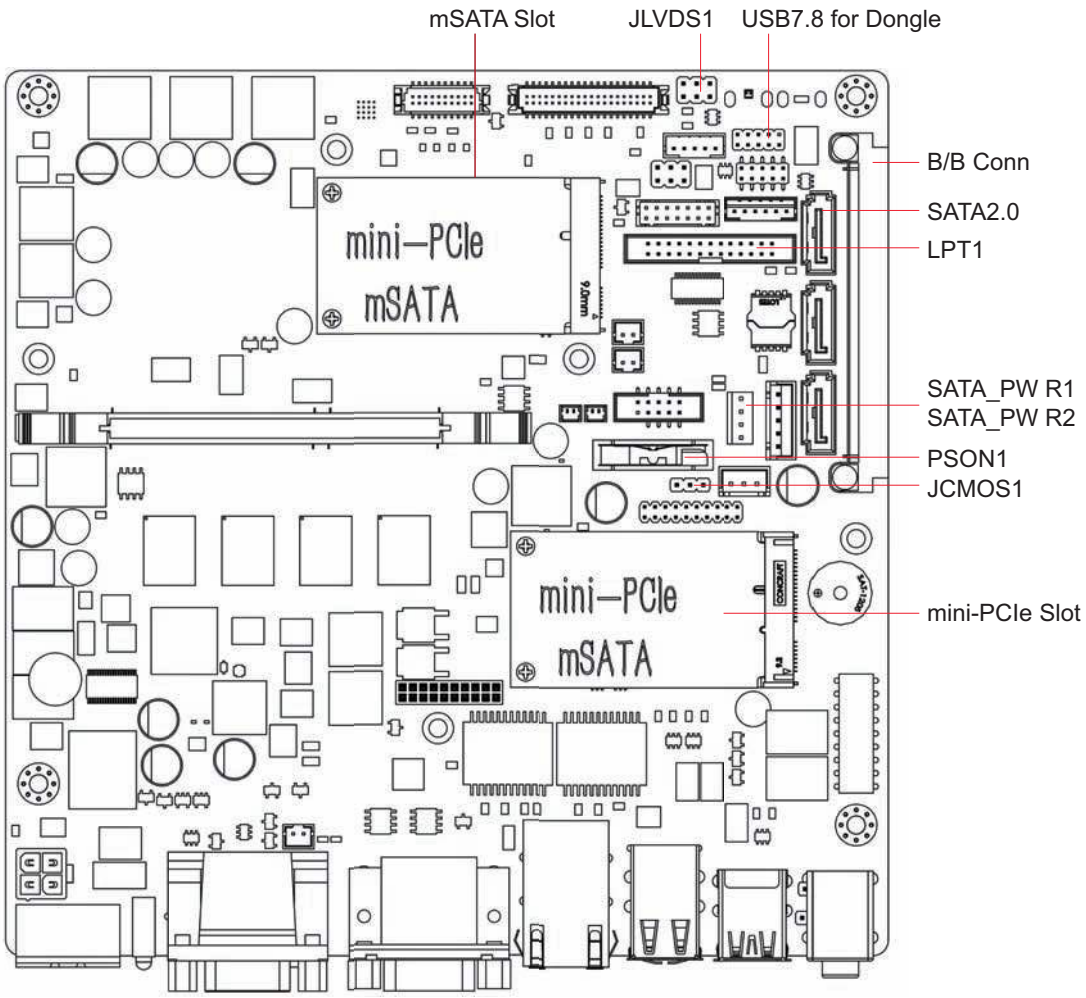
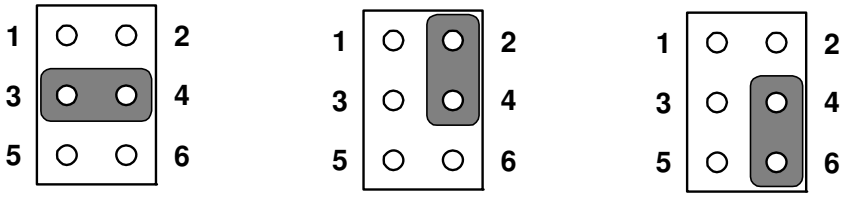


Figure 2.1 Jumper and Connector Location on Main Board

Table 2.1: Jumpers	
Label	**Function**
JLVDS1	LVDS voltage selection
JCMOS1	Clear CMOS settings
PSON1	Clear CMOS settings
VCCGPIO1	GPIO voltage selection

Table 2.2: JLVDS1: LVDS Voltage Selection	
Closed Pins	**Setting**
3-4	Setting
2-4	+V5
4-6	+V5
*Default setting	

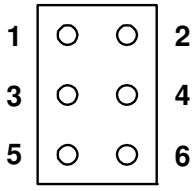


For 12V For 5V For 3.3V

Table 2.3: JCMOS1: CMOS Clear Function	
Closed Pins	**Setting**
1-2	Default*
2-3	Default*
* Default setting	

Table 2.4: PSON1: Startup-up Mode Selection	
Closed Pins	**Setting**
1-2	AT Mode
2-3	AT Mode
* Default setting	

Table 2.5: VCCGPIO1: GPIO Voltage Selection	
Closed Pins	**Setting**
1-3	Setting
2-4	Normal (+V3.3_SB)*
3-5	+V5
4-6	+V5
* Default setting	



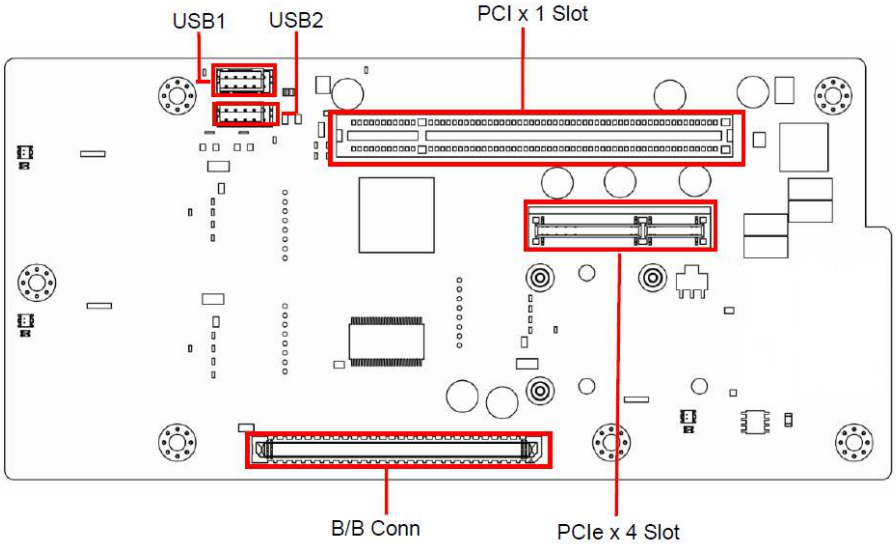


Figure 2.2 Jumper and Connector Location on Riser Board

2.3 I/O Connectors

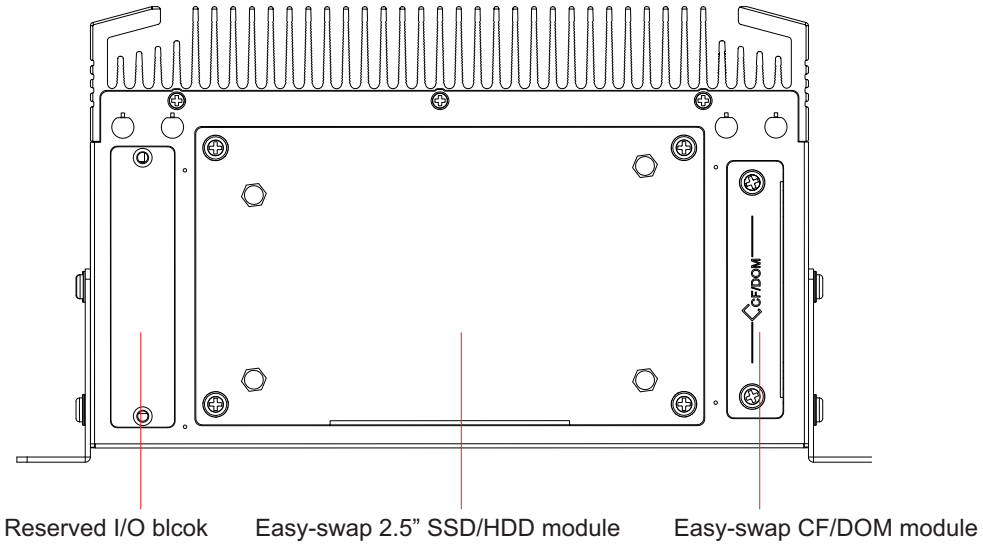


Figure 2.3 ARK-5420 Rear I/O Interfaces

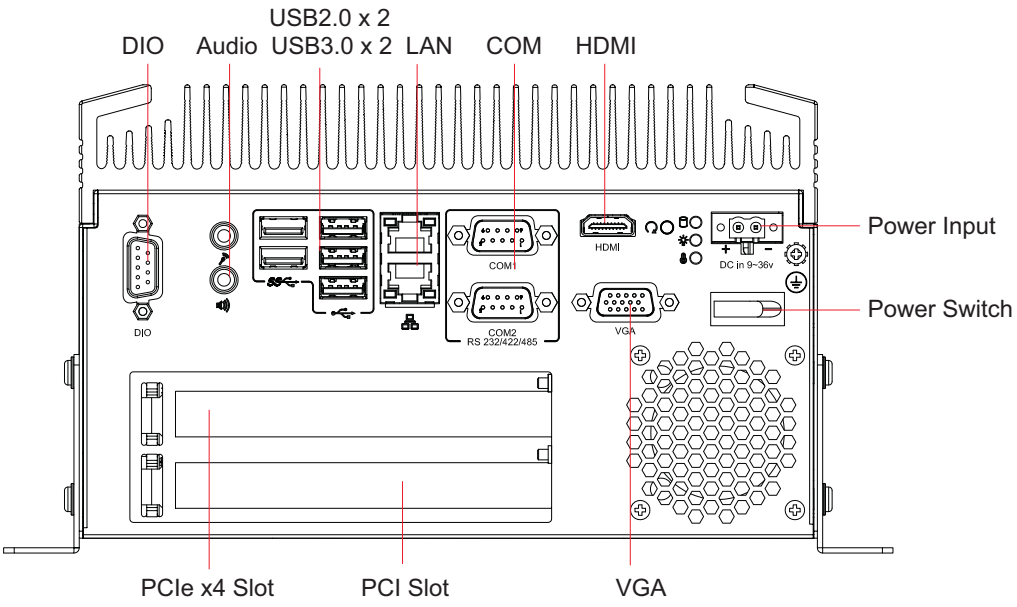


Figure 2.4 ARK-5420 Front I/O Interfaces

2.3.1 COM Connector

ARK-5420 provides two D-sub 9-pin connectors for RS-232/422/485. The default setting is RS-232.

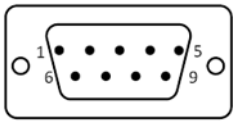


Table 2.6: COM Connector Pin Definition

	RS-232	RS-422	RS-485
Pin	**Signal Name**	**Signal Name**	**Signal Name**
1	DCD	Tx-	DATA-
2	RxD	Tx+	DATA+
3	TxD	Rx+	NC
4	DTR	Rx-	NC
5	GND	GND	GND
6	DSR	NC	NC
7	RTS	NC	NC
8	CTS	NC	NC
9	RI	NC	NC

2.3.2 HDMI Connector

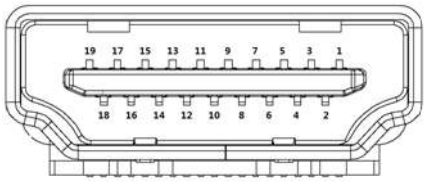


Table 2.7: HDMI Connector Pin Definition

Pin	Signal Name	Signal Name	Signal Name
1	TMDS Data2+	11	TMDS Clock Shiled
2	TMDS Data2 Shiled	12	TMDS Clock-
3	TMDS Data2-	13	Reserved
4	TMDS Data1+	14	Reserved
5	TMDS Data1 Shiled	15	SCL
6	TMDS Data1-	16	SDA
7	TMDS Data0+	17	DDC/CEC Ground
8	TMDS Data0 Shiled	18	+5V Power
9	TMDS Data0-	19	Hot Plug Detect
10	TMDS Clock+		

2.3.3 VGA Connector

ARK-5420 offers one D-sub 15-pin female connector, which supports max. resolution of 2048 x 1563.

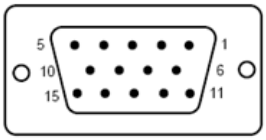


Table 2.8: VGA Connector Pin Definition

Pin	Signal Name	Pin	Signal Name
1	Red	9	+5V
2	Green	10	GND
3	Blue	11	NC
4	NC	12	DDC-DATA
5	GND	13	H-SYNC
6	GND	14	V-SYNC
7	GND	15	DDC-CLK
8	GND		

2.3.4 USB 2.0 Connector

ARK-5420 provides four USB interface connectors, which are USB EHCI, Rev. 2.0 compliant. The USB interface can be disabled in the system BIOS setup.

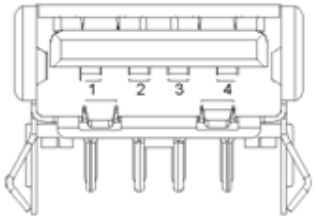


Table 2.9: USB2.0 Connector Pin Definition

Pin	Signal Name	Pin	Signal Name
1	+V5(VCC)	3	USB DATA+
2	USB DATA-	4	GND

2.3.5 USB 3.0 Connector

ARK-5420 provides two USB interface connectors, which are USB XHCI, Rev. 3.0 compliant. The USB interface can be disabled in the system BIOS setup.

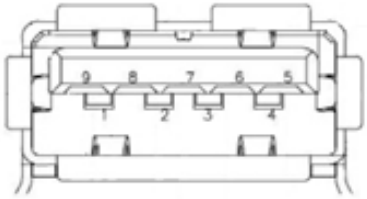


Table 2.10: USB3.0 Connector Pin Definition			
Pin	**Signal Name**	**Pin**	**Signal Name**
1	+V5(VCC)	6	StdA_SSRX+
2	D-	7	GND_DRAIN
3	D+	8	StdA_SSTX-
4	GND	9	StdA_SSTX+
5	StdA_SSRX-		

2.3.6 DIO Connector

ARK-5420 provides one 8-bit DIO, D-sub 9-pin male connector without isolation protection.

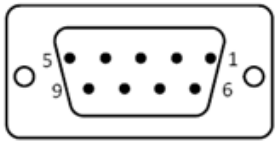
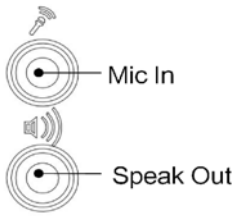


Table 2.11: DIO Connector Pin Definition			
Pin	**Signal Name**	**Pin**	**Signal Name**
1	GPIO0	6	GPIO4
2	GPIO1	7	GPIO5
3	GPIO2	8	GPIO6
4	GPIO3	9	GPIO7
5	GND		

2.3.7 Audio in Connector

ARK-5420 provides one integrated Mic-in/speaker out audio connector with DB9 type.



2.3.8 LAN(M12, A-coded, 8-pin, Female)

ARK-5420 provides 3 10/100/1000M Ethernet with M12 A-coded.

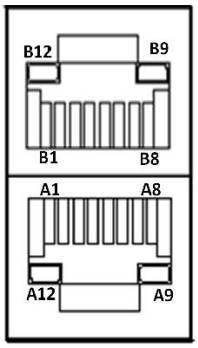


Table 2.12: Ethernet Port Pin Definition

Pin	Signal Name	Signal Name
A1/B1	MDIO0+	MDIO0+
A2/B2	MDIO0-	MDIO0-
A3/B3	MDIO1+	MDIO1+
A4/B4	MDIO2+	MDIO2+
A5/B5	MDIO2-	MDIO2-
A6/B6	MDIO1-	MDIO1-
A7/B7	MDIO3+	MDIO3+
A8/B8	MDIO3-	MDIO3-
A9/B9	LED GREEN-	LED GREEN-
A10/B10	LED GREEN+	LED GREEN+
A11/B11	1000M LED	1000M LED
A12/B12	100m/10M LED	100m/10M LED

2.3.9 Power Input

ARK-5420 provides 24V/48V/72V/110V DC voltage input.

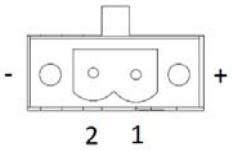


Table 2.13: Power Connector Pin Definition

Pin	Signal Name
1	Positive
2	GND

Chapter 3

System Setup

Sections include:

- Installing Mainboard mini-PCIe card and mini SATA
- Installing USB Dongle
- Installing HDD Module
- Installing Foot Stand
- Installing Notes

3.1 Introduction

The following procedures will instruct you to install all modules into the ARK-5420 system.

3.1.1 Installing Mainboard mini-PCIe Card and m-SATA

1. ARK-5420mainboard has a Mini PCIe slot and a m-SATA slot. Each one has a label for users to distinguish.
2. Insert mini-PCIe card and mSATA card to the respective slot and fix with two screws.

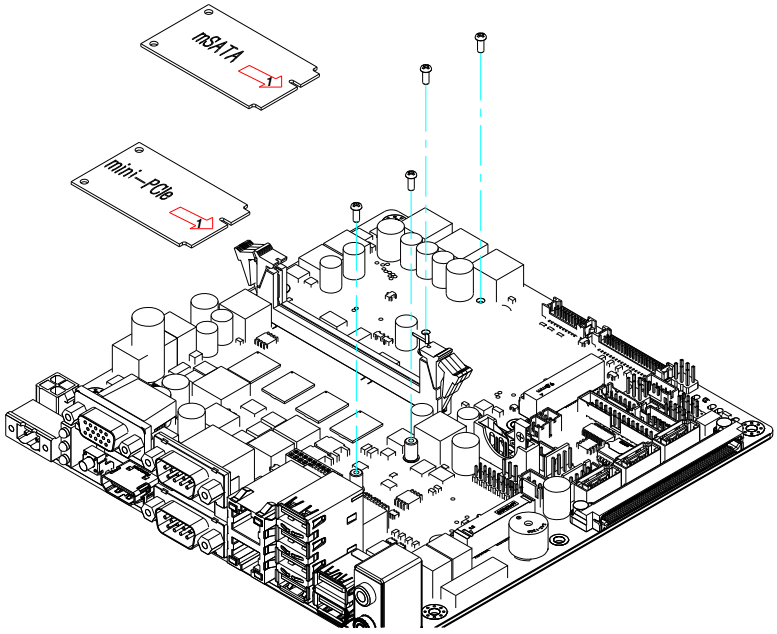


Figure 3.1 Installing Mainboard Mini-PCIe Card and m-SATA

3.1.2 Installing PCI Card and PCIE Card

ARK-5420 provides 1 PCI slot & 1 PCIE x 4 slot for customized expansion.

1. Remove screws from outside of the chassis.
2. Remove the Top Cover.
3. Assemble I/O bracket with PCI card & PCIE x 4 card.
4. Add the Top Cover.

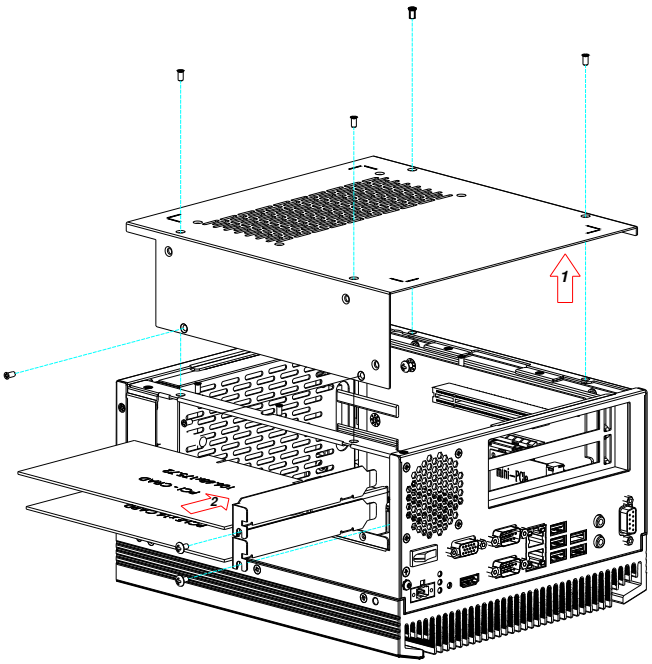


Figure 3.2 Installing PCI Card & PCIE Card

3.1.3 Installing HDD Module and Easy-swap CF Module

The ARK-5420 reserves a space for 2.5" HDD module and CF module. And its design is benefit for customers to assemble or disassemble storage without tools.

3.1.3.1 Installing CF Module

1. Fix CF module board onto CF tray.
2. Insert the CF card into CF module board and fix it with fixed plastic shell.
3. Place CF tray onto HDD bracket and secure it with the screws.
4. Insert the CF module.

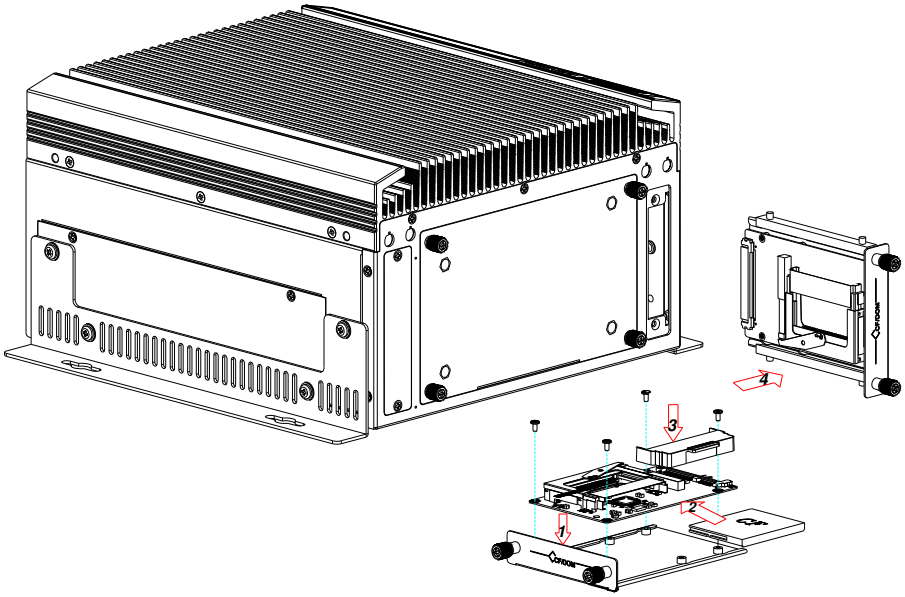


Figure 3.3 Installing CF Module

3.1.3.2 Installing HDD Module

1. Fix 4 rubbers to HDD bracket.
2. Place 2.5" HDD into HDD bracket and tighten with screws.
3. Assemble HDD bracket to HDD door.
4. Connect HDD to SATA cable.
5. Tighten up HDD door on chassis with hand locking screw.

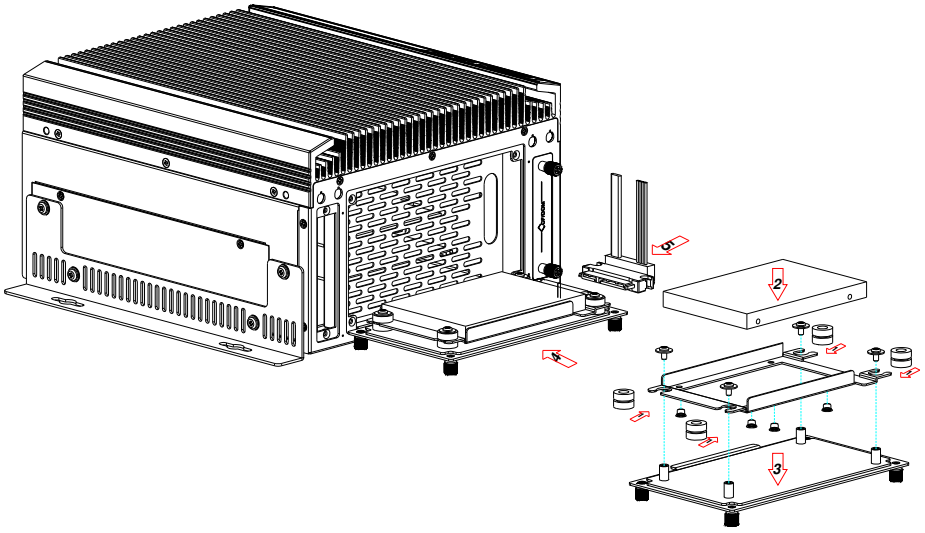


Figure 3.4 Installing HDD Module

3.1.4 Installing Foot Stand

Align the foot stands with the screw holes in the chassis side panel, and secure them with screws.

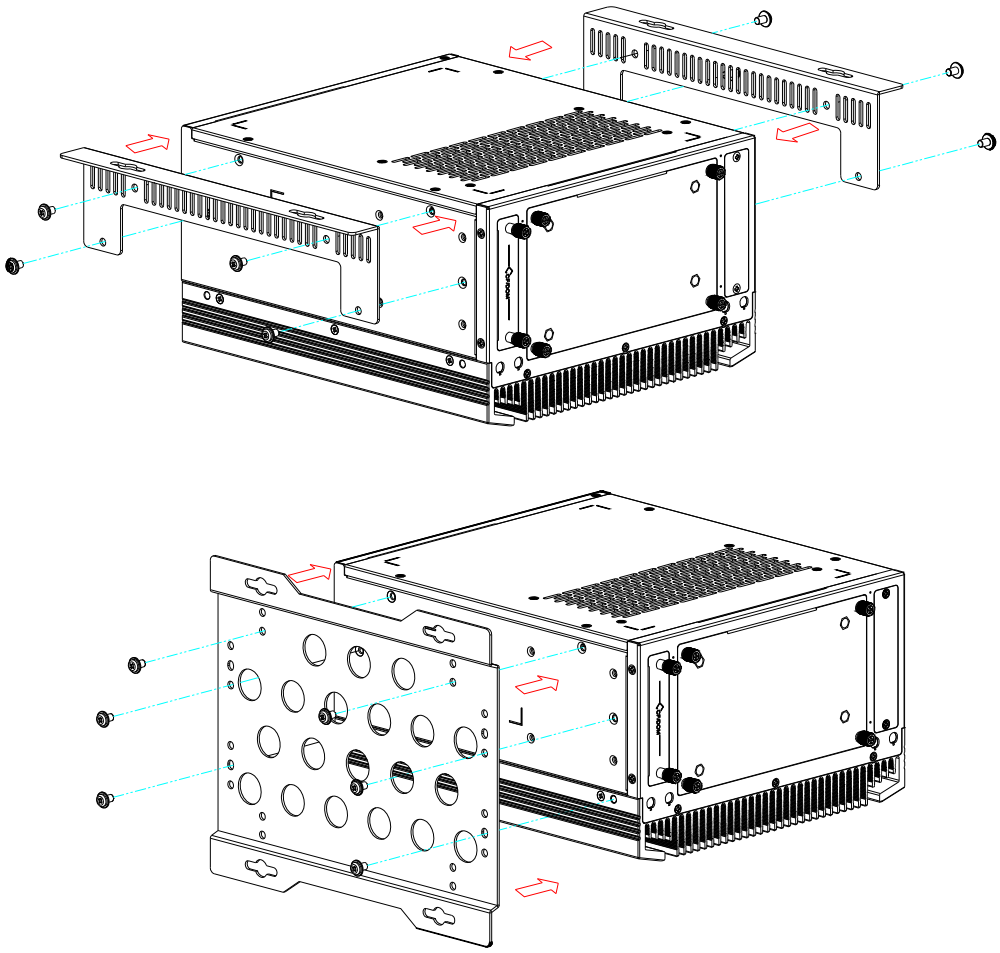


Figure 3.5 Installing Foot Stand

3.1.5 Installing FAN module (optional function)

If customer use the high power card for PCI & PCIE slot, just like POE card, we reserved the FAN module for the machine heat dissipation.

1. Remove the Top Cover.
2. Remove FAN bracket.
3. Assemble FAN on the chassis with screw.
4. Use 1700023422-01 to connect the INV CON on MB and FAN.
5. Add the Top Cover.

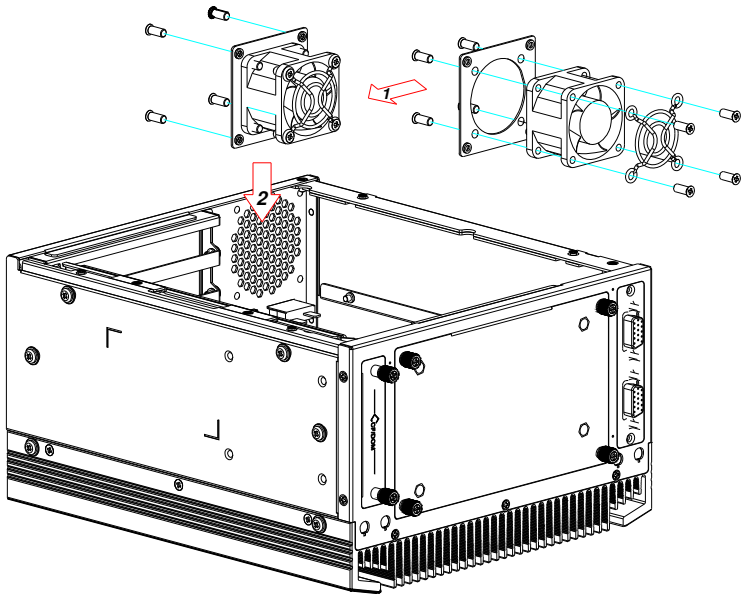


Figure 3.6 Installing FAN module

Chapter 4

BIOS Setting

4.1 Introduction

This chapter introduces how to configure BIOS for ARK-5420 series. The ARK-5420 Series system has AMI BIOS built in, with an Aptio SETUP utility that allows users to configure required settings or to activate certain system features.

The Aptio SETUP saves the configuration in the BIOS flash of the motherboard. When the power is turned off.

When the power is turned on, press the <Del> button or <F2> button during the BIOS POST (PowerOn Self Test) to access the Aptio SETUP screen.

Table 4.1: Aptio Setup Control Keys

KEY	Function
< ← > < → >	Select desired screen
< ↑ >< ↓ >	Select desired item
< Enter >	Engage item to make settings
< + >	Increase the numeric value or make changes
< - >	Decrease the numeric value or make changes
< F1 >	General help, for Setup Sub Menu
< F2 >	Load Previous Values
< F3 >	Load Optimized Default Values
< F4 >	Save changes and Exit Setup
< ESC >	Main Menu - Quit without saving changes Sub Menu - Exit current page and return to Main Menu

4.2 Entering Setup

Press <Del> or <F2> to enter AMI BIOS Aptio Setup Utility, the Main Menu will appear on the screen. Use arrow keys to select among the items and press <Enter> to accept or enter the sub-menu.

4.2.1 Main Setup

The Main BIOS setup screen has two main frames. The left frame displays all the options that can be configured. Grayed-out options cannot be configured; options in blue can. The right frame displays the key legend.

Above the key legend is an area reserved for a text message. When an option is selected in the left frame, it is highlighted in white. Often a text message will accompany it.

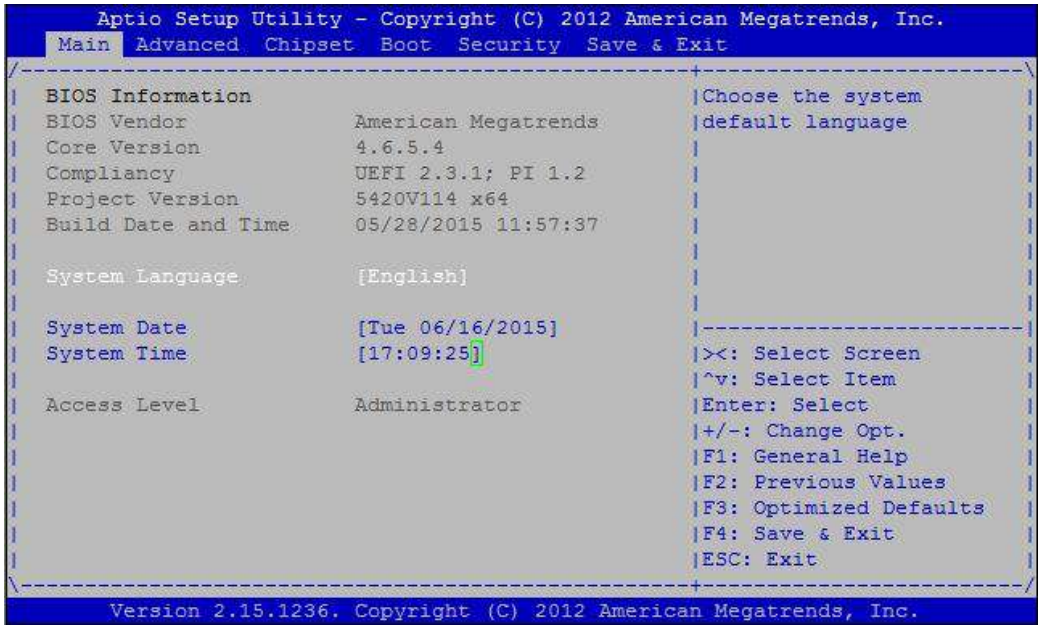


Figure 4.1: Main Setup Screen

- **System Language**
  English: DEFAULT
  Use these options to change the system language.
- **System Time** / **System Date**
  System Time DEFAULT: 01 / 01 / 2012
  System Date DEFAULT: 00:00:00
  Use this option to change the system time and date. Highlight System Time or System Date using the <Arrow> keys. Enter new values through the keyboard. Press the <Tab> key or the <Arrow> keys to move between fields. The date must be entered in MM/DD/YY format. The time must be entered in HH:MM:SS format.

4.2.2 Advanced BIOS Features Setup

Select the Advanced tab from the ARK-5420 setup screen to enter the Advanced BIOS Setup screen. You can select any of the items in the left frame of the screen, such as CPU Configuration, to go to the sub menu for that item. You can display an Advanced BIOS Setup option by highlighting it using the <Arrow> keys. All Advanced BIOS Setup options are described in this section. The Advanced BIOS Setup screen is shown below. The sub menus are described on the following pages.

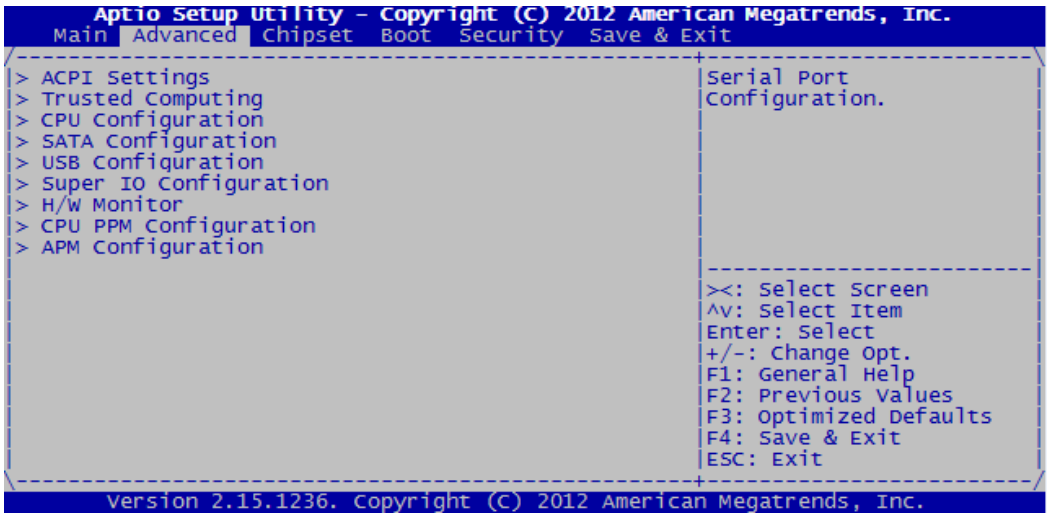


Figure 4.2: Advanced BIOS Features Setup Screen

4.2.2.1 ACPI Configuration

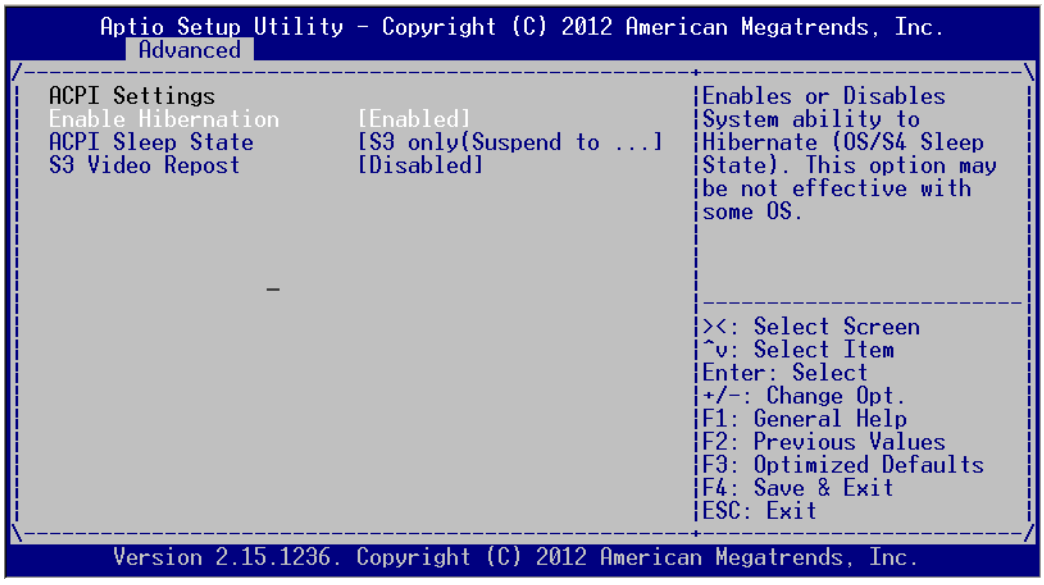


Figure 4.3 ACPI Configuration

- **Enable Hibernation**
  This item allows users to enable or disable Hibernation.
- **ACPI Sleep State**
  This item allows users to select APCI state during system hibernation.
- **S3 Video Repost**
  This item is used to decide whether to call VBIOS when the system resumes from S3/SRT. The default setting is “Disabled”.

4.2.2.2 Trusted Computing

This item allows user to setting TPM function.

Note! *TPM is optional module. P/N: PCA-TPM-00A1E*

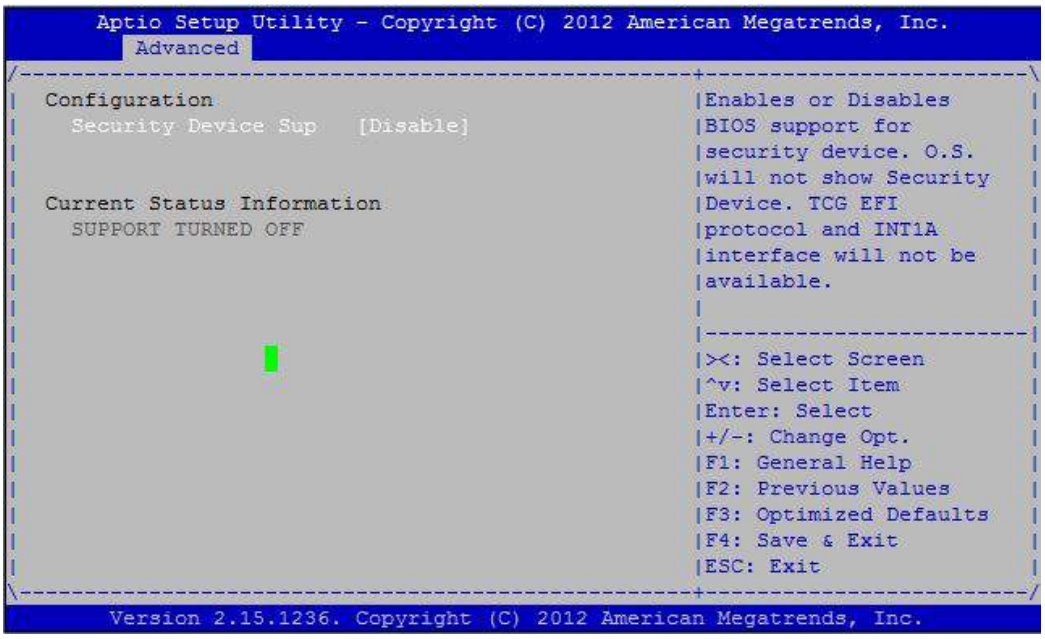


Figure 4.4 Without TPM module Configuration

- **Security Device Support**

  This item allows user to Disable or Enable. User should set to Enable the first time to set up the TPM module. Please save changes to the BIOS and re-boot system after setting.

Figure 4.5 TPM On-board Configuration

- **Security Device Support**
  This item allows user to set BIOS for TPM module support.
- **TPM State**
  This item allows user to set TPM state to "Disable" or "Enable". Function details should be configured according to the OS.
- **Current Status information**
  (These 3 items should be set according to the OS)
  - TMP Enabled Status
  - TPM Active Status
  - TPM Owner Status

4.2.2.3 CPU Configuration

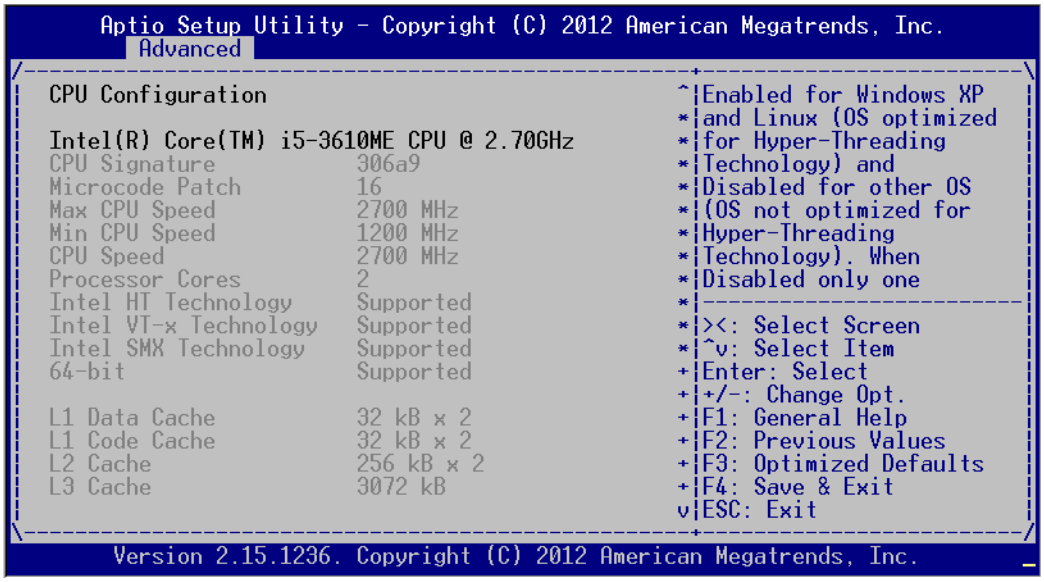


Figure 4.6: CPU Configuration (1)

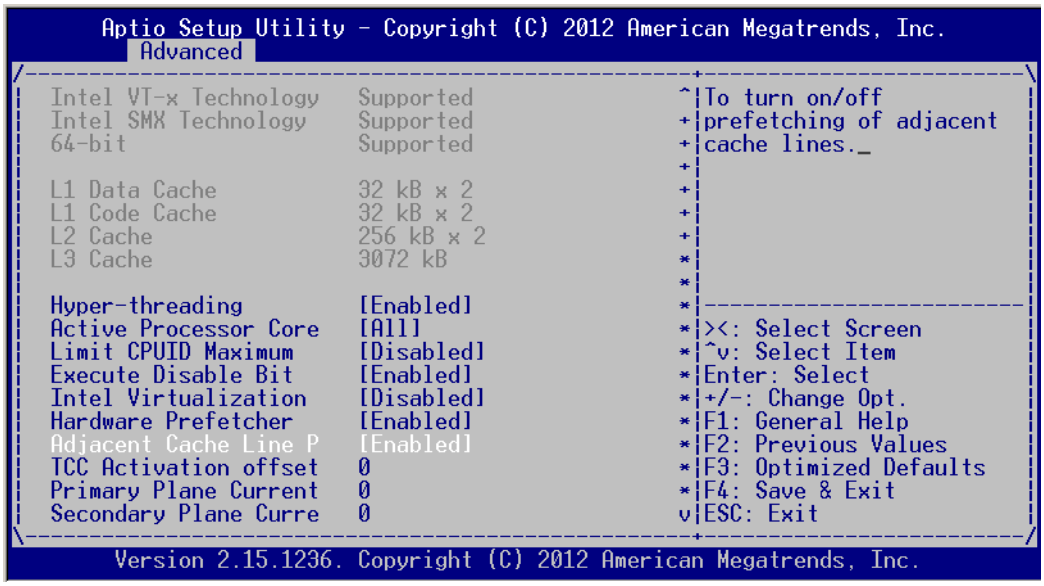


Figure 4.7 CPU Configuration (2)

- **Hyper Threading**
  This item allows users to enable or disable Intel® Hyper Threading Technology. The default setting is “Enabled”.

- **Active Processor Core**
  This item allows users to choose how many processor cores to activate when using a dual- or quad-core processor.The default setting is “All”.
- **Limit CPUID Maximum**
  This item allows users to set the limit value for CPUID. The default setting is “Disabled”.
- **Execute Disable Bit**
  This item is a hardware feature introduced by Intel® in its new generation CPU. It can help the CPU to self-protect in event of hostile attack based on buffer overflow, so as to avoid the virus attack, such as blasting wave. The default setting is “Enabled”.
- **Hardware Prefectcher**
  This item allows users to enable or disable Hardware Prefetcher Technology. The default setting is “Enabled”.
- **Adjacent Cache Line Prefetch**
  This item allows users to enable or disable sequential access to memory. The default setting is “Enabled”.
- **Intel® Virtualization Technology**
  This item is a system virtualization technology adopted in CPUs produced by Intel®. It allows multiple operating systems to run simultaneously on the same system. It adopts Vanderpool Technology, which allows multiple systems to run on the same system and applications can run in their own individual space. The default setting is “Enabled”.

4.2.2.4 SATA Configuration

Figure 4.8 SATA Configuration

- **SATA Mode Selection**
  This item allows users to select configuration mode of SATA Controller(s). The default setting is “AHCI”.

4.2.2.5 USB Configuration

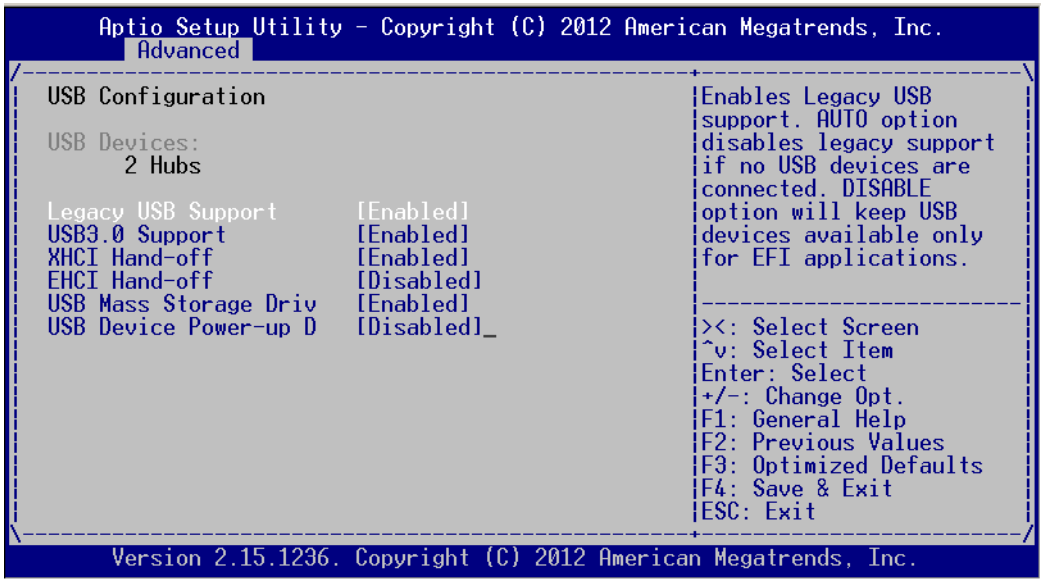


Figure 4.9: USB Configuration

- **Legacy USB Support**

  This item allows users to enable support for traditional USB. It will be automatically set as “Disabled” when no USB device is connected. The default setting is “Enabled”.

- **USB 3.0 Support**

  This item allows users to enable or disable USB 3.0 (XHCI). The default setting is “Enabled”.

- **XHCI Hand-off**

  This item is to enable or disable function of supporting OS without XHCI Hand-off feature. The default setting is “Enabled”.

- **EHCI Hand-off**

  This item is to enable or disable function of supporting OS without EHCI Hand-off feature. The default setting is “Disabled”.

- **USB Mass Storage Driver Support**

  This item allows users to set the specific type of the connected USB device.

- **USB Device Power-up Delay**

  This item allows users to enable or disable the function of USB device reporting max. delay time to host controller. The default setting is “Disabled”.

4.2.2.6 Super I/O Configuration

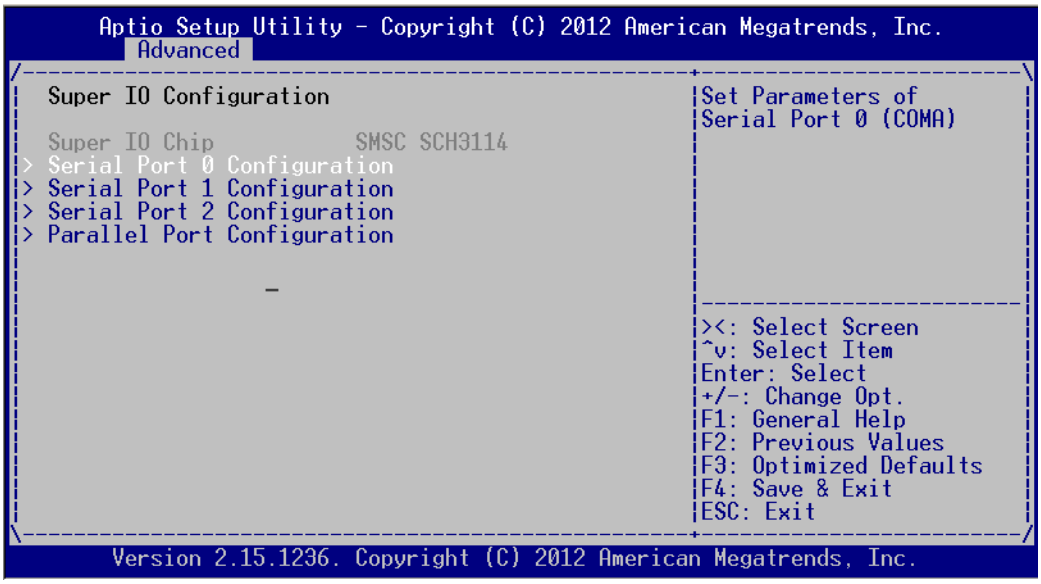


Figure 4.10: Super I/O Configuration

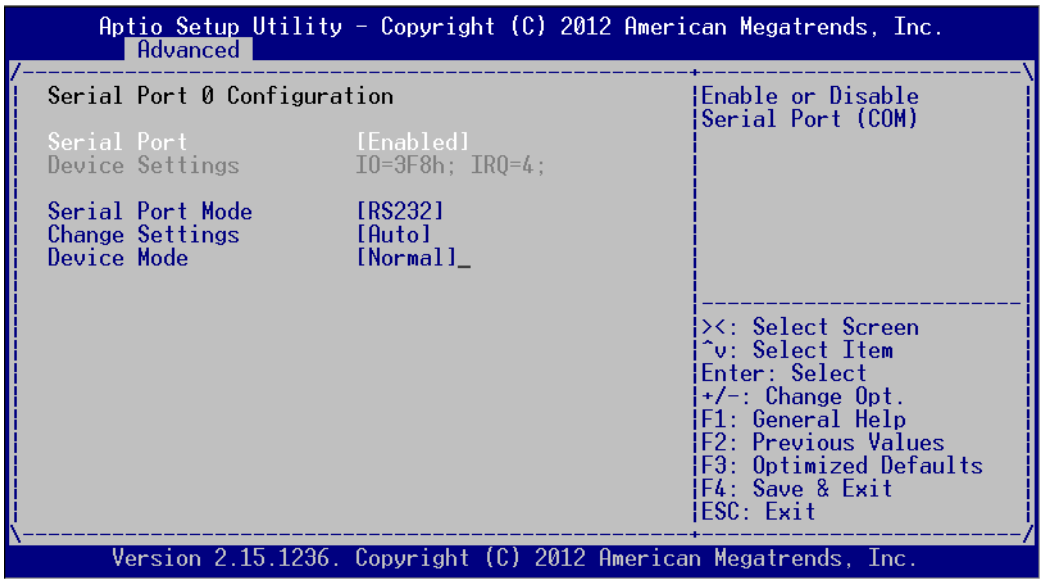


Figure 4.11 Serial Port Configuration

Serial Port 0 Configuration

- **Serial Port**

  This item allows users to open or close serial port. The default setting is “Enabled”.

- **Serial Port Mode**

  This item allows users to set serial port as RS232/422/485. The default setting is “RS232”.

- **Change Settings**

  This item allows user to change settings of serial ports and default setting is "Auto".

  IO=3F8h; IRQ=4;

  IO=3F8h; IRQ=3,4,5,6,7,10,11,12;
  This item allows users to select IO address and IRQ to change serial port settings.

- **Device Mode**

  This item allow users to select device mode. The default setting is “Normal Mode”.

Note!

- *ARK-5420 supports a third RS-232 COM port by cable expansion and it is an optional item.*
- *ARK-5420 supports arallel port by cable expansion and it is another optional item.*

4.2.2.7 Option COM Module

ARK-5420 supports different COM modules, including COM232 module/ITB-112/ITB-114.

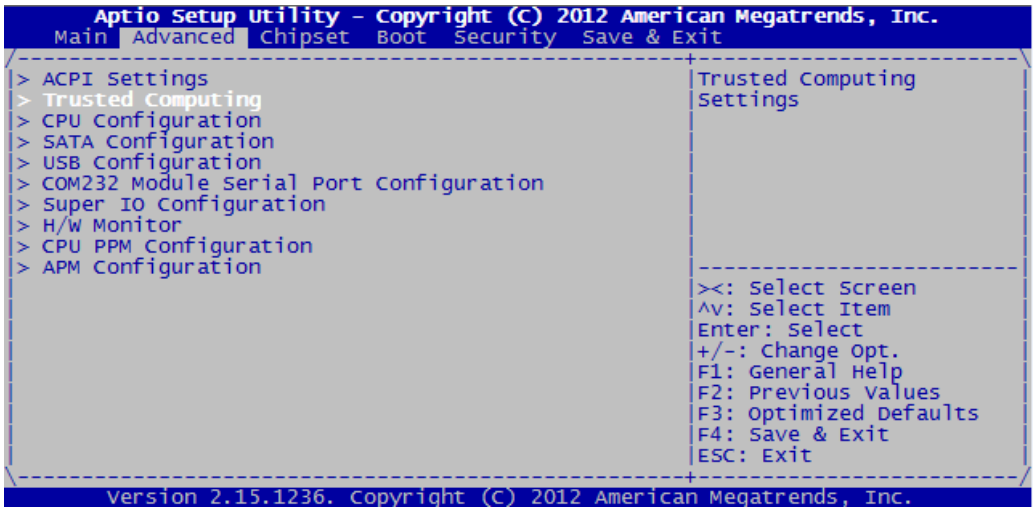
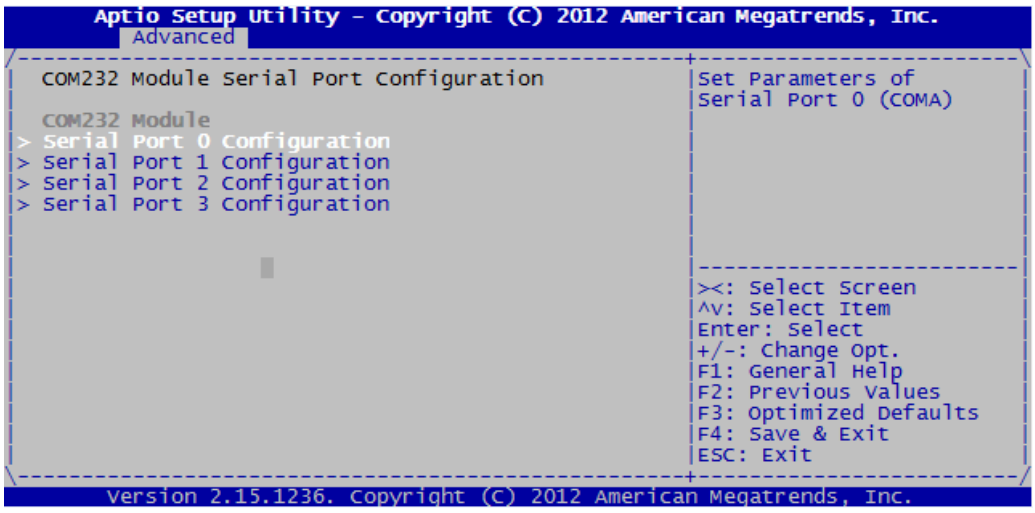
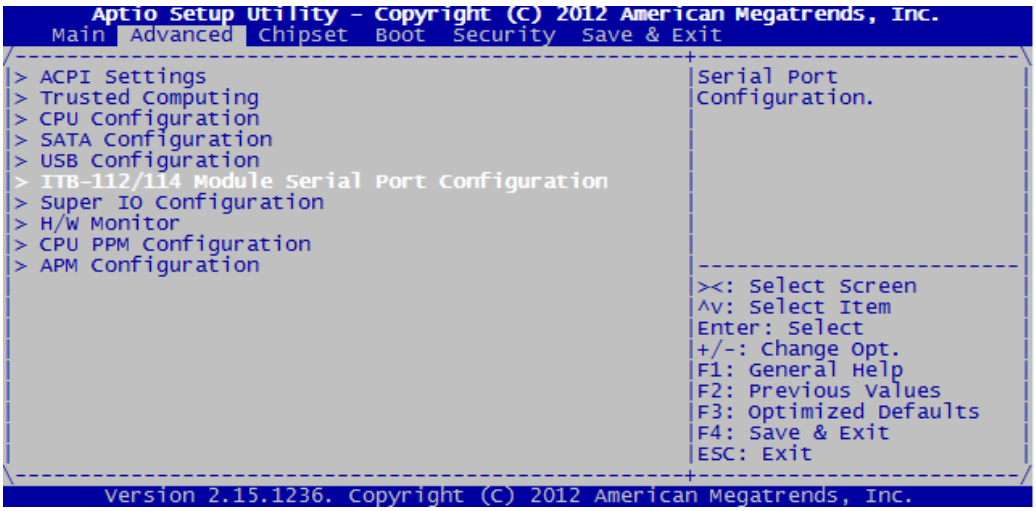


Figure 4.12 COM232 Module Serial Port Configuration

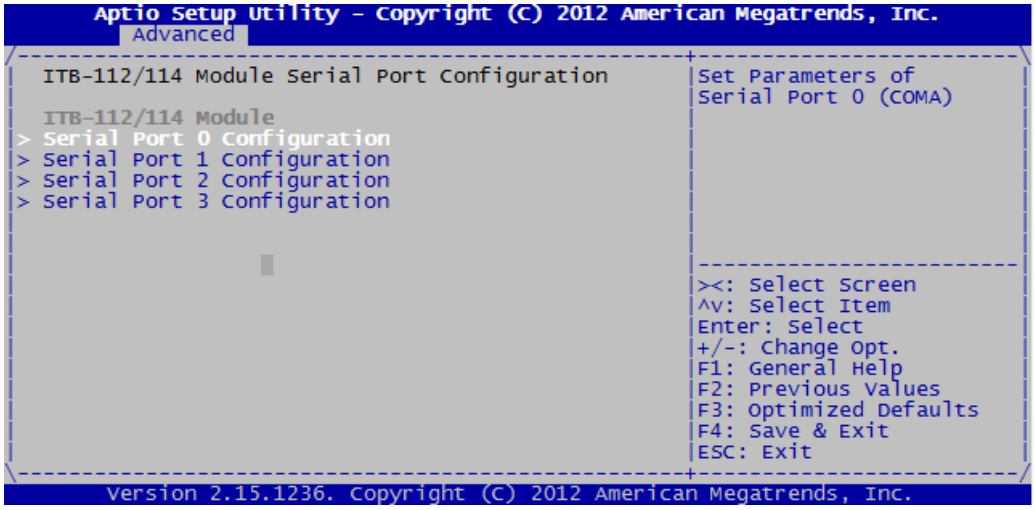
This item only shows when COM232 is assembled into an ARK-5420 system.



These items allows user to set COM232 module.



This item only appears when ITB-112 or ITB-114 assembled into ARK-5420 system.



These items allows user to set up a COM232 model.

4.2.2.8 H/W Monitor

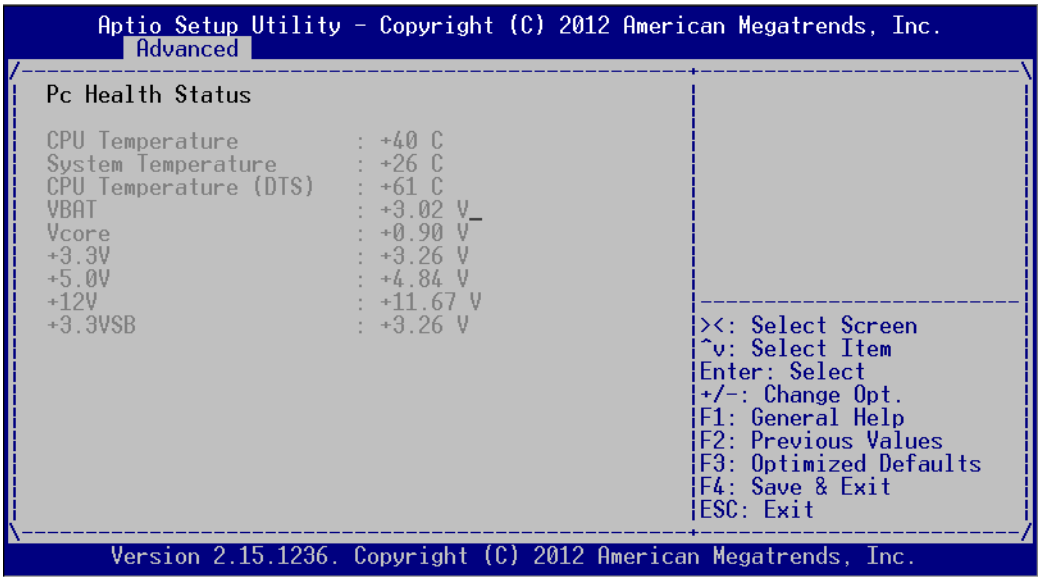


Figure 4.13: H/W Monitor Configuration

- **PC Health Status**

  This item shows hardware conditions. BIOS will display the current system temperature, CPU temperature and other related voltage values. All these parameters have certain healthy ranges; out-of-range operations should be avoided.

4.2.2.9 CPU PPM Configuration

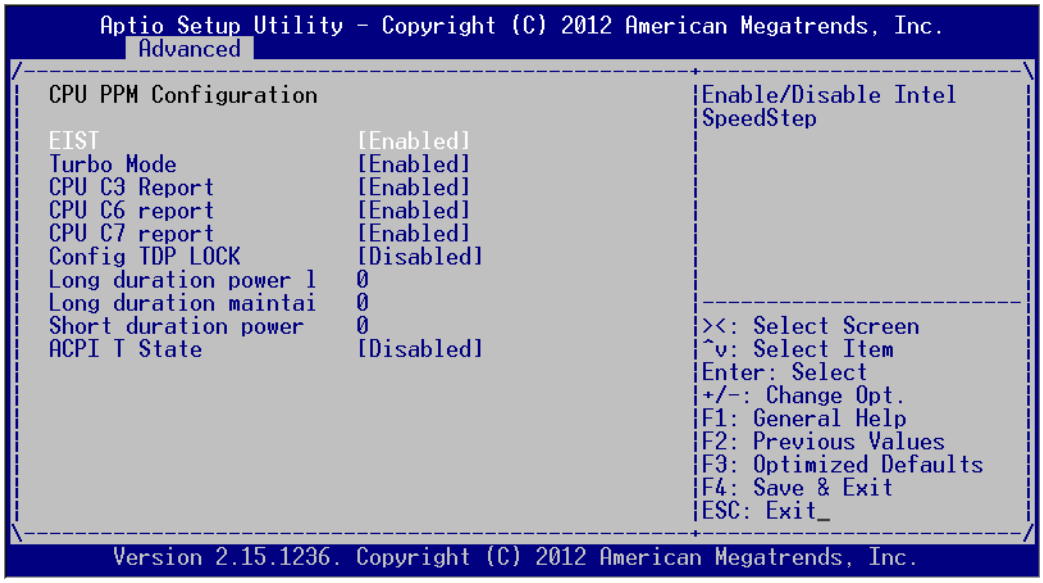


Figure 4.14: CPU PPM Configuration

- **EIST**

  This item is used to set CPU SpeedStep function. The default setting is “Enabled”.

- **Turbo Mode**

  This item is used to set CPU Turbo mode function. The default setting is “Enabled”.

- **CPU C3/C6/7 Report**

  This item is used to set CPU C-state function. The default setting is “Enabled”.

- **Config TDP LOCK**

  This item is used to set Config TDP LOCK function. The default setting is “Disabled”.

- **ACPI T State**

  This item is used to set ACPI T State function. The default setting is “Disabled”.

4.2.2.10 APM Configuration

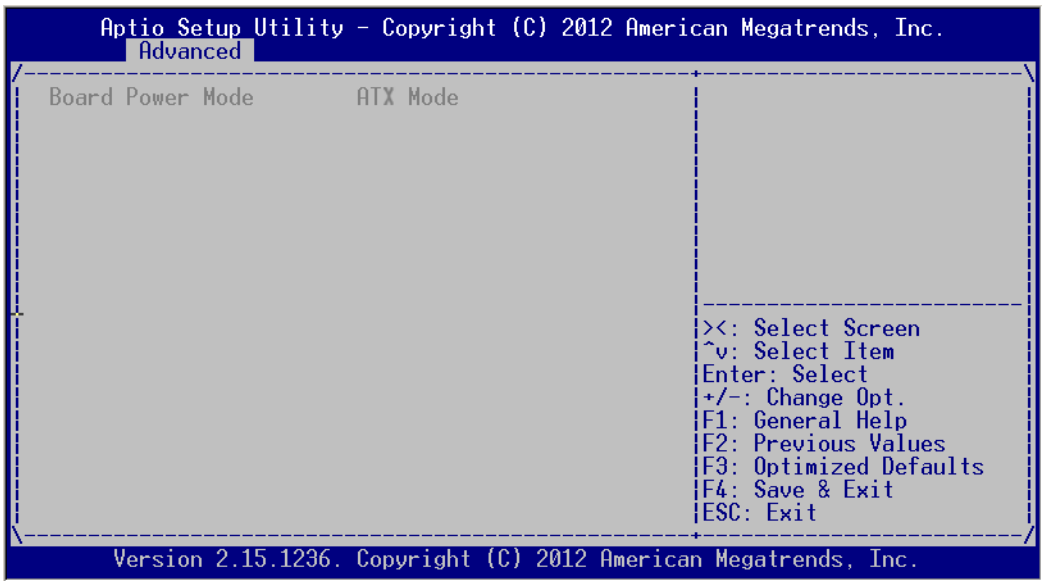


Figure 4.15: APM Configuration

- **Board Power Mode**
  This item is used to set power on mode: either AT or ATX.

4.2.3 Advanced Chipset Features Setup

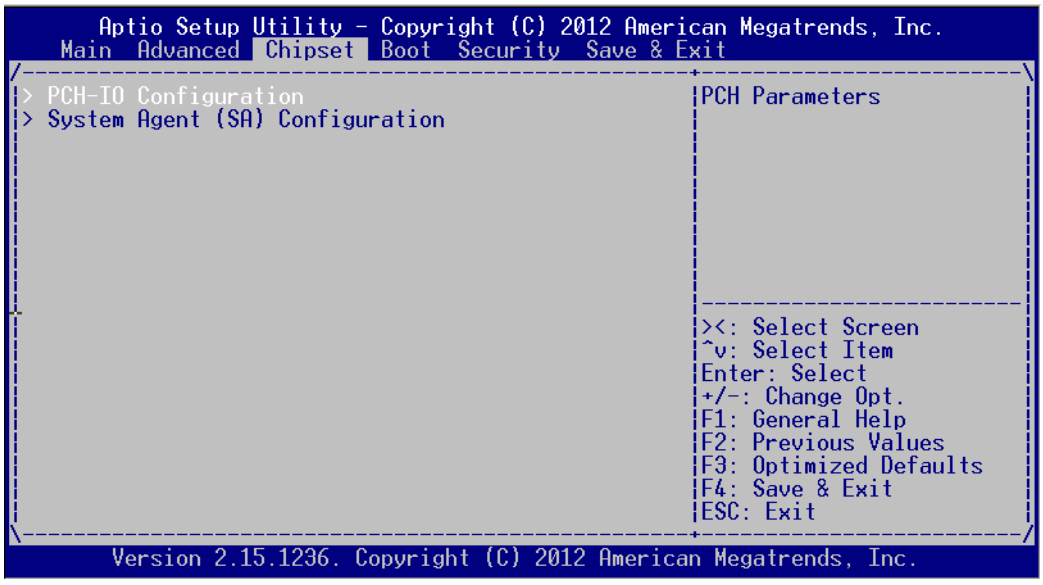


Figure 4.16 Advanced Chipset Features Setup

4.2.3.1 PCH-IO Configuration

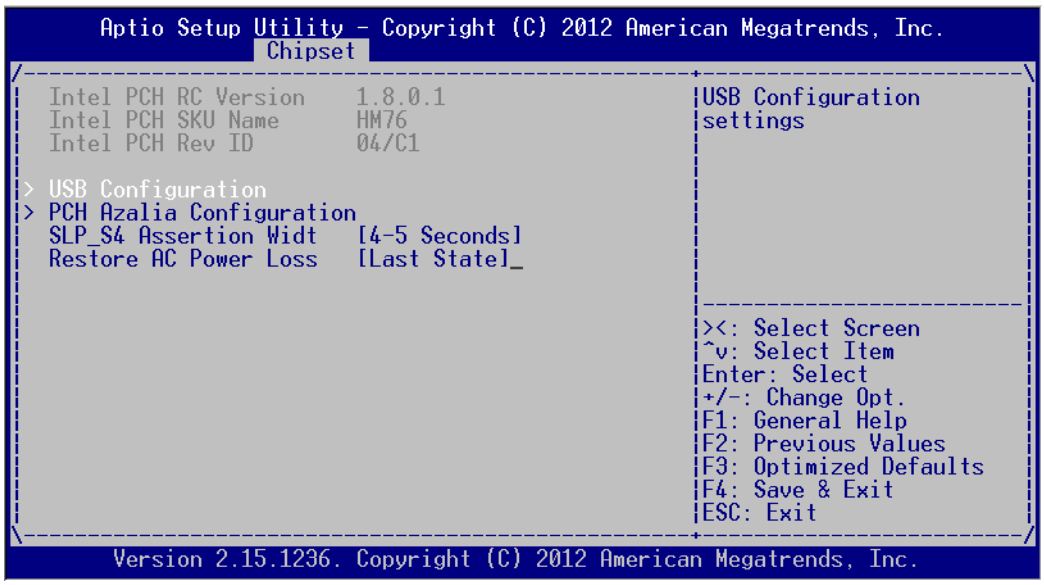


Figure 4.17 PCH-IO Configuration

- **SLP_S4 Assertion Width**
  This item is used to set the min. delay of SLP_S4# signal when booting. The default setting is “4-5 Seconds”.
- **Restore AC Power Loss**
  This item is used to set power status when mains power comes back on.
  Power Off: Power button should be pressed after the power comes on.
  Power On: No action required after the power comes on.
  Last State: Resume last state before the power went off.

- **USB Configuration**

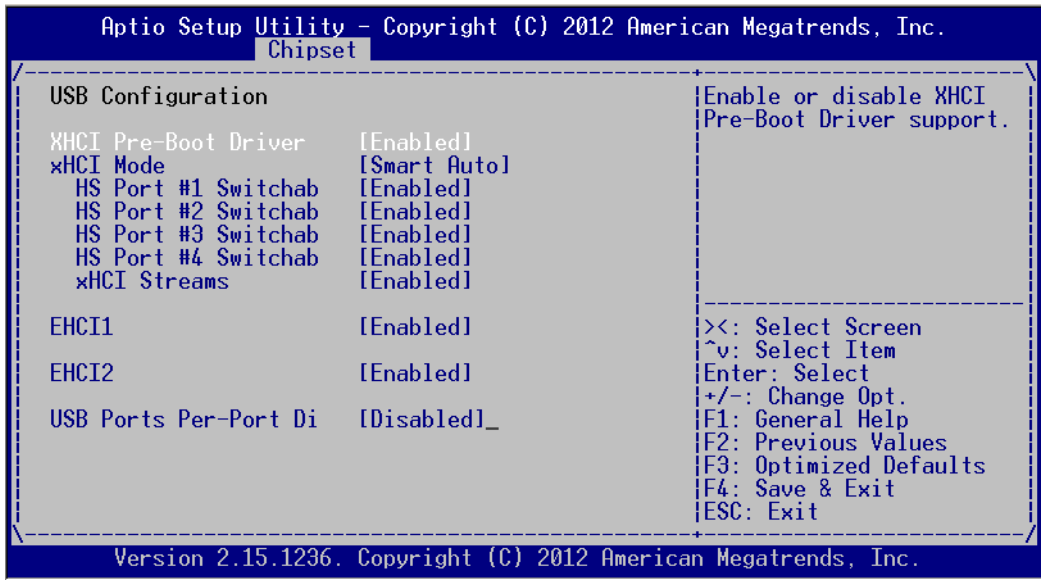


Figure 4.18 Chipset USB Configuration

  - **XHCI Pre-Boot Driver**
    This item allows users to enable or disable XHCI Pre-Boot Driver. The default setting is “Enabled”.

– **xHCI Mode**
This item is used to select xHCI controller mode. The default setting is “Smart Auto”.
– **HS Port #1/#2/#3/#4 Switchable**
Enable: BIOS will let the port connect to EHCI; Disable: BIOS will let the port connect to xHCI. The default setting is “Enable”.
– **xHCI Streams**
This item allows users to enable or disable xHCI Maximum Primary Stream Array Size.
– **EHCI1/EHCI2**
This item allows users to enable or disable EHCI #1/EHCI #2. The default setting is “Enable”.
– **USB Ports Per-Port Disable Control**
This item is used to set disable control of each USB connector.

■ PCH Azalia Configuration

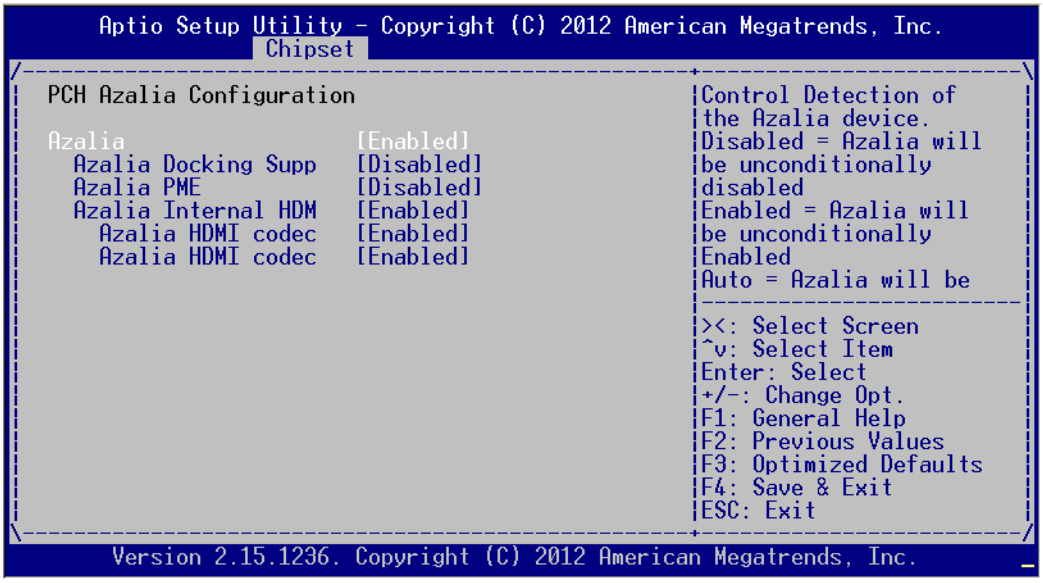


Figure 4.19 PCH Azalia Configuration

– **Azalia**
This item is used to detect any Azalia device. The default setting is “Enable”.
Disabled: Azalia will be unconditionally disabled.
Enabled: Azalia will be unconditionally Enabled.
Auto: Azalia will be enabled if present, disabled otherwise.

4.2.3.2 System Agent (SA) Configuration

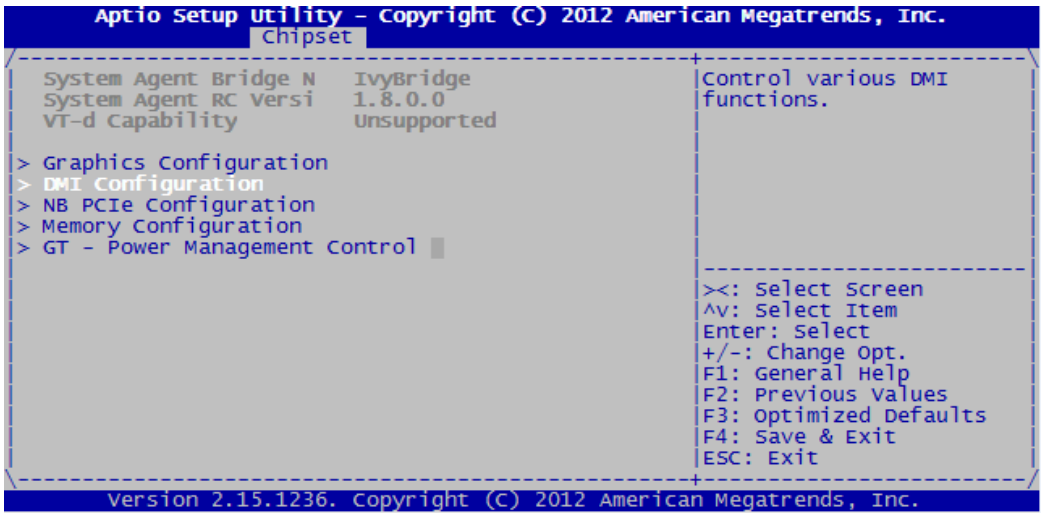


Figure 4.20: System Agent (SA) Configuration

- **Graphics Configuration**

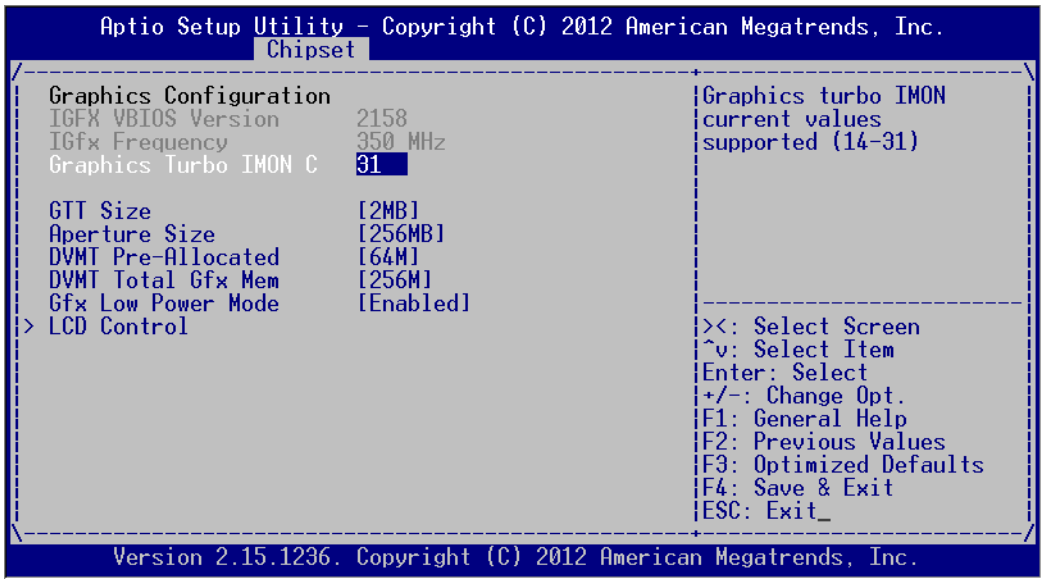


Figure 4.21 Graphics Configuration Menu

- **Graphics Turbo IMON Current**
  Graphics turbo IMON current values supported (14-31).
- **GTT Size**
  This item is used to select GTT size.
- **DVMT Total Gfx Mem**
  This item allows users to select memory size of DVMT Total.
- **Gfx Low Power Mode**
  This item allows users to enable of disable Low Power mode.

– **LCD Control**

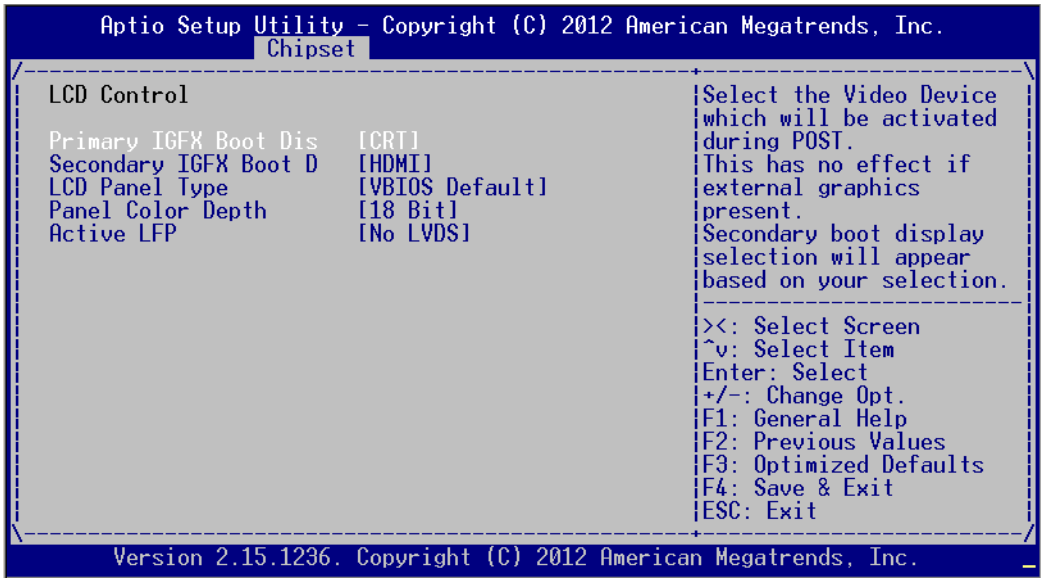


Figure 4.22 LCD Control

4.2.3.3 DMI Configuration

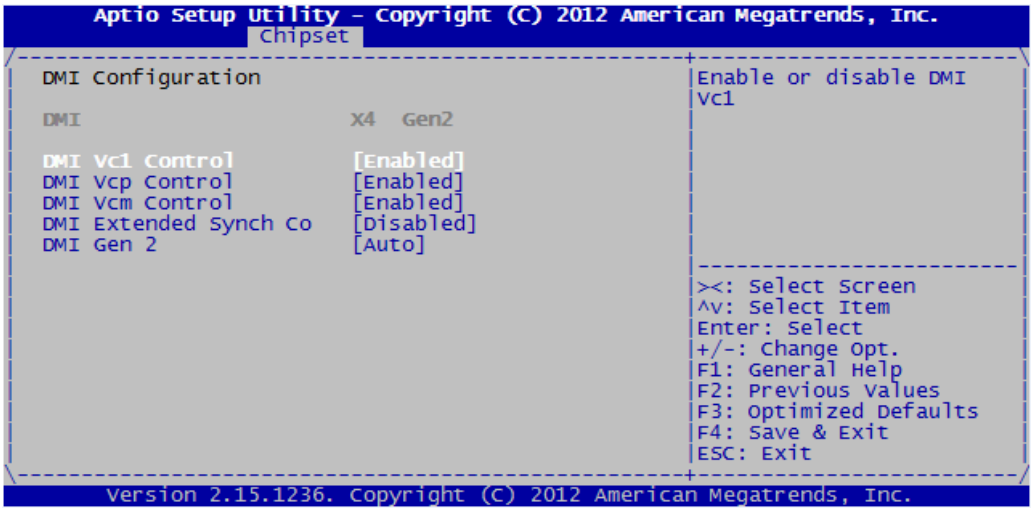


Figure 4.23 DMI Configuration

- **DMI Vc1 Control**
  This item is used to set DMI Vc1 control and Default setting is "Enabled".
- **DMI Vcp Control**
  This item is used to set DMI Vcp control and Default setting is "Enabled".
- **DMI Vcm Control**
  This item is used to set DMI Vcm control and Default setting is "Enabled".
- **DMI Extended Synch Control**
  This item is used to set DMI Extended Synch control and default setting is "Disabled".
- **DMI Gen2**
  This item is used to set DMI Gen2. This item can be setting at "Auto", “Enabled” and "Disabled". The default setting is "Auto".

4.2.3.4 NB PCIe Configuration

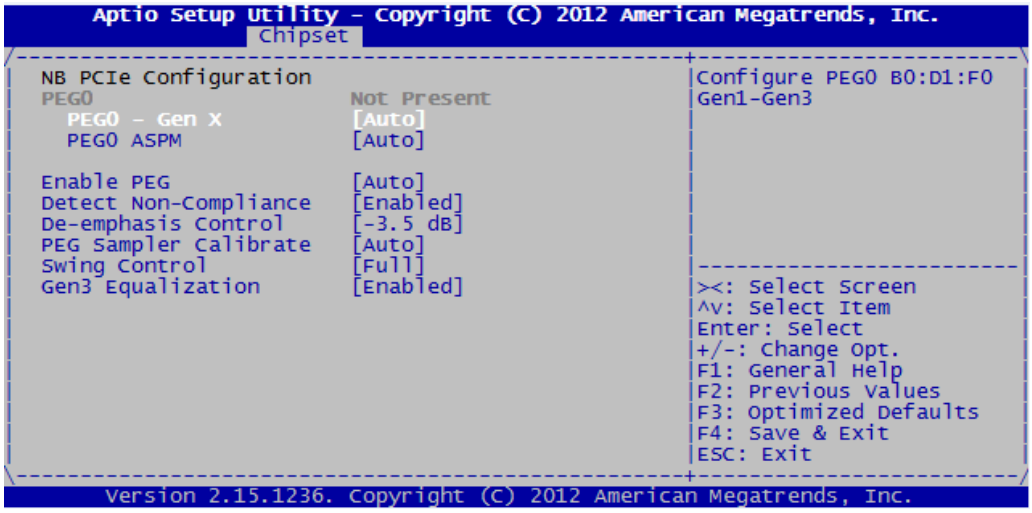


Figure 4.24 NB PCIe Configuration

- **PEGO - Gen X**

  This item is used to set PCIe Gen function level and default setting is "Auto". The user can setting "Gen1", "Gen2" or "Gen3".

- **PEGO ASPM**

  This item is used to set PEGO ASPM function and default setting is "Auto". The user can setting "Disabled", "ASPM L0s", "ASPM L1", "ASPM L0sL1".

- **Enable PEG**

  This item is used to set PEG function and default setting is "Auto".

- **Detect Non-Compliance Device**

  This item is used to set system to detect Non-compliance device and default setting is "Enabled".

- **De-emphasis Control**

  This item is used to set different De-emphasis values and default setting is "-3.5dB".

- **PEG sampler Calibrate**

  This item is used to set PEG sampler Calibrate and default setting is "Auto".

- **Swing Control**

  This item is used to set Swing control and default setting is "Full". The user also can set "Reduced" or "Half" mode.

- **Gen3 Equalization**

  This item is used to set Gen3 Equalization function and default is “Enabled”.

4.2.3.5 Memory Information

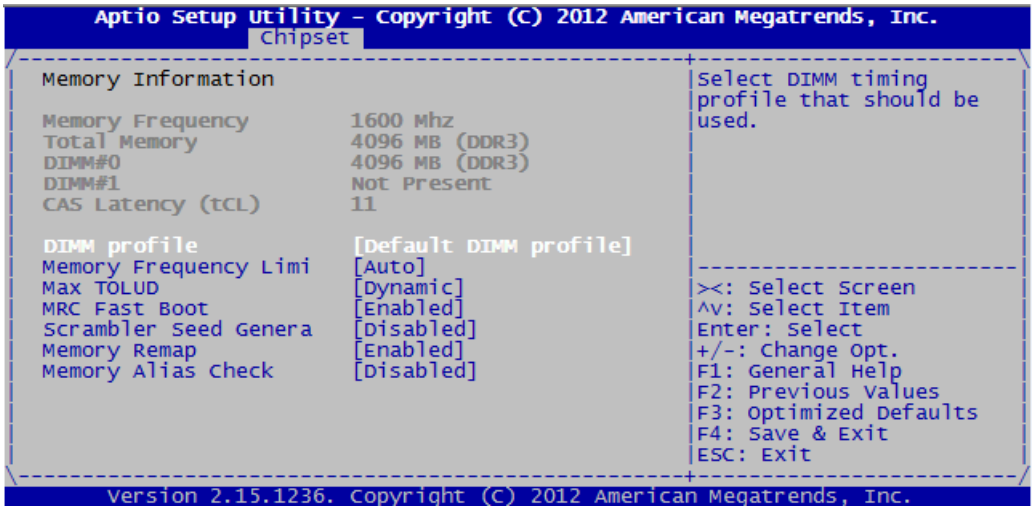


Figure 4.25 Memory Information

- **DIMM profile**
  This item is used to set the DIMM profile.
- **Memory Frequency Limiter**
  This item is used to set Memory Frequency Limiter and default setting is "Auto".
- **Max TOLUD**
  This item is used to set Memory Max TOLUD and default setting is "Dynamic".
- **MRC Fast Boot**
  This item is used to set MRC Fast Boot.
- **Scrambler Seed Generation off**
  This item is used to set Scrambler Seed Generation Off and default setting is "Disabled".
- **Memory Remap**
  This item is used to set memory remap.
- **Memory Alias Check**
  This item is used to set "Memory alias Check" function and default is "Disabled".

4.2.3.6 GT- Power Management Control

- **RC6 (Render Standby)**
  This item is used to set RC6 (Render Standby) function and default setting is "Enabled".
- **RC6+(Deep RC6)**
  This item is used to set RC6+ (Deep RC6) function and default setting is "Enabled".
- **GT Over Clocking Support**
  This item is used to set GT OverClocking support function and default is "Disabled".

4.2.4 Boot Setup

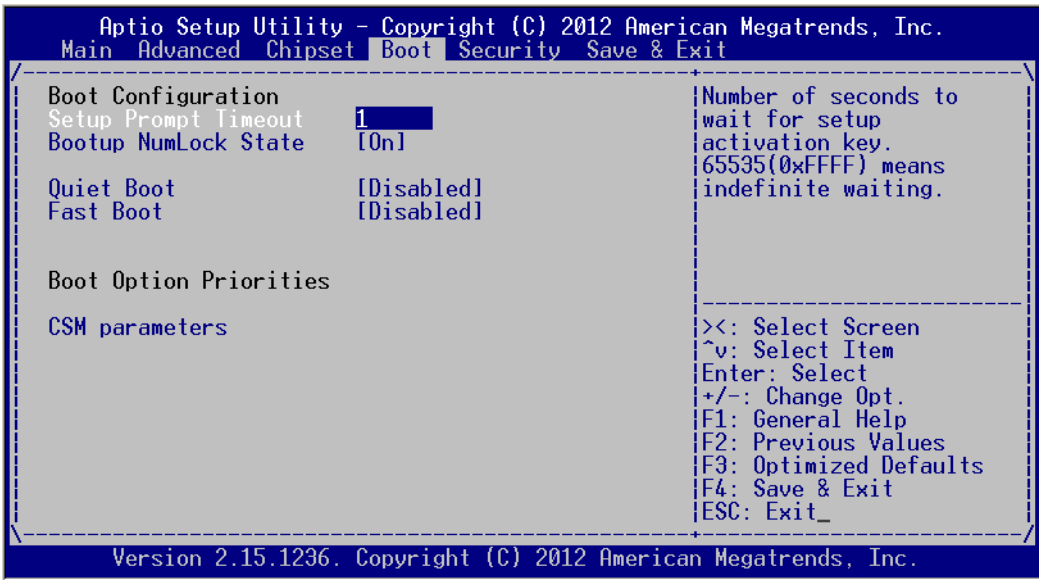


Figure 4.26: Boot Setup

4.2.4.1 Boot Configuration

- **Setup Prompt Timeout**
  This item is the waiting time of pressing Setup button. If Setup button is not pressed within the setting time, system will continue to boot.
- **Bootup NumLock State**
  This item allows users to active Bootup NumLock State function after the system is power on to DOS. The default setting is “On”.
  On: NumLock function is on when system boots.
  Off: Keypad is set for cursor control arrows when system boots.
- **Quiet Boot**
  If set to “Disabled”, BIOS will display normal POST information; if set to “Enabled”, BIOS will show OEM icon rather than POST information.
- **Fast Boot**
  This item allows BIOS to skip some testing procedures during booting so as to reduce system boot-up time. The default setting is “Disabled”.

4.2.4.2 Boot Option Priorities

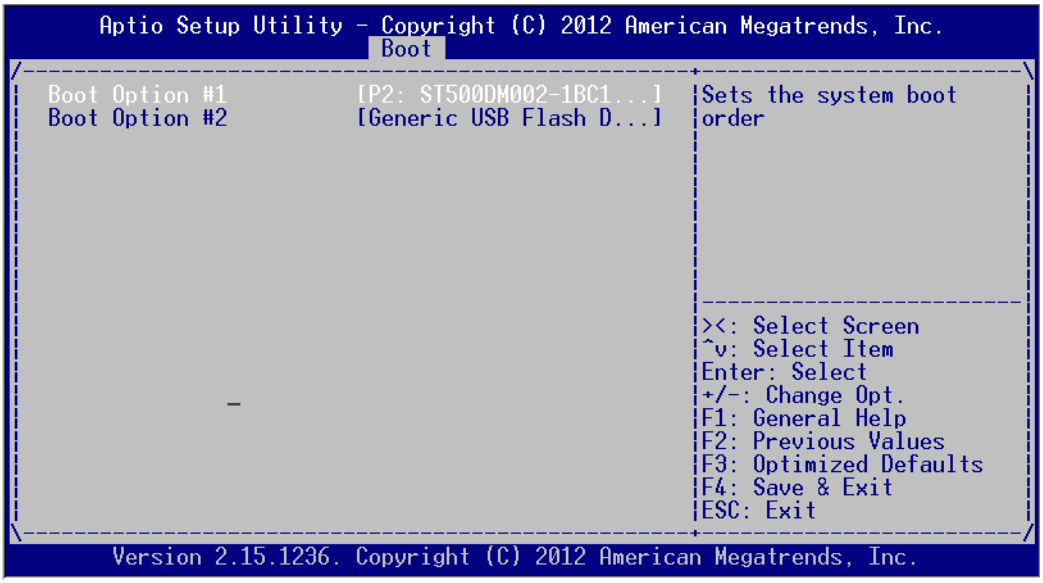


Figure 4.27 Boot Option Priorities

This item is used to set device boot sequence.

4.2.4.3 CSM Parameter

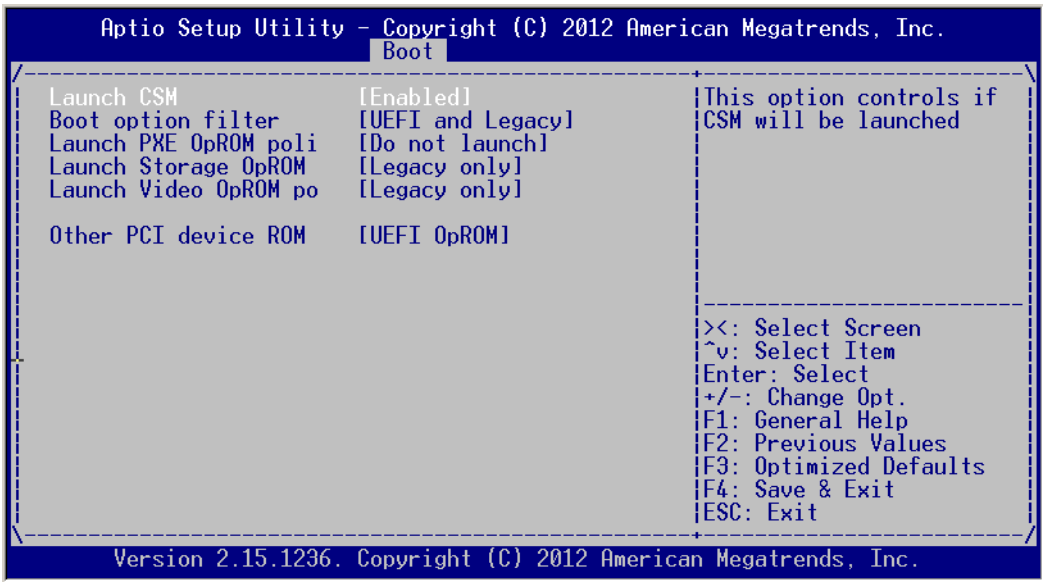


Figure 4.28: CSM Parameter

- **Launch CSM**
  This item allows user to enable or disable CSM. The default setting is “Enabled”.
- **Boot option filter**
  This item is used to control boot device system. The default setting is “UEFI and Legacy”.
- **Launch PXE OpROM policy**
  This item is used to control UEFI execution and backward compatibility of PXE OpROM. The default setting is “Do not Launch”.
- **Launch Storage OpROM policy**
  This item is used to control UEFI execution and backward compatibility of PXE OpROM. The default setting is ““Legacy only”.

- **Launch Video OpROM policy**
  This item is used to control UEFI execution and backward compatibility of PXE OpROM. The default setting is ““Legacy only”.
- **Other PCI device ROM priority**
  This item is used for PCI device that is not the same as network, which is defined by massive storage or video booted by OpROM.

4.2.5 Security Setup

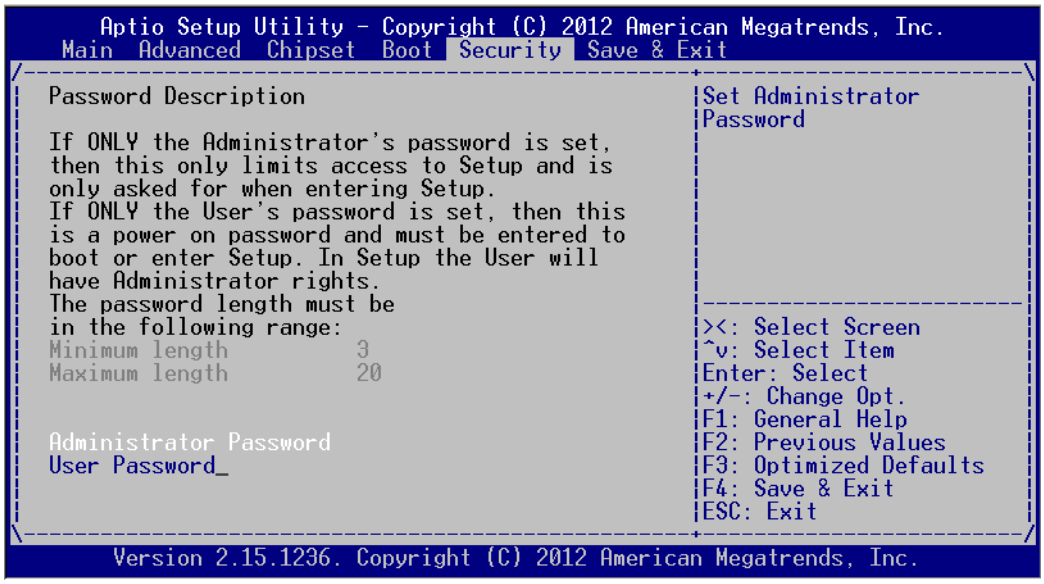


Figure 4.29: Setup Security Menu

- **Administrator Password**
  This item is used to set Administrator Password.
- **User Password**
  This item is used to set User Password.

4.2.6 Save & Exit Setup

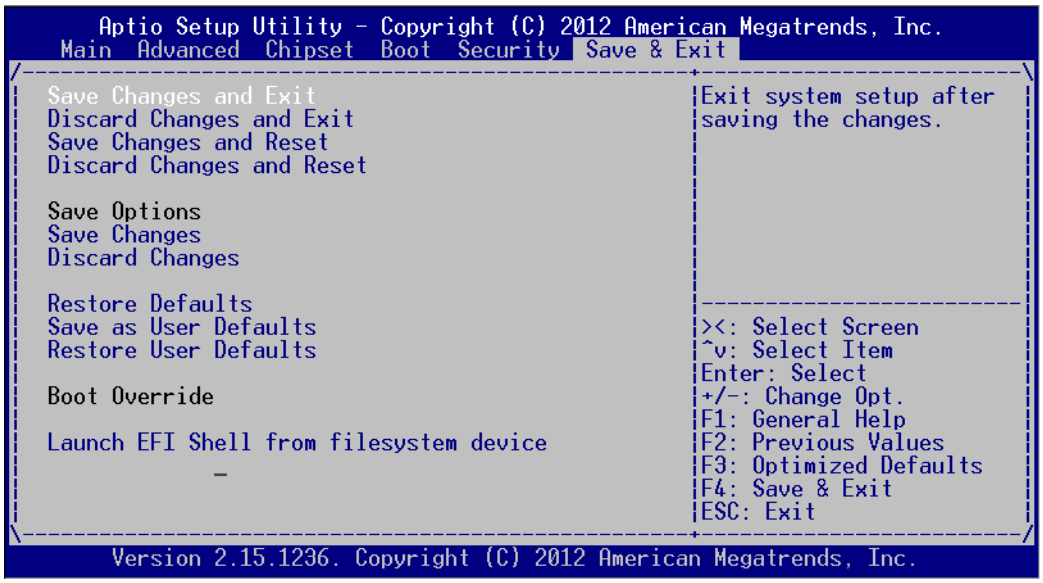


Figure 4.30: Setup Save & Exit Menu

- **Save Changes and Exit**
  When you have completed system configuration, select this option to save your changes, exit BIOS setup and reboot the computer so the new system configuration parameters can take effect.
  1. Select Save Changes and Exit from the Exit menu and press <Enter>. The following message appears:
     Save Configuration Changes and Exit Now?
     [Ok] [Cancel]
  2. Select Ok or Cancel.

- **Discard Changes and Exit**
  Select this option to quit Setup without making any permanent changes to the system configuration.
  1. Select Exit Discard Changes and Exit from the Exit menu and press <Enter>. The following message appears:
     Discard Changes and Exit Setup Now?
     [Ok] [Cancel]
  2. Select Ok to discard changes and exit.

- **Save Changes and Reset**
  When you have completed system configuration, select this option to save your changes, exit BIOS setup and reboot the computer so the new system configuration parameters can take effect.
  1. Select Save Changes and Reset and press <Enter>. The following message appears:
     Save configuration and Reset?
     [Yes] [No]
  2. Select Ok or Cancel.

- **Discard Changes and Reset**
  Select this option to quit Setup without making any permanent changes to the system configuration.
  1. Select Discard Changes and Reset from the Exit menu and press <Enter>.
     The following message appears:
     Discard Changes and Reset Setup Now?
     [Ok] [Cancel]
  2. Select Ok to discard changes and exit.
- **Save Changes**
  This item allows users to save changes done so far to any of the options.
- **Discard Changes**
  This item allows users to discard changes done so far to any of the options.
- **Restore Defaults**
  This item allows users to restore/load default values for all the options.
- **Save as User Defaults**
  This item allows users to save the changes done so far as user defaults.
- **Restore User Defaults**
  This item allows users to restore the user defaults to all the options.
- **Boot Override**
  This item allows users to set boot device.
- **Launch EFI Shell from file system device**
  This item allows booting of EFI shell from system file device.

s

Chapter 5

Driver Installation

Sections include:

- Chipset Windows Driver Setup
- VGA Windows Driver Setup
- ME Windows Driver Setup
- LAN Windows Driver Setup
- USB 3.0 Windows Driver Setup
- Audio Windows Driver Setup

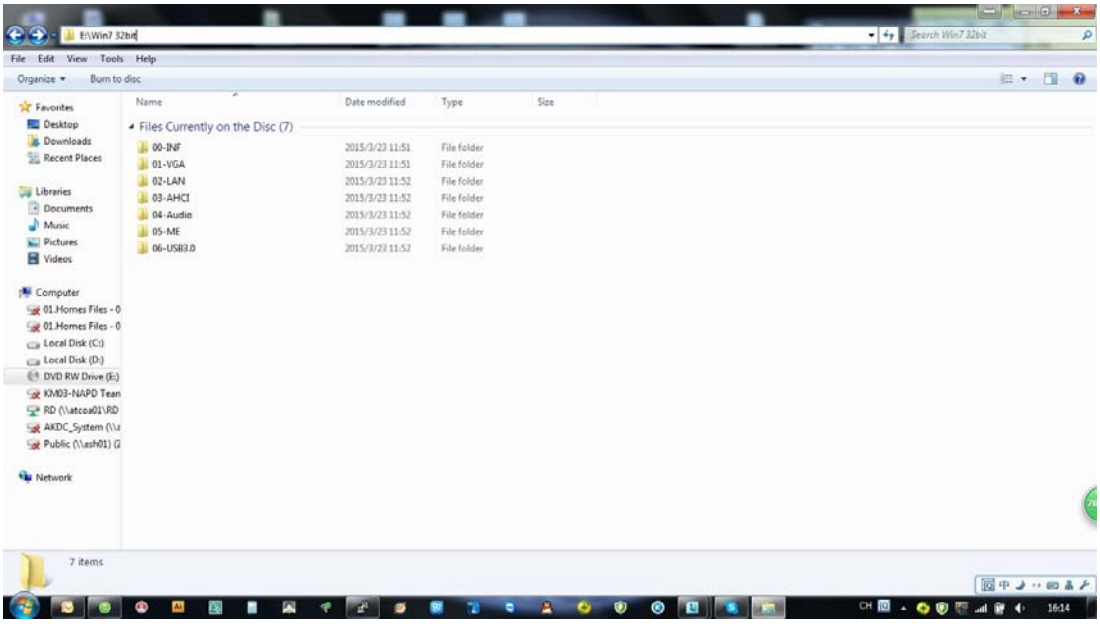
5.1 Introduction

Advantech offers a complete range of Device Driver and software supports for Windows programming developers. You can apply the Windows Device Drivers to the most popular Windows Programming tools, such as Visual C++, Visual Basic, Borland C++ Builder and Borland Delphi.

Here Windows 7 is taken as an example.

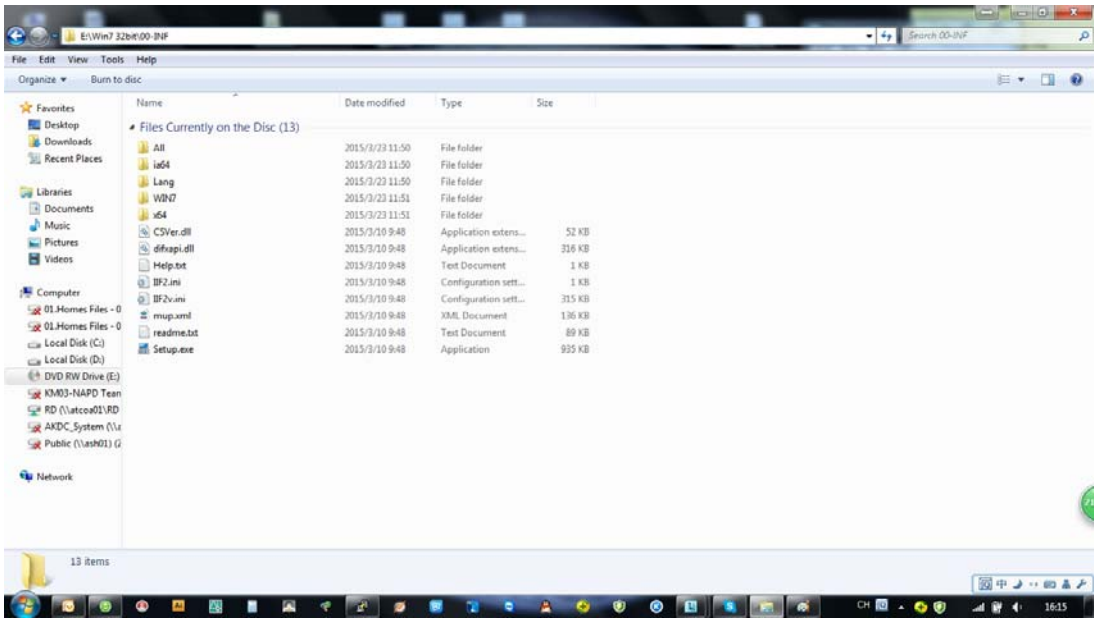
5.2 Driver Installation

Insert the driver CD into your system's CD-ROM drive. You can see the ITA-5730 driver folder items.



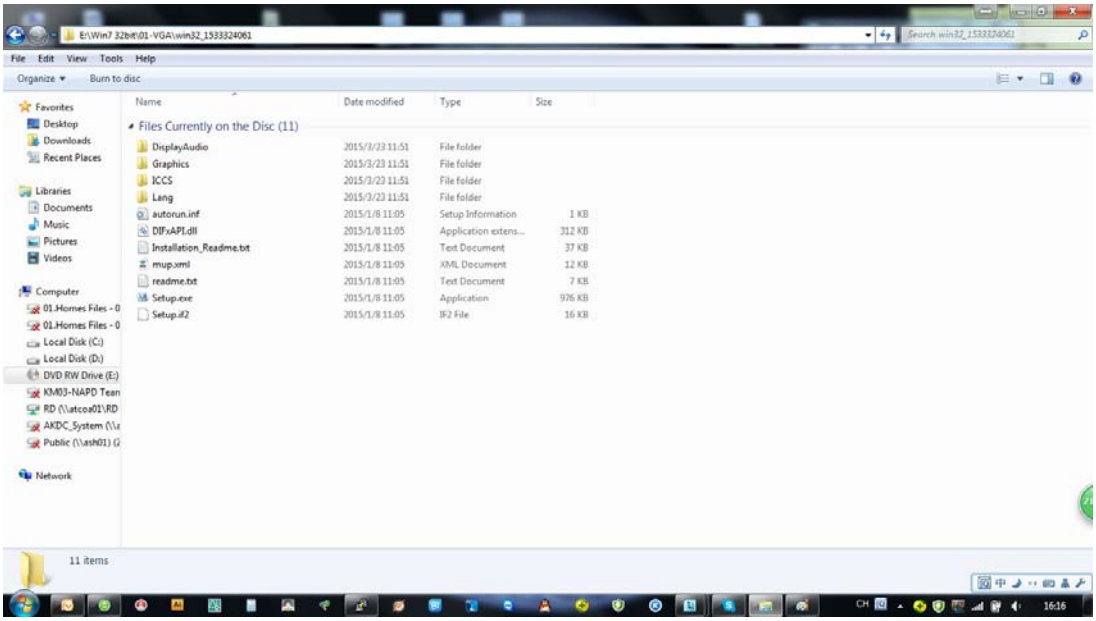
5.2.1 Chipset Windows Driver Setup

Insert the driver CD into your system's CD-ROM drive. You can see the driver folder items. Navigate to the "Drv_01Chipset" folder and click "Setup" to complete the installation of the driver.



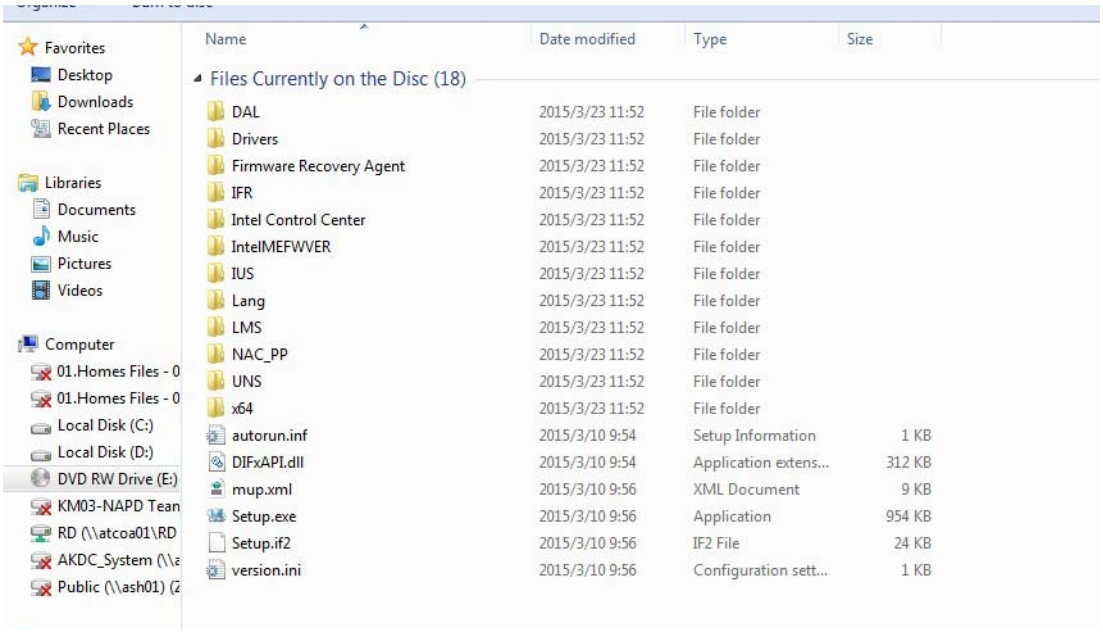
5.2.2 VGA Windows Driver Setup

Insert the driver CD into your system's CD-ROM drive. You can see the driver folder items. Navigate to the "Drv_02VGA" folder and click "Setup" to complete the installation of the drivers.



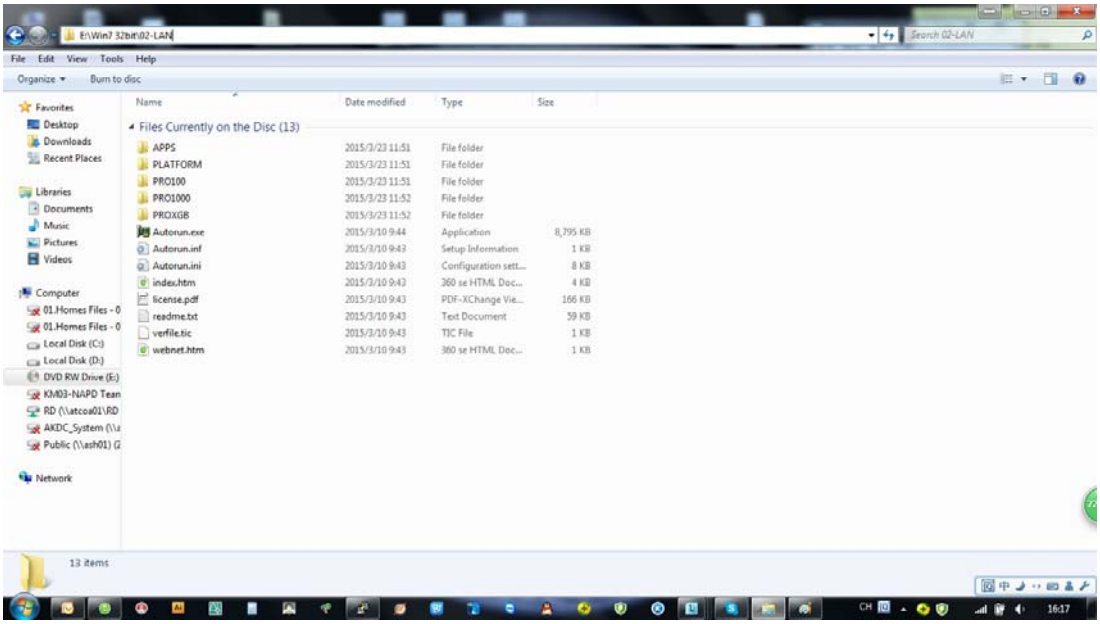
5.2.3 ME Windows Driver Setup

Insert the driver CD into your system's CD-ROM drive. You can see the driver folder items. Navigate to the "Drv_03ME" folder and click "Setup" to complete the installation of the drivers.



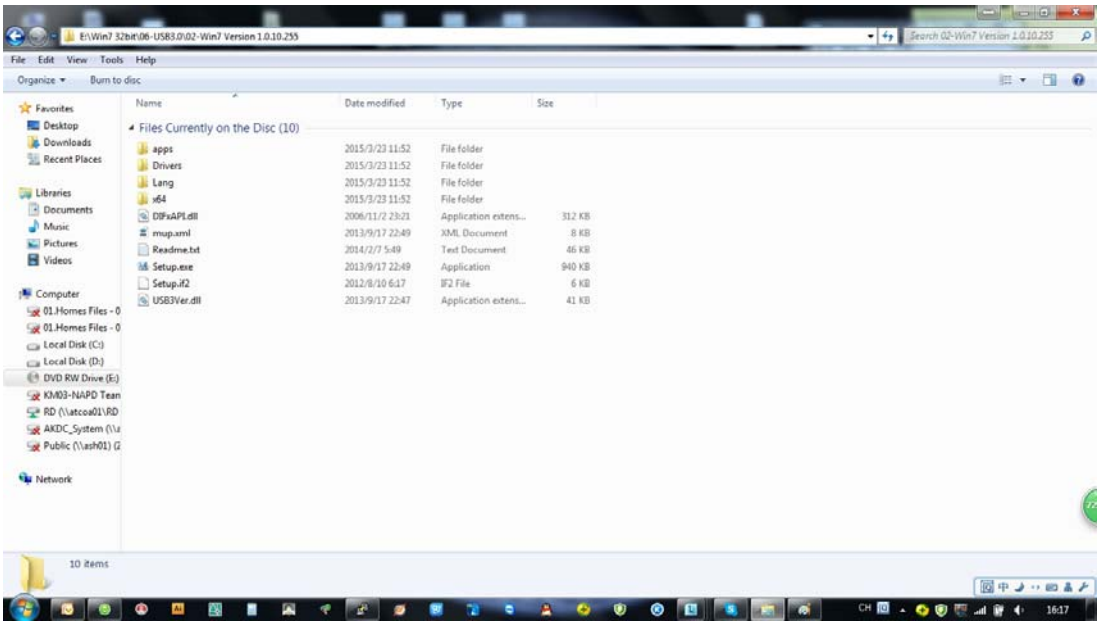
5.2.4 LAN Windows Driver Setup

Insert the driver CD into your system's CD-ROM drive. You can see the driver folder items. Navigate to the "Drv_04LAN" folder and click "Autorun" to complete the installation of the drivers.



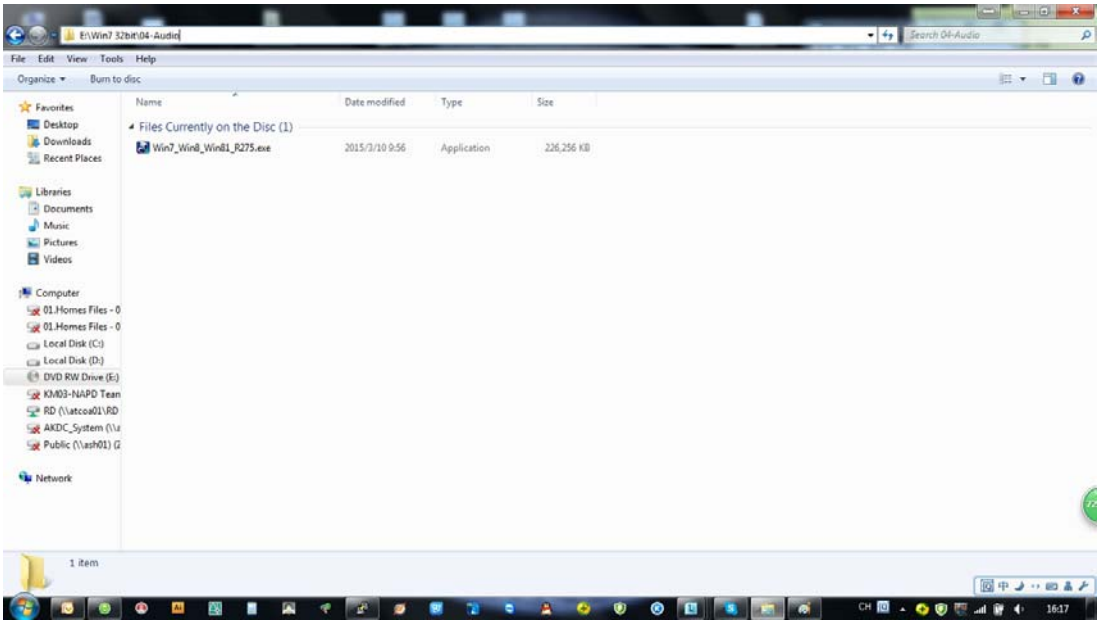
5.2.5 USB 3.0 Windows Driver Setup

Insert the driver CD into your system's CD-ROM drive. You can see the driver folders items. Navigate to the "Drv_05USB3.0" folder, and click "Setup" to complete the installation of the drivers.



5.2.6 Audio Windows Driver Installation

Insert the driver CD into your system's CD-ROM drive. You can see the driver folders items. Navigate to the "Drv_ 06AUDIO"" folder and click "WDM_R264.exe" to complete the installation of the drivers.



Chapter 6

GPIO Programming

This chapter introduces GPIO programming Guide.

Please carefully read and study the below screenshots and source codes in blue. Please download programming specifications for the PCA955 NXP semiconductor.

6.1 ARK-5420 Digital DIO Definition

See Section 2.3.6.

6.2 Configuration Sequence

ARK-5420's GPIO is realized through PCA9554 GPIO IC connected to ICH SMBUS. Therefore, the configuration and access to GPIO IC is completed by IO Space accessing ICH SMBUS controller.

Below is the diagram of ICH SMBUS IO Space:

SMB_BASE + Offset	Mnemonic	Register Name	Default	Type
00h	HST_STS	Host Status	00h	R/WC, RO, R/WC (special)
02h	HST_CNT	Host Control	00h	R/W, WO R/W
03h	HST_CMD	Host Command	00h	R/W
04h	XMIT_SLVA	Transmit Slave Address	00h	R/W
05h	HST_D0	Host Data 0	00h	R/W
06h	HST_D1	Host Data 1	00h	R/W

For ARK-5420, IO address of the above SMB_BASE is 0xF040.

The detailed SMBUS IO control access code, please refer to Chapter 3.

The corresponding SMBUS slave address of PCA9554 of GPIO 00 - GPIO 07 on ARK-5420 is 0x40 (8bit address):

GPIO 00 – GPIO 07: PCA9554 0x40 (IO0 – IO7)

Below are pinouts for PCA9554:

Table 6.1: Pin Description

Symbol	Pin			Description
	DIP16, SO16, SSOP16, TSSOP16	HVQFN16	SSOP20	
A0	1	15	6	address input 0
A1	2	16	7	address input 1
A2	3	1	9	address input 2
IO0	4	2	10	input/output 0
IO1	5	3	11	input/output 1
IO2	6	4	12	input/output 2
IO3	7	5	14	input/output 3
Vss	8	6	15	supply ground
IO4	9	7	16	input/output 4
IO5	10	8	17	input/output 5
IO6	11	9	19	input/output 6
IO7	12	10	20	input/output 7
INT	13	11	1	interrupt output (open-drain)

Below is the diagram of PCA9554 register:

Table 6.2: Command Byte

Command	Protocol	**Function**
0	read byte	Input Port register
1	read/write byte	Output Port register
2	read/write byte	Polarity Inversion register
3	read/write byte	Configuration register

The command byte is the first byte to follow the address byte during a write transmission. It is used as a pointer to determine which of the following registers will be written or read.

PCA9554 has in all 4 registers to control GPIO.

Register 0 - Input Port register

This register is a read-only port. It reflects the incoming logic levels of the pins, regardless of whether the pin is defined as an input or an output by Register 3. Writes to this register have no effect.

The default 'X' is determined by the externally applied logic level, normally '1' when no external signal externally applied because of the internal pull-up resistors.

Table 6.3: Register 0 - Input Port Register Bit Description

Bit	Symbol	Access	Value	Description
7	I7	read only	X	determined by externally applied logic level
6	I6	read only	X	
5	I5	read only	X	
4	I4	read only	X	
3	I3	read only	X	
2	I2	read only	X	
1	I1	read only	X	
0	I0	read only	X	

If one GPIO Pin is set to Input, you can read input value from the bit that register 0 corresponds to.

Register 1 - Output Port register

This register reflects the outgoing logic levels of the pins defined as outputs by Register 3. Bit values in this register have no effect on pins defined as inputs. Reads from this register return the value that is in the flip-flop controlling the output selection, **not** the actual pin value.

Table 6.4: Register 1 - Output Port Register Bit Description

Bit	Symbol	Access	Value	Description
7	O7	R	1*	reflects outgoing logic levels of pins defined as outputs by Register 3
6	O6	R	1*	
5	O5	R	1*	
4	O4	R	1*	
3	O3	R	1*	
2	O2	R	1*	
1	O1	R	1*	
0	O0	R	1*	

If one GPIO Pin is set to Output, you can read input value from the bit that register 1 corresponds to.

Register 2 - Polarity Inversion register

This register allows the user to invert the polarity of the Input Port register data. If a bit in this register is set (written with '1'), the corresponding Input Port data is inverted. If a bit in this register is cleared (written with a '0'), the Input Port data polarity is retained.

Table 6.5: Register 2 - Polarity Inversion Register Bit Description

Bit	Symbol	Access	Value	Description
7	N7	R/W	0*	inverts polarity of Input Port register data
6	N6	R/W	0*	0 = Input Port register data retained (default value)
5	N5	R/W	0*	1 = Input Port register data inverted
4	N4	R/W	0*	
3	N3	R/W	0*	
2	N2	R/W	0*	
1	N1	R/W	0*	
0	N2	R/W	0*	

If one GPIO Pin is set to Input, you can control the polarity of input pin from the bit that register 2 corresponds to.

Register 3 - Configuration register

This register configures the directions of the I/O pins. If a bit in this register is set, the corresponding port pin is enabled as an input with high-impedance output driver. If a bit in this register is cleared, the corresponding port pin is enabled as an output. At reset, the I/Os are configured as inputs with a weak pull-up to VDD.

Table 6.6: Register 3 - Configuration Register Bit Description

Bit	Symbol	Access	Value	Description
7	C7	R/W	1*	configures the directions of the I/O pins
6	C6	R/W	1*	0 = corresponding port pin enabled as an output
5	C5	R/W	1*	1 = corresponding port pin configured as input
4	C4	R/W	1*	
3	C3	R/W	1*	
2	C2	R/W	1*	
1	C1	R/W	1*	
1	C0	R/W	1*	

Register 3 is used to set each GPIO as Input or Output:

If the bit is '0', the corresponding GPIO pin is set as Output; If the bit is '1', the corresponding GPIO pin is set as Input.

Example:

Take ARK-5420 as an example. Assume GPIO 00 is set as Output and GPIO 7 is set as Input, with two pins interconnected, how to set the corresponding register? GPIO 00 corresponds to PCA9554 0x40 IO0, while GPIO 07 corresponds to PCA9554 0x40 IO7.

- **Set GPIO 00 as Output:**

1. Read SMBUS slave 0x40 register 3 byte value;
2. Set bit 0 of the value read in step 1 as 0 and write it to SMBUS slave 0x40 register 3;
3. Read SMBUS slave 0x40 register 1 byte value;
4. Set bit 0 of the value read in step 3 as 0 or 1 according to low or high of the output value, then write it back to SMBUS slave 0x40 register 1.

- **Set GPIO 07 as Input:**

1. Read SMBUS slave 0x40 register 3 byte value;
2. Set bit 7 of the value read in step 1 as 1 and write it to SMBUS slave 0x40 register 3;
3. Read SMBUS slave 0x40 register 0 byte value;
4. Decide low or high of the input value through bit7 value read in step3.

6.3 Function Call for Reference

ICH SMBUS Access Code

(The following code is realized by simulating the access of BIOS to SMBUS. It uses Borand C++ 3.1 for compiling and is successfully tested under DOS (So far, it is not tested under other OS).

```
#define SMBUS_PORT 0xF040//SMB_BASE?0xF040
typedefunsigned char BYTE;

////////////////////////////////////////////////////////////////
////////////////////////////////////
BYTE   smbus_read_byte(BYTE addr, BYTE offset)
// Read SMBUS Register byte value. Read one byte value each
time. addr is slave address (such as 0x40), and offset is
register offset.
{
      int i;
      BYTE data;

      outportb(SMBUS_PORT + 4, (addr | 1));//   Write   slave
address to SMB_BASE + 4 (When reading, bit 0 of slave address
should be set as 1, so here  addr|1 is available)
      newiodelay();//delay
      newiodelay();//delay

      chk_smbus_ready();// Whether SMBUS is ready
```

```
      outportb(SMBUS_PORT + 3, offset);// Write register off-
set to SMB_BASE + 3
      newiodelay();//delay
      newiodelay();//delay

      outportb(SMBUS_PORT + 2, 0x48);// Write SMBUS command to
SMB_BASE + 2. 0x48 means starting byte data transmission
      newiodelay();//delay
      newiodelay();//delay

      for (i = 0; i <= 0x100; i++)
      {
          newiodelay();//longer delay
      }

      chk_smbus_ready();//Whether SMBUS is ready
      return(inportb(SMBUS_PORT + 5));// Byte value read from
SMB_BASE + 5
}

////////////////////////////////////////////////////////////////
////////////////////////////////////
void  smbus_write_byte(BYTE addr, BYTE offset, BYTE value)
// Write SMBUS Register byte value. Write one byte value each
time. addr is slave address (such as 0x40), and offset is
register offset.
{
      int i;

      outportb(SMBUS_PORT + 4, addr);// Write slave address to
SMB_BASE + 4 (When writing, slave address bit 0 should be set
as 0)
      moredelay();//longer delay
      moredelay();//longer delay

      chk_smbus_ready();//Whether SMBUS is ready

      outportb(SMBUS_PORT + 3, offset);// Write register off-
set to SMB_BASE + 3
      moredelay();//longer delay
      moredelay();//longer delay

      outportb(SMBUS_PORT + 5, value);//Write  data  value  to
SMB_BASE + 5
      moredelay();//longer delay
      moredelay();//longer delay
```

```
      outportb(SMBUS_PORT + 2, 0x48);// Write SMBUS command to
SMB_BASE + 2. 0x48 means starting byte data transmission.
      moredelay();//longer delay
      moredelay();//longer delay

      for (i = 0; i <= 0x100; i++)
      {
          newiodelay();//longer delay
      }

      chk_smbus_ready();//?Whether SMBUS is ready
}

////////////////////////////////////////////////////////////////
////////////////////////////////////
int   chk_smbus_ready()
//To decide whether SMBUS is ready or has completed the action,
you should wait for a long time to check whether SMBUS has
successfully transmitted the command. Since error may rarely
occurs, BIOS code does not make judgement on the return value
of this function in read and write of SUMBUS byte.
{
      int i, result = 1;
      BYTE data;

      for (i = 0; i <= 0x800; i++)
      {
          //SMB_BASE + 0 is SMBUS status value
          data = inportb(SMBUS_PORT);//Read   SMBUS   status
value once
          data = check_data(SMBUS_PORT);//Read  SMBUS  status
value several timesoutportb(SMBUS_PORT, data);//?Write    back
SMBUS status value which will clear status value (Write 1 to
the corresponding bit means clearing status)

          if (data & 0x02)
          {   //If bit 1 is set (which means the command is
completed), SMBUS is ready
              result = 0;//SMBUS ready
              break;
          }

          if (!(data & 0xBF))
          {   //If all bits are 0 except bit 2 (which means
error occurs on SMBUS), SMBUS is ready
              result = 0;//SMBUS ready
              break;
          }
```

```
            if (data & 0x04)
            {   //If bit 2 is set (which means error occurs on
SMBUS), error occurs on SMBUS which is rarely the case
                result = 1;//SMBUS error
                break;
            }
        }

        returnresult;
}

////////////////////////////////////////////////////////////////
////////////////////////////////////
BYTE   check_data(WORD addr)
{
        int  i;
        BYTE data;

        for(i = 0; i <= 6; i++)
        {
            data = inportb(addr);
            if (data != 0)
                break;
        }

        returndata;
}

////////////////////////////////////////////////////////////////
////////////////////////////////////
void   newiodelay()
//Shorter delay
{
        outportb(0xeb, 0);//IO port 0xeb No real device occu-
pies. Write a value to this port can realize delay function.
You can also choose other method according to the real situa-
tion.
}
////////////////////////////////////////////////////////////////
////////////////////////////////////
void   moredelay()
//Longer delay
{
        int  i;
        for (i = 0; i < 20; i++)
        {
```

```
            outportb(0xeb, 0);//IO port 0xeb No real device
occupies. Write a value to this port can realize delay func-
tion. You can also choose other method according to the real
situation.
        }
}

************************************************************
**********
```

GPIO Simcodes

(Here GPIO 00 and GPIO 07 in Chapter 2 are taken as examples)

```
Output High to GPIO 00:
        data = smbus_read_byte(0x40, 0x03);// Read slave 0x40
register 3 byte
        data &= 0xfe;//bit 0 is set as 0
        smbus_write_byte(0x40, 0x03, data)//Write back. GPIO 00
is set for output
        data = smbus_read_byte(0x40, 0x01)//Read slave 0x40
register 1
        data |= 0x01;//bit 0 is set as 1 which stands for high
        smbus_write_byte(0x40, 0x01, data)//Write back. Output
high value

Read Input Value from GPIO 07:
        data = smbus_read_byte(0x40, 0x03);//Read slave 0x40
register 3 byte
        data |= 0x80;//bit 7??1
        smbus_write_byte(0x40, 0x03, data)//Write back. GPIO 07
is set for input
        data = smbus_read_byte(0x40, 0x00)//Read slave 0x40
register 0. Then, the response value of bit 7 should know
whether the input is low or high
```

Appendix A

Programming the Watchdog Timer

A.1 Programming the Watchdog Timer

The ARK-5420's watchdog timer can be used to monitor system software operation and take corrective action if the software fails to function within the programmed period. This section describes the operation of the watchdog timer and how to program it.

A.1.1 Watchdog Timer Overview

The watchdog timer is built into the super I/O controller SMSC SCH3114. It provides the following user-programmable functions:

- Can be enabled or disabled via user program
- Timer can be set from 1 to 255 seconds or 1 to 255 minutes
- Generates an interrupt or resets signal if the software fails to reset the timer
- before time-out

A.1.2 Programming the Watchdog Timer

The I/O port address of the watchdog timer is 680h (hex).

Table A.1: Watchdog Timer Registers

Address: 680h (hex) Register	Read/ Write	Description
65 (hex)	write	Set seconds or minutes as units for the timer. Write 0 to bit 7: set second as counting unit. [default] Write 1 to bit 7: set minutes as counting unit.
66 (hex)	write	0: Stop timer [default] 01~FF (hex): The amount of the count, in seconds or min- utes, depends on the value set in register 65 (hex). This number decides how long the watchdog timer waits for strobe before generating an interrupt or reset signal. Writing a new value to this register can reset the timer to count with the new value.
67 (hex)	read/ write	Configure watchdog timer Bit 1:Write 1 to enable keyboard to reset the timer, 0 to dis- able. [default] Bit 2: Write 1 to enable mouse to reset the timer, 0 to dis- able.[default] Bit 7~4: Set the interrupt mapping of watchdog timer: 1111=IRQ15 …… 0011=IRQ3 0010=IRQ2 0001=IRQ1 0000=Disable [default]
68 (hex)	read/ write	Control watchdog timer Bit0: Read watchdog state; 1=Timer timeout Bit2: Write 1 to immediately generate timeout signal, and automat- ically return to 0 (Write only). Bit3: Writer 1 to allow triggering of timer timeout when P20 is effec- tive, 0 to disable. [default]

A.1.3 Example Program

```
;------------------------------------------------------
```

1. Enable watchdog timer and set 10 sec. as timeout interval.

```
;------------------------------------------------------
Mov dx,A65h ; Select register 65h, watchdog timer I/O port
address 680h+ register shifts 65h
Mov al,80h ; Set second as counting unit
Out dx,al
Mov dx,A66h ; Select register 66h, watchdog timer I/O port
address 680h+ register shift 66h
Mov al,10 ; Set timeout interval as 10 seconds and start count-
ing
Out dx,al

;------------------------------------------------------
```

2. Enable watchdog timer and set 5 min. as timeout interval.

```
;------------------------------------------------------
Mov dx,A65h ; Select register 65h, watchdog timer I/O port
address 680h+ register shifts 65h
Mov al,00h ; Set minute as counting unit
Out dx,al
680h
Mov dx,A66h ; Select register 66h, watchdog timer I/O port
address 680h+ register shifts 66h
Mov al,5 ;Set timeout interval as 5 minutes and start counting
Out dx,al

;------------------------------------------------------
```

3. Enable watchdog timer to be reset by mouse.

```
;------------------------------------------------------
Mov dx,A67h ; Select register 67h, watchdog timer I/O port
address 680h+ register shifts 67h
In al,dx
Or al,4h ; Enable watchdog timer to be reset by mouse
Out dx,al

;------------------------------------------------------
```

4. Enable watchdog timer to be reset by keyboard.

```
;------------------------------------------------------
Mov dx,A67h ; Select register 67h, watchdog timer I/O port
address 680h+ register shifts 67h
In al,dx
Or al,2h ; Enable watchdog timer to be reset by keyboard
Out dx,al

;------------------------------------------------------
```

5. Generate a time-out signal without timer counting.

```
;------------------------------------------------------
```

```
Mov dx,A68h ; Select register 68h, watchdog timer I/O port
address 680h+ register shifts 68h
In al,dx
Or al,4h ; Generate a time-out signal
Out dx,al
;-------------------------------------------------------
```

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