National Semiconductor

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PC87560UBD — PCI System I/O

1.0 General Description

The PC87560 is a highly integrated IC which incorporates PCI Interface, Bus Mastering Fast IDE Controller, Universal Serial Bus (USB) Host Controller, commonly-used I/O peripherals, and power management functions. When used in conjunction with the PC87550, the PC87560 provides all the peripheral and power management functions for efficient design of notebook computers and docking stations.

The PCI Interface provides up to 33 MHz PCI Bus frequency. Address re-mapping via PCI configuration registers is provided to support Plug and Play-capable systems.

The IDE Controller provides two channels with programmable access timing per channel/drive and a maximum sustained data transfer rate of 16 MBytes/sec. A multi-tasking DMA engine assures channel concurrency.

Peripheral functions include one Floppy Disk Controller (FDC), one parallel port (IEEE 1284), and two standard serial ports (one with Universal Infrared (UIR) capability). The FDC supports tri-mode floppy drives, Perpendicular Recording, and enhanced Tape Drive Register (TDR) operation. An external floppy disk may be multiplexed on the parallel port. The parallel port supports all standard operational modes. Both standard serial ports (16550 UARTs) support MIDI baud rates. The second serial port may be configured as a UIR serial port in IrDA1.0 SIR, IrDA1.1 MIR and FIR, Sharp-IR, or Remote TV compatible modes. Each peripheral function can be individually disabled.

System Interface functions include two 8237 DMA Controllers, two 8259 Interrupt Controllers, an 8254-compatible System Timer, CPU reset control, and numeric coprocessor error support. The DMA Controllers support seven channels (Master/Slave modes), DMA channel routing for Plug and Play compatibility, and ISA–compatible timing. The Interrupt Controllers support PCI native interrupts and interrupt routing. Edge– and level–triggering are individually programmable for each interrupt line. A PCIway Serial Interrupt interface (Master or Slave mode) is supported for docking.

Interfaces to ROM/FLASH ROM, a Real Time Clock (RTC), and Keyboard Controller (KBC) are provided. The PC87560 enables I/O subsystem expansion via a 16-bit Fast Expansion Bus (FX Bus) and provides Fast GateA20 and I/O peripheral design flexibility.

Advanced Configuration and Power Interface (ACPI) 1.0 compliance offers complete power management when combined with peripheral port access monitors, back powering protection, a system event register, and a full set of shadow registers. An on-chip Burst Serial Interface (BSER) communicates power management activity when used in conjuction with the PC87550 Host Bridge.

The USB OHCI Host Controller is a PCI Master device with two root hub ports. An optimized List–Queue Manager enables transfer scheduling and management. Dynamic rescheduling of data transfers and real–time device attaching/detaching are supported. Legacy keyboard and mouse support is also included.

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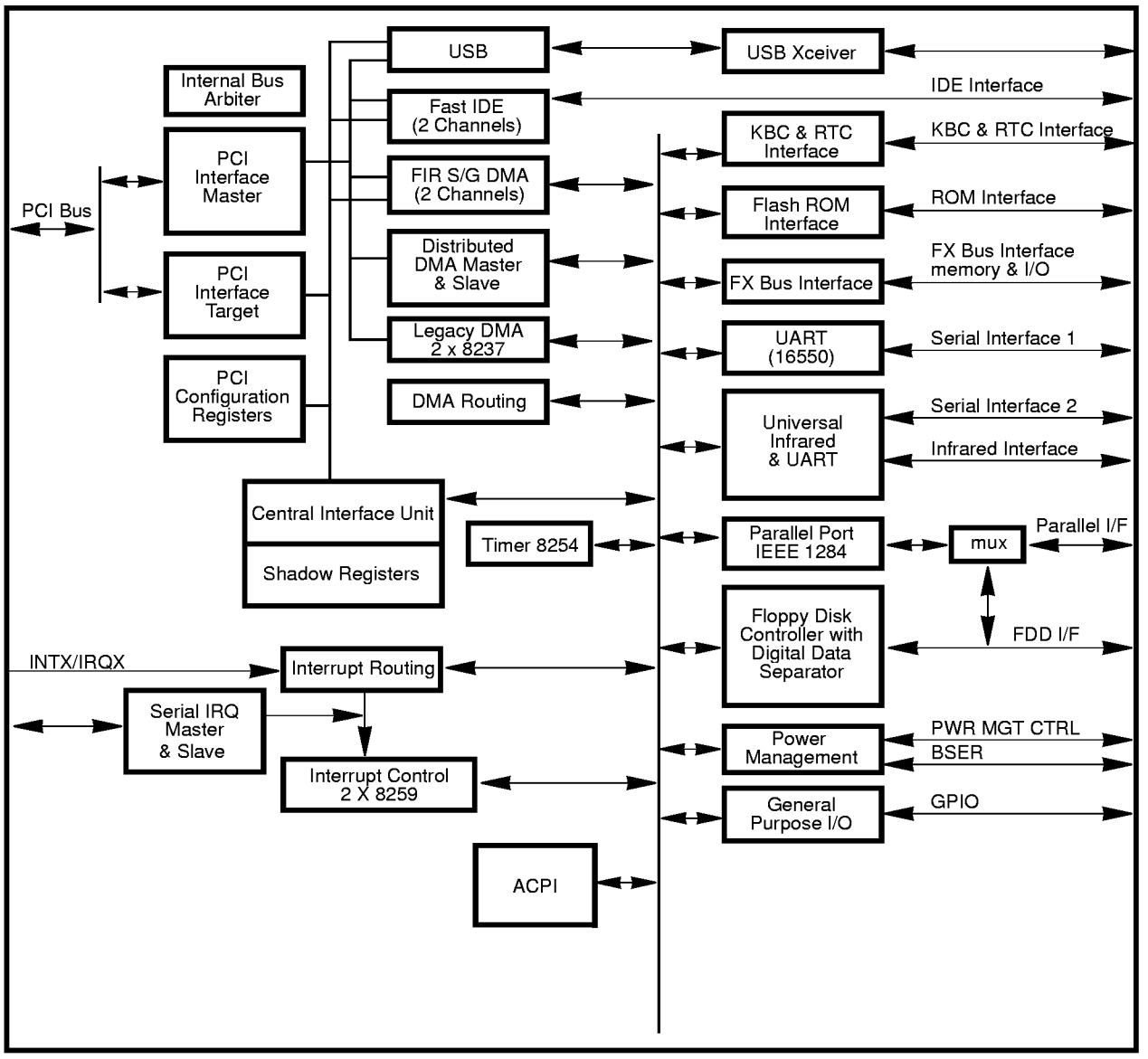
2.0 Features

- **PCI Bus Interface**
  - PCI 2.1 and PCI Mobile Design Guide 1.0 compliant
  - 32-bit PCI Bus with up to 33 MHz PCI Bus frequency
- **Fast Bus Master IDE Controller**
  - Access timing programmable per channel/drive
  - 16 MBytes/sec maximum data transfer rate
  - 2 IDE channels (primary and secondary)
  - SFF 8038i and SFF8022i compliant
- **I/O Peripherals**
  - ***Floppy Disk Controller:*** Software compatible with the PC8477, the NEC µPD765A and the N82077; Perpendicular Recording drive support; Support for enhanced Tape Drive Register (TDR); Tri-mode floppy and FM Mode support
  - ***IEEE 1284 compatible Parallel Port:*** Compatible, Nibble, Byte, ECP, EPP 1.7, and EPP1.9 mode support; Floppy Interface multiplexed on this port
  - ***Two Standard Serial Ports (16550 UARTs):*** MIDI baud rate supported on both ports; Second port configurable as serial port or UIR port
  - ***Universal Infrared (UIR) Port:*** IrDA 1.0 SIR, IrDA 1.1 MIR and FIR, Sharp-IR and Consumer Remote compatible; Programmable pulse width of 1.6 µs or 3/16 bit time
- **System Interface**
  - ***Two DMA Controllers:*** Seven 8237 compatible channels; distributed DMA Master and Slave modes; 2 Double-Word Buffers for PCI Bus transfers; Support for preemption and rearbitration for each PCI Bus transfer cycle
  - ***FX Bus (Non-Bus Master ISA Bus):*** Programmable timing for ISA compatible peripherals; 2 Programmable I/O range Chip Selects; 1 Programmable Memory Range; 1 programmable, fragmented I/O window with Chip select for Sound Blaster compatibility; 4 Channel DMA and 3 channel Interrupt support
  - ***Interfaces to External Devices:*** Up to 256 KBytes of ROM/FLASH ROM (with special 1 MB ROM space for PowerPC platforms); 8051 and PC87570 style keyboard controllers with Fast GateA20, Fast reset and remappable Chip Select; DS1287 style Real-Time Clock; X86 CPU interface support
  - ***Two 8259 Interrupt Controllers:*** Native PCI internal request support; edge– or level–trigger individually programmable on a per channel basis
  - ***8254 Compatible System Timer:*** with 3 timer channels
  - ***Numeric Coprocessor Error Support (Port F0)***
- **Power Management**
  - Advanced Configuration and Power Interface (ACPI) 1.0 specification compliant
  - Slave Mode: Power management control in the NorthBridge
  - Peripheral port access monitors (FDC, Serial 1&2, IDE 1&2, USB, and Parallel ports)
  - Shadow registers and one System event register
  - Back powering protection from printer, FDC and IDE interfaces
- **Universal Serial Bus (USB) Host Controller**
  - USB 1.0 and OpenHCI 1.0a compliant
  - Two Root Hub Ports with integrated transceivers
  - Full-speed (12 Mbps) and Low-speed device transfer protocols
  - Legacy keyboard and mouse support
- **General**
  - Mixed 3.3/5 Volt operation
  - 316-pin BGA package

3.0 Block Diagram



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4.0 Pin Descriptions

This section describes the signals available in the PC87560 device and associates each signal with a pin in the 316-pin BGA package. A package drawing is also provided.

The nomenclature for the values used in the "Voltage" column in the following tables is shown in Table I.

TABLE I. Nomenclature for Voltage Values

Voltage Value	Impact on the Associated Signal/Pin(s)
3/5V	When the chip is powered by 3V (VDD=3.3V), the I/O is 3.3V. When the chip is powered by 5V (VDD=5V), the I/O is 5V.
3/5VT	When the chip is powered by 3V (VCC=3.3V), the I/O is 3.3V with 5V tolerant inputs. When the chip is powered by 5V (VCC=5V), the I/O is 5V.
3/5V_PM	This signal is supported by the ACPI logic and powered by the VDD_PM input. When the ACPI logic is powered by 3V (VDD_PM=3.3V), the I/O is 3.3V. When the ACPI logic is powered by 5V (VDD_PM=5V), the I/O is 5V.
Open Drain	This output signal or set of output signals are always Open Drain signals capable of directly driving associated CPU signals. These outputs must have an external pull-up resistor to the appropriate supply voltage.

4.1 PCI INTERFACE

TABLE II. PCI Interface

Symbol(s)	Pin(s)	Type	Voltage	Function
Bus Interface				
AD[31:0]	C14, D14, A15, B15, C15, D15, A16, B16, C16, D16, A17, B17, C17, A18, B18, D17, A19, C18, C19, C20, D18, D19, D20, E17, E18, E19, E20, F17, F18, F19, F20, G17	I/O	3/5V	**Address and Data.** The Address and Data signals are multiplexed. The direction of these pins is defined as follows: **Phase** / **Target** / **Bus Master** Address Phase / Input / Output Read Data Phase / Output / Input Write Data Phase / Input / Output
C/BE[3:0]	G18, G19, G20, H17	I/O	3/5V	**Command or Byte Enable.** Signals are multiplexed bus command or byte enables.
DEVSEL#	D11	I/O	3/5V	**Device Select.** When driven active low, this signal indicates the driving device has decoded its address as the target of the current access.
FRAME#	B11	I/O	3/5V	**Frame.** Cycle Frame is driven by the initiator to indicate the beginning and duration of an access.
IDSEL	B14	I	3/5V	**Initialization Device Select.** Used as a chip select during configuration read and write transactions.
IRDY#	B12	I/O	3/5V	**Initiator Ready.** Indicates that the initiator is ready to complete the current data phase of the transaction.

TABLE II. PCI Interface (Continued)

Symbol(s)	Pin(s)	Type	Voltage	Function
LOCK#	A11	I	3/5V	**Lock.** Indicates an atomic operation that may require multiple transactions to complete.
PAR	D12	I/O	3/5V	**Parity.** Parity is even across AD[31:0] and C/BE[3:0]. PAR directionality follows the AD[31:0] directionality.
PCICLK	A14	I	3/5V	**PCI Clock.** The PCI clock input can be any frequency from 0-33MHz.
PCIRST#	D13	O	3/5V	**PCI Reset.** PCIRST# is used to reset PCI Bus devices and is asserted following RESET_IN#. PCIRST# will be de–asserted a minimum of 1ms after RESET_IN# is de–asserted.
PERR#	A13	I/O	3/5V	**Parity Error.** Used for reporting data parity errors during all PCI transactions except a Special Cycle. PERR# is an output when AD[31:0] and PAR are inputs and is an input when AD[31:0] and PAR are outputs.
SERR#	A12	I/O	3/5V	**System Error.** Used for reporting address parity errors, data parity errors on the Special Cycle command, or any other system error where the result will be catastrophic. When reporting address parity errors, SERR# is an output. As an input to the PC87560, any PCI device can pulse the SERR# to indicate a catastrophic error condition.
STOP#	C11	I/O	3/5V	**Stop**. Indicates that the current target is requesting the initiator to stop the current transaction.
TRDY#	C12	I/O	3/5V	**Target Ready.** Indicates that the target of the current data phase of the transaction is ready to be completed.
Bus Arbiter				
SIOGNT#	C13	I	3/5V	**System I/O Grant.** This signal is asserted from the host controller allowing the PC87560 to become the PCI Bus Master.
SIOREQ#	B13	O	3/5V	**System I/O Request.** This signal is asserted to request the host controller to allow the PC87560 to become PCI Bus Master.
Interrupts				
INTA#, INTB#, INTC#, INTD#	A9, D10, C10, B10	I	3/5V	**Interrupt Request A, B, C, and D.** These four active–low, shareable interrupt requests may be used by PCI devices to make an interrupt request.

4.2 FAST BUS MASTER IDE CONTROLLER INTERFACE

TABLE III. Fast Bus Master IDE Controller Interface

Symbol(s)	Pin(s)	Type	Voltage	Function
CH1_CS1#, CH1_CS3#	U9, V9	O	3/5V	**Channel 1 Chip Select 1 and 3.** CH1_CS1# is the chip select signal to select the Channel 1 Command Block Registers. CH1_CS3# is the chip select signal to select the Control Block Registers of Channel 1.
CH2_CS1#, CH2_CS3#	V10, W10	O	3/5V	**Channel 2 Chip Select 1 and 3.** CH2_CS1# is the chip select signal to select the Channel 2 Command Block Registers. CH2_CS3# is the chip select signal to select the Control Block Registers of Channel 2.

TABLE III. Fast Bus Master IDE Controller Interface (Continued)

Symbol(s)	Pin(s)	Type	Voltage	Function
CH1_DMREQ	Y9	I	3/5VT	**Channel 1 DMA Request.** This signal is used when the IDE device is configured to use the pseudo DMA handshake mode or when using the internal IDE DMA controller. When asserted, this signals the PC87560 that the selected drive on Channel 1 is ready to transfer data.
CH2_DMREQ	Y11	I	3/5VT	**Channel 2 DMA Request.** This signal is used when the IDE device is configured to use the pseudo DMA handshake mode or when using the internal IDE DMA controller. When asserted, this signals the PC87560 that the selected drive on Channel 2 is ready to transfer data.
CH1_DMACK#	U10	O	3/5V	**Channel 1 DMA Acknowledge.** This signal is used when the PC87560's IDE Controller is configured to use the pseudo DMA handshake mode or when using the internal IDE DMA controller. This signal indicates to the selected drive on Channel 1 that data has either been accepted, or that data is available.
CH2_DMACK#	W11	O	3/5V	**Channel 2 DMA Acknowledge.** This signal is used when the PC87560's IDE Controller is configured to use the pseudo DMA handshake mode or when using the internal IDE DMA controller. This signal indicates to the selected drive on Channel 2 that data has either been accepted, or that data is available.
CH1_INT, CH2_INT	W9, Y10	I	3/5VT	**Channel 1 and Channel 2 Drive Interrupts.** These signals are used to interrupt the host system. CH1_INT is asserted when the IDE drive(s) on Channel 1 have a pending interrupt. CH2_INT is asserted when the IDE drive(s) on Channel 2 have a pending interrupt.
DA[2:0]	W16, V16, U16	O	3/5V	**Drive Address.** When accessing the IDE drive, these pins are the address bits 2-0 used to access a register or data port in the drive.
DD[15:0]	W12, V12, U12, Y13, W13, V13, U13, Y14, W14, V14, U14, Y15, W15, V15, U15, Y16	I/O	3/5VT	**Drive Data Bus.** When accessing the IDE drive, this is an 8- or 16-bit bi-direction data bus between the PC87560 chip and the drive. The lower 8 bits are also used for non-data 8-bit transfers (such as registers and ECC bytes).
DIORDY	V11	I	3/5VT	**Drive I/O Channel Ready.** When accessing the IDE drive, this signal is negated (low) to extend a Programmable I/O (PIO) disk transfer cycle of any register access (read or write) when the drive is not ready to respond to a data transfer request. When an IDE drive no longer desires to extend the cycle, DIORDY will be placed in TRI-STATE® by the IDE drive(s) and pulled high by an external pull-up resistor.
DIOR#	U11	O	3/5V	**Drive I/O Read.** This is the read strobe signal for both channels. When active low, DIOR# enables data from a register or the data port of the drive onto the IDE Drive data bus.

TABLE III. Fast Bus Master IDE Controller Interface (Continued)

Symbol(s)	Pin(s)	Type	Voltage	Function
DIOW#	Y12	O	3/5V	**Drive I/O Write.** This is the write strobe signal for both channels. The rising edge of DIOW# clocks data from the IDE Drive data bus into the register or the data port of the IDE drive.
DRST#	Y8	O	3/5V	**Drive Reset.** This signal from the IDE Controller is asserted active (low) during power up or under software control. DRST# will remain active low as long as the PCI Reset signal (PCIRST#) is asserted low or as long as the drive reset bit in the IDE Controller is set to one. **NOTE:** This signal will be driven active low for a maximum of 2 msec. following the rising edge of RESET_IN#. It is the system designer's responsibility to guarantee that no accesses are made if the IDE drive devices use this signal as reset and the PC87560's PCIRST# is not used as the PCI Bus reset. In such a case, the PC87560 cannot guarantee that a PCI Bus Cycle will not occur while DRST# remains active (low). If the PC87560's PCIRST# (pin D13) is used as the PCI Bus reset, no PCI Bus access will occur until DRST# is de–asserted (high).

4.3 I/O PERIPHERALS

The following tables identify the signals and pins associated with particular peripheral functions. These functions include the Floppy Disk Controller, Parallel Port/Floppy Interface, Serial Interface Ports 1 and 2, and the Universal Infrared Interface.

4.3.1 Floppy Disk Controller (FDC)

TABLE IV. FDC Controller Interface

Symbol(s)	Pin(s)	Type	Voltage	Function
DENSL[1:0]	D2, D3	O	3/5V	**Density Select 0 and 1.** Indicates high or low density FDC data rate is selected.
DIR#	E1	O	3/5V	**Direction.** This signal determines the direction of movement of the selected floppy disk drive head during a seek operation.
DSKCHG#	N3	I	3/5VT	**Disk Change.** This input signal indicates if floppy disk drive door is open.
DS[1:0]#	E3, E2	O	3/5V	**Drive Select 0 and 1.** These active–low signals are used to decode Drive Select outputs which control four floppy disk drives.
HDSEL#	F1	O	3/5V	**Head Select.** This signal detainees which side of the FDD is accessed. Active low selects side 1, inactive high selects side 0.
INDEX#	G2	I	3/5VT	**Index.** This input signal indicates the beginning of an FDD track.
MSEN[1:0]	G3, G4	I	3/5VT	**Media Sense 0 and 1.** These input pins act as media sensors. Each pin has a 40kΩ internal pull-up resistor.
MTR[1:0]#	D1, E4	O	3/5V	**Motor Select 0 and 1.** These active low signals are the motor enable lines for floppy disk drives 0 and 1. They are encoded with information to control four Floppy Disk Drives.
RDATA#	N2	I	3/5VT	**Read Data.** This input signal is the raw read from the floppy disk drive.

TABLE IV. FDC Controller Interface (Continued)

Symbol(s)	Pin(s)	Type	Voltage	Function
STEP#	F4	O	3/5V	**Step.** This signal issues pulses to the floppy disk drive at a programmable rate to move the head during a seek operation.
TRK0#	M4	I	3/5VT	**Track 0.** This signal indicates to the controller that the head of the selected floppy disk drive is at track zero.
WDATA#	F3	O	3/5V	**Write Data.** This is the write precompensated data that is written to selected FDD. Precompensation is selectable.
WGATE#	F2	O	3/5V	**Write Gate.** This output signal enables the write circuitry of the selected floppy disk drive. WGATE# is designed to prevent writing to the disk when the power is cycled.
WP#	N1	I	3/5VT	**Write Protect.** This input indicates that the disk in the selected floppy disk drive is write protected.

4.3.2 Parallel Port/Floppy Interface

TABLE V. Parallel Port/Floppy Interface

Symbol(s)	Pin(s)	Type	Voltage	Function
ACK#/DS1#	T3	I/O	3/5VT	**Acknowledge or Drive Select 1.** Signal indicates Acknowledge in Parallel Port mode or Drive Select 1 in Floppy mode.
AFD#/ DSTRB#/ DENSL0	V3	O	3/5V	**Automatic Feed XT, DataStrobe#, or Density Select 0.** Signal indicates Automatic Feed XT in compatibility Parallel Port mode, DataStrobe# in ECP mode, or Density Select 0 In Floppy mode.
BUSY#/ WAIT#/ MTR1#	T4	I/O	3/5VT	**Busy, Wait, or Motor Select 1.** Signal indicates Busy in compatibility Parallel Port mode, Wait in ECP mode, or Motor Select 1 in Floppy mode.
ERR#/ HDSEL#	V2	I/O	3/5VT	**Error or Head Select.** Signal indicates Error in Parallel Port mode or Head Select in Floppy mode.
INIT#/DIR#	V1	O	3/5V	**Initialize or Direction.** Signal indicates Initialize in Parallel Port mode or Direction in Floppy mode.
PD0/INDEX#	P3	I/O	3/5VT	**Data 0 or Index#.** Signal indicates Data 0 in Parallel Port mode or Index in Floppy mode.
PD1/TRK0#	P4	I/O	3/5VT	**Data 1 or Track 0.** Signal indicates Data 1 in Parallel Port mode or Track 0 in Floppy mode.
PD2/WP#	R1	I/O	3/5VT	**Data 2 or Write Protect.** Signal indicates Data 2 in Parallel Port mode or Write Protect in Floppy mode.
PD3/RDATA#	R2	I/O	3/5VT	**Data 3 or Read Data.** Signal indicates Data 3 in Parallel Port mode or Read Data in Floppy mode.
PD4/ DSKCHG#	R3	I/O	3/5VT	**Data 4 or Disk Change.** Signal indicates Data 4 in Parallel Port mode or Disk Change in Floppy mode.

TABLE V. Parallel Port/Floppy Interface (Continued)

Symbol(s)	Pin(s)	Type	Voltage	Function
PD5/MSEN0	R4	I/O	3/5VT	**Data 5 or Media Sense 0.** Signal indicates Data 5 in Parallel Port mode or Media Sense 0 in Floppy mode.
PD6/DENSL1	T2	I/O	3/5VT	**Data 6 or Density Select 1.** Signal indicates Data 6 in Parallel Port mode or Density Select 1 in Floppy mode.
PD7/MSEN1	T1	I/O	3/5VT	**Data 7 or Media Sense 1.** Signal indicates Data 7 in Parallel Port mode or Media Sense 1 in Floppy mode.
PE/WDATA#	U1	I/O	3/5VT	**Paper End or Write Data.** Signal indicates Paper End in Parallel Port mode or Write Data in Floppy mode.
PNF	N4	I	3/5VT	**Printer Not Floppy (PNF).** This input is disabled when the PNF Select bit (Bit 0 of the Function 1 System I/O Configuration Register at configuration offset 5Ch) is a zero. When this input is a zero and the PNF Select bit is a one, the FDC signals are multiplexed onto the Parallel Port/ Floppy pins. When this input is a one and the PNF Select bit is a one, the Parallel Port signals are multiplexed onto the Parallel Port/Floppy pins.
SLCT/ WGATE#	U2	I/O	3/5VT	**Select or Write Gate.** Signal indicates Select in Parallel Port mode or Write Gate in Floppy mode.
SLIN#/ ASTB#/ STEP#	U3	O	3/5V	**Select Input, Strobe, or Step.** Signal indicates Select Input in compatibility Parallel Port mode, Strobe in ECP mode, or Step in Floppy mode.
STB#/WRITE#	P2	O	3/5V	**Data Strobe or Write Strobe.** Signal provides Data Strobe in compatibility Parallel Port mode or Write Strobe in ECP mode.

4.3.3 Serial Interface (Ports 1 and 2)

TABLE VI. Serial Interface

Symbol(s)	Pin(s)	Type	Voltage	Function
CTS[1:0]#	U8, Y4	I	3/5VT	**Clear To Send.** Indicates Clear to Send for Serial Ports 1 and 2.
DCD[1:0]#	Y6, U4	I	3/5VT	**Data Carrier Detect.** Indicates Data Carrier Detect for Serial Ports 1 and 2.
DSR[1:0]#	U7, W3	I	3/5VT	**Data Set Ready.** Data Set Ready for Serial Ports 1 and 2.
DTR[1:0]#	V8, U5	O	3/5V	**Data Terminal Ready.** Indicates Data Terminal Ready for Serial Ports 1 and 2.
RTS[1:0]#	W7, V4	O	3/5V	**Request To Send.** Indicates RequesT to Send for Serial Ports 1 and 2.
RI[1:0]#	W8, V5	I	3/5VT	**Ring Indicator.** Indicates that either Serial Port 1 or 2 is receiving a ring signal.
SIN[1:0]	V7, Y3	I	3/5VT	**Serial Data Input.** Indicates Serial Data Input for Serial Ports 1 and 2.
SOUT[1:0]	Y7, W4	O	3/5V	**Serial Data Output.** Indicates Serial Data Output for Serial Ports 1 and 2.

4.3.4 Universal Infrared (UIR) Interface (Serial Port 2)

TABLE VII. Universal Infrared (UIR) Interface

Symbol(s)	Pin(s)	Type	Voltage	Function
ID[0]/IRSEL0/ IRRX2	U6	I/O	3/5VT	**ID0, Infrared Select 0, or Infrared Receive Data 2.** Indicates ID0 for Plug and Play support, Infrared Select 0, or Infrared Receive Data 2.
ID[2:1]/ IRSEL[2:1]	W6, V6	I/O	3/5VT	**ID[2:1] or Infrared Select 2-1.** Indicates ID[2:1] for Plug and Play support or Infrared Select 2-1.
IRRX	Y5	I	3/5VT	**Infrared Receive Data.** Signal indicates Infrared Receive Data.
IRTX	W5	O	3/5V	**Infrared Transmit Data.** Indicates Infrared Transmit Data.

4.4 CPU INTERFACE

TABLE VIII. CPU Interface

Symbol(s)	Pin(s)	Type	Voltage	Function
CPUINIT	D6	O	Open Drain	**CPU Initialization.** This signal with a pull-up resistor can be used to drive the CPU's INIT pin during power-up (RESET_IN# active) or when the PC87560 detects a shutdown special cycle on the PCI Bus. CPUINIT will also be active if a soft reset is initiated via Port 92, or a snooped Fast Reset (if Fast Reset is enabled) or KBRST# is asserted (if Fast Reset is disabled).
CPUINT	C5	O	Open Drain	**CPU Interrupt.** This signal with a pull-up resistor can be used to drive the CPU INT pin.
CPURST	A5	O	Open Drain	**CPU Reset.** This signal with a pull-up resistor can be used to drive the CPU Reset signal of the CPU. The PC87560 releases CPURST during power-up (RESET_IN# active). CPURST is driven inactive (low) a minimum of 2ms after RESET_IN# is driven inactive to allow the CPU's clock and VCC time to stabilize. CPURST is driven inactive low synchronously to the rising edge of PCICLK.
FERR#	C6	I	3/5V	**Numeric Coprocessor Error.** This signal is the Numeric Coprocessor Error input from the CPU.
FGA20	B5	O	Open Drain	**Fast Gate A20.** This signal with a pull-up resistor can be used to drive the CPU A20M# pin. If the USB Legacy Keyboard Support function is enabled, it will be the source for this output. Otherwise, if the Fast GateA20 strapping option is enabled, this would be the source of this signal. If both the USB Legacy Keyboard Support function and the Fast Gate A20 strapping option are disabled, then the Keyboard GateA20 input (KBGA20) will drive this signal.
IGNNE#	B6	O	Open Drain	**Ignore Numeric Error.** This signal with a pull-up resistor may be used to drive the CPU IGNNE# pin.
NMI	A6	O	Open Drain	**Non Maskable Interrupt.** This signal with a pull-up resistor may be used to drive the CPU's NMI signal. This signal will go active (high) when a PCI System Error occurs.

TABLE VIII. CPU Interface (Continued)

Symbol(s)	Pin(s)	Type	Voltage	Function
PM_PWRGOOD	H4	I	3/5VT_PM	**Power Management Power Good.** When PM_PWRGOOD is asserted (high), it indicates that the VDD_PM power is on and valid. When PM_PWRGOOD is de-asserted (low), it will reset all PC87560 functions that are powered by VDD_PM.
RESET_IN#	H2	I	3/5VT_PM	**Reset Input.** When de–asserted (high), RESET_IN# is an indication to the PC87560 that power and PCICLK have been stable for at least 1ms. When RESET_IN# is asserted (low), the PC87560 resets all functions powered by VDD and asserts CPURST, CPUINIT and PCIRST#. RESET_IN# can be driven asynchronously.

4.5 FX BUS (FXB) INTERFACE

TABLE IX. FXB Interface

Symbol(s)	Pin(s)	Type	Voltage	Function
AUDIOCS#	P19	O	3/5V	**Audio Chip Select.** This active-low output Chip Select provides support for a compatible, fragmented Sound Blaster I/O map.
BHE#	M18	O	3/5V	**Byte High Enable.** This FX Bus signal is asserted low to indicate that high (odd) data byte is being transferred. Only 16-bit devices use this signal.
DACK0#/ DOCKEN#	J18	I/O	3/5VT	**DMA Acknowledge 0 or Dock Enable.** During normal operation, this pin will act as the active-low DMA Acknowledge output signal associated with the DRQ[0] input. During a power-up reset, this pin will become an input strapping option and is sampled on the rising edge of RESET_IN#. This I/O signal has a weak pull-down resistor; thus, it will default low unless an external pull-up resistor is used. If this pin is sampled low, the PC87560 will indicate that it is in a Docking Station (Its Function 1 Device ID will be 000Eh). If this pin is sampled high, then the PC87560 will indicate that it is in a Notebook Motherboard (Its Function 1 Device ID will be 0011h).
DACK1#/ FENCFG	J19	I/O	3/5VT	**DMA Acknowledge 1 or Function Enable Configuration.** During normal operation, this pin will act as the active-low DMA Acknowledge output signal associated with the DRQ[1] input. During a power-up reset, this pin will become an input strapping option and is sampled on the rising edge of RESET_IN#. This I/O signal has a weak pull-down resistor; thus, it will default low unless an external pull-up resistor is used. If this pin is sampled low, all of the PC87560 functions are disabled. If this pin is sampled high, then the PC87560 functions will operate normally as defined.
DACK2#/ FGA20EN	J20	I/O	3/5VT	**DMA Acknowledge 2 or Fast Gate A20 Enable.** During normal operation, this pin will act as the active-low DMA Acknowledge output signal associated with the DRQ[2] input. During a power-up reset, this pin will become an input strapping option and is sampled on the rising edge of RESET_IN#. This I/O signal has a weak pull-down resistor; thus, it will default low unless an external pull-up resistor is used. If this pin is sampled low, the Fast GateA20 and the Fast Keyboard Reset logic will be disabled. If this pin is sampled high, the Fast GateA20 and the Fast Keyboard Reset logic will be enabled.

TABLE IX. FXB Interface (Continued)

Symbol(s)	Pin(s)	Type	Voltage	Function
DACK3#/ SIRQMST	K17	I/O	3/5VT	**DMA Acknowledge 3 or Serial Interrupt Request Master.** During normal operation, this pin will act as the active-low DMA Acknowledge output signal associated with the DRQ[3] input. During a power-up reset, this pin will become an input strapping option and is sampled on the rising edge of RESET_IN#. This I/O signal has a weak pull-down resistor; thus, it will default low unless an external pull-up resistor is used. If this pin is sampled low, the Serial Interrupt interface logic will be operate as a Slave. If this pin is sampled high, the Serial Interrupt interface logic will operate as the Master.
DRQ[3:0]	L20, K20, K19, K18	I	3/5VT	**DMA Requests 3-0.** These DMA request pins may be steered to any of the internal PC87560 8237 DMA Controllers' request inputs.
FXA[20]/ POWERPC	Y17	O	3/5V	**FX Address 20 or PowerPC ROM Chip Select Range Enable.** During normal operation, this signal drives out the most significant address bit on the FX Bus. During a reset (when RESET_IN# is low), this pin provides an input strapping option. By default, this I/O has a weak pull-down resistor that is enabled whenever RESET_IN# is active low unless a 10KΩ is applied. The rising edge of RESET_IN# samples this pin. If it is sampled low, the PowerPC ROM Chip Select memory range (FFF00000-FFFFFFFFh) will not be decoded by the PC87560 to generate an active ROMCS# signal and an associated FX Bus cycle. If this pin is sampled high, the PowerPC ROM chip select memory range will be decoded along with the appropriate associated FX Bus cycle
FXA[19:4]/ FXD[15:0]	W17, V17, Y18, W18, V18, W20, U17, V19, V20, U18, U19, U20, T17, T18, T19, T20	I/O	3/5VT	**FX Address 19-4 or FX Data Bus 15-0.** This is the multiplexed FX address/data bus. During FX Bus address phases, the appropriate address will be driven onto these pins by the PC87560. During FX Bus data phases, the PC87560 will drive out the appropriate data during write cycles and will put these signals in TRI-STATE during read cycles, thus acting as inputs.
FXA[3]/ IDE_3v_EN#	R17	I/O	3/5VT	**FX Address 3 or IDE Interface 3 Volt Drive Strength Enable.** During normal operation, this signal is an output for address bit 3 on the FX Bus. During a power–up reset (when RESET_IN# is low), this pin is an input strapping option. This I/O has a weak pull–down resistor that is enabled whenever RESET_IN# is active low causing the pin to default to a low signal state unless an external pull–up resistor is applied. If sampled low, the IDE Interface drivers are optimized for a 3V system. If sampled high, the IDE Interface drivers are optimized for a 5V system. **NOTE:** This strapping option must be configured for the correct system voltage to ensure that the IDE Interface signals adhere to the ATA specification.
FXA[2:0]	R18, R19, R20	I/O	3/5VT	**FX Address 2-0.** These three signals are the least significant address bits on the FX Bus.
FXASTB#	P20	O	3/5V	**FX Address Strobe.** During the FX Bus address phase, the falling edge of FXASTB# is used to latch the address FXA[19:4] off the multiplexed FXA[19:4]/FXD[15:0] pins.

TABLE IX. FXB Interface (Continued)

Symbol(s)	Pin(s)	Type	Voltage	Function
FXCS[1:0]#	P17, P18	O	3/5V	**FX Chip Select 0 and 1.** These active–low signals are programmable I/O address range chip selects to select external devices on the FX bus.
FXIOCS16#	N20	I	3/5VT	**FX I/O Chip Select 16 Bit.** This input signal is driven active (low) by 16-bit I/O devices when they are being addressed and this signal will be used by the PC87560's FX Bus Controller to appropriately steer data for I/O cycles.
FXIRQ[2:0]	H20, H19, H18	I	3/5VT	**FX Bus Interrupt Request 2-0.** These are general purpose interrupts that are internally routed (configurable) to the interrupt lines of the 8259s.
FXIORDY	N19	I/O	3/5VT	**FX I/O Ready.** When accessing the FX Bus, this signal may be negated (low) by the device being accessed to extend the FX Bus transfer cycle.
FXIOR#	N17	O	3/5VT	**FX I/O Read.** This is the FX Bus I/O read strobe. The pulse width of this signal is programmable.
FXIOW#	N18	O	3/5VT	**FX I/O Write.** This is the FX Bus I/O write strobe. The pulse width of this signal is programmable.
FXMEMCS16#	M17	I	3/5VT	**FX Memory Chip Select 16 Bit.** This input signal is driven active (low) by 16-bit memory devices when they are being addressed and this signal will be used by the PC87560's FX Bus Controller to appropriately steer data for memory cycles.
FXMEMR#	M19	O	3/5V	**FX Memory Read.** This is the FX Bus Memory read strobe. This signal will strobe active for every memory read cycle on the FX Bus.
FXMEMW#	M20	O	3/5V	**FX Memory Write.** This is the FX Bus Memory write strobe. This signal will strobe active for every memory write cycle on the FX Bus
FXSMEMR#	L17	O	3/5V	**FX System Memory Read.** This is the FX Bus System Memory read strobe. This signal will strobe active only for memory reads on the FX Bus with addresses below 1Meg.
FXSMEMW#	L18	O	3/5V	**FX System Memory Write.** This is the FX Bus System Memory write strobe. This signal will strobe active only for memory writes on the FX Bus with address below 1Meg.
TC/MRTRYD#	J17	I/O	3/5VT	**Terminal Count or Memory Retry Disable.** During normal operation, this pin will act as the Terminal Count (TC) of a compatible 8237 DMA Controller. During a power-up reset, this pin will become an input strapping option and is sampled on the rising edge of RESET_IN#. This I/O signal has a weak pull-down resistor; thus, it will default low unless an external pull-up resistor is used. If it is sampled low, memory reads from the ROM BIOS will not be retried on the PCI Bus. If this pin is sampled high, memory reads from the ROM BIOS will be retried on the PCI Bus. **NOTE**: If the reads from the ROM BIOS are not retried, it would tend to violate the standard 16 PCI clock Target Initial Latency requirement. If the purpose of these read cycles is to perform a POST Code copy of the ROM image to memory, this will be compliant with the PCI Local Bus Specification Revision 2.1.

4.6 SYSTEM ROM, KBC AND RTC INTERFACES

TABLE X. ROM, KBC and RTC Interfaces

Symbol(s)	Pin(s)	Type	Voltage	Function
ROM/FLASH ROM				
ROMCS#	L19	O	3/5V	**ROM Chip Select.** This signal will be active (low) any time there is a memory access to the (configurable) ROM BIOS memory range.
Keyboard Controller				
KBCS#	B8	O	3/5V	**Keyboard Controller Chip Select.** This pin is asserted during read or write accesses to the keyboard's programmable I/O locations.
KBGA20	C8	I	3/5VT	**Keyboard GateA20 input.** Gate A20 input from an external keyboard controller.
KBINT	C9	I	3/5VT	**Keyboard Interrupt.** Keyboard interrupt request from an external keyboard controller.
KBRST#	D8	I	3/5VT	**Keyboard Reset input.** Keyboard Reset from an external keyboard controller.
MINT	D9	I	3/5VT	**Mouse Interrupt.** Mouse interrupt request from an external keyboard controller.
Real-Time Clock				
PMCS#	A7	O	3/5V	**Power Management Chip Select.** This pin may be configured to assert during an I/O read/write to addresses KBCBAR+2h, and KBCBAR+6h.
RTCCS#	A8	O	3/5V	**Real Time Clock Chip Select.** This pin is asserted during I/O read or write accesses to the RTC location 71h. When VMKBC is selected (Function1, Reg. 5Ch, bit 4 = "1"), this pin is asserted during I/O read or write accesses to locations 70h and 71h.
RTCINT#	J4	I	3/5VT_PM	**Real Time Clock Interrupt.** Active low Real Time Clock interrupt.

4.7 POWER MANAGEMENT/GPIO/PC87550 INTERFACES

TABLE XI. Power Management/GPIO Interfaces

Symbol(s)	Pin(s)	Type	Voltage	Function
AEN/GPIO0	C3	I/O	3/5VT	**Address Enable (FX Bus) or General Purpose I/O 0.** When this pin is configured as the AEN signal, it will function as the FX Bus Address Enable signal for FX Bus cycles. When this pin is configured as a General Purpose I/O, this pin is accessed through the General Purpose I/O register Bit 0.
BSERCLK3	D7	I	3/5VT	**Burst Serial Clock.** This pin is the Burst Serial Interface clock for the serial system and power management bus (BSER1TO3/BSER3TO1).
BSER3TO1	C7	O	3/5V	**Burst Serial 3 to 1.** Communicates system and power management information from the PC87560 to the PC87550 Host Bridge.
BSER1TO3	B7	I	3/5VT	**Burst Serial 1 to 3.** Communicates system and power management information from the PC87550 Host Bridge to the PC87560.

TABLE XI. Power Management/GPIO Interfaces (Continued)

Symbol(s)	Pin(s)	Type	Voltage	Function
CLKRUN#	A10	I/O	3/5V	**Clock Run.** Clock Run is used to request starting or stopping the PCI clock as well as indicating the clock status. The PC87560 can request the Central Resource to start or maintain the interface clock by assertion of CLKRUN#. The Central Resource is responsible for maintaining CLKRUN# asserted, and for driving it high to the deasserted state. CLKRUN# defaults low (active) upon deassertion of reset. CLKRUN# is a sustained as a TRI-STATE I/O signal.
EX_PME/ GPIO7/	J2	I/O	3/5VT_PM	**External Power Management Event input or General Purpose I/O 7.** When this pin is configured as EX_PME, this input will signal an External Power Management Event to the ACPI logic. This signal is driven by an external source to generate a PME. When used as a General Purpose I/O pin, this pin is accessed through the General Purpose I/O register Bit 7.
EX_PME_EC/ EVENT1	J3	I/O	3/5VT_PM	**External Power Management Event input from Embedded Controller or Event 1.** When this signal functions as EX_PME_EC, it operates as the ACPI External Power Management Event input signal from the Embedded Controller (EC). It is used by the EC to generate PME events or to wake-up the system. When EX_PME_EC is asserted high and the PC87560 is in a sleep state (SUSPEND# = 0) and the RTCINT# signal is inactive high, then the EC_STS bit will be set. When power management is configured in slave mode, EVENT1 is an output and will be asserted whenever one of the system events occurs in the System Events 1 Register. This pin can be connected to the EXTACT0 pin of the PC87550 Host Bridge.
GPIO2	A3	I/O	3/5VT	**General Purpose I/O 2.** This pin is accessed through the General Purpose I/O register Bit 2. It may be configured to operate as either a Totem-Pole driver (default) or as an Open Drain driver (to support a bit-bang I^2C interface).
GPIO3	C4	I/O	3/5VT	**General Purpose I/O 3.** This pin is accessed through the General Purpose I/O register Bit 3. It may be configured to operate as either a Totem-Pole driver (default) or as an Open Drain driver (to support a bit-bang I^2C interface).
IDE_INT1/ GPIO4	B4	I/O	3/5VT	**IDE Interrupt 1 Output or General Purpose I/O 4.** When this pin is configured as a GP I/O pin, this pin is accessed through the General Purpose I/O register Bit 4. When configured as the IDE_INT1 pin, it will be the output of the IDE Channel 1 Interrupt Request.
IDE_INT2/ GPIO5	A4	I/O	3/5VT	**IDE Interrupt 2 Output or General Purpose I/O 5.** When this pin is configured as a GP I/O pin, this pin is accessed through the General Purpose I/O register Bit 5. When configured as the IDE_INT2 pin, it will be the output of the IDE Channel 2 Interrupt Request.

TABLE XI. Power Management/GPIO Interfaces (Continued)

Symbol(s)	Pin(s)	Type	Voltage	Function
ID3/GPIO1	B3	I/O	3/5VT	**Infrared ID3 Input or General Purpose I/O 1.** When this pin is configured to operate as the ID3 pin, it will act as the ID3 Infrared input signal to the UIR module. When this pin is configured as a General Purpose I/O, this pin is accessed through the General Purpose I/O register Bit 1. **NOTE**: When configured as a General Purpose I/O, the value driven will continue to be driven to the UIR module as the ID3 Infrared input signal. It is the responsibility of the hardware and software system designer to avoid any conflicts between the configuration of this pin and the associated (if any) Infrared Driver software.
SLPEN#	H3	O	3/5V_PM	**Sleep Enable.** This signal indicates a request for the ACPI Embedded Controller to enter an ACPI sleep mode.This signal will go active (low) when the SLP_EN bit in the PM1b_CNT register is set to one. The Embedded Controller will acknowledge this request by asserting SUSPEND# low. To exit the sleep mode the Embedded Controller may de-assert the SUSPEND# signal high, the PC87560's ACPI logic will clear the SLP_EN bit and de-assert SLPEN# high in response. **NOTE:** The SLPEN# signal is simply the inversion of the SLP_EN bit; it is the software's responsibility to only set this bit when the appropriate Sleep Type has been programmed.
SMI_SB	J1	O	3V_PM	**System Management Interrupt.** This signal is asserted high whenever an I/O trap occurs, a system event occurred, an SMI occurred through the Serial Interrupt bus, or when an ACPI SMI is generated. SMI_SB is an active high output to a PCI Bus Host Controller and will remain asserted until software clears the condition causing the SMI. **NOTE:** This signal is driven by a Totem Pole driver. **NOTE:** The ACPI output is a combination of the legacy PC87560 and ACPI SMIs. These two sources are internally ORed to drive the SMI_SB signal.
SUSPEND#	H1	I	3/5VT_PM	**SUSPEND.** This input signal is driven by the ACPI Embedded Controller to acknowledge entering and exiting the ACPI sleep states S3-S1.The Embedded Controller will assert SUSPEND# low in response to the PC87560 asserting the SLPEN# signal low. This results in the system entering one of the S1-S3 states depending on the programming of the Sleep Type bits (SLP_TYP[2:0]). When the Embedded Controller de-asserts SUSPEND# high (after asserting it low), the PC87560 will transition from S3-S1 back to S0 by clearing the SLP_EN bit. **NOTE:** The Sleep Type bits (SLP_TYP[2:0]) will not be effected when SLP_EN is cleared by the rising edge of SUSPEND#.
USB_INT/ GPIO6	D5	I/O	3/5VT	**USB Interrupt Output or General Purpose I/O 6.** When this pin is configured as a GP I/O pin, this pin is accessed through the General Purpose I/O register Bit 6. When this pin is configured as the USB_INT pin, it will be the output of the USB Host Controller's Interrupt Request.

4.8 UNIVERSAL SERIAL BUS (USB) HOST CONTROLLER INTERFACE

TABLE XII. USB Host Controller Interface

Symbol(s)	Pin(s)	Type	Voltage	Function
OC_SENSE1#	L4	I	3/5VT	**Over-Current Sense Port 1 input.** USB Root Hub Over-Current Sense Port 1 is used in conjunction with an external bus power regulator to indicate to the host controller when a bus overcurrent shutdown has occurred.
OC_SENSE2#	M1	I	3/5VT	**Over-Current Sense Port 2 input.** USB Root Hub Over-Current Sense Port 2 is used in conjunction with an external bus power regulator to indicate to the host controller when a bus overcurrent shutdown has occurred.
PORT1D+, PORT1D-	K3, K2	I/O	3V	**Port 1 Differential Signal Pair.** USB Root Hub Differential Signal pair for Port 1.
PORT2D+, PORT2D-	L1, L2	I/O	3V	**Port 2 Differential Signal Pair.** USB Root Hub Differential Signal pair for Port 2.
PWRCTL1#	M2	O	3/5V	**Power Control Port 1 Output.** USB Root Hub Control Port 1 is used in conjunction with an external USB bus power regulator to enable or disable bus power.
PWRCTL2#	M3	O	3/5V	**Power Control Port 2 Output.** USB Root Hub Control Port 2 is used in conjunction with an external USB bus power regulator to enable or disable bus power.
USB_ACT	K4	O	3/5V_PM	**USB Activity.** When active (high), this output indicates that there has been activity on the USB ports. The USB Status (USB_STS) bit is set any time there is a transition on either USB Receiver.This output is used to support ACPI wake-up via activity on the USB ports.

4.9 CLOCK SIGNALS

TABLE XIII. Clocks

Symbol(s)	Pin(s)	Type	Voltage	Function
14.318CLK	C1	I	3/5VT	**14.318 MHz Clock.**
48CLK	P1	I	3/5VT	**48 MHz Clock.**

4.10 MISCELLANEOUS SIGNALS

TABLE XIV. Miscellaneous

Symbol(s)	Pin(s)	Type	Voltage	Function
SINT	B9	I/O	3/5V	**Serial Interrupt I/O.** This signal is used for Serial Interrupt Input or Output for a Docking Interface.
SPKR	C2	O	3/5V	**Speaker Output.** This signal is used for Speaker Output.
TEST#	A2	I	3/5VT	**Test.** This input has a weak pull-up resistor and in normal operation should be a ***No Connect.***

4.11 POWER AND GROUND

TABLE XV. Power and Ground

Symbol(s)	Pin(s)	Type	Voltage	Function
AVSS	L3	USB GND		**Analog Ground.** This pin is the USB transceiver ground return. **NOTE:** This pin should be connected to the system ground plane on a separate trace from the digital VSS pins.
VDD	E7, E8, E10, E11, E13, E14, G5, G16, H5, H16, K5, K16, L5, L16, N5, N16, P5, P16, T7, T8, T10, T11, T13, T14	Power (Note 1)	3/5V	**+5V or +3.3V Core and I/O Buffer Power input.** These VDD pins are used to provide power to the core and to the I/O buffers (except for the ACPI circuitry and I/Os).
VDD_PM	G1	Power (Note 1)	3/5V	**+5V or +3.3V Power Management and I/O Power input.** This VDD_PM pin provides power to the ACPI circuitry and to the I/Os only.
VREF	K1	USB Power	3V	**Voltage Reference.** USB 3.3 Volt voltage reference. 3.3 Volts must be supplied to this pin from an external regulator if VDD=VDD_PM=3.3 Volts. The USB_REG_EN bit (Bit) of the USB Regulator Control Register at ACPIBAR+1Fh) is used to select the PC87560's on-chip regulator. Following a PM_PWRGOOD transition, the PC87560's on-chip regulator will be disabled. **NOTE:** If an external regulator is used, it must be sequenced at the same time as VDD_PM. When the PC87560's on-chip regulator is used, a 10 microfarad capacitor should be connected externally to the VREF and AVSS pins to provide additional stability. No other device should be connected to this pin when the PC87560's on-chip regulator is enabled.
VSS	E5, E6, E9, E12, E15, E16, F5, F16, J5, J9, J10, J11, J12, J16, K9, K10, K11, K12, L9, L10, L11, L12, M5, M9, M10, M11, M12, M16, R5, R16, T5, T6, T9, T12, T15, T16	GND		**Ground**.

Note 1. When powered on, both VDD and VDD_PM must be the same voltage (VDD=5V and VDD_PM=5V) or (VDD=3.3V and VDD_PM=3.3V). Furthermore VDD_PM may be powered by either 5V or 3.3V when VDD is not being powered, but VDD_PM must be present ***before or at the same time as*** VDD is applied.

4.12 PIN NUMBER TO SIGNAL SYMBOL CROSS-REFERENCE

Pin	Signal Symbol
A1	NC
A2	TEST#
A3	GPIO2
A4	IDE_INT2/GPIO5
A5	CPURST
A6	NMI
A7	PMCS#
A8	RTCCS#
A9	INTA#
A10	CLKRUN#
A11	LOCK#
A12	SERR#
A13	PERR#
A14	PCICLK
A15	AD29
A16	AD25
A17	AD21
A18	AD18
A19	AD15
A20	NC
B1	NC
B2	NC
B3	ID3/GPIO1
B4	IDE_INT1/GPIO4
B5	FGA20
B6	IGNNE#
B7	BSER1TO3
B8	KBCS#
B9	SINT
B10	INTD#
B11	FRAME#
B12	IRDY#
B13	SIOREQ#
B14	IDSEL
B15	AD28
B16	AD24
B17	AD20
B18	AD17
B19	NC
B20	NC
C1	14.318CLK
C2	SPKR
C3	AEN/GPIO0
C4	GPIO3

Pin	Signal Symbol
C5	CPUINT
C6	FERR#
C7	BSER3TO1
C8	KBGA20
C9	KBINT
C10	INTC#
C11	STOP#
C12	TRDY#
C13	SIOGNT#
C14	AD31
C15	AD27
C16	AD23
C17	AD19
C18	AD14
C19	AD13
C20	AD12
D1	MTR1#
D2	DENSL1
D3	DENSL0
D4	NC
D5	USB_INT/GPIO6
D6	CPUINIT
D7	BSERCLK3
D8	KBRST#
D9	MINT
D10	INTB#
D11	DEVSEL#
D12	PAR
D13	PCIRST#
D14	AD30
D15	AD26
D16	AD22
D17	AD16
D18	AD11
D19	AD10
D20	AD9
E1	DIR#
E2	DS0#
E3	DS1#
E4	MTR0#
E5	VSS
E6	VSS
E7	VDD
E8	VDD

Pin	Signal Symbol
E9	VSS
E10	VDD
E11	VDD
E12	VSS
E13	VDD
E14	VDD
E15	VSS
E16	VSS
E17	AD8
E18	AD7
E19	AD6
E20	AD5
F1	HDSEL#
F2	WGATE#
F3	WDATA#
F4	STEP#
F5	VSS
F6	NC
F7	NC
F8	NC
F9	NC
F10	NC
F11	NC
F12	NC
F13	NC
F14	NC
F15	NC
F16	VSS
F17	AD4
F18	AD3
F19	AD2
F20	AD1
G1	VDD_PM
G2	INDEX#
G3	MSEN1
G4	MSEN0
G5	VDD
G6	NC
G7	NC
G8	NC
G9	NC
G10	NC
G11	NC
G12	NC

Pin	Signal Symbol
G13	NC
G14	NC
G15	NC
G16	VDD
G17	AD0
G18	C/BE3
G19	C/BE2
G20	C/BE1
H1	SUSPEND#
H2	RESET_IN#
H3	SLPEN#
H4	PM_PWRGOOD
H5	VDD
H6	NC
H7	NC
H8	NC
H9	NC
H10	NC
H11	NC
H12	NC
H13	NC
H14	NC
H15	NC
H16	VDD
H17	C/BE0
H18	NC
H19	NC
H20	NC
J1	SMI_SB
J2	EX_PME/GPIO7
J3	EX_PME_EC/EVENT1
J4	RTCINT#
J5	VSS
J6	NC
J7	NC
J8	NC
J9	VSS
J10	VSS
J11	VSS
J12	VSS
J13	NC
J14	NC
J15	NC
J16	VSS
J17	NC

Pin	Signal Symbol
J18	DACK0#/DOCKEN#
J19	DACK1#/FENCFG
J20	DACK2#/FGA20EN
K1	VREF
K2	PORT1D-
K3	PORT1D+
K4	USB_ACT
K5	VDD
K6	NC
K7	NC
K8	NC
K9	VSS
K10	VSS
K11	VSS
K12	VSS
K13	NC
K14	NC
K15	NC
K16	VDD
K17	DACK3#/SIRQMST
K18	DRQ0
K19	DRQ1
K20	DRQ2
L1	PORT2D+
L2	PORT2D-
L3	AVSS
L4	OC_SENSE1#
L5	VDD
L6	NC
L7	NC
L8	NC
L9	VSS
L10	VSS
L11	VSS
L12	VSS
L13	NC
L14	NC
L15	NC
L16	VDD
L17	NC
L18	NC
L19	ROMCS#
L20	DRQ3
M1	OC_SENSE2#
M2	PWRCTL1#

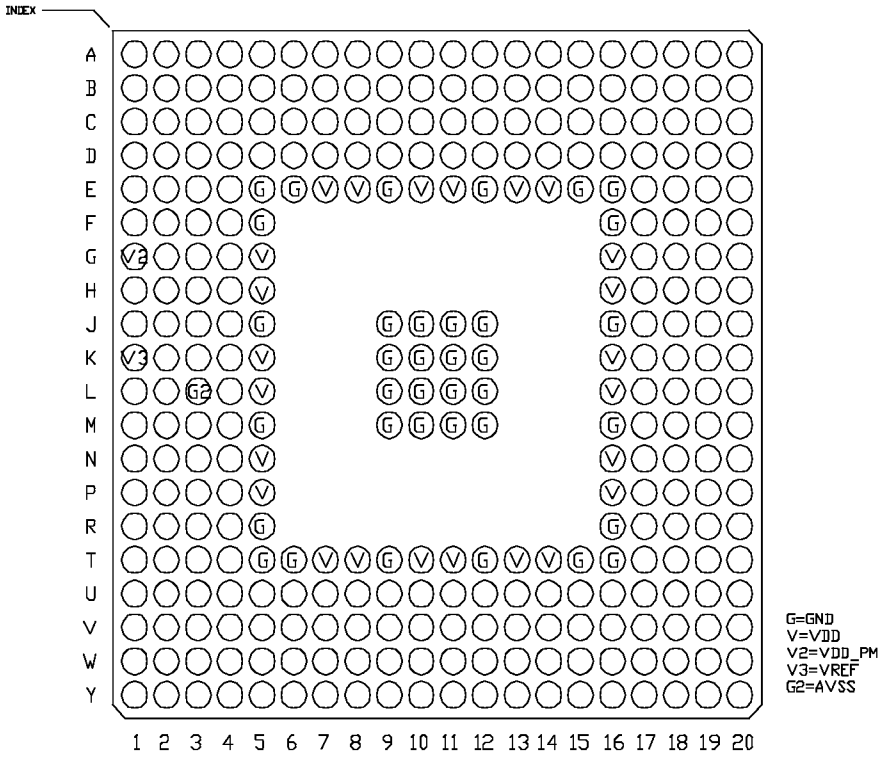
Pin	Signal Symbol
M3	PWRCTL2#
M4	TRK0#
M5	VSS
M6	NC
M7	NC
M8	NC
M9	VSS
M10	VSS
M11	VSS
M12	VSS
M13	NC
M14	NC
M15	NC
M16	VSS
M17	NC
M18	BHE#
M19	NC
M20	NC
N1	WP#
N2	RDATA#
N3	DSKCHG#
N4	PNF
N5	VDD
N6	NC
N7	NC
N8	NC
N9	NC
N10	NC
N11	NC
N12	NC
N13	NC
N14	NC
N15	NC
N16	VDD
N17	NC
N18	NC
N19	NC
N20	NC
P1	48CLK
P2	STB#/WRITE#
P3	PD0/INDEX#
P4	PD1/TRK0#
P5	VDD
P6	NC
P7	NC

Pin	Signal Symbol
P8	NC
P9	NC
P10	NC
P11	NC
P12	NC
P13	NC
P14	NC
P15	NC
P16	VDD
P17	NC
P18	NC
P19	AUDIOCS#
P20	FXASTB#
R1	PD2/WP#
R2	PD3/RDATA#
R3	PD4/DSKCHG#
R4	PD5/MSEN0
R5	VSS
R6	NC
R7	NC
R8	NC
R9	NC
R10	NC
R11	NC
R12	NC
R13	NC
R14	NC
R15	NC
R16	VSS
R17	FXA3/IDE_3V_EN#
R18	FXA3
R19	FXA2
R20	FXA0
T1	PD7/MSEN1
T2	PD6/DENSL1
T3	ACK#/DS1#
T4	BUSY#/WAIT#/MTR1#
T5	VSS
T6	VSS
T7	VDD
T8	VDD
T9	VSS
T10	VDD
T11	VDD
T12	VSS

Pin	Signal Symbol
T13	VDD
T14	VDD
T15	VSS
T16	VSS
T17	FXA7/FXD3
T18	FXA6/FXD2
T19	FXA5/FXD1
T20	FXA4/FXD0
U1	PE/WDATA#
U2	SLCT/WGATE#
U3	SLIN#/ASTB#/STEP#
U4	DCD0#
U5	DTR0#
U6	ID[0]/IRSEL0/IRRX2
U7	DSR1#
U8	CTS1#
U9	CH1_CS1#
U10	CH1_DMACK#
U11	DIOR#
U12	DD13
U13	DD9
U14	DD5
U15	DD1
U16	DA0
U17	FXA13/FXD9
U18	FXA10/FXD6
U19	FXA9/FXD5
U20	FXA8/FXD4
V1	INIT#/DIR#
V2	ERR#/HDSEL#
V3	AFD#/DSTRB#/ DENSL0
V4	RTS0#
V5	RI0#
V6	ID1/IRSEL1
V7	SIN1
V8	DTR1#
V9	CH1_CS3#
V10	CH2_CS1#
V11	DIORDY
V12	DD14
V13	DD10
V14	DD6
V15	DD2
V16	DA1

Pin	Signal Symbol
V17	FXA18/FXD14
V18	FXA15/FXD11
V19	FXA12/FXD8
V20	FXA11/FXD7
W1	NC
W2	NC
W3	DSR0#
W4	SOUT0
W5	IRTX
W6	ID2/IRSEL2
W7	RTS1#
W8	RI1#
W9	CH1_INT
W10	CH2_CS3#
W11	CH2_DMACK#
W12	DD15
W13	DD11
W14	DD7
W15	DD3
W16	DA2
W17	FXA19/FXD15
W18	FXA16/FXD12
W19	NC
W20	FXA14/FXD10
Y1	NC
Y2	NC
Y3	SIN0
Y4	CTS0#
Y5	IRRX
Y6	DCD1#
Y7	SOUT1
Y8	DRST#
Y9	CH1_DMREQ
Y10	CH2_INT
Y11	CH2_DMREQ
Y12	DIOW#
Y13	DD12
Y14	DD8
Y15	DD4
Y16	DD0
Y17	FXA[20]/POWERPC
Y18	FXA17/FXD13
Y19	NC
Y20	NC

4.13 CONNECTION DIAGRAM



316-pin Pin Ball Grid Array (PBGA) Package
Order Number PC87560UBD
NS Package Number UBD316

Viewed from the Top (looking through the package)

5.0 Functional Overview

The PC87560 is a highly integrated IC which incorporates PCI Interface, Bus Mastering Fast IDE Controller, Universal Serial Bus (USB) Host Controller functions, commonly-used I/O peripheral functions, and power management functions for efficient design of notebook computers and docking stations. When used in conjunction with the PC87550, the PC87560 provides all the peripheral and power management functions for a complete PCI-based, AT-compatible computer system. The PC87560 enables implementation of Plug and Play systems including dongle support. It operates at 3.3V or 5V and is available in a 316-pin BGA package.

5.1 PCI INTERFACE

The on-chip PCI Interface is PCI 2.1 and PCI Mobile Design Guide 1.0 compliant. The chip provides a 32-bit PCI bus with up to 33 MHz PCI Bus frequency and reset control. Address re-mapping via PCI configuration registers is provided for all internal functions to support Plug and Play-capable systems. Positive decoding is supported for notebook designs and subtractive decoding is supported for docking station applications.

5.2 FAST BUS MASTER IDE CONTROLLER

The IDE Controller provides SFF 8038 compliant Bus Mastering. Two IDE channels, primary and secondary, are supported with programmable IDE access timing per channel/drive. A multi-tasking DMA engine assures channel concurrency. Ten double-word write FIFOs per channel sustain 16 MBytes/sec maximum transfer rate on the IDE bus with bursts of eight double-words on the PCI Bus. ATAPI with SFF8022i compliance and ANSI ATA PIO modes 0-4 and DMA modes 0-2 are supported.

5.3 I/O PERIPHERALS

Peripheral functions provided by the PC87560 include one Floppy Disk Controller (FDC), one parallel port, and two 16550 serial ports. The second serial port may be configured as a standard serial port or as a Universal Infrared (UIR) serial port. To optimize design flexibility, each internal peripheral function can be individually disabled.

5.3.1 Floppy Disk Controller

The Floppy Disk Controller (FDC) is software compatible with the DP8477, the NEC µPD765A, and the N82077. Tri-mode floppy drive support as well as Perpendicular Recording and enhanced Tape Drive Register (TDR) support are provided. FDC performance is optimized by its 65% dynamic window margin. One legacy DMA channel is supported and the Floppy Interface is multiplexed on the parallel port for optional attachment of an external floppy drive.

5.3.2 IEEE 1284 Compatible Parallel Port

The IEEE 1284-compatible parallel port supports all five operational modes: Compatibility mode, Nibble mode, Byte mode, Extended Capabilities Port (ECP) mode and Enhanced Parallel Port (EPP) 1.7 and 1.9 modes. In addition, one legacy DMA channel is supported.

5.3.3 Serial Ports

Two standard serial ports (16550 UARTs) are integrated on-chip. The second serial port is configurable as either a standard serial port or as an Universal Infrared (UIR) serial port. MIDI baud rate is supported by both ports.

5.3.3.1 Standard Serial Ports

The NS16550A compatible serial ports support MIDI baud rates and are capable of supporting up to 1.5 Mbaud baud rates.

5.3.3.2 Universal Infrared Port

The Universal Infrared (UIR) port is IrDA 1.0 SIR, IrDA 1.1 MIR and FIR, Sharp-IR and Consumer Remote compatible. Both 1.152 Mb/sec and 4 Mb/sec rates supported. Pulse width is programmable to either 1.6 µs or 3/16 of a bit time. Two independent Scatter/Gather DMA channels are integrated on-chip (one receive, the other transmit). Two legacy 8237 DMA channels are supported as well. Transmit deferral is supported. Transmit and receive FIFOs have selectable 16- or 32-level thresholds.

5.4 SYSTEM INTERFACE

The System Interface functions provided by the PC87560 include two DMA Controllers, an FX Bus, interfaces to ROM/FLASH ROM, Keyboard controller, Real-time Clock, two 8259 Interrupt Controllers, and an 8254-compatible System Timer. The X86 CPU interface supports numeric coprocessor error support (via Port F0).

5.4.1 DMA Controllers

The legacy and distributed DMA Controllers support seven 8237 compatible channels in both Master and Slave modes. DMA channel routing is provided for Plug and Play compatibility. Two double-word buffers facilitate PCI Bus transfers and support is provided for preemption and re-arbitration for each PCI Bus transfer cycle. ISA-compatible Type “A”, “B”, and “F”, timing is also supported.

5.4.2 FX Bus

I/O subsystem expansion is enabled via a 16-bit Fast Expansion Bus (FX Bus). The FX Bus (a non-Bus Master ISA Bus) has programmable timing for ISA-compatible peripherals, two programmable I/O range Chip Selects, one programmable memory range, and one programmable fragmented I/O window with Chip Select (for Sound Blaster compatibility). Support for IORDY, IOCS16# and MEMCS16# signals, four DMA channels, and three interrupt channels is also provided.

5.4.3 Interfaces to System Devices

Interfaces are provided to ROM/FLASH ROM, a Keyboard Controller (KBC), and a Real Time Clock (RTC). X86 CPU interface support is also provided.

5.4.3.1 ROM/FLASH ROM Interface

The ROM/FLASH ROM Interface supports up to 256KBytes of ROM or FLASH ROM. It supports up to 1 MB of ROM/ FLASH ROM in PowerPC mode.

5.4.3.2 Keyboard Controller Interface

The Keyboard Controller (KBC) interface communicates with either 8051 or PC87570 style keyboard controllers. The Keyboard Chip Select is re-mappable anywhere in the 64-KByte I/O range. Fast GateA20 and Fast Keyboard Reset are supported.

5.4.3.3 Real-Time Clock Interface

The Real-Time Clock (RTC) Interface supports DS1287 style clocks.

5.4.4 Interrupt Controllers

Two 8259 Interrupt Controllers support PCI native interrupts. Both edge–triggering and level–triggering are individually programmable for each interrupt line for docking station support. Programmable interrupt routing is provided for Plug and Play operation. In addition, the PCIway Serial Interrupt is supported in both Master and Slave modes.

5.4.5 System Timer

The 8254–compatible system timer provides three timer channels.

5.5 POWER MANAGEMENT

The PC87560 features Advanced Configuration and Power Interface (ACPI) revision 1.0 compliance. Eight general purpose I/Os ports, peripheral port access monitors (for the FDC, parallel, serial, and IDE ports), back powering protection (from a connected printer, the FDC interface, and the IDE Controller interface), CLKRUN# signal support, one system event register, and a full set of shadow registers complete the standard power management functions supported by the device. An additional Burst Serial Interface (BSER) is contained on-chip for designs which utilize the PC87560 in conjuction with the PC87550 Host Bridge. In these designs, the BSER communicates PC87560 power management activity to the PC87550. Power management control is provided by the North Bridge (PC87550) when the PC87560 is operating in Slave mode.

5.6 UNIVERSAL SERIAL BUS (USB) HOST CONTROLLER

The Universal Serial Bus (USB) Host Controller is USB 1.0 and OpenHCI 1.0a compliant. It contains a PCI Master Scatter/Gather DMA channel and two root hub ports. Transfer protocols for both Full-Speed (FS) and Low-Speed (LS) USB devices are supported. An optimized List-Queue Manager is used for transfer scheduling and management. The USB Host Controller supports dynamic re-scheduling of data transfers and real-time device attaching/detaching. The PC87560 also provides legacy keyboard/mouse emulation, integrated transceivers, and comprehensive power management support.

6.0 Register Summary

The PC87560 has PCI Configuration Registers and Standard I/O Registers. The device has three configuration register sets, one each for the IDE Controller, the I/O Peripherals, and the USB Controller. The standard I/O registers are accessed through the PCI bus and are used with the DMA Controllers, Timers, Interrupt Controllers, Serial Ports, Parallel Port, Floppy Disk Controller, Power Management functions.

6.1 CONFIGURATION REGISTERS SUMMARY

The PC87560 will acknowledge all PCI Bus Configuration cycles (by asserting DEVSEL# active low) when the IDSEL input is asserted high, address bits 1-0 of the Configuration cycle are both zeros, and address bits 10-8 correspond to one of the three internal functions.

The Configuration Registers can be accessed as byte, word (16 bits) or DWord (32 bits) quantities. In all of these accesses only byte enables are used; AD[1:0] is always 00b when accessing the Configuration Registers. All multi-byte fields use "little-endian" ordering (that is, lower addresses contain the least significant parts of the fields). Registers marked “Reserved” will be decoded and will return zeros when read unless otherwise noted. “x” in an address indicates a “Don’t care”.

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TABLE XVI. Function 000b (IDE) Configuration Registers

Address/Register Number (hex)	R/W	Description	Default Value (hex)
00-01	R	Vendor ID	100B
02-03	R	Device ID	0002
04-05	R/W	Command Register (CMD)	0000
06-07	R/W	Status Register (SR)	0200
08	R	Rev ID	03
09	R/W	Programming Interface (PIF)	8A
0A	R	Sub-Class Code	01
0B	R	Class Code	01
0C	R/W	Cache Line Size	00
0D	R/W	Latency Timer	00
0E	R	Header Type	80
0F	R	Reserved	All zeros
10-13	R/W	Base Address Register 0 (F0BAR0)	FFFFFFF9
14-17	R/W	Base Address Register 1 (F0BAR1)	FFFFFFFD
18-1B	R/W	Base Address Register 2 (F0BAR2)	FFFFFFF9
1C-1F	R/W	Base Address Register 3 (F0BAR3)	FFFFFFFD
20-23	R/W	Base Address Register 4 (F0BAR4)	FFFFFFF1
24-3F	R	Reserved	All zeros
40	R/W	IDE Control Register 1	00
41	R/W	IDE Control Register 2	00
42	R/W	IDE Control Register 3	00
43	R	Write Buffer Status	00
44	R/W	IDE Channel 1 Device 1 Data Read Timing Register	85
45	R/W	IDE Channel 1 Device 1 Data Write Timing Register	85
46-47	R	Reserved	All zeros
48	R/W	IDE Channel 1 Device 2 Data Read Timing Register	85
49	R/W	IDE Channel 1 Device 2 Data Write Timing Register	85
4A-4B	R	Reserved	All zeros
4C	R/W	IDE Channel 2 Device 1 Data Read Timing Register	85
4D	R/W	IDE Channel 2 Device 1 Data Write Timing Register	85
4E-4F	R	Reserved	All zeros
50	R/W	IDE Channel 2 Device 2 Data Read Timing Register	85
51	R/W	IDE Channel 2 Device 2 Data Write Timing Register	85
52-53	R	Reserved	All zeros
54	R/W	IDE Command and Control Block Timing Register	B7
55	R/W	IDE Sector size	EE
56-57	R	Reserved	All zeros
58	R	Channel 1 Drive 0 Device Control Register	xx
59	R	Channel 1 Drive 1 Device Control Register	xx
5A-5B	R	Reserved	All zeros

TABLE XVI. Function 000b (IDE) Configuration Registers (Continued)

Address/Register Number (hex)	R/W	Description	Default Value (hex)
5C	R	Channel 2 Drive 0 Device Control Register	xx
5D	R	Channel 2 Drive 1 Device Control Register	xx
5E-FF	R	Reserved	All zeros

TABLE XVII. Function 001b (I/O Peripherals) Configuration Registers

Address/Register Number (hex)	R/W	Description	Default Value (hex)
00-01	R	Vendor ID	100B
02-03	R	Device ID	0011 or 000E
04-05	R/W	Command Register (CMD)	000F
06-07	R/W	Status Register (SR)	0200
08	R	Rev ID	01
09	R/W	Programming Interface (PIF)	00
0A	R	Sub-Class Code	80
0B	R	Class Code	06
0C	R/W	Cache Line Size	00
0D	R/W	Latency Timer	00
0E	R	Header Type	80
0F-3F	R	Reserved	All zeros
40-43	R/W	FX Bus I/O Region 0 Base Address Register	00000000
44-47	R/W	FX Bus I/O Region 1 Base Address Register	00000000
48-4B	R/W	FX Bus I/O Region 2 Base Address Register	00000000
4C-4F	R/W	Distributed DMA Remap Base Address Register	00000000
50-53	R/W	Reserved	All zeros
54-57	R	Reserved	All zeros
58-59	R/W	System Configuration Register	0024
5A-5B	R/W	Function Enable Register For Decoding	FFBF
5C	R/W	System I/O Configuration Register	00
5D	R/W	Special Function Enable Register	00
5E	R	Parallel Port Identification Register (PPDID)	10
5F	R/W	Parallel Port Mode Select Register	00
60	R	Reserved	All zeros
61	R/W	DMA Routing Control Register 4	00
62	R/W	ROM Configuration Register	00
63	R/W	DMA Routing Control Register 1	67
64	R/W	DMA Routing Control Register 2	00
65	R/W	DMA Routing Control Register 3	00
66	R/W	DMA Channel Control Register	00
67-68	R/W	Interrupt Level/Edge triggering Control Registers 1 and 2	0000
69-6C	R/W	Interrupt Routing Control Registers 1–4	00FE6534
6D-70	R/W	Interrupt Routing Control Registers 5–8	0000C100
71	R/W	Interrupt Routing Control Registers 9	00
72-73	R/W	Internal (FM Master Bus) Arbiter Control Register	4C88
74-75	R/W	FX Bus I/O Region 2 Mask Register	All zeros
76-77	R/W	FX Bus Timing Control Register	00
78	R/W	FX Bus Control Register	00
79	R/W	General Purpose I/O Configuration Register	00
7A	R/W	General Purpose I/O Direction Register	00
7B	R/W	Serial Interrupt Control Register	00
7C-7D	R/W	Serial Interrupt Enable Register	0000
7E	R/W	Reserved Configuration Offset 7Eh Register	01
7F	R/W	Audio Chip Select Control Register	00
80-83	R/W	FX Bus Memory Range Control Register 1	00000000
84-87	R/W	Keyboard Controller Base Address Register (KBCBAR)	00000060
88-8B	R/W	Advance Configuration and Power Interface Base Address Register (ACPIBAR)	00000000
8C-8F	R/W	Power Management Base Address Register (PMBAR0)	FFFFFF01

TABLE XVII. Function 001b (I/O Peripherals) Configuration Registers (Continued)

Address/Register Number (hex)	R/W	Description	Default Value (hex)
90-93	R/W	Floppy Disk Controller Base Address Register (FDCBAR)	000003F1
94-97	R/W	Serial Port 1 Base Address Register (SP1BAR)	000003F9
98-9B	R/W	Serial Port 2 Base Address Register (SP2BAR)	000002F9
9C-9F	R/W	Parallel Port Base Address Register (PPBAR)	00000379
A0-FF	R	Reserved	All zeros

TABLE XVIII. Function 010b (USB) Configuration Registers

Address/Register Number (hex)	R/W	Description	Default Value (hex)
00-01	R	Vendor ID	100B
02-03	R	Device ID	0012
04-05	R/W	Command Register (CMD)	0000
06-07	R/W	Status Register (SR)	0000
08	R	Rev ID	01
09	R	Programming Interface (PIF)	10
0A	R	Sub-Class Code	03
0B	R	Class Code	0C
0C	R	Reserved	All zeros
0D	R/W	Latency Timer	00
0E	R	Header Type	80
0F	R	Reserved	All zeros
10-13	R/W	Open HCI Base Address Register (OHCIBAR)	00000000
14-17	R/W	NSC USB Base Address Register (NUSBBAR)	00000000
18-3B	R	Reserved	All zeros
3C	R/W	Interrupt Line Register	FF
3D	R	Interrupt Pin Register	04
3E-FF	R	Reserved	All zeros

6.2 OPERATIONAL REGISTERS SUMMARY

Table XIX, Table XX, and Table XXI list a summary of the operational registers in each of the three major function blocks of the PC87560. The I/O peripherals (Function 001) registers are organized by each of the devices within this function.

All multi-byte fields use "little-endian" ordering (that is, lower addresses contain the least significant parts of the fields). Registers marked “Reserved” will be decoded and will return zeros when read unless otherwise noted. “x” in an address indicates a “Don’t care”.

TABLE XIX. Function 000b (IDE) Operational Registers Summary

Base Address	I/O Address/ Offset (hex)	Fixed or Mappable	Read/ Write	Description	Default Value (hex)
F0BAR4	00	F	R/W	Channel 1 Bus Master IDE Command Register	00
F0BAR4	01			Reserved	All zeros
F0BAR4	02	F	R/W	Channel 1 Bus Master IDE Status Register	00
F0BAR4	03			Reserved	All zeros
F0BAR4	04-07	F	R/W	Channel 1 Bus Master IDE PRD Table Address	00000000
F0BAR4	08	F	R/W	Channel 2 Bus Master IDE Command Register	00
F0BAR4	09			Reserved	All zeros
F0BAR4	0A	F	R/W	Channel 2 Bus Master IDE Status Register	00
F0BAR4	0B			Reserved	All zeros
F0BAR4	0C-0F	F	R/W	Channel 2 Bus Master IDE PRD Table Address	00000000
F0BAR2	(0170-0177h default)	M	R/W	IDE Channel 2 Data and Command Registers (legacy mode) (Note 2)	Unspecified
F0BAR0	(01F0-01F7h default)	M	R/W	IDE Channel 1 Data and Command Registers (legacy mode) (Note 2)	Unspecified
F0BAR3	(0376h default)	M	R/W	IDE Channel 2 Control Register (legacy mode) (Note 2)	Unspecified
F0BAR1	(03F6h default)	M	R/W	IDE Channel 1 Control Register (legacy mode) (Note 2)	Unspecified

Note 2: Only the I/O decoding is performed on-chip. This register resides external to the PC87560 device.

TABLE XX. Function 001b (I/O Peripherals) Operational Registers Summary

Base Address	I/O Address/ Offset (hex)	Fixed or Remapp-able	Read/ Write	Description	Default Value (hex)
Floppy Disk Controller (Default I/O Address range is 03F0-03F7h; except for 03F6h)					
FDCBAR	00	M	R	Status Register A (SRA)	00
FDCBAR	01	M	R	Status Register B (SRB)	C7
FDCBAR	02	M	R/W	Digital Output Register (DOR)	00
FDCBAR	03	M	R/W	Tape Drive Register (TDR)	10
FDCBAR	04	M	R	Main Status Register (MSR)	00
FDCBAR	04	M	W	Data Rate Select Register (DSR)	02
FDCBAR	05	M	R/W	Data Register (FIFO)	
FDCBAR	07	M	R	Digital Input Register (DIR)	79
FDCBAR	07	M	W	Configuration Control Register (CCR)	02
Parallel Port (Default I/O Address range is 0378-03F7h)					
PPBAR	00	M	R/W	SPP/EPP Data Register (DTR)	00
PPBAR	01	M	R	SPP/EPP Status Register (STR)	FF
PPBAR	02	M	R/W	SPP/EPP Control Register (CTR)	C4
PPBAR	03	M	R/W	EPP/ECP Address (ADDR)	00

TABLE XX. Function 001b (I/O Peripherals) Operational Registers Summary (Continued)

Base Address	I/O Address/ Offset (hex)	Fixed or Remapp-able	Read/ Write	Description	Default Value (hex)
PPBAR	04	M	R/W	EPP Data Port 0 (DATA0)	00
PPBAR	05	M	R/W	EPP Data Port 1 (DATA1)	00
PPBAR	06	M	R/W	EPP Data Port 2 (DATA2)	00
PPBAR	07	M	R/W	EPP Data Port 3 (DATA3)	00
PPBAR	000	M	R/W	ECP Data Register (DATAR)	00
PPBAR	000	M	W	ECP Address FIFO Register (AFIFO)	00
PPBAR	001	M	R	ECP Status Register (DSR)	07
PPBAR	002	M	R	ECP Control Register (DCR)	0D
PPBAR	400	M	W	Parallel Port Data FIFO Register (CFIFO)	00
PPBAR	400	M	R/W	ECP Data FIFO (DFIFO)	00
PPBAR	400	M	R/W	Test FIFO Register (TFIFO)	00
PPBAR	400	M	R	Configuration Register A (CNFGA)	15
PPBAR	401	M	R	Configuration Register B (CNFGB)	00
PPBAR	402	M	R	Extended Control Register (ECR)	15
PPBAR	403	M	R/W	ECP Extended Index Register (EIR)	00
PPBAR	404	M	R/W	ECP Extended Data Register (EDR)	00
PPBAR	405	M	R	ECP Extended Auxiliary Status Register (EAR)	00
	00	M	R	Control0, Second Level	00
	02	M	R	Control2, Second Level	00
	04	M	R	Control4, Second Level	07
	05	M	R	PP Confg0, Second Level	00
Serial Ports					
SP2BAR	02F8h-02FFh	M		Serial Port 2 (Note 4)	
SP1BAR	03F8h-03FFh	M		Serial Port 1 (Note 4)	
DMA Controllers					
	0000-000F	F		Legacy 8237 DMA Channels 3-0 (Note 4)	
	0080-008F	F		Legacy 8237 DMA Low Page Segment Address Registers (Note 4)	
	00C0-00DF	F		8237 DMA 2 Channels 5-7 (Note 4)	
	040B	F		DMA Channels 3-0 Extended Mode Register	
	0480-048F	F		Legacy 8237 DMA High Page Segment Address Registers (Note 4)	
	04D6	F		DMA Channels 7-5 Extended Mode Register	
External Devices and Legacy I/O					
KBCBAR	0 (0060 default)	M	R/W	Keyboard Controller Data Port (Note 3)	xx
	0061	F	R/W	Port 61	00
KBCBAR	0062, 0066	M		VM KBC Power Management Registers (Note 3)	xx
KBCBAR	4 (0064 default)	M	R/W	Keyboard Controller Command Port (Note 3)	xx

TABLE XX. Function 001b (I/O Peripherals) Operational Registers Summary (Continued)

Base Address	I/O Address/ Offset (hex)	Fixed or Remapp-able	Read/ Write	Description	Default Value (hex)
	0070-0071	F	R/W	Port 70, RTC and lower 128 Bytes of CMOS RAM (Note 3)	xxxx
	0092	F	R/W	Port 92	00
	00F0	F	W	Port F0	00
Interrupt Controllers and System Timer					
	0020-0021	F		8259 Interrupt Controller 1 Registers (Note 4)	
	0040-0043	F		8254 System Timer Registers (Note 4)	
	00A0-00A1	F		8259 Interrupt Controller 2 Registers (Note 4)	
Power Management (Default I/O Address is 00-FFh for registers mappable from PMBAR)					
PMBAR	00	M	R/W	General Purpose I/O Register	00
PMBAR	01			Reserved	All zeros
PMBAR	02	M	R	Miscellaneous Status Register	00
PMBAR	03	M	R/W	TRI-STATE Control Register	00
PMBAR	04	M	R/W	Function Power Mode Register	3F
PMBAR	05	M	R/W	Serial Port 2 Power Mode Register	01
PMBAR	06	M	R	Global Status Register	1C
PMBAR	07-0B			Reserved	All zeros
PMBAR	0C-0F	M	R/W	Global System Management Interrupt (SMI) I/O Trap Enable Register	00000000
PMBAR	10-13			Reserved	All zeros
PMBAR	14-17	M	R/WCM	Power Management Global Status Register	00000000
PMBAR	18-19	M	R/W	Primary Activity (PA) Enable Register	0000
PMBAR	1A-1B	M	R/W	Secondary Activity (SA) Enable Register	0000
PMBAR	1C-53			Reserved	All zeros
PMBAR	54-57	M	R/W	System Event 1 Control Register	00000000
PMBAR	58-5B	M	R/W	System Event 1 Status Register	00000000
PMBAR	5C-6B			Reserved	All zeros
PMBAR	6C-AF	M		Zero Volt Suspend Shadow Registers	
PMBAR	B0-FF			Reserved	All zeros
	00B2	F	R/W	Advanced Power Management Control Register (APMC)	00
	00B3	F	R/W	Advanced Power Management Status Register (APMS)	00
ACPIBAR	00-01	M	R/WCM	Power Management 1b Status Register (PM1b_STS)	0000
ACPIBAR	02-03	M	R/W	Power Management 1b Enable Register (PM1b_EN)	0000
ACPIBAR	04-05	M	R/W	Power Management 1b Control Register (PM1b_CNT)	0000
ACPIBAR	06-07		R	Reserved	All zeros
ACPIBAR	08-0B	M	R	Power Management Timer Register (PM_TMR)	00000000
ACPIBAR	0C-0D	M	R/WCM	General Purpose Status Register (GP_STS)	0000
ACPIBAR	0E-0F	M	R/W	General Purpose Enable Register (GP_EN)	0000

TABLE XX. Function 001b (I/O Peripherals) Operational Registers Summary (Continued)

Base Address	I/O Address/ Offset (hex)	Fixed or Remapp-able	Read/ Write	Description	Default Value (hex)
ACPIBAR	10	M	R/WCM	ACPI BIOS Status Register (ACPI_BIOS_STS)	00
ACPIBAR	11	M	R/W	ACPI BIOS Enable Register (ACPI_BIOS_EN)	00
ACPIBAR	12	M	R/W	ACPI Function Control Register	00
ACPIBAR	13-1E		R	Reserved	All zeros
ACPIBAR	1F	M	R/W	USB Regulator Control Register	00

Note 3. Only the I/O decoding is performed on-chip. This register resides external to the PC87560 device.
Note 4. See the full datasheet for register listings and descriptions.

TABLE XXI. Function 010b (USB) Operational Registers Summary

Base Address	I/O Address/ Offset (hex)	Fixed or Remapp-able	R/W	Description	Default Value (hex)
OHCIBAR	000	M	R	HcRevision Register	00000110
OHCIBAR	004	M	R/W	HcControl Register	00000000
OHCIBAR	008	M	R/W	HcCommandStatus Register	00000000
OHCIBAR	00C	M	R/W	HcInterruptStatus Register	00000000
OHCIBAR	010	M	R/W	HcInterruptEnable Register	00000000
OHCIBAR	014	M	R/W	HcInterruptDisable Register	00000000
OHCIBAR	018	M	R/W	HcHCCA Register	00000000
OHCIBAR	01C	M	R/W	HcPeriodCurrentED Register	00000000
OHCIBAR	020	M	R/W	HcControlHeadED Register	00000000
OHCIBAR	024	M	R/W	HcControlCurrentED Register	00000000
OHCIBAR	028	M	R/W	HcBulkHeadED Register	00000000
OHCIBAR	02C	M	R/W	HcBulkCurrentED Register	00000000
OHCIBAR	030	M	R/W	HcDoneHead Register	00000000
OHCIBAR	034	M	R/W	HcFmInterval Register	00000000
OHCIBAR	038	M	R/W	HcFmRemaining Register	00000000
OHCIBAR	03C	M	R/W	HcFmNumber Register	00000000
OHCIBAR	040	M	R/W	HcPeriodicStart Register	00002A2F
OHCIBAR	044	M	R/W	HcLSThreshold Register	00000628
OHCIBAR	048	M	R/W	HcRhDescriptorA	00000000
OHCIBAR	04C	M	R/W	HcRhDescriptorB	00001203
OHCIBAR	050	M	R/W	HcRhStatus	00000000
OHCIBAR	054	M	R/W	HcRhPortStatus[1]	00000000
OHCIBAR	058	M	R/W	HcRhPortStatus[2]	00000000
OHCIBAR	05C	M	R/W	HcRhPortStatus[3] (Note 5)	00000000
OHCIBAR	060-FFF	M	R	Reserved	All zeros
NUSBBAR	00	M	R/W	NscControl Register	90000014
NUSBBAR	04	M	R/WCM	NscCommandStatus	00000000
NUSBBAR	08-30	M	R	Reserved	All zeros
NUSBBAR	34	M	R	NscRootHubStatus	00000000

Note 5. This port is not available externally.

7.0 Electrical Characteristics

7.1 DC SPECIFICATIONS

7.1.1 Absolute Maximum Ratings

(Notes 6 and 7)

Symbol	Parameter	Conditions	Min	Max	Units
V_{DD}	Supply Voltage		-0.5	7.0	V
V_I	Input Voltage		-0.5	V_{DD} + 0.5	V
V_O	Output Voltage		-0.5	V_{DD} + 0.5	V
T_{STG}	Storage Temperature		-65	+165	°C
P_D	Power Dissipation			1	W
T_{PKG}	Package Soldering Temperature (40 seconds)	Measured at top of package.		+220	°C

Note 6: Absolute Maximum Ratings are those values beyond which damage to the device may occur.
Note 7: Unless otherwise specified all voltages are referenced to ground.

7.1.2 Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{DD}	Supply Voltage	3.3V operation	3.0	3.3	3.6	V
V_{DD}	Supply Voltage	5V operation	4.75	5.0	5.25	V
T_A	Operating Temperature		0		+70	°C
V_{ZAP}	ESD Tolerance	C_{ZAP} = 100 pF, R_{ZAP} = 1.5 kW (Note 8)	1500			V

Note 8: Value based on test complying with NSC SOP5-028 human body model ESD testing using the ETS-910 tester.

7.1.3 5V On-State Supply Current

T_A = 25°C, PCICLK=33MHz, V_{DD}=V_{DD_PM}=5V, V_{REF}(EXTERNAL)=3.3V

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{DD}	Main (VDD) Supply Current	All measure-ments in system with DOS prompt running.		75.2		mA
I_{DD_PM}	Power Management (VDD_PM) Supply Current			204		µA
I_{REF}	USB Tranceiver Supply Current			4.2		mA

7.1.4 5V Doze-State Supply Current

T_A = 25°C, PCICLK=33MHz, V_{DD}=V_{DD_PM}=5V, V_{REF}(EXTERNAL)=3.3V

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{DD}	Main (VDD) Supply Current			27.5		mA
I_{DD_PM}	Power Management (VDD_PM) Supply Current			209		µA
I_{REF}	USB Tranceiver Supply Current			4.2		mA

7.1.5 5V Sleep-State Supply Current

T_A = 25°C, PCICLK=33MHz, V_{DD}=V_{DD_PM}=5V, V_{REF}(EXTERNAL)=3.3V

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{DD}	Main (VDD) Supply Current			27.5		mA
I_{DD_PM}	Power Management (VDD_PM) Supply Current			209		µA
I_{REF}	USB Tranceiver Supply Current			4.2		mA

7.1.6 5V Suspend-State Supply Current

T_A = 25°C, PCICLK=33MHz, V_{DD}=V_{DD_PM}=5V, V_{REF}(EXTERNAL)=3.3V

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{DD}	Main (VDD) Supply Current			0.1		µA
I_{DD_PM}	Power Management (VDD_PM) Supply Current			0.13		µA
I_{REF}	USB Tranceiver Supply Current			0.01		µA

7.1.7 3.3V On-State Supply Current

T_A = 25°C, PCICLK=33MHz, V_{DD}=V_{DD_PM}=3.3V, V_{REF}(EXTERNAL)=3.3V

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{DD}	Main (VDD) Supply Current	All measure-ments in system with DOS prompt running.		19.1		mA
I_{DD_PM}	Power Management (VDD_PM) Supply Current			65.1		µA
I_{REF}	USB Tranceiver Supply Current			4.2		mA

7.1.8 3.3V Doze-State Supply Current

T_A = 25°C, PCICLK=33MHz, V_{DD}=V_{DD_PM}=3.3V, V_{REF}(EXTERNAL)=3.3V

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{DD}	Main (VDD) Supply Current			6.85		mA
I_{DD_PM}	Power Management (VDD_PM) Supply Current			65.1		µA
I_{REF}	USB Tranceiver Supply Current			4.2		mA

7.1.9 3.3V Sleep-State Supply Current

T_A = 25°C, PCICLK=33MHz, V_{DD}=V_{DD_PM}=3.3V, V_{REF}(EXTERNAL)=3.3V

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{DD}	Main (VDD) Supply Current			6.85		mA
I_{DD_PM}	Power Management (VDD_PM) Supply Current			65.1		µA
I_{REF}	USB Tranceiver Supply Current			4.2		mA

7.1.10 3.3V Suspend-State Supply Current

T_A = 25°C, PCICLK=33MHz, V_{DD}=V_{DD_PM}=3.3V, V_{REF}(EXTERNAL)=3.3V

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{DD}	Main (VDD) Supply Current			0.1		µA
I_{DD_PM}	Power Management (VDD_PM) Supply Current			0.1		µA
I_{REF}	USB Tranceiver Supply Current			0.013		µA

7.1.11 Pin Capacitance (Excluding PCI Bus Signal Pins)

T_A = 25°C, f = 1 MHz

Symbol	Parameter	Conditions	Min	Typ	Max	Units
C_{IN}	Input Pin Capacitance			5	7	pF
C_{IN1}	Clock Input Capacitance			8	10	pF
C_{IO}	I/O Pin Capacitance			10	12	pF
C_O	Output Pin Capacitance			6	8	pF
C_{XCVR}	USB Tranceiver Pin Capicitance				20	pF

7.1.12 Pin Capacitance/Inductance for PCI Bus Signal Pins

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$C_{P,IN}$	PCI Input Pin Capacitance				10	pF
$C_{P,CLK}$	PCI Clock Input Capacitance				12	pF
L_{PIN}	Pin Inductance				20	nH

7.1.13 PCI Interface (Including SINT Pin)

T_A= 0–70°C

Symbol	Parameter	VDD=5V			VDD=3.3V			Units
		Min	Typ	Max	Min	Typ	Max	
V_{IL}	Input Threshold Voltage, Low		0.8			0.99		V
V_{IH}	Input Threshold Voltage, High		2.0			1.65		V
V_{OL}	Output Voltage, Low			0.4			0.4	V
V_{OH}	Output Voltage, High	2.5			2.5			V
I_{OL}	Output Drive Current, Low		7			5		mA
I_{OH}	Output Drive Current, High		20			5		mA

7.1.14 Fast Bus Master IDE Controller Interface

T_A= 0–70°C (Note 9)

Symbol	Parameter	VDD=5V			VDD=3.3V			Units
		Min	Typ	Max	Min	Typ	Max	
V_{IL}	Input Threshold Voltage, Low		0.8			0.8		V
V_{IH}	Input Threshold Voltage, High		2.0			2.0		V
V_{OL}	Output Voltage, Low			0.4			0.4	V
V_{OH}	Output Voltage, High	2.5			2.5			V
I_{OL}	Output Drive Current, Low		15			14		mA
I_{OH}	Output Drive Current, High		12			9		mA

Note 9: Inputs pins for this interface have integrated Back Drive protection.

7.1.15 Floppy Disk Controller (FDC) Interface

T_A= 0–70°C (Note 10)

Symbol	Parameter	VDD=5V			VDD=3.3V			Units
		Min	Typ	Max	Min	Typ	Max	
V_{IL}	Input Threshold Voltage, Low		0.8			0.8		V
V_{IH}	Input Threshold Voltage, High		2.0			2.0		V
V_{IL}	Output Voltage, Low			0.4			0.4	V
V_{OH}	Output Voltage, High	2.5			2.5			V
I_{OL}	Output Drive Current, Low		24			24		mA
I_{OH}	Output Drive Current, High		20			4.5		mA

Note 10: Inputs pins for this interface have integrated Back Drive protection.

7.1.16 Parallel Port/Floppy Disk Interface

T_A= 0–70°C (Note 11)

Symbol	Parameter	Conditions	VDD=5V			VDD=3.3V			Units
			Min	Typ	Max	Min	Typ	Max	
V_{IL}	Input Threshold Voltage, Low			0.8			0.8		V
V_{IH}	Input Threshold Voltage, High			2.0			2.0		V
V_{OL}	Output Voltage, Low				0.4		0.4		V
V_{OH}	Output Voltage, High		2.5			2.5			V
I_{OL}	Output Drive Current, Low	STB/WRITE#, PD0-5, PD7 pins only		14			12		mA
I_{OH}	Output Drive Current, High			14			5		mA
I_{OL}	Output Drive Current, Low	All other output and I/O pins		24			24		mA
I_{OH}	Output Drive Current, High			20			4.5		mA

Note 11: Inputs pins for these interfaces have integrated Back Drive protection.

7.1.17 Serial Port 1 and Serial Port 2/UIR Port Interface

T_A= 0–70°C (Note 12)

Symbol	Parameter	Conditions	VDD=5V			VDD=3.3V			Units
			Min	Typ	Max	Min	Typ	Max	
V_{IL}	Input Threshold Voltage, Low			0.8			0.8		V
V_{IH}	Input Threshold Voltage, High			2.0			2.0		V
V_{OL}	Output Voltage, Low				0.4			0.4	V
V_{OH}	Output Voltage, High		2.5			2.5			V
I_{OL}	Output Drive Current, Low	IRSEL0-2 pins only		14			12		mA
I_{OH}	Output Drive Current, High			14			5		mA
I_{OL}	Output Drive Current, Low	All other output and I/O pins		12			10		mA
I_{OH}	Output Drive Current, High			6			4		mA

Note 12: Input pins for these interfaces have integrated Back Drive protection.

7.1.18 CPU Interface

T_A= 0–70°C (Note 13 and 14)

Symbol	Parameter	VDD=5V			VDD=3.3V			Units
		Min	Typ	Max	Min	Typ	Max	
V_{IL}	Input Threshold Voltage, Low		0.8			0.8		V
V_{IH}	Input Threshold Voltage, High		2.0			2.0		V
V_{OL}	Output Voltage, Low			0.4			0.4	V
V_{OH}	Output Voltage, High		NA			NA		V
I_{OL}	Output Drive Current, Low		4			4		mA
I_{OH}	Output Drive Current, High		NA			NA		mA

Note 13: Input pins for these interfaces have integrated Back Drive protection.
Note 14: Output pins are Open-Drain.

7.1.19 FX Bus, ROM, KBD, RTC, SPKR Interfaces

T_A= 0–70°C (Note 15)

Symbol	Parameter	VDD=5V			VDD=3.3V			Units
		Min	Typ	Max	Min	Typ	Max	
V_{IL}	Input Threshold Voltage, Low		0.8			0.8		V
V_{IH}	Input Threshold Voltage, High		2.0			2.0		V
V_{OL}	Output Voltage, Low			0.4			0.4	V
V_{OH}	Output Voltage, High	2.5			2.5			V
I_{OL}	Output Drive Current, Low		4			4		mA
I_{OH}	Output Drive Current, High		4			2.5		mA

Note 15: Inputs pins for these interfaces have integrated Back Drive protection.

7.1.20 Power Management/GPIO Interface

T_A= 0–70°C (Note 16)

Symbol	Parameter	Conditions	VDD=5V			VDD=3.3V			Units
			Min	Typ	Max	Min	Typ	Max	
V_{IL}	Input Threshold Voltage, Low			0.8			0.8		V
V_{IH}	Input Threshold Voltage, High			2.0			2.0		V
V_{IL}	Input Threshold Voltage, Low	BSERCLK3 pin only		0.8			0.99		V
V_{IH}	Input Threshold Voltage, High			2.0			1.65		V
V_{OL}	Output Voltage, Low				0.4			0.4	V
V_{OH}	Output Voltage, High		2.5			2.5			V
I_{OL}	Output Drive Current, Low	GPIO2-3 pins only		14			12		mA
I_{OH}	Output Drive Current, High			14			5		mA
I_{OL}	Output Drive Current, Low	BSER3TO1 pin only		15			14		mA
I_{OH}	Output Drive Current, High			12			9		mA
I_{OL}	Output Drive Current, Low	All other output and I/O pins		4			4		mA
I_{OH}	Output Drive Current, High			4			2.5		mA

Note 16: Input pins for these interfaces have integrated Back Drive protection.

7.1.21 Universal Serial Bus Interface

T_A= 0–70°C (Note 17)

Symbol	Parameter	Conditions	VDD=5V			VDD=3.3V			Units
			Min	Typ	Max	Min	Typ	Max	
V_{IL}	Input Threshold Voltage, Low			0.8			0.8		V
V_{IH}	Input Threshold Voltage, High			2.0			2.0		V
V_{SE}	Single Ended Input Threshold Voltage	PORT1D+/-, PORT2D+/- pins only	0.8		2.0	0.8		2.0	V
V_{ID}	Input Differential Voltage	PORT1D+/-, PORT2D+/- pins only	200			200			mV
V_{OL}	Output Voltage, Low	PORT1D+/-, PORT2D+/- pins only			0.4			0.4	V
V_{OH}	Output Voltage, High		2.5			2.5			V

Symbol	Parameter	Conditions	VDD=5V			VDD=3.3V			Units
			Min	Typ	Max	Min	Typ	Max	
V_{IL}	Output Voltage, Low	PWRCTL1,2#, USB_ACT pins only			0.4			0.4	V
V_{OH}	Output Voltage, High		2.5			2.5			V
I_{OZ}	Output Tri-State Leakage	PORT1D+/-, PORT2D+/- pins only	-10		+10	-10		+10	uA
I_{OL}	Output Drive Current, Low	PWRCTL1,2#, USB_ACT pins only		4			4		mA
I_{OH}	Output Drive Current, High			4			4		mA

Note 17: Input pins for these interfaces have integrated Back Drive protection; namely OC_SENSE1#, OC_SENSE2#.

7.1.22 Clock Interface

T_A= 0–70°C (Note 18)

Symbol	Parameter	VDD=5V			VDD=3.3V			Units
		Min	Typ	Max	Min	Typ	Max	
V_{IL}	Input Threshold Voltage, High		0.8			0.99		V
V_{IH}	Input Threshold Voltage, Low		2.0			1.65		V

Note 18: The 14.318 MHz clock has integrated Back Drive protection.

7.2 AC TIMING SPECIFICATIONS

7.2.1 AC Test Waveforms

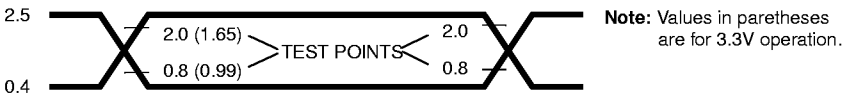


FIGURE 1. AC Testing Input/Output Waveform

7.3 CLOCK TIMING

Symbol	Parameter	Min	Max	Units	Notes
t_{CH}	CLK High Pulse Width	11		ns	
t_{CL}	CLK Low Pulse Width	11		ns	
t_{CP}	CLK Period	30		ns	

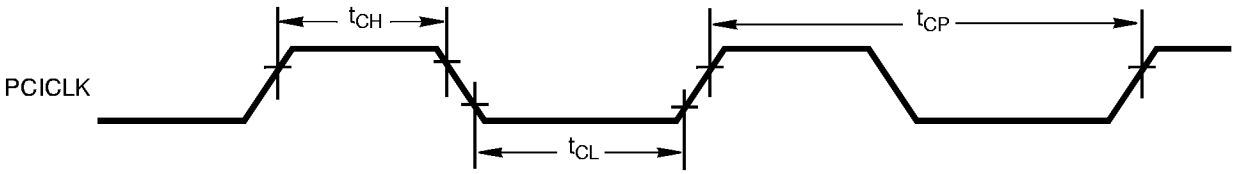


FIGURE 2. Clock Timing

7.4 PCI TIMING

Symbol	Parameter	Min	Max	Units	Notes
t_{PCI_SU}	PCI Signals Input Setup Time to CLK	7		ns	
t_{PCI_VAL}	PCI Signals, CLK to Output Valid (bussed signals)	2	11	ns	
t_{PCI_VAL}(ptp)	PCI Signals, CLK to Output Valid (point–to–point signals)	2	12	ns	
	CLK Slew Rate (Input)	1	4	V/ns	
	RST# Slew Rate (Output)	50		mV/ns	
t_{ON}	Float to Active Delay	2		ns	
t_{OFF}	Active to Float Delay		28	ns	
t_{PCI_H}	Input Hold Time from CLK	0		ns	
t_{PCI_RST}	Reset Active Time After Power Stable	1		ms	
$t_{PCI\_RST-CLK}$	Reset Active Time After CLK Stable	100		us	
$t_{PCI\_RST-OFF}$	Reset Active to Output Float Delay		40	ns	
t_{PCI_CR}	CLK to CLKRUN# Valid	2	11	ns	
t_{PCI_CR-SET}	CLKRUN# Input Setup Time to CLK	7		ns	

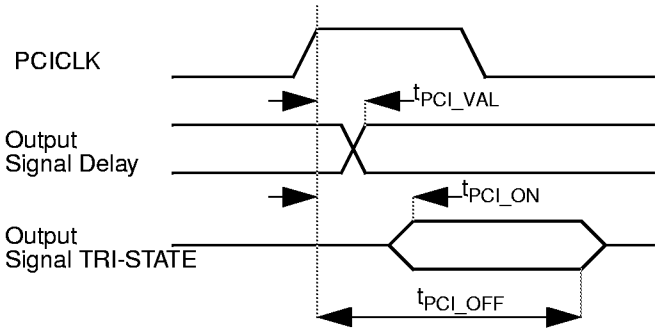


FIGURE 3. PCI Bus Output Signals

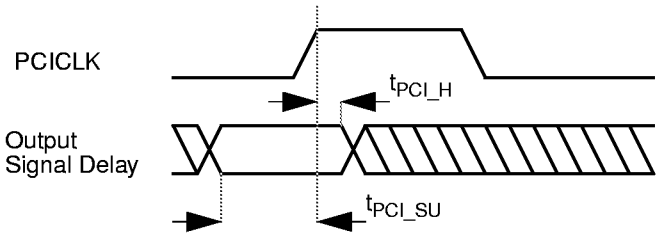


FIGURE 4. PCI Bus Input Signals

7.5 UART TIMING

7.5.1 Transmitter Timing

Symbol	Parameter	Min	Max	Units	Notes
t_{IRTXW}	IRTX pulse width	1.6us	3/16	Baud Out Cycles	

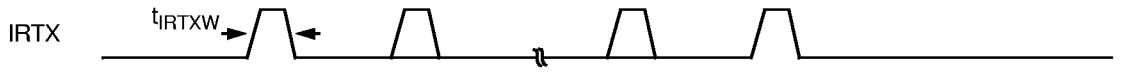


FIGURE 5. Transmitter Timing

7.5.2 Receiver Timing

Symbol	Parameter	Min	Max	Units	Notes
t_{IRRXW}	IRRX pulse width	1.6us	6/16	Baud Out Cycles	

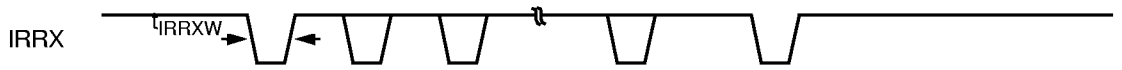


FIGURE 6. Receiver Timing

7.6 INFRARED INTERFACE TIMING

Symbol	Parameter	Conditions	Min	Max	Units	Notes
t_{CMW}	Modulation Signal Pulse Width in Sharp-IR and Consumer-IR	Transmitter	t_{CWN}-25	t_{CWN}+25	ns	Note 19
		Receiver	500		ns	
t_{CMP}	Modulation Signal Period in Sharp-IR and Consumer-IR	Transmitter	t_{CPN}-25	t_{CPN}+25	ns	Note 20
		Receiver	t_{MMIN}	t_{MMAX}	ns	Note 21
t_{BT}	Single Bit Time in UART and Sharp-IR	Transmitter	t_{BTN}-25	t_{BTN}+25	ns	Note 22
		Receiver	t_{BTN}-2%	t_{BTN}+2%		Note 22
S_{DRT}	SIR Data Rate Tolerance of Normal Data Rate	Transmitter		± 0.87%		
		Receiver		± 2.0%		
t_{SJT}	SIR Leading Edge Jitter (Percent of Nominal Bit Duration)	Transmitter		± 2.5%		
		Receiver		± 6.0%		
t_{SPW}	SIR Pulse Width	Transmitter, Variable Width	(3/16) x t_{BTN} -15	(3/16) x t_{BTN} +15	ns	Note 22
		Transmitter, Fixed Width	1.48	1.78	µs	
		Receiver	1		µs	
M_{DRT}	MIR Data Rate Tolerance of Normal Data Rate.	Transmitter		± 0.1%		
		Receiver		± 0.15%		
t_{MJT}	MIR Leading Edge Jitter (Percent of Nominal Bit Duration)	Transmitter		± 2.9%		
		Receiver		± 6.0%		

Symbol	Parameter	Conditions	Min	Max	Units	Notes
t_{MPW}	MIR Pulse Width	Transmitter	t_{MWN} -15	t_{MWN} +15	ns	Note 23
		Receiver	60		ns	
F_{DRT}	FIR Data Rate Tolerance of Nominal Data Rate	Transmitter		± 0.01%		
		Receiver		± 0.01%		
t_{FJT}	FIR Leading Edge Jitter (Percent of Nominal Bit Duration)	Transmitter		± 4.0%		
		Receiver		± 25.0%		
t_{FPW}	FIR Single Pulse Width	Transmitter	115	135	ns	Note 24
		Receiver, Leading Edge Jitter = 0ns	80	175	ns	Note 24
		Receiver, Leading Edge Jitter = ± 25ns	90	150	ns	Note 24
t_{FDPW}	FIR Double Pulse Width	Transmitter	115	135	ns	Note 24
		Receiver, Leading Edge Jitter = 0ns	205	300	ns	Note 24
		Receiver, Leading Edge Jitter = ± 25ns	215	310	ns	Note 24

Note 19: t_{CWN} is the nominal pulse width of the modulation signal for Sharp-IR and Consumer-IR modes. It is determined by the MCPW[2:0] and TXHSC bits in the IRTXMC and RCCFG registers.

Note 20: t_{CPN} is the nominal period of the modulation signal for Sharp-IR and Consumer-IR modes. It is determined by the MCFR[4:0] and TXHSC bits in the IRTXMC and RCCFG registers.

Note 21: t_{MMIN} and t_{MMAX} define the time range within which the period of the incoming subcarrier signal has to fall in order for the signal to be accepted by the receiver. These time values are determined by the content of register IRRXDC and the setting of bit RXHSC in the RCCFG register.

Note 22: t_{BTN} is the nominal bit time in UART, Sharp-IR, SIR, and Consumer-IR modes. It is determined by setting the baud generator divisor register.

Note 23: t_{MWN} is the nominal pulse width for MIR mode. It is determined by the MPW[3:0] and MDRS bits in the MIR_PW and IRCR2 registers.

Note 24: The receiver pulse width requirements for various jitter values can be obtained by assuming a linear pulse-width/jitter relationship. For example, if the jitter is +/- 10 ns, the width of a single pulse must fall between 84 and 165 ns.

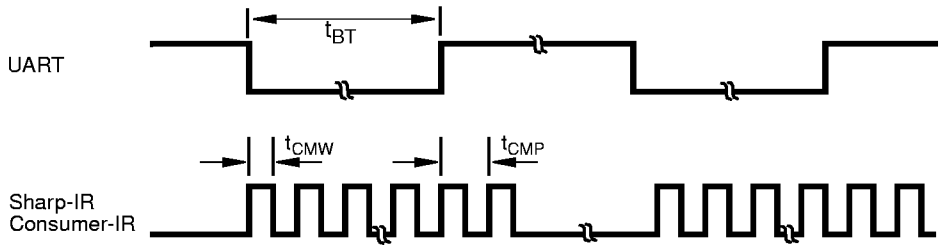
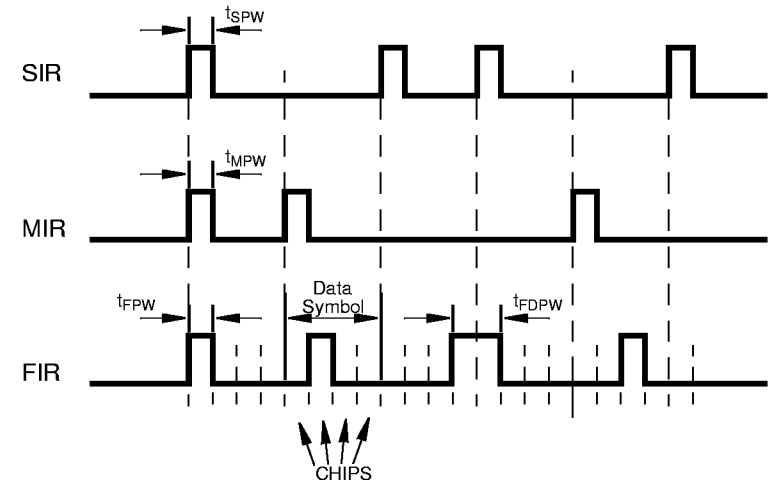


FIGURE 7. UART, Sharp-IR, and Consumer-IR Timing



Note: The signals shown here represent the infrared signals at the IRTX output.
The infrared signals at the IRRXn inputs have opposite polarity.

FIGURE 8. SIR, MIR, and FIR Timing

7.7 PARALLEL PORT TIMING

7.7.1 Standard Parallel Port Timing

Symbol	Parameter	Min	Max	Units	Notes
t_{PDH}	Port Data Hold	500		ns	
t_{PDS}	Port Data Setup	500		ns	
t_{SW}	STB# Width	500		ns	

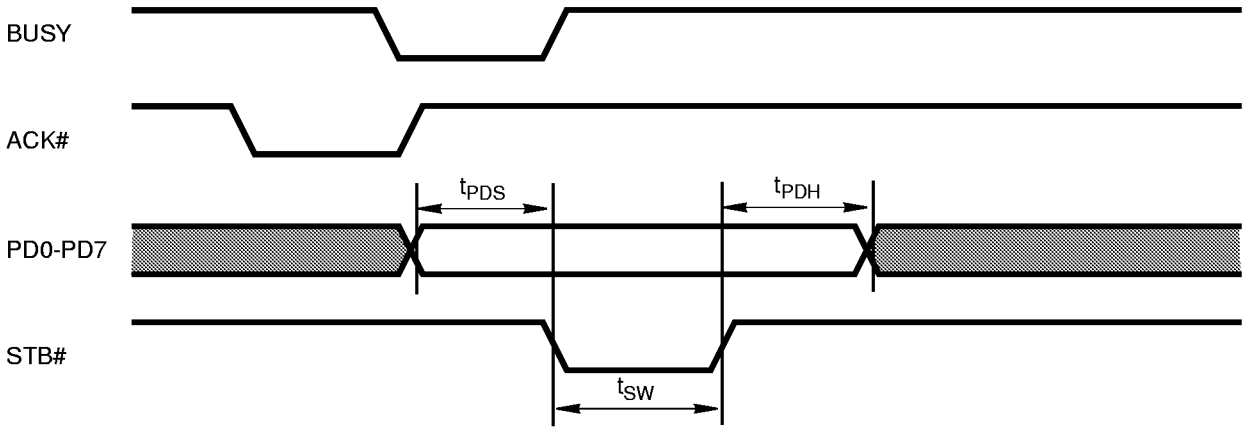


FIGURE 9. Typical Parallel Port Data Exchange

7.7.2 Enhanced Parallel Port (EPP) Mode 1.7 Timing

Symbol	Parameter	Min	Max	Units	Notes
t_{WPW17}	WRITE# Pulse Width	500		ns	
t_{DAPW17}	DSTRB# or ASTRB# Pulse Width	500		ns	
t_{WPD17h}	PD[7:0] Hold Time from WRITE# de-asserting (high)	50		ns	
t_{WEST17}	WRITE# asserting (low) to DSTRB# or ASTRB# asserting (low)	0		ns	
t_{STDW17}	DSTRB# or ASTRB# de-asserting (high) to WRITE# de-asserting (high)	0		ns	Note 1
t_{WPDS17}	PD[7:0] Valid from WRITE# asserting (low)		15	ns	
t_{EPDW17}	PD[7:0] Valid setup time to DSTRB# or ASTRB# de-asserting (high) for Parallel Port Reads	80		ns	
t_{EPD17h}	PD[7:0] Valid hold time from DSTRB# or ASTRB# de-asserting (high) for Parallel Port Reads	0		ns	
t_{WV17}	WRITE# or DSTRB# or ASTRB# asserted to WAIT# active (low) to guarantee the insertion of wait states		400	ns	

Note 25: The PC87560 design guarantees that WRITE# will not change from low to high before DSTRB# or ASTRB# goes from low to high.

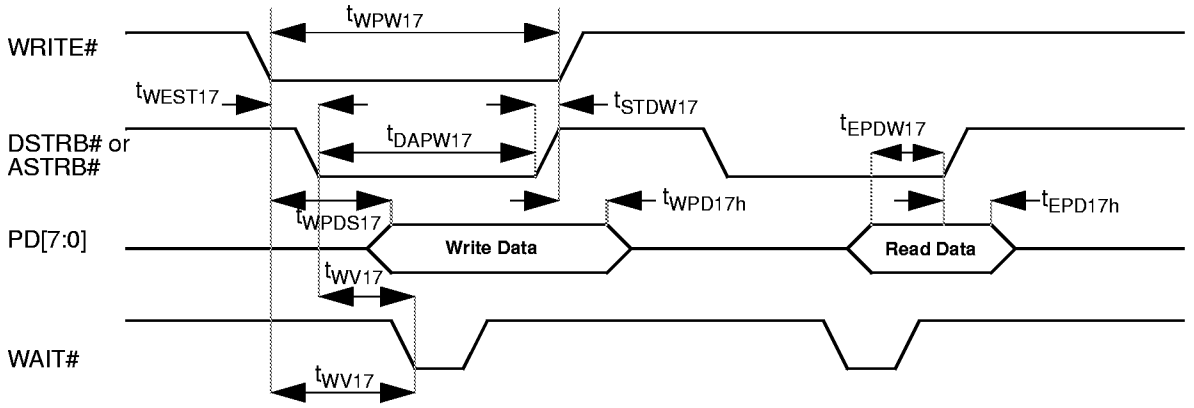


FIGURE 10. EPP Mode 1.7 Timing

7.7.3 Enhanced Parallel Port (EPP) Mode 1.9 Timing

Symbol	Parameter	Min	Max	Units	Notes
t_{WPW19}	WRITE# Pulse Width	500		ns	
t_{DAPW19}	DSTRB# or ASTRB# Pulse Width	500		ns	
t_{WPD19h}	PD[7:0] Hold Time from WRITE# de-asserting (high)	0		ns	
t_{WEST19}	WRITE# asserting (low) to DSTRB# or ASTRB# asserting (low)		10	ns	
t_{STDW19}	DSTRB# or ASTRB# de-asserting (high) to WRITE# de-asserting (high)	0		ns	Note 26
t_{WPDS19}	PD[7:0] Valid from WRITE# asserting (low)		15	ns	
t_{EPDW19}	PD[7:0] Valid setup time to DSTRB# or ASTRB# de-asserting (high) for Parallel Port Reads	80		ns	
t_{EPD19h}	PD[7:0] Valid hold time from DSTRB# or ASTRB# de-asserting (high) for Parallel Port Reads	0		ns	
t_{WW19a}	WRITE# asserted from WAIT# active (low)		45	ns	Note 27
t_{WST19a}	DSTRB# or ASTRB# asserted from WAIT# active (low)		65	ns	Note 27
t_{WW19ia}	WRITE# de-asserted (high) from WAIT# active (low)		45	ns	

Note 26: The PC87560 design guarantees that WRITE# will not change from low to high before DSTRB# or ASTRB# goes from low to high.
Note 27: This specification when the WAIT# signal being inactive high is the cause for delaying the assertion of WRITE# and/or DSTRB# or ASTRB#. When WAIT# is asserted (low) before any EPP activity is initiated these specification have no meaning.

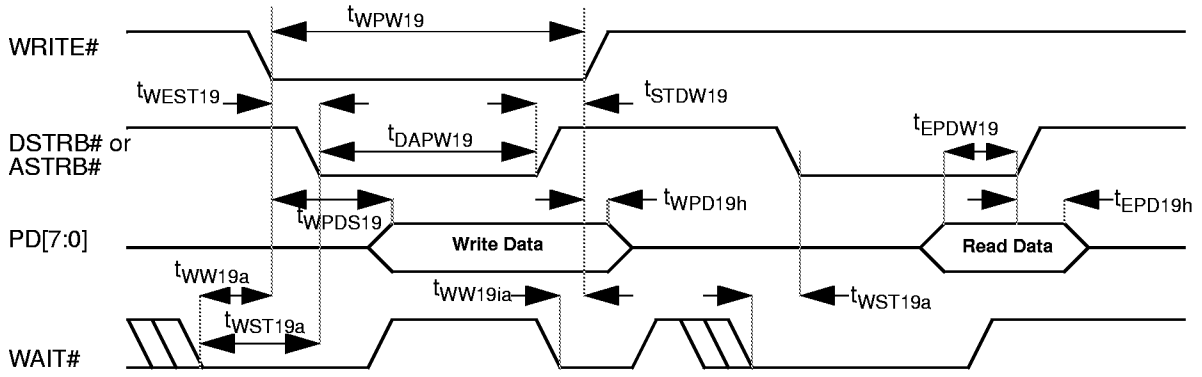


FIGURE 11. EPP Mode 1.9 Timing

7.7.4 Extended Capabilities Port (ECP) Mode Timing - Forward

Symbol	Parameter	Min	Max	Units	Notes
t_{ECDSF}	Data Setup time before STB# Active (low)	0		ns	
t_{ECDHF}	Data Hold time after BUSY# Inactive (high)	0		ns	
t_{ECLHF}	BUSY# Inactive (high) after STB# Active (low)	75		ns	
t_{ECHHF}	STB# Inactive (high) after BUSY# Inactive (high)	0	1	s	
t_{ECHLF}	BUSY# Inactive (high) Hold time after STB# Inactive (low)	0	35	ms	
t_{ECLLF}	STB# Active (low) after BUSY# Inactive (low)	0		ns	

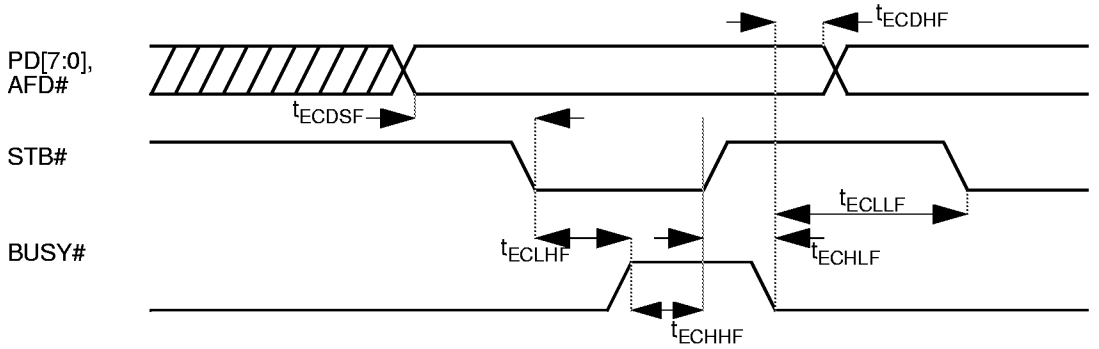


FIGURE 12. ECP Parallel Port Forward Timing

7.7.5 Extended Capabilities Port (ECP) Mode Timing - Backward

Symbol	Parameter	Min	Max	Units	Notes
t_{ECDSB}	Data Setup time before ACK# Active (low)	0		ns	
t_{ECDHB}	Data Hold time after AFD# Inactive (high)	0		ns	
t_{ECLHB}	AFD# Inactive (high) after ACK# Active (low)	75		ns	
t_{ECHHB}	ACK# Inactive (high) after AFD# Inactive (high)	0	1	s	
t_{ECHLB}	AFD# Inactive (high) Hold time after ACK# Inactive (low)	0	35	ms	
t_{ECLLB}	ACK# Active (low) after AFD# Inactive (low)	0		ns	

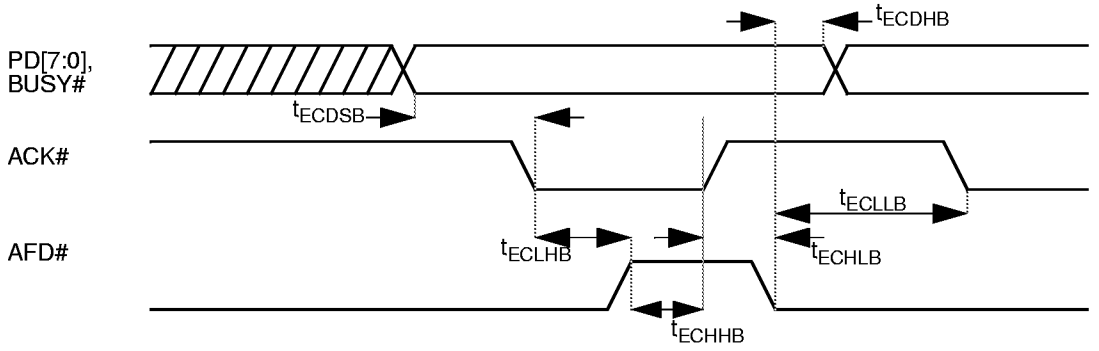


FIGURE 13. ECP Parallel Port Backward Timing

7.8 BSERIAL INTERFACE TIMING

Symbol	Parameter	Min	Max	Units	Notes
t_{BS_CLK}	BSERCLKV3 Period	30	40	ns	
t_{BSER_H}	BSER1TO3 Input Hold time from BSERCLKV3	2		ns	
t_{BSER_SU}	BSER1TO3 Input Setup time to BSERCLKV3	5		ns	
t_{BSER_VAL}	BSER3TO1 Output Valid time from BSERCLKV3	2	25	ns	

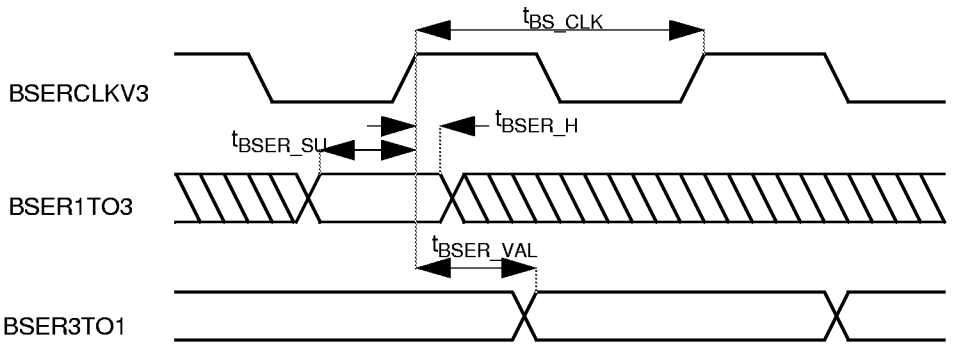


FIGURE 14. Burst Serial (BSER) Timing

7.9 DMA TIMING

7.9.1 ISA Compatible Timing

Symbol	Parameter	Min	Max	Units	Notes
t_{D1}	DACK# to FXIOR#	100		ns	
t_{D2}	FXA/FXD = FFFFh, setup time to the falling edge of FXIOR# or FXIOW#	100		ns	
t_{D3}	FXIOR# or FXIOW# rising to FXASTB# rising	30		ns	
t_{D4_RD}	TC valid setup time to the rising edge of FXIOR#	500		ns	
t_{D4_WR}	TC valid setup time to the rising edge of FXIOW#	400		ns	
t_{D5}	FXIOR# Width	760		ns	
t_{D6}	FXA/FXD turn off		12	ns	
t_{D7}	Read Data Setup	80		ns	
t_{D8}	Read Hold	0		ns	
t_{D9}	FXIOR# Inactive to DACK# Inactive	120		ns	
t_{D10}	TC valid hold time from the rising edge of FXIOR# or FXIOW#	60		ns	
t_{D11_RD}	DRQ Removal Time for FX Bus I/O Read cycles (DMA Write Transfer)	200		ns	Note 28
t_{D11_WR}	DRQ Removal Time for FX Bus I/O Write cycles (DMA Read Transfer)	140		ns	Note 28
t_{D12}	DACK# to FXIOW#	320		ns	
t_{D13}	FXIOW# Width	460		ns	
t_{D14}	FXIOW# Inactive to DACK# Inactive	150		ns	
t_{D15}	Write Data Setup Time	400		ns	
t_{D16}	Write Data Hold Time	20		ns	
t_{D17}	Max Delay Between FXIORDY and FXIOR# in order to Insert Wait States		500	ns	Note 29
t_{D18}	Cycle Finish after Removal of FXIORDY	120		ns	Note 29

Symbol	Parameter	Min	Max	Units	Notes
t_{D19}	Max Delay Between FXIORDY and FXIOW# in order to Insert Wait States		260	ns	Note 29
t_{D20}	AEN Valid to FXIOR# or FXIOW# active command strobe	100		ns	
t_{D21}	AEN Valid from FXIOR# or FXIOW# active command strobe	30		ns	
t_{D22}	FXA[19:4] setup time to the falling edge of FXASTB#	20		ns	
t_{D23}	FXA[19:4] hold time from the falling edge of FXASTB#	10		ns	

Note 28: In Demand Mode DRQ needs to be removed before this time so the next DMA cycle will not be generated.
Note 29: Traditionally the I/O device associated with a DMA transfer is not suppose to de-assert the IORDY signal low. However, if an I/O device violates this standard rule, the PC87422's FX Bus will insert Wait States similar to the ISA Bus.

7.9.2 Type "A" Timing

Symbol	Parameter	Min	Max	Units	Notes
t_{D1}	DACK# to FXIOR#	66		ns	
t_{D2}	FXA/FXD = FFFFh, setup time to the falling edge of FXIOR# or FXIOW#	100		ns	
t_{D3}	FXIOR# or FXIOW# rising to FXASTB# rising	30		ns	
t_{D4_RD}	TC valid setup time to the rising edge of FXIOR#	300		ns	
t_{D4_WR}	TC valid setup time to the rising edge of FXIOW#	200		ns	
t_{D5}	FXIOR# Width	395		ns	
t_{D6}	FXA/FXD turn off		12	ns	
t_{D7}	Read Data Setup	115		ns	
t_{D8}	Read Hold	0		ns	
t_{D9}	FXIOR# Inactive to DACK# Inactive	94		ns	
t_{D10}	TC valid hold time from the rising edge of FXIOR# or FXIOW#	60		ns	
t_{D11_RD}	DRQ Removal Time for FX Bus I/O Read cycles (DMA Write Transfer)	200		ns	Note 30
t_{D11_WR}	DRQ Removal Time for FX Bus I/O Write cycles (DMA Read Transfer)	155		ns	Note 30
t_{D12}	DACK# to FXIOW#	186		ns	
t_{D13}	FXIOW# Width	220		ns	
t_{D14}	FXIOW# Inactive to DACK# Inactive	150		ns	
t_{D15}	Write Data Setup Time	200		ns	
t_{D16}	Write Data Hold Time	20		ns	
t_{D17}	Max Delay Between FXIORDY and FXIOR# in order to Insert Wait States		390	ns	Note 31
t_{D18}	Cycle Finish after Removal of FXIORDY	60		ns	Note 31
t_{D19}	Max Delay Between FXIORDY and FXIOW# in order to Insert Wait States		150	ns	Note 31
t_{D20}	AEN Valid to FXIOR# or FXIOW# active command strobe	100		ns	
t_{D21}	AEN Valid from FXIOR# or FXIOW# active command strobe	30		ns	
t_{D22}	FXA[19:4] setup time to the falling edge of FXASTB#	20		ns	
t_{D23}	FXA[19:4] hold time from the falling edge of FXASTB#	10		ns	

Note 30: In Demand Mode DRQ needs to be removed before this time so the next DMA cycle will not be generated.
Note 31: Traditionally the I/O device associated with a DMA transfer is not suppose to de-assert the IORDY signal low. However, if an I/O device violates this standard rule, the PC87422's FX Bus will insert Wait States similar to the ISA Bus.

7.9.3 Type “B” Timing

Symbol	Parameter	Min	Max	Units	Notes
t_{D1}	DACK# to FXIOR#	66		ns	
t_{D2}	FXA/FXD = FFFFh, setup time to the falling edge of FXIOR# or FXIOW#	100		ns	
t_{D3}	FXIOR# or FXIOW# rising to FXASTB# rising	30		ns	
t_{D4_RD}	TC valid setup time to the rising edge of FXIOR#	200		ns	
t_{D4_WR}	TC valid setup time to the rising edge of FXIOW#	180		ns	
t_{D5}	FXIOR# Width	275		ns	
t_{D6}	FXA/FXD turn off		12	ns	
t_{D7}	Read Data Setup	115		ns	
t_{D8}	Read Hold	0		ns	
t_{D9}	FXIOR# Inactive to DACK# Inactive	29		ns	
t_{D10}	TC valid hold time from the rising edge of FXIOR# or FXIOW#	30		ns	
t_{D11_RD}	DRQ Removal Time for FX Bus I/O Read cycles (DMA Write Transfer)	200		ns	Note 32
t_{D11_WR}	DRQ Removal Time for FX Bus I/O Write cycles (DMA Read Transfer)	155		ns	Note 32
t_{D12}	DACK# to FXIOW#	186		ns	
t_{D13}	FXIOW# Width	215		ns	
t_{D14}	FXIOW# Inactive to DACK# Inactive	94		ns	
t_{D15}	Write Data Setup Time	130		ns	
t_{D16}	Write Data Hold Time	20		ns	
t_{D17}	Max Delay Between FXIORDY and FXIOR# in order to Insert Wait States		270	ns	
t_{D18}	Cycle Finish after Removal of FXIORDY	60		ns	
t_{D19}	Max Delay Between FXIORDY and FXIOW# in order to Insert Wait States		150	ns	
t_{D20}	AEN Valid to FXIOR# or FXIOW# active command strobe	100		ns	
t_{D21}	AEN Valid from FXIOR# or FXIOW# active command strobe	30		ns	
t_{D22}	FXA[19:4] setup time to the falling edge of FXASTB#	20		ns	
t_{D23}	FXA[19:4] hold time from the falling edge of FXASTB#	10		ns	

Note 32: In Demand Mode DRQ needs to be removed before this time so the next DMA cycle will not be generated.

7.9.4 Type "F" Timing

Symbol	Parameter	Min	Max	Units	Notes
t_{D1}	DACK# to FXIOR#	66		ns	
t_{D2}	FXA/FXD = FFFFh, setup time to the falling edge of FXIOR# or FXIOW#	100		ns	
t_{D3}	FXIOR# or FXIOW# rising to FXASTB# rising	30		ns	
t_{D4_RD}	TC valid setup time to the rising edge of FXIOR#	120		ns	
t_{D4_WR}	TC valid setup time to the rising edge of FXIOW#	100		ns	
t_{D5}	FXIOR# Width	140		ns	
t_{D6}	FXA/FXD turn off		12	ns	
t_{D7}	Read Data Setup	60		ns	
t_{D8}	Read Hold	0		ns	
t_{D9}	FXIOR# Inactive to DACK# Inactive	29		ns	
t_{D10}	TC valid hold time from the rising edge of FXIOR# or FXIOW#	30		ns	
t_{D11_RD}	DRQ Removal Time for FX Bus I/O Read cycles (DMA Write Transfer)	80		ns	Note 33
t_{D11_WR}	DRQ Removal Time for FX Bus I/O Write cycles (DMA Read Transfer)	80		ns	Note 33
t_{D12}	DACK# to FXIOW#	100		ns	
t_{D13}	FXIOW# Width	110		ns	
t_{D14}	FXIOW# Inactive to DACK# Inactive	94		ns	
t_{D15}	Write Data Setup Time	90		ns	
t_{D16}	Write Data Hold Time	20		ns	
t_{D17}	Max Delay Between FXIORDY and FXIOR# in order to Insert Wait States		45	ns	Note 34
t_{D18}	Cycle Finish after Removal of FXIORDY	60		ns	Note 34
t_{D19}	Max Delay Between FXIORDY and FXIOW# in order to Insert Wait States		30	ns	Note 34
t_{D20}	AEN Valid to FXIOR# or FXIOW# active command strobe	100		ns	
t_{D21}	AEN Valid from FXIOR# or FXIOW# active command strobe	30		ns	
t_{D22}	FXA[19:4] setup time to the falling edge of FXASTB#	20		ns	
t_{D23}	FXA[19:4] hold time from the falling edge of FXASTB#	10		ns	

Note 33: In Demand Mode DRQ needs to be removed before this time so the next DMA cycle will not be generated.
Note 34: Traditionally the I/O device associated with a DMA transfer is not suppose to de-assert the IORDY signal low. However, if an I/O device violates this standard rule, the PC87422's FX Bus will insert Wait States similar to the ISA Bus.

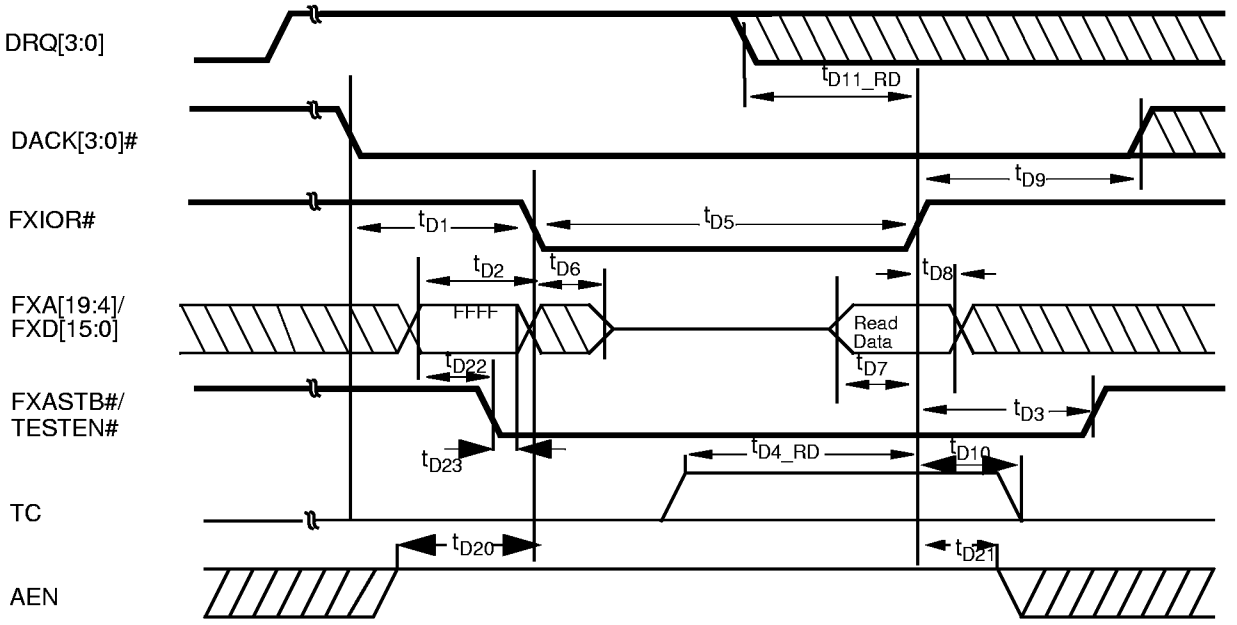


FIGURE 15. DMA FX Bus I/O Read Cycle (DMA Write Transfer)

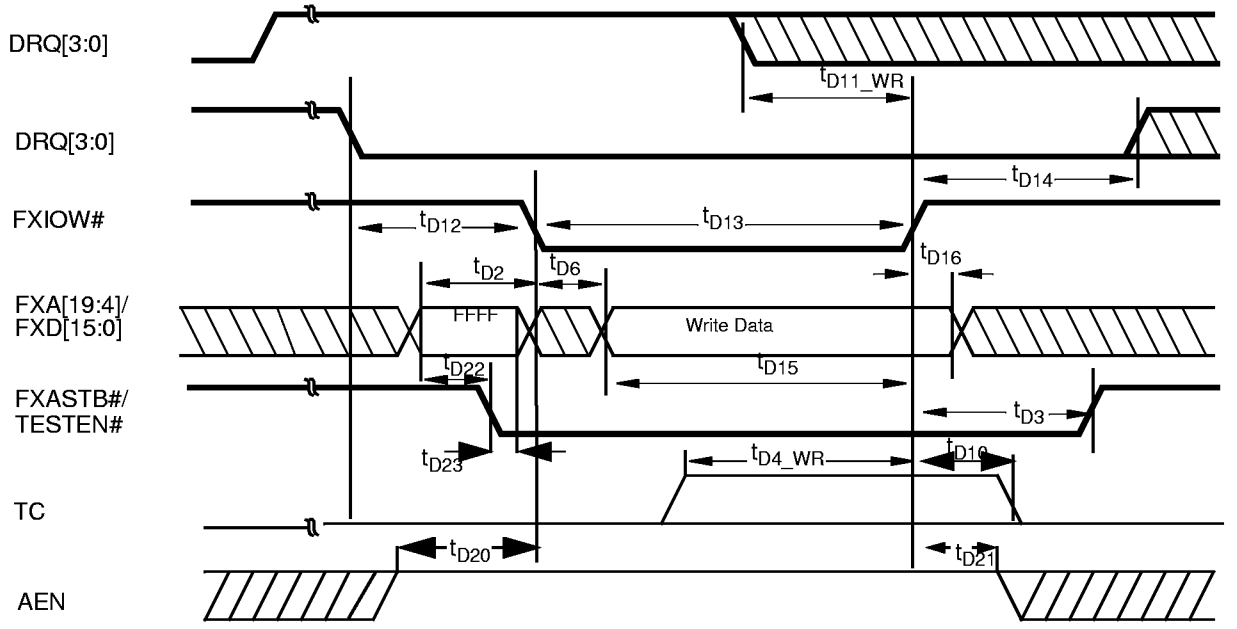


FIGURE 16. DMA FX Bus I/O Write Cycle (DMA Read Transfer)

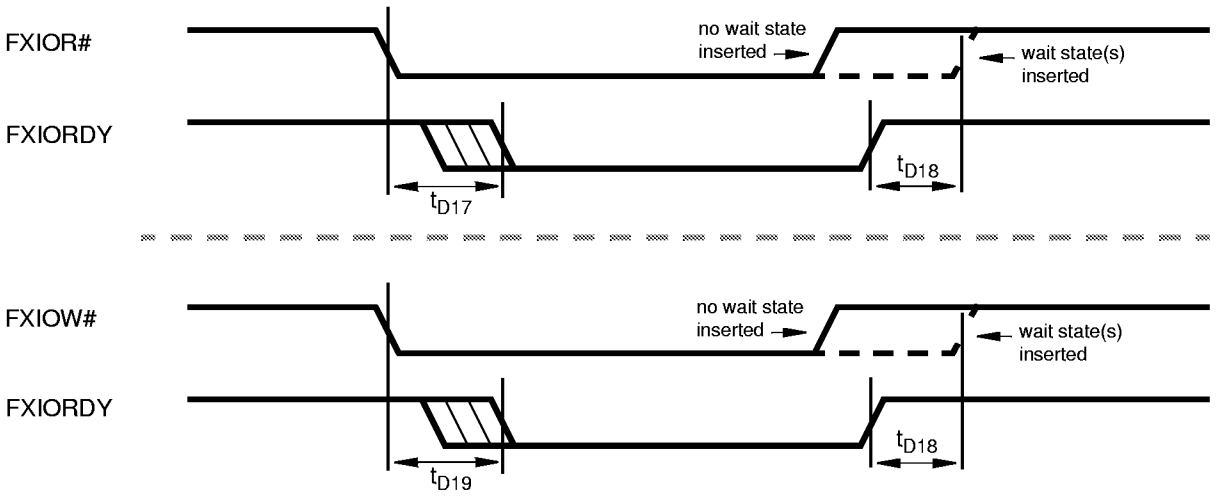


FIGURE 17. DMA FX Bus I/O Cycle Wait State Insertion

7.10 FAST EXTERNAL (FX) BUS TIMING

7.10.1 ISA Compatible Timing Mode

Symbol	Parameter	Min	Max	Units	Notes
1	FXASTB# pulse width	20		ns	
2	FXA[19:4] setup time to the falling edge of FXASTB#	20		ns	
3	FXA[19:4] hold time from the falling edge of FXASTB#	10		ns	
4	FXA[20:0], BHE# setup time to the falling edge of the command strobe (FXIOR#, FXIOW#, FXMEMR#, FXMEMW#, FXSMEMR# and/or FXSMEMW#)	110		ns	
5	FXCS[1:0]#, AUSIOCS#,KBCS#, ROMCS#, RTCCS# setup to the falling edge of the command strobe (FXIOR#, FXIOW#, FXMEMR#, FXMEMW#, FXSMEMR# and/or FXSMEMW#)	60		ns	
6	FXA[19:4]/FXD[15:0] TRI-STATE before the falling edge of the read command strobe (FXIOR#, FXMEMR# and/or FXSMEMR#)	0		ns	
7	FXD[15:0] valid Write Data Out before the falling edge of the write command strobe (FXIOW#, FXMEMW# and/or FXSMEMR#)	20		ns	
8	FXMEMCS16# setup to the memory command strobe (FXMEMR#, FXMEMW#, FXSMEMR# and/or FXS-MEMW#) to guarantee the proper cycle timing as well as proper data reading	100		ns	Note 35
9	FXIOCS16# setup to the command strobe (FXIOR# or FXIOW#) to guarantee the proper cycle timing as well as proper data reading	100		ns	Note 36
10	8-bit Command Strobe (FXMEMR#, FXMEMW#, FXSMEMR# and/or FXSMEMW#) pulse width	520		ns	Note 37
10	16-bit Command Strobe (FXMEMR#, FXMEMW#, FXSMEMR# and/or FXSMEMW#) pulse width	160		ns	Note 37
11	FXIORDY inactive low setup to the end of the command strobe (FXIOR#, FXIOW#, FXMEMR#, FXMEMW#, FXSMEMR# and/or FXSMEMW#) to insert additional wait states	120		ns	
12	Command strobe (FXIOR#, FXIOW#, FXMEMR#, FXMEMW#, FXSMEMR# and/or FXSMEMW#) active hold time from FXIORDY asserted active high	120		ns	

Symbol	Parameter	Min	Max	Units	Notes
13	Valid FXD[15:0] Read Data In setup time to the rising edge of the read command strobe (FXIOR#, FXMEMR# and/or FXSMEMR#).	100		ns	
14	Valid FXD[15:0] Read Data In hold time from the rising edge of the read command strobe (FXIOR#, FXMEMR# and/or FXSMEMR#)	0		ns	
15	FXMEMCS16#, FXIOCS16# valid hold time from the rising edge of the command strobe (FXIOR#, FXIOW#, FXMEMR#, FXMEMW#, FXSMEMR# and/or FXSMEMW#)	0		ns	
16	FXA[20, 3:0], BHE# hold time from the rising edge of the command strobe (FXIOR#, FXIOW#, FXMEMR#, FXMEMW#, FXSMEMR# and/or FXSMEMW#)	20		ns	
16	FXD[15:0] Write Data Out hold time from the rising edge of the write command strobe (FXIOW#, FXMEMW# and/or FXSMEMW#)	20		ns	
16	FXASTB# inactive low hold time from the rising edge of the command strobe (FXIOR#, FXIOW#, FXMEMR#, FXMEMW#, FXSMEMR# and/or FXSMEMW#)	20		ns	
17	FXA[19:4]/FXD[15:0] TRI-STATE hold time following the rising edge of the read command strobe (FXIOR#, FXMEMR# and/or FXSMEMR#)	20		ns	
18	Command strobe (FXIOR#, FXIOW#, FXMEMR#, FXMEMW#, FXSMEMR# and/or FXSMEMW#) going inactive to next active command strobe	170		ns	
19	AEN Valid to FXIOR# or FXIOW# active command strobe	100		ns	
20	AEN Valid from FXIOR# or FXIOW# going inactive	20		ns	

Note 35: To adhere to ISA Bus timing; 6, 8 or 10 PCI Clock periods of Command Recovery time should be programmed for FX Bus Memory cycles.
Note 36: To adhere to ISA Bus timing; 8 or 10 PCI Clock periods of Command Recovery time should be programmed for FX Bus I/O cycles.
Note 37: This is for the default timing of the FX Bus.

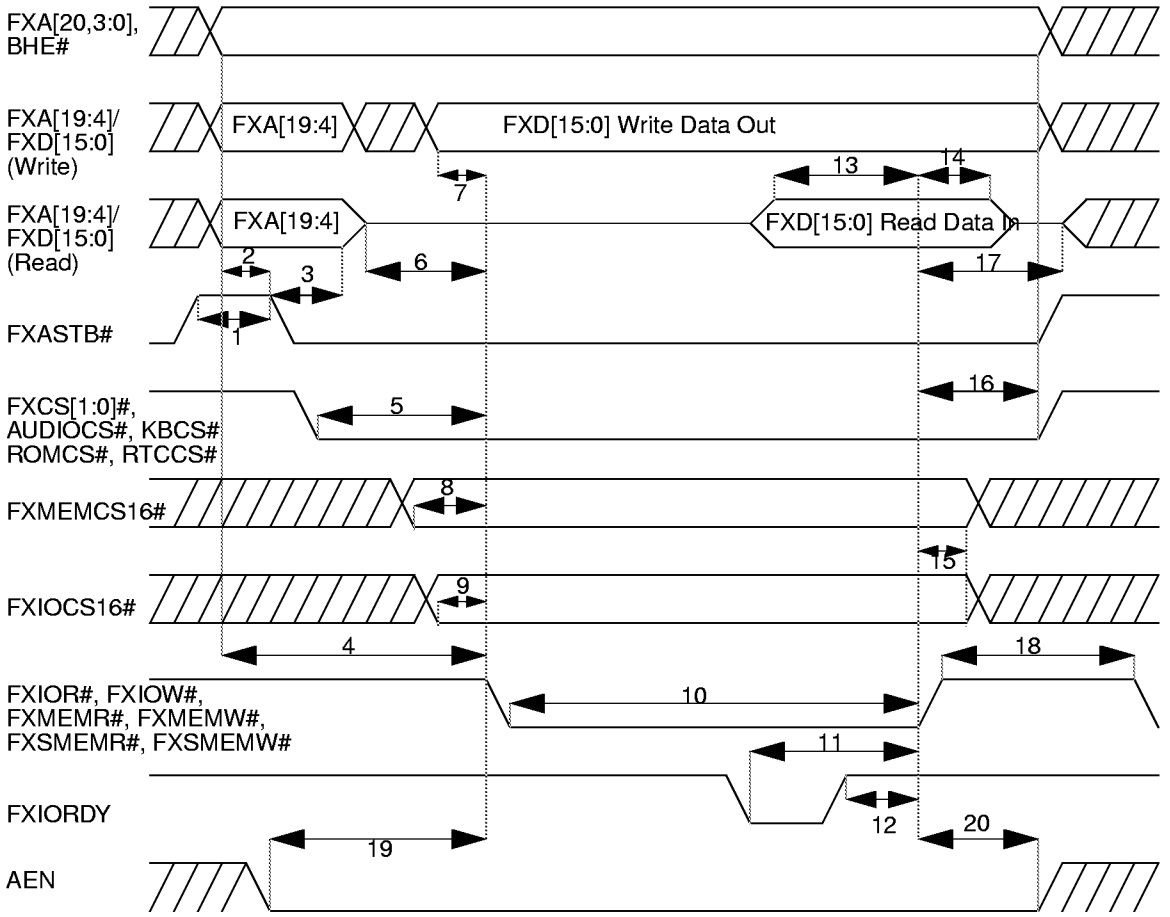


FIGURE 18. FX Bus Timing

7.10.2 Programmable Timing Modes

Symbol	Parameter	Min	Max	Units	Notes
1	FXASTB# pulse width.	20		ns	
2	FXA[19:4] setup time to the falling edge of FXASTB#	20		ns	
3	FXA[19:4] hold time from the falling edge of FXASTB#	10		ns	
4	FXA[20:0], BHE# setup time to the falling edge of the command strobe (FXIOR#, FXIOW#, FXMEMR#, FXMEMW#, FXSMEMR# and/or FXSMEMW#)	t_{CMDCLY} - 50		ns	Note 38
5	FXCS[1:0]#, AUSIOCS#,KBCS#, ROMCS#, RTCCS# setup to the falling edge of the command strobe (FXIOR#, FXIOW#, FXMEMR#, FXMEMW#, FXSMEMR# and/or FXSMEMW#)	t_{CMDCLY} - 70		ns	Note 38
6	FXA[19:4]/FXD[15:0] TRI-STATE before the falling edge of the read command strobe (FXIOR#, FXMEMR# and/or FXSMEMR#)	0		ns	
7	FXD[15:0] valid Write Data Out before the falling edge of the write command strobe (FXIOW#, FXMEMW# and/or FXSMEMR#)	20		ns	

Symbol	Parameter	Min	Max	Units	Notes
8	FXMEMCS16# setup to the memory command strobe (FXMEMR#, FXMEMW#, FXSMEMR# and/or FXSMEMW#) to guarantee the proper cycle timing as well as proper data reading.	100		ns	Note 40
9	FXIOCS16# setup to the command strobe (FXIOR# or FXIOW#) to guarantee the proper cycle timing as well as proper data reading.	100		ns	Note 39
10	8-bit Command Strobe (FXMEMR#, FXMEMW#, FXSMEMR# and/or FXSMEMW#) pulse width.	t_{CMD8} - 25		ns	Notes 42, 41
10	16-bit Command Strobe (FXMEMR#, FXMEMW#, FXSMEMR# and/or FXSMEMW#) pulse width.	t_{CMD16} - 25		ns	Notes 41, 43
11	FXIORDY inactive low setup to the end of the command strobe (FXIOR#, FXIOW#, FXMEMR#, FXMEMW#, FXSMEMR# and/or FXSMEMW#) to insert additional wait states	120		ns	
12	Command strobe (FXIOR#, FXIOW#, FXMEMR#, FXMEMW#, FXSMEMR# and/or FXSMEMW#) active hold time from FXIORDY asserted active high	120		ns	
13	Valid FXD[15:0] Read Data In setup time to the rising edge of the read command strobe (FXIOR#, FXMEMR# and/or FXSMEMR#)	100		ns	
14	Valid FXD[15:0] Read Data In hold time from the rising edge of the read command strobe (FXIOR#, FXMEMR# and/or FXSMEMR#)	0		ns	
15	FXMEMCS16#, FXIOCS16# valid hold time from the rising edge of the command strobe (FXIOR#, FXIOW#, FXMEMR#, FXMEMW#, FXSMEMR# and/or FXSMEMW#)	0		ns	
16	FXA[20, 3:0], BHE# hold time from the rising edge of the command strobe (FXIOR#, FXIOW#, FXMEMR#, FXMEMW#, FXSMEMR# and/or FXSMEMW#)	20		ns	
16	FXD[15:0] Write Data Out hold time from the rising edge of the write command strobe (FXIOW#, FXMEMW# and/or FXSMEMW#)	20		ns	
16	FXASTB# inactive low hold time from the rising edge of the command strobe (FXIOR#, FXIOW#, FXMEMR#, FXMEMW#, FXSMEMR# and/or FXSMEMW#)	20		ns	
17	FXA[19:4]/FXD[15:0] TRI-STATE hold time following the rising edge of the read command strobe (FXIOR#, FXMEMR# and/or FXSMEMR#)	20		ns	
18	Command strobe (FXIOR#, FXIOW#, FXMEMR#, FXMEMW#, FXSMEMR# and/or FXSMEMW#) going inactive to next active command strobe	t_{CMDLY} - 0		ns	Note 38
19	AEN Valid to FXIOR# or FXIOW# active command strobe	100		ns	
20	AEN Valid from FXIOR# or FXIOW# going inactive	20		ns	

Note 38: The variable t_{CMDLY} is equal to the number of programmed Command Delay states multiplied by the PCI Clock period. The number of programmed Command Delay states is controlled by the values programmed into Function 1 FX Bus Timing Control Register (at Configuration offset 76h-77h) and Function 1 FX Bus Memory Range Control Register 1 (at Configuration offset 80h-83h); along with exactly which FX Bus region is being accessed.

Note 39: To adhere to ISA Bus timing; 8 or 10 PCI Clock periods of Command Recovery time should be programmed for FX Bus I/O cycles.

Note 40: To adhere to ISA Bus timing; 6, 8 or 10 PCI Clock periods of Command Recovery time should be programmed for FX Bus Memory cycles.

Note 41: This is for the default timing of the FX Bus.

Note 42: The variable t_{CMD8} is equal to the number of programmed 8-bit Command Active states multiplied by the PCI Clock period. The number of programmed Command Delay states is controlled by the values programmed into Function 1 FX Bus Timing Control Register (at Configuration offset 76h-77h) and Function 1 FX Bus Memory Range Control Register 1 (at Configuration offset 80h-83h); along with exactly which FX Bus region is being accessed.

Note 43: The variable t_{CMD16} is equal to the number of programmed 16-bit Command Active states multiplied by the PCI Clock period. The number of programmed Command Delay states is controlled by the values programmed into Function 1 FX Bus Timing Control Register (at Configuration offset 76h-77h) and Function 1 FX Bus Memory Range Control Register 1 (at Configuration offset 80h-83h); along with exactly which FX Bus region is being accessed.

7.11 FDC TIMING

7.11.1 Clock Timing

Symbol	Parameter	Min	Max	Units	Notes
t_{ICP}	Internal Clock Period	Table XXII		ns	
t_{DRP}	Data Rate Period	Table XXII		ns	

TABLE XXII. Nominal t_{ICP}, t_{DRP} Values (Note 44)

MFM Data Rates	t_{DRP}	t_{ICP}	t_{ICP} Value	Units
1 Mbps	1000	3 x t_{CP}	125	ns
500 kbps	2000	3 x t_{CP}	125	ns
300 kbps	3333	3 x t_{CP}	208	ns
250 kbps	4000	6 x t_{CP}	250	ns

Note 44: See Section 7.3 "Clock Timing" for t_{CP} values.

7.11.2 Write Data Timing

Symbol	Parameter	Min	Max	Units	Notes
t_{HDH}	HDSEL# Hold from WGATE# Inactive	750			
t_{HDS}	HDSEL# Setup to WGATE# Active	100			
t_{WDW}	Write Data Pulse Width	Table XXIII			

TABLE XXIII. Minimum t_{WDW} Values

MFM Data Rates	t_{DRP}	t_{WDW}	t_{WDW} Value	Units
1 Mbps	1000	2 x t_{ICP}	250	ns
500 kbps	2000	2 x t_{ICP}	250	ns
300 kbps	3333	2 x t_{ICP}	375	ns
250 kbps	4000	2 x t_{ICP}	500	ns

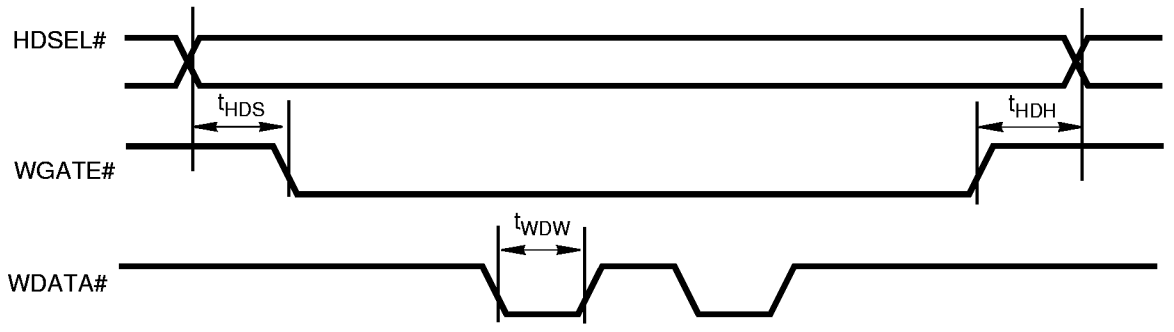


FIGURE 19. Write Data Timing

7.11.3 Read Data Timing

Symbol	Parameter	Min	Max	Units	Notes
t_{RDW}	Read Data Pulse Width	50		ns	

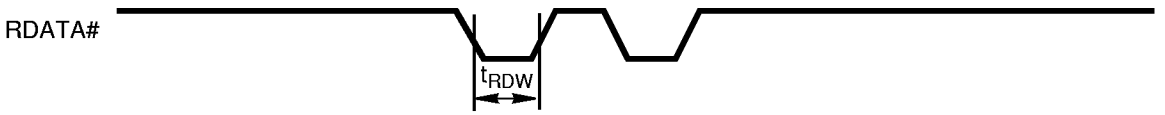


FIGURE 20. Read Data Timing

7.11.4 Drive Control Timing

Symbol	Parameter	Min	Max	Units	Notes
t_{DRV}	DR0-3#, MTR0-3# from End of WR#		100	ns	
t_{DST}	DIR# Setup to STEP# Active	6			
t_{IW}	Index Pulse Width	100		ns	
t_{STD}	DIR# Hold from STEP# Inactive	t_{STR}		ms	
t_{STP}	STEP# Active High Pulse Width	8			
t_{STR}	STEP# Rate Time	1		ms	

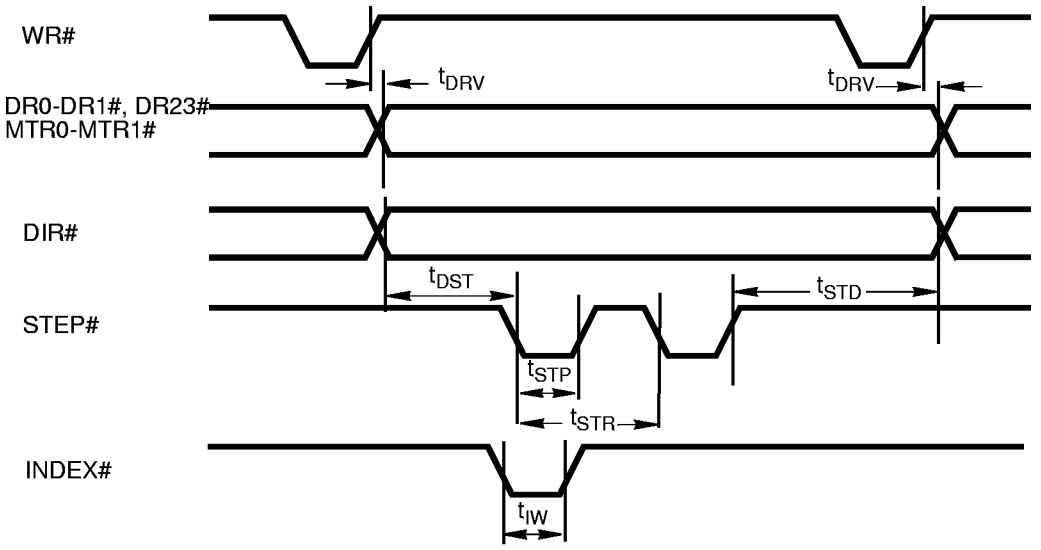


FIGURE 21. Drive Control Timing

7.12 RESET TIMING

Symbol	Parameter	Min	Max	Units	Notes
t_{R-PCI}	PCIRST# Active after PWRGOOD (to PCI Bus)	1		ms	
t_{R-CPU}	CPURST Active after PWRGOOD (to CPU)	2		ms	Note 45
t_{R-INIT}	CPUINIT TRI-STATE during a CPU Warm Reset	460		ns	Note 46

Note 45: The PC87560 will TRI-STATE its CPURST output until it drives it inactive (low). A pull-up resistor connected to the CPU's I/O power rail is required to pull the signal high.

Note 46: The PC87560 will TRI-STATE its CPUINIT output for sixteen PCI Clock periods during a CPU Warm Reset. A pull-up resistor connected to the CPU's I/O power rail is required to pull the signal high.

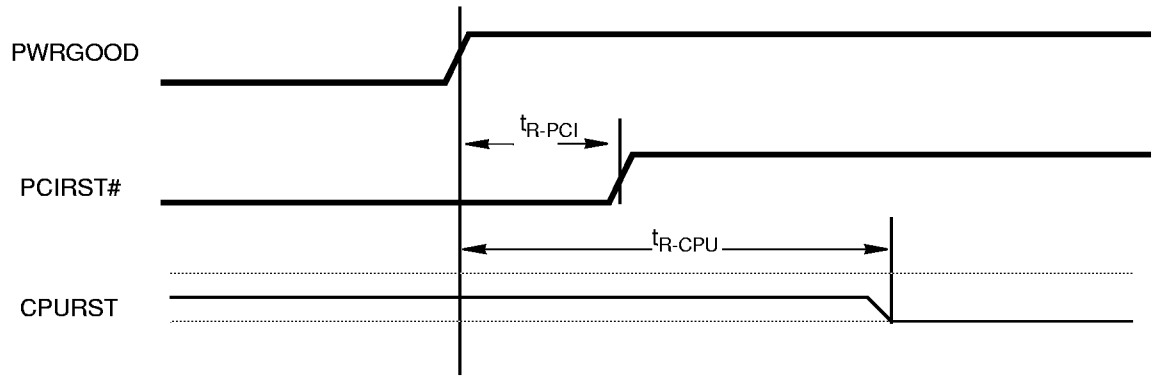


FIGURE 22. Reset Timing

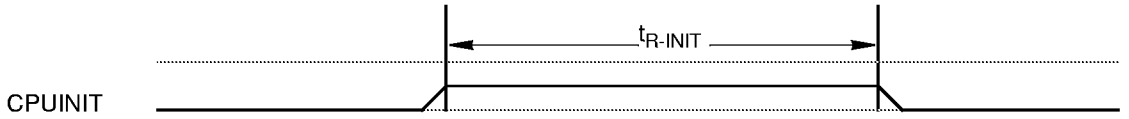


FIGURE 23. Warm Reset CPUINIT

7.13 IDE INTERFACE TIMING FOR DMA TRANSFERS

Symbol	Parameter	Mode 0ns		Mode 1ns		Mode 2ns	
		Min	Max	Min	Max	Min	Max
t_{DMA_0}	IDE DMA DIOR# and DIOW# Access Cycle Time	480		150		120	
t_{DMA_D}	IDE DIOR# and DIOW# Command Strobe Active Time	215		80		70	
t_{DMA_F}	IDE Read Data Hold Time from DIOR# rising	5		5		5	
t_{DMA_G}	IDE Data Setup Time to DIOR#/DIOW# rising	100		30		20	
t_{DMA_H}	IDE Write Data Hold Time from DIOW# rising	20		15		10	
t_{DMA_I}	IDE CH1_DMACK# or CH2_DMACK# Setup Time to DIOR# or DIOW# Command Strobe falling	0		0		0	
t_{DMA_J}	IDE CH1_DMACK# or CH2_DMACK# Hold Time from DIOR# or DIOW# Command Strobe rising	20		5		5	

Symbol	Parameter	Mode 0ns		Mode 1ns		Mode 2ns	
		Min	Max	Min	Max	Min	Max
t_{DMA_K}	IDE DIOR# Command Strobe Inactive Time	50		50		25	
	IDE DIOW# Command Strobe Inactive Time	215		50		25	
t_{DMA_L}	IDE DIOR# Command Strobe active to CH1_DMREQ or CH2_DMREQ valid to indicate if another transfer cycle is to be performed		120		40		35
	IDE DIOR# or DIOW# Command Strobe active to CH1_DMREQ or CH2_DMREQ valid to indicate if another transfer cycle is to be performed		40		40		35
t_{DMA_Z}	IDE CH1_DMACK# or CH2_DMACK# inactive to Read Data TRI-STATE		20		25		25

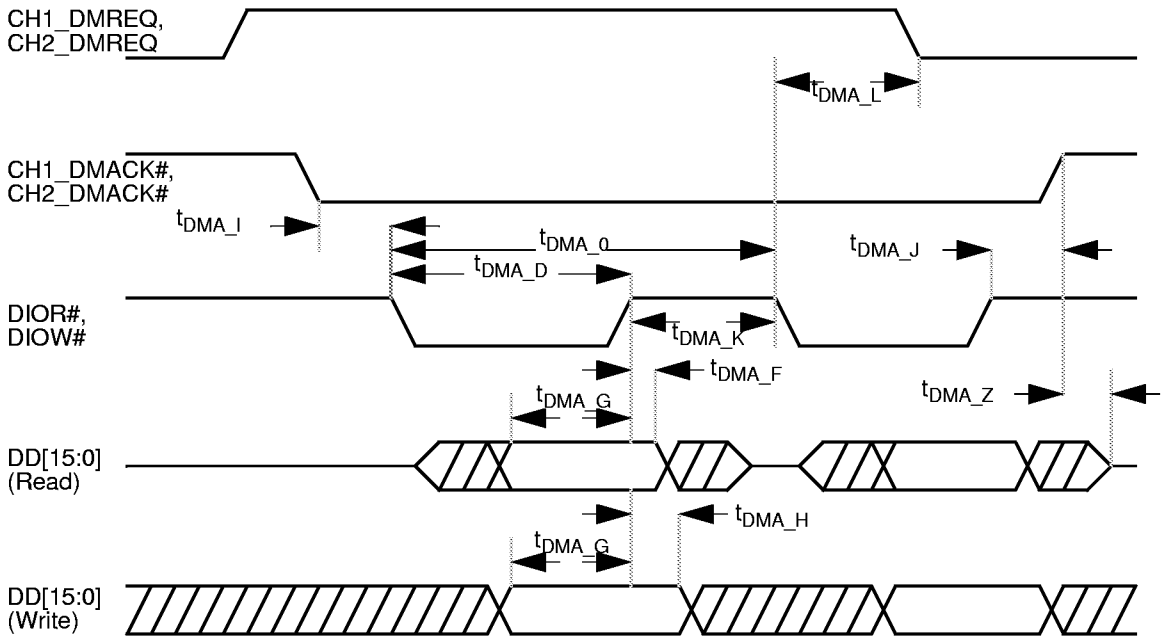
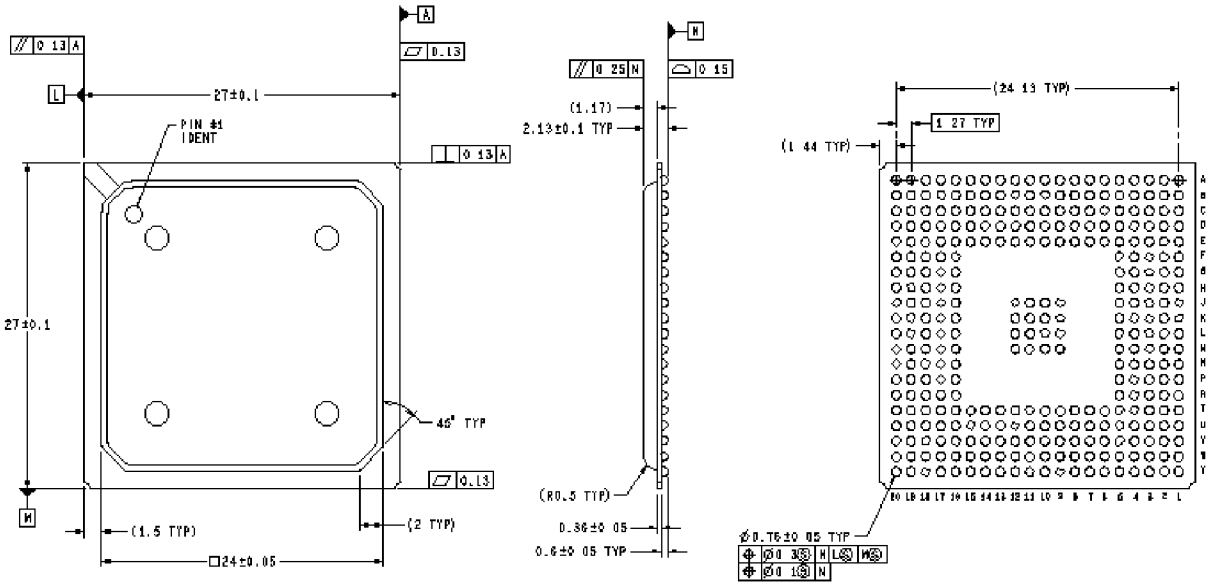


FIGURE 24. IDE DMA Timing

8.0 Physical Dimensions



DIMENSIONS ARE IN MILLIMETERS

316-pin Pin Ball Grid Array (PBGA) Package
Order Number PC87560UBD
NS Package Number UBD316

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