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April 1<sup>st</sup>, 2010 Renesas Electronics Corporation

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# MOS FIELD EFFECT TRANSISTOR 2SK4212A

# **SWITCHING N-CHANNEL POWER MOS FET**

#### DESCRIPTION

The 2SK4212A is N-channel MOS FET device that features a low on-state resistance and excellent switching characteristics, and designed for low voltage high current applications such as DC/DC converter with synchronous rectifier.

### **FEATURES**

Low on-state resistance

 $R_{DS(on)1} = 8.0 \text{ m}\Omega \text{ MAX.} \text{ (Vgs} = 10 \text{ V, I}_D = 30 \text{ A)}$ 

 $R_{DS(on)2}$  = 14 m $\Omega$  MAX. (VGS = 4.5 V, ID = 20 A)

• Low total gate charge

Q<sub>G</sub> = 24 nC TYP. (V<sub>DD</sub> = 15 V, V<sub>GS</sub> = 10 V, I<sub>D</sub> = 30 A)

- 4.5 V drive available
- Avalanche capability ratings

#### ORDERING INFORMATION

	PART NUMBER	LEAD PLATING	PACKING		PACKAGE			
	2SK4212A-ZK-E1-AY Note	Dura Cn (Tin)	Tono 2500 p/rool	U	TO 252 (MD 27K) to 0.27 c			
	2SK4212A-ZK-E2-AY Note	Pure Sn (Tin)	Tape 2500 p/reel		TO-252 (MP-3ZK) typ. 0.27 g			

Note Pb-free (This product does not contain Pb in external electrode).

# ABSOLUTE MAXIMUM RATINGS (TA = 25°C)

Drain to Source Voltage (V <sub>GS</sub> = 0 V)	VDSS	30	V
Gate to Source Voltage (VDS = 0 V)	Vgss	±20	V
Drain Current (DC) (Tc = 25°C)	I <sub>D(DC)</sub>	±48	Α
Drain Current (pulse) Note1	ID(pulse)	±125	Α
Total Power Dissipation (Tc = 25°C)	P <sub>T1</sub>	35	W
Total Power Dissipation (T <sub>A</sub> = 25°C)	P <sub>T2</sub>	1.0	W
Channel Temperature	Tch	150	°C
Storage Temperature	T <sub>stg</sub>	-55 to +150	°C
Single Avalanche Current Note2	las	16	Α
Single Avalanche Energy Note2	Eas	25	mJ

2. Starting T<sub>ch</sub> = 25°C, V<sub>DD</sub> = 15 V, R<sub>G</sub> = 25  $\Omega$ , V<sub>GS</sub> = 20  $\rightarrow$  0 V, L = 0.1 mH

**Notes 1.** PW  $\leq$  10  $\mu$ s, Duty Cycle  $\leq$  1%

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(TO-252)



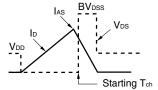
# **ELECTRICAL CHARACTERISTICS (TA = 25°C)**

	1					
CHARACTERISTICS	SYMBOL	TEST CONDITIONS		TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	IDSS	V <sub>DS</sub> = 30 V, V <sub>GS</sub> = 0 V			10	μΑ
Gate Leakage Current	Igss	V <sub>GS</sub> = ±16 V, V <sub>DS</sub> = 0 V			±100	nA
Gate to Source Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	1.5		3.0	V
Forward Transfer Admittance Note	y <sub>fs</sub>	V <sub>DS</sub> = 5 V, I <sub>D</sub> = 12 A	9	19		S
Drain to Source On-state Resistance Note	R <sub>DS(on)1</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 30 A		7.2	8.0	mΩ
	R <sub>DS(on)2</sub>	V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 20 A		10.4	14	mΩ
Input Capacitance	Ciss	V <sub>DS</sub> = 15 V,		1200		pF
Output Capacitance	Coss	V <sub>GS</sub> = 0 V,		180		pF
Reverse Transfer Capacitance	Crss	f = 1 MHz		100		pF
Turn-on Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = 15 V, I <sub>D</sub> = 30 A,		14		ns
Rise Time	tr	V <sub>GS</sub> = 10 V,		11		ns
Turn-off Delay Time	td(off)	$R_G = 3 \Omega$		43		ns
Fall Time	tf			10		ns
Total Gate Charge	Q <sub>G</sub>	V <sub>DD</sub> = 15 V,		24		nC
Gate to Source Charge	Qgs	V <sub>GS</sub> = 10 V,		3		nC
Gate to Drain Charge	Q <sub>GD</sub>	In = 30 A		7		nC
Body Diode Forward Voltage Note	V <sub>F(S-D)</sub>	I <sub>F</sub> = 30 A, V <sub>GS</sub> = 0 V		0.89	1.5	V
Reverse Recovery Time	trr	IF = 30 A, VGS = 0 V,		21		ns
Reverse Recovery Charge	Qm	di/dt = 100 A/μs		12		nC

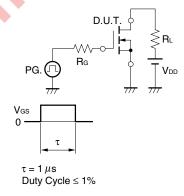
Note Pulsed

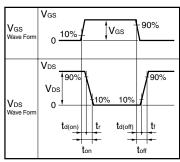
# **TEST CIRCUIT 1 AVALANCHE CAPABILITY**

# $\begin{array}{c} \text{D.U.T.} \\ \text{PG.} \\ \text{PG.} \\ \text{V}_{\text{OS}} = 20 \rightarrow 0 \text{ V} \end{array} \begin{array}{c} \text{D.U.T.} \\ \text{V}_{\text{DD}} \\ \text{V}_{\text{DD}} \end{array}$



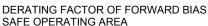
# TEST CIRCUIT 2 SWITCHING TIME

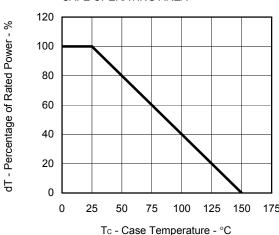




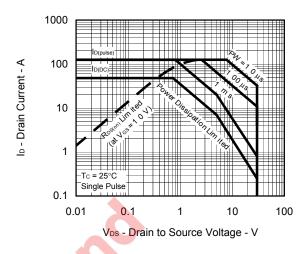
## **TEST CIRCUIT 3 GATE CHARGE**

# TYPICAL CHARACTERISTICS (TA = 25°C)

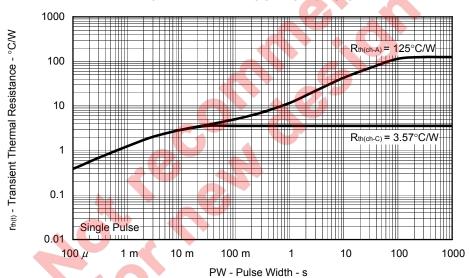




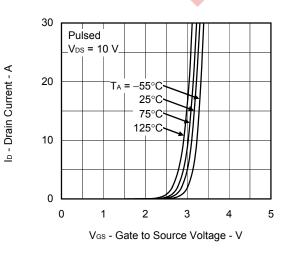
#### FORWARD BIAS SAFE OPERATING AREA



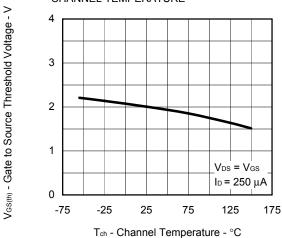
# TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH

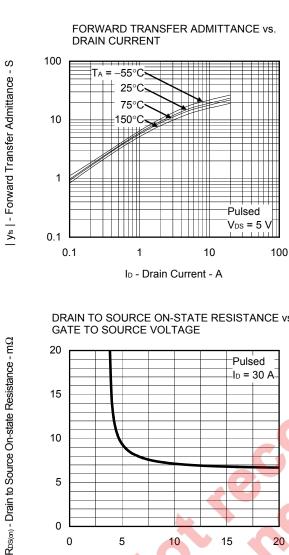


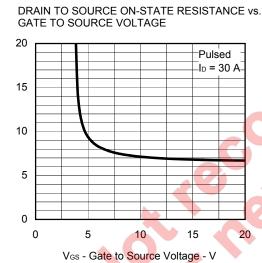
#### FORWARD TRANSFER CHARACTERISTICS

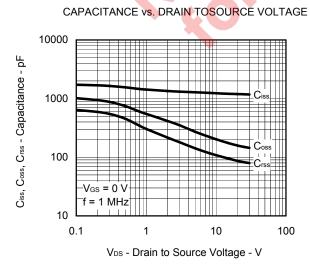


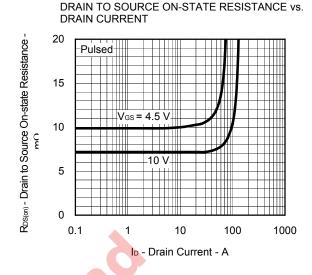
GATE TO SOURCE THRESHOLD VOLTAGE vs. CHANNEL TEMPERATURE

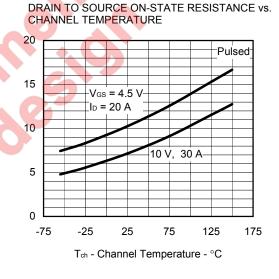


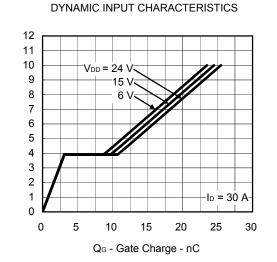








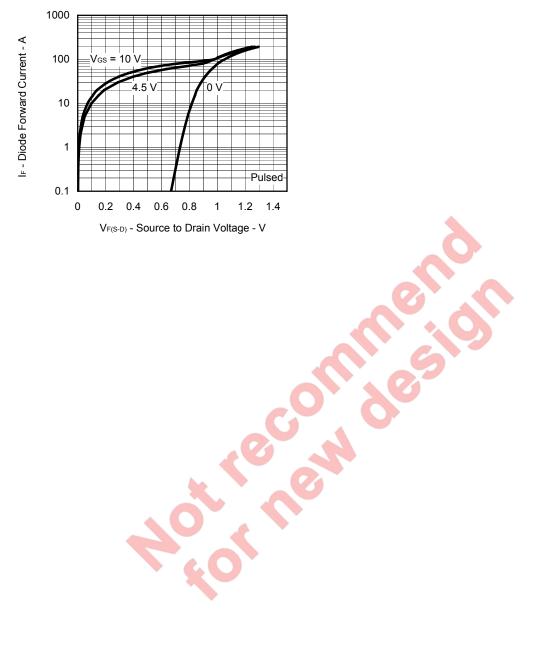




RDS(m) - Drain to Source On-state Resistance

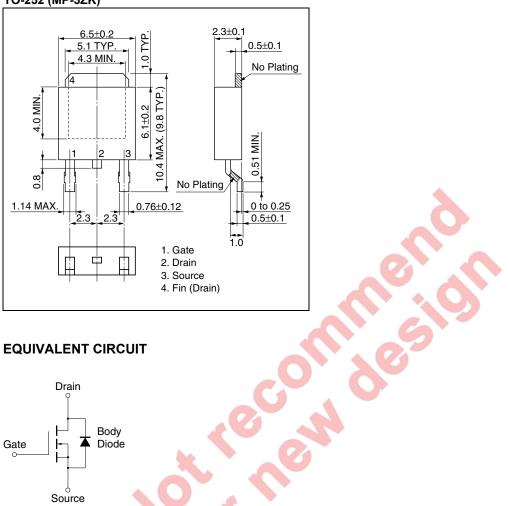
Ves - Gate to Source Voltage - V

#### SOURCE TO DRAIN DIODE FORWARD VOLTAGE

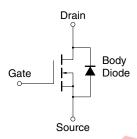


# PACKAGE DRAWINGS (Unit: mm)

# TO-252 (MP-3ZK)



# **EQUIVALENT CIRCUIT**



Remark Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.

6

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