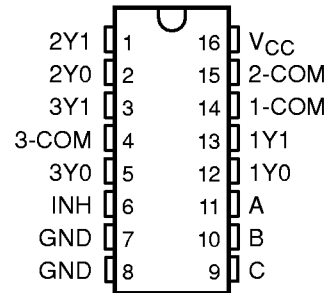


SN54LV4053A, SN74LV4053A TRIPLE 2-CHANNEL ANALOG MULTIPLEXERS/DEMULTIPLEXERS

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- **EPIC™ (Enhanced-Performance Implanted CMOS) Process**
- **High On-Off Output-Voltage Ratio**
- **Low Crosstalk Between Switches**
- **Individual Switch Controls**
- **Extremely Low Input Current**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Package Options Include Plastic Small-Outline (D, NS), Shrink Small-Outline (DB), Thin Very Small-Outline (DGV), Thin Shrink Small-Outline (PW), Ceramic Flat (W) Packages, and Standard Plastic (N) and Ceramic (J) DIPs**

SN54LV4053A . . . J OR W PACKAGE
SN74LV4053A . . . D, DB, DGV, N, NS, OR PW PACKAGE
(TOP VIEW)



description

These triple 2-channel CMOS analog multiplexers/demultiplexers are designed for 2-V to 5.5-V V_{CC} operation.

The 'LV4053A devices handle both analog and digital signals. Each channel permits signals with amplitudes up to 5.5 V (peak) to be transmitted in either direction.

Applications include signal gating, chopping, modulation or demodulation (modem), and signal multiplexing for analog-to-digital and digital-to-analog conversion systems.

The SN54LV4053A is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LV4053A is characterized for operation from -40°C to 85°C .

FUNCTION TABLE

INPUTS				ON CHANNELS
INH	C	B	A	
L	L	L	L	1Y0, 2Y0, 3Y0
L	L	L	H	1Y1, 2Y0, 3Y0
L	L	H	L	1Y0, 2Y1, 3Y0
L	L	H	H	1Y1, 2Y1, 3Y0
L	H	L	L	1Y0, 2Y0, 3Y1
L	H	L	H	1Y1, 2Y0, 3Y1
L	H	H	L	1Y0, 2Y1, 3Y1
L	H	H	H	1Y1, 2Y1, 3Y1
H	X	X	X	None



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**TEXAS
INSTRUMENTS**

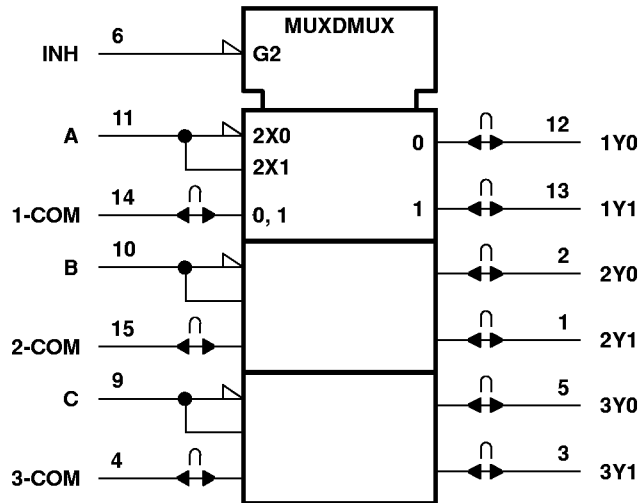
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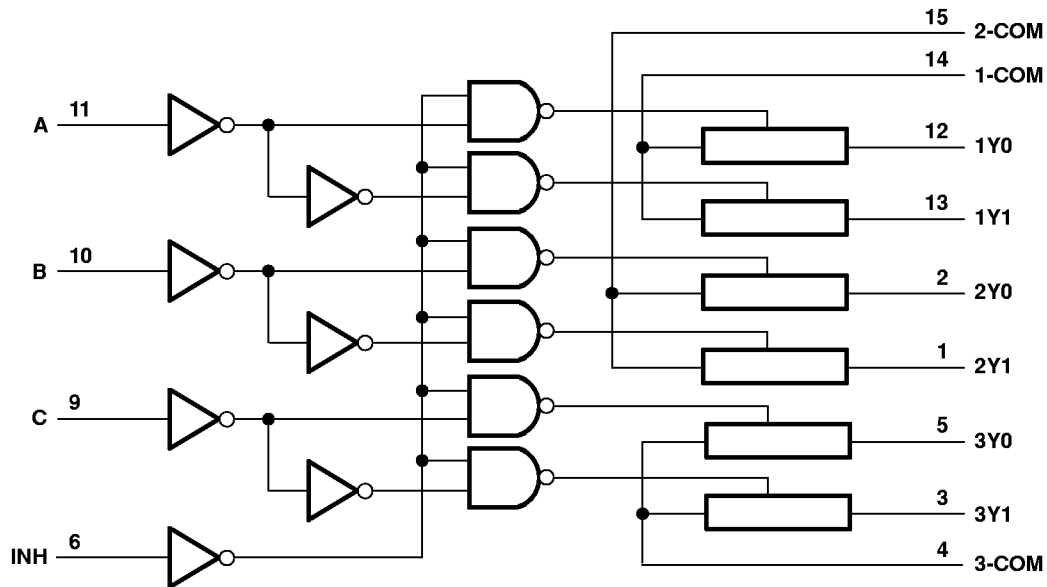
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



SN54LV4053A, SN74LV4053A TRIPLE 2-CHANNEL ANALOG MULTIPLEXERS/DEMULPLEXERS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	–0.5 V to 7.0 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7.0 V
Switch I/O voltage range, V_{IO} (see Note 1 and Note 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–20 mA
I/O diode current, I_{IOK} ($V_{IO} < 0$ or $V_{IO} > V_{CC}$)	±50 mA
Switch through current, I_T ($V_{IO} = 0$ to V_{CC})	±25 mA
Continuous current through V_{CC} or GND	±50 mA
Package thermal impedance, θ_{JA} (see Note 3):	
D package	113°C/W
DB package	131°C/W
DGV package	180°C/W
N package	78°C/W
NS package	111°C/W
PW package	149°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. This value is limited to 7 V maximum.
 3. The package thermal impedance is calculated in accordance with JEDEC 51, except for through-hole packages, which use a trace length of zero.

recommended operating conditions (see Note 4)

		SN74LV4053A		SN74LV4053A		UNIT	
		MIN	MAX	MIN	MAX		
V_{CC}	Supply voltage	2‡	5.5	2‡	5.5	V	
V_{IH}	High-level input voltage, control inputs	$V_{CC} = 2$ V	1.5	1.5		V	
		$V_{CC} = 2.3$ V to 2.7 V	$V_{CC} \times 0.7$	$V_{CC} \times 0.7$			
		$V_{CC} = 3$ V to 3.6 V	$V_{CC} \times 0.7$	$V_{CC} \times 0.7$			
		$V_{CC} = 4.5$ V to 5.5 V	$V_{CC} \times 0.7$	$V_{CC} \times 0.7$			
V_{IL}	Low-level input voltage, control inputs	$V_{CC} = 2$ V	0.5	0.5		V	
		$V_{CC} = 2.3$ V to 2.7 V	$V_{CC} \times 0.3$	$V_{CC} \times 0.3$			
		$V_{CC} = 3$ V to 3.6 V	$V_{CC} \times 0.3$	$V_{CC} \times 0.3$			
		$V_{CC} = 4.5$ V to 5.5 V	$V_{CC} \times 0.3$	$V_{CC} \times 0.3$			
V_I	Control input voltage	0	5.5	0	5.5	V	
V_{IO}	Input/output voltage	0	V_{CC}	0	V_{CC}	V	
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 2.3$ V to 2.7 V	0	200	0	200	ns/V
		$V_{CC} = 3$ V to 3.6 V	0	100	0	100	
		$V_{CC} = 4.5$ V to 5.5 V	0	20	0	20	
T_A	Operating free-air temperature	–55	125	–40	85	°C	

‡ With supply voltages at or near 2 V, the analog switch on-state resistance becomes very nonlinear. It is recommended that only digital signals be transmitted at these low supply voltages.

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			SN54LV4053A		SN74LV4053A		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
R _{on} On-state switch resistance	I _T = 2 mA, V _I = V _{CC} or GND, V _{INH} = V _{IL} (see Figure 1)	2.3 V	41	180		225		225	Ω	
		3 V	30	150		190		190		
		4.5 V	23	75		100		100		
R _{on(P)} Peak on-state resistance	I _T = 2 mA, V _I = V _{CC} to GND, V _{INH} = V _{IL}	2.3 V	139	500		600		600	Ω	
		3 V	63	180		225		225		
		4.5 V	35	100		125		125		
ΔR _{on} Difference in on-state resistance between switches	I _T = 2 mA, V _I = V _{CC} to GND, V _{INH} = V _{IL}	2.3 V	2	30		40		40	Ω	
		3 V	1.6	20		30		30		
		4.5 V	1.3	15		20		20		
I _I Control input current	V _I = V _{CC} or GND	5.5 V			±0.1		±1		±1	μA
I _{soff} Off-state switch leakage current	V _I = V _{CC} and V _O = GND, or V _I = GND and V _O = V _{CC} , V _{INH} = V _{IH} (see Figure 2)	5.5 V			±0.1		±1		±1	μA
I _{son} On-state switch leakage current	V _I = V _{CC} or GND, V _{INH} = V _{IH} (see Figure 3)	5.5 V			±0.1		±1		±1	μA
I _{CC} Supply current	V _I = V _{CC} or GND	5.5 V					20		20	μA
C _{IC} Control input capacitance					2					pF
C _{IS} Common terminal capacitance					8.2					pF
C _{OS} Switch terminal capacitance					5.6					pF
C _T Feed-through capacitance					0.5					pF

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**switching characteristics over recommended operating free-air temperature range,
V_{CC} = 2.5 V ± 0.2 V (unless otherwise noted)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	T _A = 25°C			SN54LV4053A		SN74LV4053A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH} , t _{PHL}	Propagation delay time	COM or Y _n	Y _n or COM C _L = 15 pF, (see Figure 4)		2.5	10		16		16	ns
t _{PZH} , t _{PZL}	Enable delay time	INH	COM or Y _n C _L = 15 pF, (see Figure 5)		7.6	18		23		23	ns
t _{PHZ} , t _{PLZ}	Disable delay time	INH	COM or Y _n C _L = 15 pF, (see Figure 5)		7.7	18		23		23	ns
t _{PLH} , t _{PHL}	Propagation delay time	COM or Y _n	Y _n or COM C _L = 50 pF, (see Figure 4)		4.4	12		18		18	ns
t _{PZH} , t _{PZL}	Enable delay time	INH	COM or Y _n C _L = 50 pF, (see Figure 5)		8.8	28		35		35	ns
t _{PHZ} , t _{PLZ}	Disable delay time	INH	COM or Y _n C _L = 50 pF, (see Figure 5)		11.7	28		35		35	ns

**switching characteristics over recommended operating free-air temperature range,
V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	T _A = 25°C			SN54LV4053A		SN74LV4053A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH} , t _{PHL}	Propagation delay time	COM or Y _n	Y _n or COM C _L = 15 pF, (see Figure 4)		1.6	6		10		10	ns
t _{PZH} , t _{PZL}	Enable delay time	INH	COM or Y _n C _L = 15 pF, (see Figure 5)		5.3	12		15		15	ns
t _{PHZ} , t _{PLZ}	Disable delay time	INH	COM or Y _n C _L = 15 pF, (see Figure 5)		6.1	12		15		15	ns
t _{PLH} , t _{PHL}	Propagation delay time	COM or Y _n	Y _n or COM C _L = 50 pF, (see Figure 4)		2.9	9		12		12	ns
t _{PZH} , t _{PZL}	Enable delay time	INH	COM or Y _n C _L = 50 pF, (see Figure 5)		6.1	20		25		25	ns
t _{PHZ} , t _{PLZ}	Disable delay time	INH	COM or Y _n C _L = 50 pF, (see Figure 5)		8.9	20		25		25	ns

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switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	$T_A = 25^\circ\text{C}$			SN54LV4053A		SN74LV4053A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH} , t _{PHL} Propagation delay time	COM or Y _n	Y _n or COM	C _L = 15 pF, (see Figure 4)	0.9	4		7		7	ns	
t _{PZH} , t _{PZL} Enable delay time	INH	COM or Y _n	C _L = 15 pF, (see Figure 5)	3.8	8		10		10	ns	
t _{PHZ} , t _{PLZ} Disable delay time	INH	COM or Y _n	C _L = 15 pF, (see Figure 5)	4.6	8		10		10	ns	
t _{PLH} , t _{PHL} Propagation delay time	COM or Y _n	Y _n or COM	C _L = 50 pF, (see Figure 4)	1.8	6		8		8	ns	
t _{PZH} , t _{PZL} Enable delay time	INH	COM or Y _n	C _L = 50 pF, (see Figure 5)	4.3	14		18		18	ns	
t _{PHZ} , t _{PLZ} Disable delay time	INH	COM or Y _n	C _L = 50 pF, (see Figure 5)	6.3	14		18		18	ns	

analog switch characteristics

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V _{CC}	$T_A = 25^\circ\text{C}$			UNIT
					MIN	TYP	MAX	
Frequency response (switch on)	COM or Y _n	Y _n or COM	C _L = 50 pF, R _L = 600 Ω, f _{in} = 1 MHz (sine wave) (see Note 5 and Figure 6)	2.3 V		30	MHz	
				3 V		35		
				4.5 V		50		
Crosstalk (between any switches)	COM or Y _n	Y _n or COM	C _L = 50 pF, R _L = 600 Ω, f _{in} = 1 MHz (sine wave) (see Note 6 and Figure 7)	2.3 V		-45	dB	
				3 V		-45		
				4.5 V		-45		
Crosstalk (control input to signal output)	INH	COM or Y _n	C _L = 50 pF, R _L = 600 Ω, f _{in} = 1 MHz (square wave) (see Figure 8)	2.3 V		20	mV	
				3 V		35		
				4.5 V		65		
Feedthrough attenuation (switch off)	COM or Y _n	Y _n or COM	C _L = 50 pF, R _L = 600 Ω, f _{in} = 1 MHz (see Note 6 and Figure 9)	2.3 V		-45	dB	
				3 V		-45		
				4.5 V		-45		
Sine-wave distortion	COM or Y _n	Y _n or COM	C _L = 50 pF, R _L = 10 kΩ, f _{in} = 1 kHz (sine wave) (see Figure 10)	V _I = 2 V _{p-p}	2.3 V	0.1		
				V _I = 2.5 V _{p-p}	3 V	0.1		
				V _I = 4 V _{p-p}	4.5 V	0.1		

NOTES: 5. Adjust f_{in} voltage to obtain 0-dBm output. Increase f_{in} frequency until dB meter reads -3 dB.
 6. Adjust f_{in} voltage to obtain 0-dBm input.

operating characteristics, $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
C _{pd} Power dissipation capacitance	f = 10 MHz	5.3	pF

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PARAMETER MEASUREMENT INFORMATION

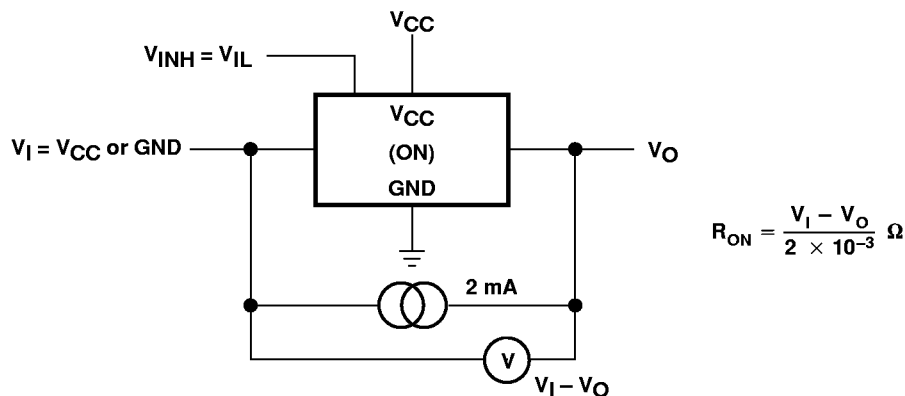


Figure 1. On-State Resistance Test Circuit

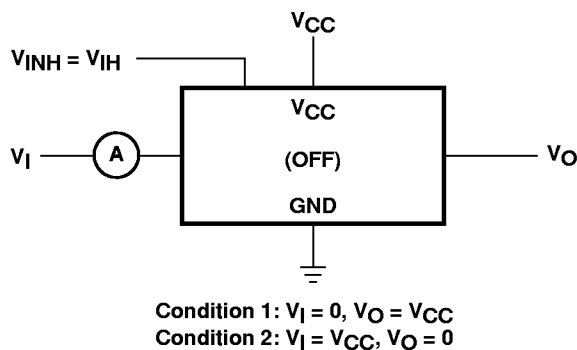


Figure 2. Off-State Switch Leakage-Current Test Circuit

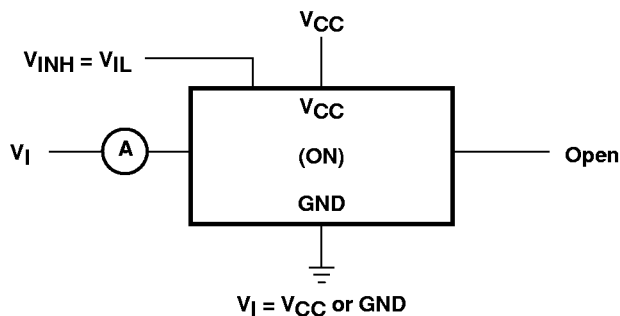


Figure 3. On-State Switch Leakage-Current Test Circuit

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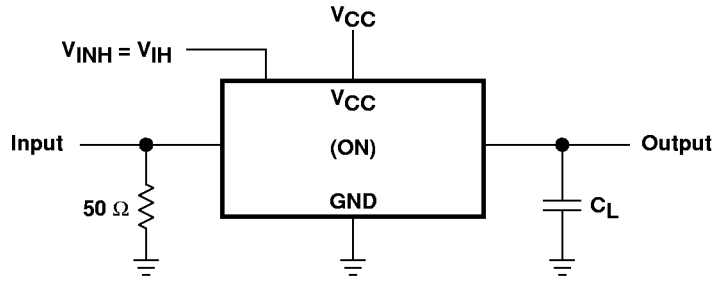


Figure 4. Propagation Delay Time, Signal Input to Signal Output

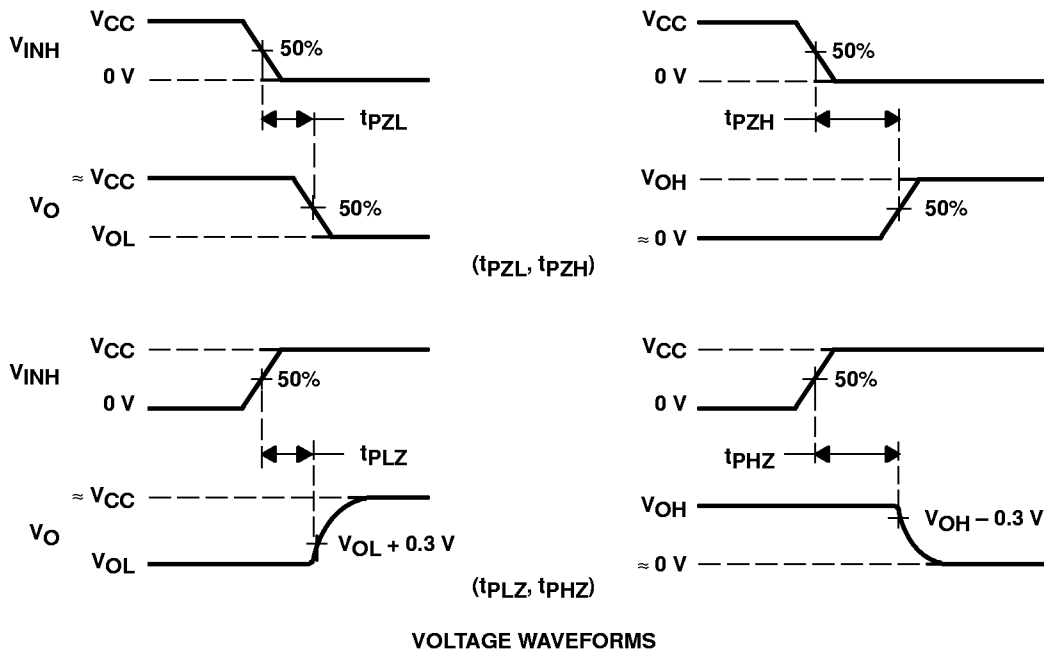
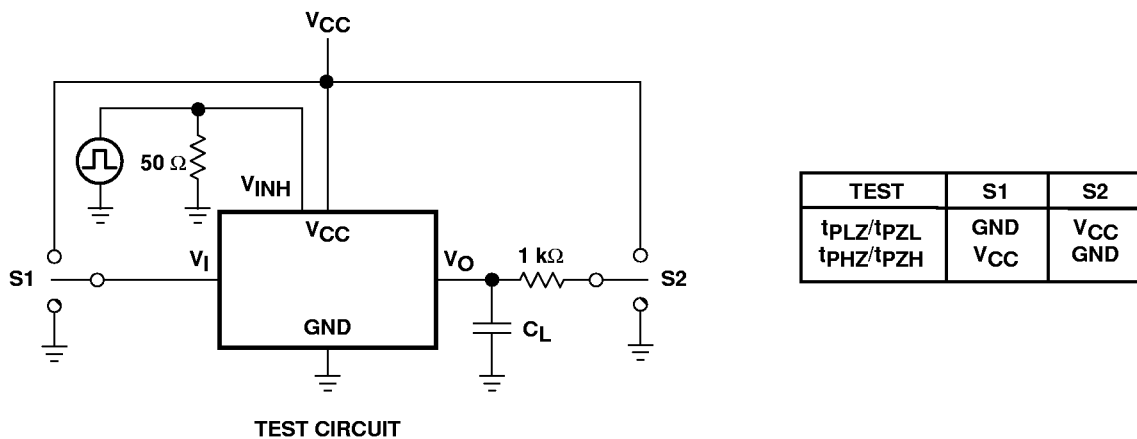
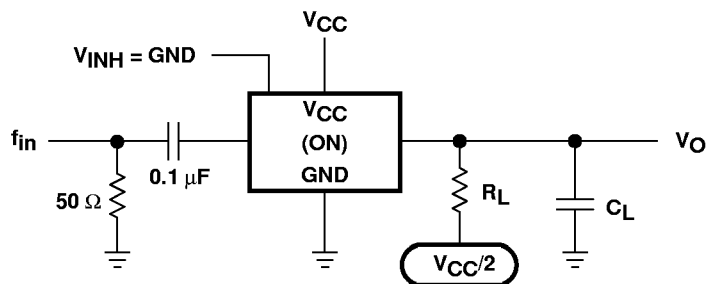


Figure 5. Switching Time (t_{PZL} , t_{PLZ} , t_{PZH} , t_{PHZ}), Control to Signal Output

PARAMETER MEASUREMENT INFORMATION



NOTE A: f_{in} is a sine wave.

Figure 6. Frequency Response (Switch On)

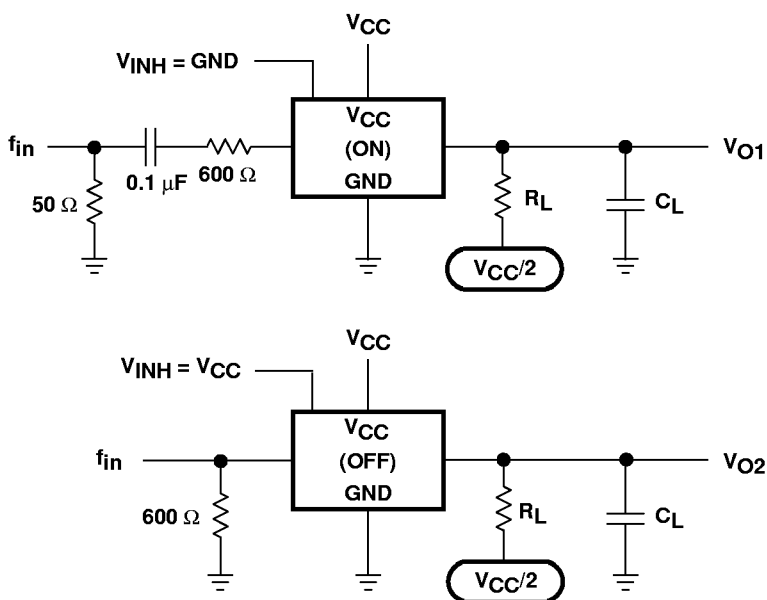


Figure 7. Crosstalk Between Any Two Switches

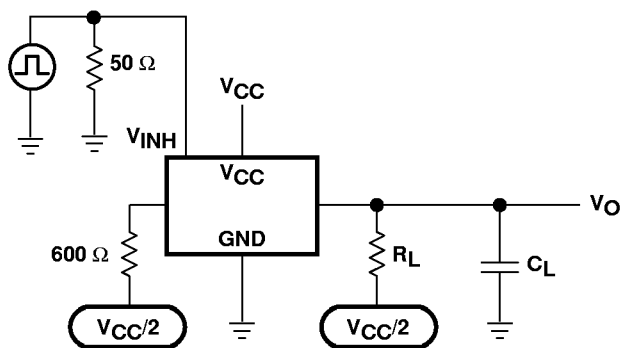


Figure 8. Crosstalk Between Control Input and Switch Output

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PARAMETER MEASUREMENT INFORMATION

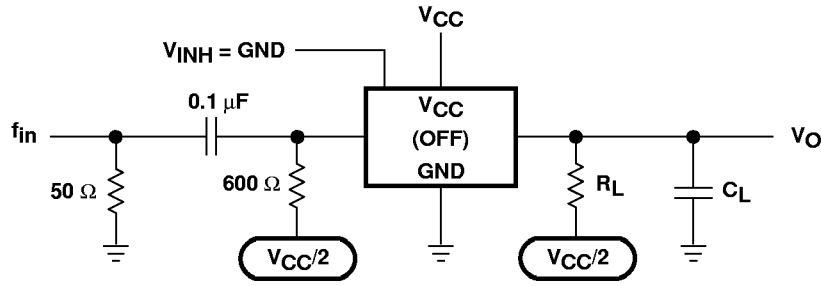


Figure 9. Feed-Through Attenuation (Switch Off)

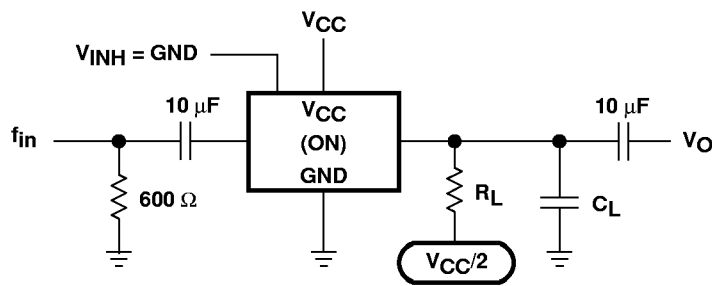


Figure 10. Sine-Wave Distortion

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