MP3376

8-Channel, Synchronous, Boost, WLED Driver with I²C Interface

DESCRIPTION

The MP3376 is a synchronous boostconverter with eight current channels designed to drive WLED arrays for LCDpanelsin tablets and notebook backlighting applications.

The MP3376 uses peak-current-mode and pulse-width modulation (PWM) control to maintainboost converter regulation. The MP3376employs a standard I²C digital interface to set the operation mode,switching frequency, full-scale current for each channel, sync or non-sync mode, dimming mode and duty, and various protection thresholds.

The MP3376 features high efficiency with a small on resistance of the switching MOSFET. The synchronous rectifier saves PCB size and total BOM cost.

The MP3376 is available in a QFN-24 (4mmx4mm) package.

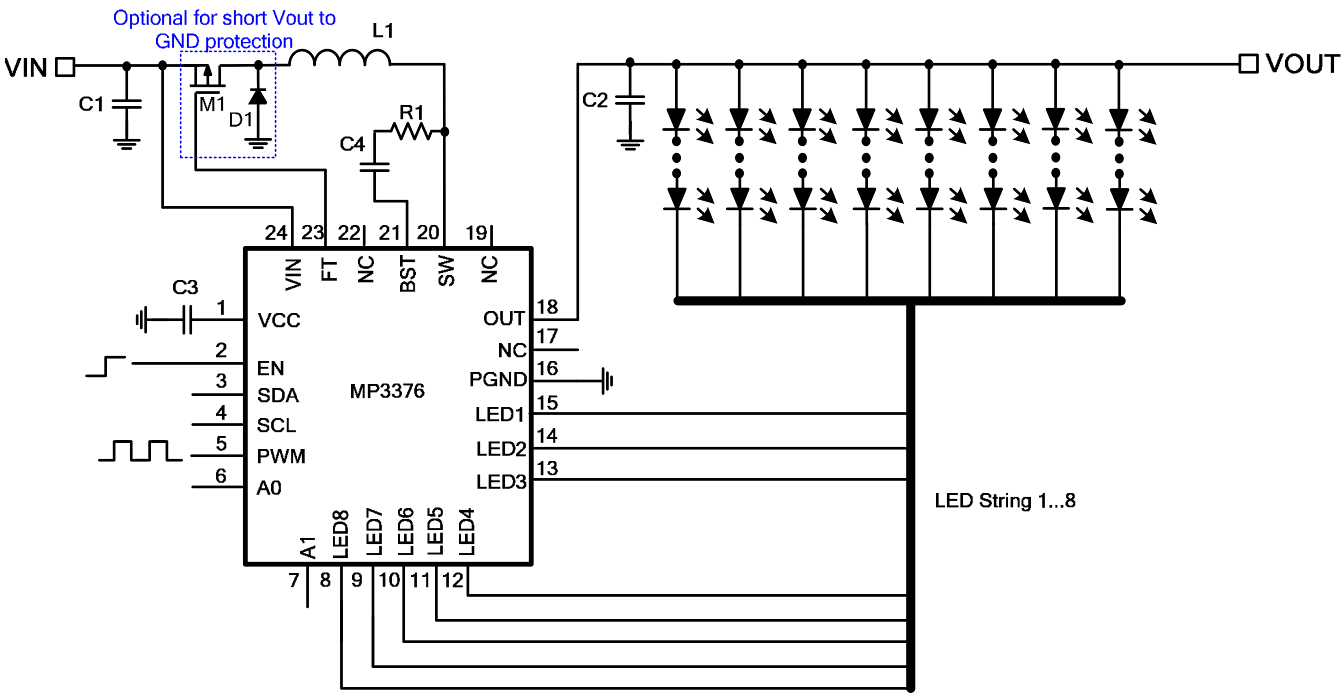
FEATURES

- 8Channels with Max50mA/Channel
- Synchronous Converter with LS-FET/HS-FET 160mΩ/260mΩOn Resistance
- 3V to 30V Input Voltage Range
- Up to 36V Output Voltage
- Max 2.5% Current Matching
- 350kHz/500kHz/650kHz/800kHz/950kHz/1.2MHz/1.8MHz/2.4MHz Selectable Switching Frequency
- A0, A1 Pins for FourI²C Addresses
- 0mA to 50mA Full-Scale Current Set, 8-Bit,0.196mA/Step
- Selectable Sync or Non-Sync Mode
- Multi-Dimming Operation Mode Including:
  - Analog Dimming ModethroughExternal PWM Input
  - Analog Dimming Modethrough I²C Interface
  - MixedDimming Mode throughExternal PWM Input with6.25%/12.5%/25%/50%Transfer Point
  - MixedDimming Mode through I²C Interface with 6.25%/12.5%/25%/50% Transfer Point
- Customizable Default Register Values
- Linear Smooth Dimming with 2/4/8/16/32/64/128µs for Per-StepSlope Set
- Unused LED String Auto-Disable during Start-Up
- LED Short/Open, OTP, OCP, Inductor or Diode Short Protection
  - 2.5 / 5 / 7.5 / 10V LED Short Threshold
  - 24/31/36V OVP Threshold
  - 1.8 /2.5A Cycle-by-Cycle Current Limit
- Free for Adjacent Pin Short Test
- Available in a QFN-24(4mmx4mm)Package

APPLICATIONS

- Tablets/Notebooks
- Automotive Displays

TYPICAL APPLICATION



ORDERING INFORMATION

Part Number*	Package	Top Marking
MP3376GR-XXXX**	QFN-24 (4mmx4mm)	*See Below*

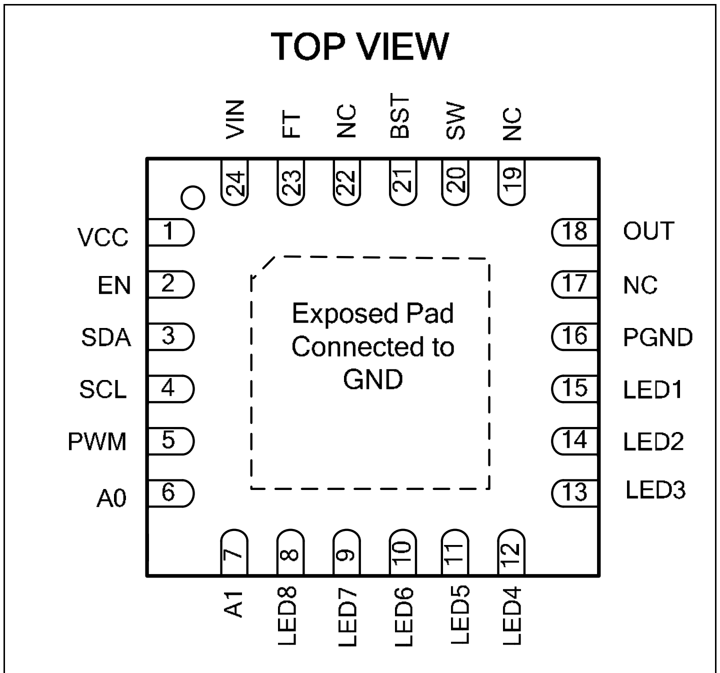
* For Tape & Reel, add suffix –Z (e.g. MP3376GR-XXXX-Z)
** “XXXX” is the register setting option. The factory default is “0000.” This content can be viewed in Table 1 through Table 6. For custom options, please contact an MPS FAE to obtain a “XXXX” value.

TOP MARKING

MPSYWW
MP3376
LLLLLL

MPS: MPS prefix
Y: Year code
WW: Week code
MP3376: Part number
LLLLLL: Lot number

PACKAGE REFERENCE



QFN-24 (4mmx4mm)

ABSOLUTE MAXIMUM RATINGS (1)

V_{SW}, V_{OUT} .... -0.3V to +40V
V_{FT} .... V_{IN}-6V to V_{IN}
V_{LEDX} .... -0.3V to +40V
V_{BST} .... -0.3V to V_{SW}+6V
V_{IN} .... -0.3V to +32V
All other pins .... -0.3V to +6.5V
Junction temperature .... 150°C
Lead temperature .... 260°C
Continuous power dissipation T_A = 25°C (2)
QFN-24 (4mmx4mm) 2.7W

Recommended Operating Conditions (3)

Supply voltage (VIN) .... 3V to 30V
Operating junction temp. (T_J) ... -40°C to +125°C

Thermal Resistance (4)

	θ_{JA}	θ_{JC}	
QFN-24 (4mmx4mm)	46	10	°C/W

NOTES:
1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

VIN =3.7V, V_{EN} = 2V, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Operating input voltage	V_{IN}		2.7		30	V
Supply current (quiescent)	I_Q	VIN=V_{EN}=3.7V, no switching		5.4		mA
Supply current (shutdown)	I_{ST}	V_{EN}=0V, VIN=3.7V			1	μA
Input UVLO threshold	V_{IN_UVLO}	Rising edge		2.5		V
Input UVLO hysteresis				200		mV
LDO output voltage	V_{CC}	V_{EN}=2V, 6V<VIN<30V, 0<I_{VCC}<10mA	4.4	4.9	5.4	V
EN on threshold	V_{EN_ON}	V_{EN}rising	1.2			V
EN off threshold	V_{EN_OFF}	V_{EN}falling			0.4	V
EN pull-down resistor	R_{P_EN}			500		kΩ
A0, A1 low threshold	V_{A_Lo}	$V_A$falling			0.4	V
A0, A1 high threshold	V_{A_Hi}	V_A rising	1.2			V
A0, A1 pull-up resistor	R_{P_A}			500		kΩ
Step-Up Converter						
Low-side MOSFETonresistance	R_{DS_LS}	VIN=6V		160		mΩ
High-side MOSFETonresistance	R_{DS_HS}	VIN=6V		260		mΩ
SW leakage current	I_{SW_LK}	V_{SW}=40V			1	μA
Switching frequency	F_{SW}	FS2:0bits=011b	720	800	880	kHz
Maximum duty cycle	D_{MAX}	Sync mode, F_{SW}=800kHz	90	94		%
		Non-sync mode, F_{SW}=800kHz	93	95		%
SW current limit	I_{SW_LIMIT}	Duty=90%, ILIM bit=1b	2	2.5	3	A
Current Dimming						
PWM input low threshold	V_{PWM_LO}	V_{PWM}falling			0.4	V
PWM input high threshold	V_{PWM_HI}	V_{PWM}rising	1.2			V
PWM pull-down resistor	R_{P_PWM}			500		kΩ
Mix dimming transfer point		DIMT1:0 bits=10b		25		%
LEDcurrent up/down slope	T_{STEP}	TSLP2:0 bits=010b		8		μs
PWM dimming frequency set by I²C	F_{PWM}	FPWM3:0 bits=1010b		22		kHz
LED Current Regulator						
LEDX regulation voltage	V_{HD}	I_{LED}=20mA	350	420	490	mV
Current matching(5)		I_{LED}=20mA			2.5	%
Full-scale current		ISET7:0 bits=FFh	49	50	51	mA
		ISET7:0 bits=66h	19.6	20	20.4	mA

ELECTRICAL CHARACTERISTICS *(continued)*

VIN =3.7V, V_{EN} = 2V, T_A = 25°C, unless otherwise noted.

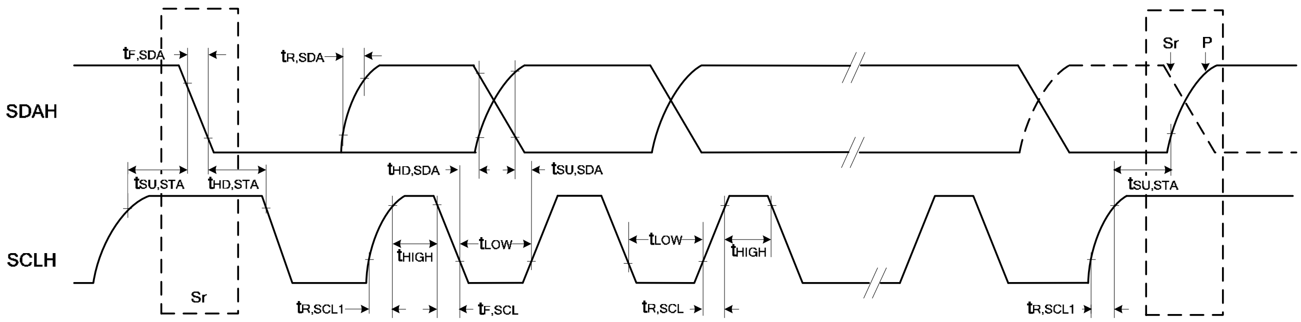
Parameter	Symbol	Condition	Min	Typ	Max	Units
Protection						
Over-voltage protection threshold	V_{OVP}	Rising edge, OVP1:0 bits=10b	34.5	36	37.5	V
OVP UVLO threshold	V_{OVP_UV}	Step-up converter fails		1.2		V
LEDX over-voltage threshold	V_{LEDX_OV}	LEDS1:0 bits=10b		7.5		V
LEDX over-voltage fault timer		F_{SW}=1.2MHz	1.5	1.8	2	ms
LEDX UVLO threshold	V_{LEDX_UV}			100		mV
Thermal shutdown threshold	T_{ST}	Rising edge		150		°C
		Hysteresis		20		°C
FT pull-down current	I_{FT}		50	60	70	µA
FT voltagew/ respect to VIN	$V_{FT\text{-}IN}$	VIN=12V, $V_{FT\text{-}IN}$=VIN-V_{FT}		6		V
I²C Interface						
Input logic low	V_{IL}				0.4	V
Input logic high	V_{IH}		1.3			V
Output logic low	V_{OL}	I_{LOAD}=3mA			0.4	V
SCLclock frequency	f_{SCL}				1200	kHz
Set-up time for repeated start condition	$t_{SU,STA}$		160			ns
Hold time for repeated start condition	$t_{HD,STA}$		160			ns
Low time for SCLHclock	t_{LOW}		160			ns
High time for SCLHclock	t_{HIGH}		60			ns
Data set-up time	$t_{SU,DAT}$		10			ns
Data hold time	$t_{HD,DAT}$		0(6)		70	ns
Rise time of SCLHclock	$t_{R,SCL}$		10		40	ns
Rise time of SCLHclock after repeated start and acknowledge bit	$t_{R,SCL1}$		10		80	ns
Fall time of SCLHclock	$t_{F,SCL}$		10		40	ns
Rise time of SDAHdata	$t_{R,SDA}$		10		80	ns
Fall time of SDAHdata	$t_{F,SDA}$		10		80	ns
Set-up time for stop condition	$t_{SU,STO}$		160			ns
Capacitive load for SDAHlineand SCLHline	C_B(7)				100	pF
Capacitive load for SDAH+SDAlineand SCLH+SCL line	C_B				400	pF

NOTES:

5) Matching is defined as the difference of the maximum to minimum current divided by 2 times the average current.

6) A device must provide a data hold timeinternally to bridge the undefined part between VIL and VIHof the falling edge of the SCLH signal. An input circuit with a threshold as low as possible for the falling edge of SCLH signal minimizes the hold time.

7) For the bus line load CB between 100pF and 400pF, the timing parameters must be increasedlinearly.



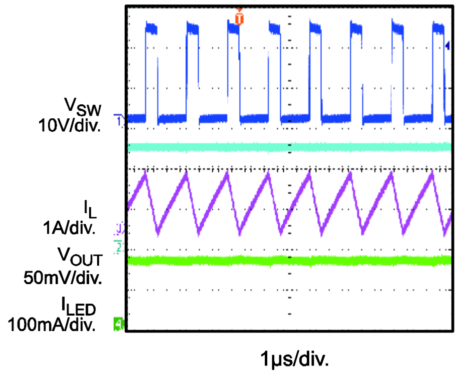
Sr: Repeated START Condition
P: STOP Condition

I2C Compatible Interface Timing Diagram

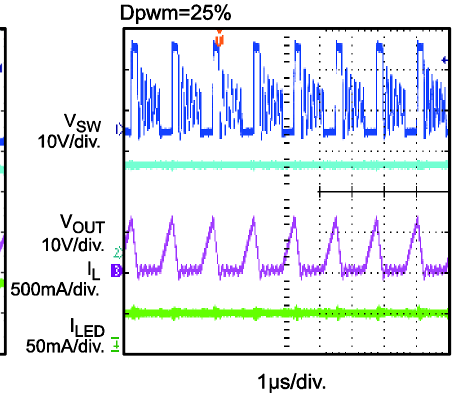
TYPICAL PERFORMANCE CHARACTERISTICS

VIN = 7V, 8LEDs in series, 8 strings, 20mA/string, L = 4.7µH, T_A = 25°C, unless otherwise noted.

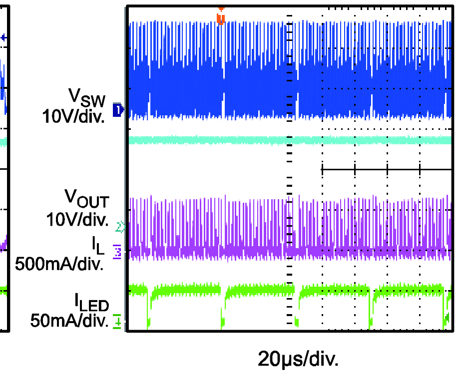
Analog Dimming Mode
steady state



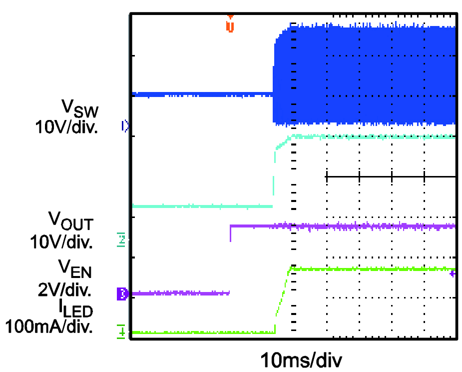
Mix Dimming Mode
with 25% transfer point
Dpwm=25%



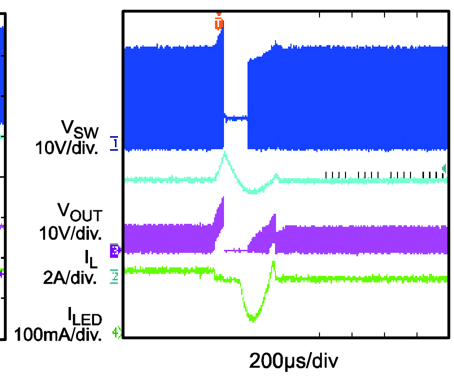
Mix Dimming Mode
with 25% transfer point
Dpwm=24%



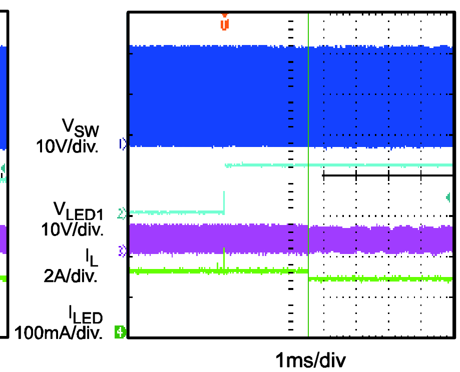
EN power on



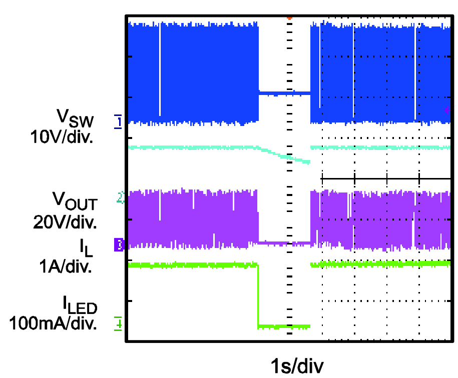
Open LED Protection
Vovp=31V



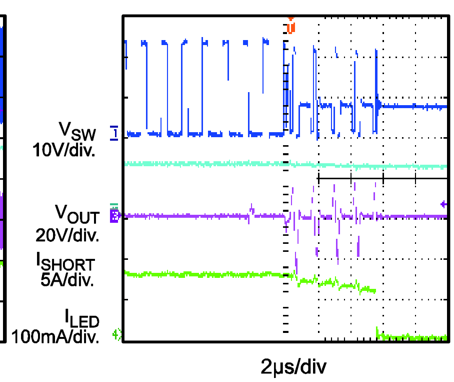
Short LED Protection
Short channel LED1



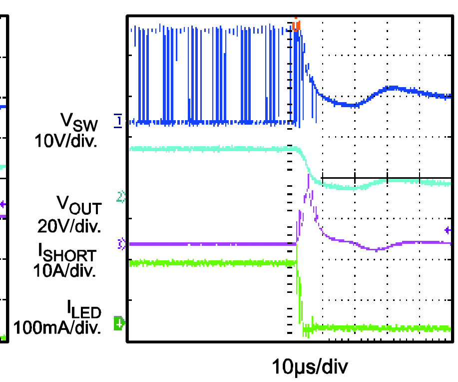
Thermal Protection



Short Indutor Protection



Short Diode Protection



PIN FUNCTIONS

Pin #	Name	Description
1	VCC	**4.9V LDO output.** VCC provides power for the internal logic and gate driver. Place a ceramic capacitor as close to VCCas possible to reduce noise.
2	EN	**IC enable.** PullEN high to enable the IC;pullEN lowto make the IC enter shutdown mode.
3	SDA	**I²C interface data input.**
4	SCL	**I²C interface clock input.**
5	PWM	**PWM signal input.** Connect PWM to VCC if not used.
6	A0	**IC select.**A0 is pulled high internally.
7	A1	**IC select.**A1 is pulled high internally.
8	LED8	**LED current source 8 output.** If LED8 is unused, tie it to GND.
9	LED7	**LED current source 7 output.** If LED7 is unused, tie it to GND.
10	LED6	**LED current source 6 output.** If LED6is unused, tie it to GND.
11	LED5	**LED current source 5 output.** If LED5 is unused, tie it to GND.
12	LED4	**LED current source 4 output.**If LED4 is unused, tie it to GND.
13	LED3	**LED current source 3 output.** If LED3 is unused, tie it to GND.
14	LED2	**LED current source 2 output.** If LED2 is unused, tie it to GND.
15	LED1	**LED current source 1 output.** If LED1 is unused, tie it to GND.
16	PGND	**Power ground.**
17,19, 22	NC	**No connection.**
18	OUT	**Synchronous boost output.**
20	SW	**Switching node.**
21	BST	**Bootstrap capacitor node for the high-side MOSFET.**Connect a 100nFceramic capacitor and a 47Ω resistor in series between BST and SW for synchronous mode.
23	FT	**Input disconnection PMOS gate driver.** If there is no fault, FT is pulled low to turn on the external PMOS. Float FT and connect the inductor to VIN directly if the disconnection function is not needed.
24	VIN	**IC input power.** Place a ceramic capacitor as close to VINas possible to reduce noise.
	EP	**Exposed pad.** Connect the EP to GND.

BLOCK DIAGRAM

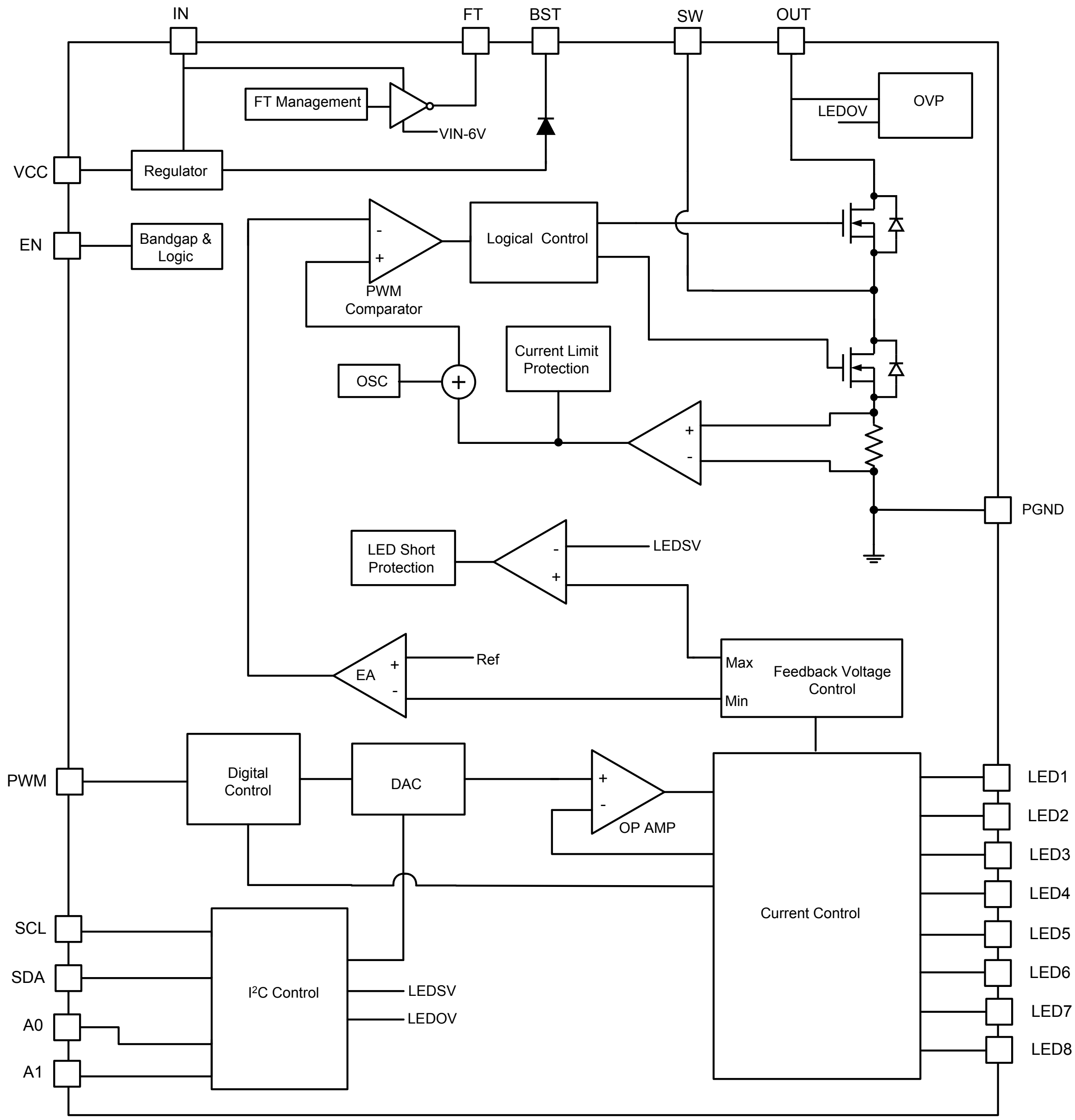


Figure 1: Functional Block Diagram

OPERATION

The MP3376isa programmable, constant-frequency, peak-current-mode, step-up converter with up to eight channels of regulated current sources to drivean array of white LEDs. The MP3376provides a fully integrated solution that saves PCB size and total solution cost. For ease of use, an I^2C interface is also integrated intothe IC.

Internal 4.9V Regulator

The MP3376 includes an internal linear regulator (VCC). When VIN is greater than6V, this regulator outputs a 4.9V power supply to the internal MOSFET gate driver and internal control circuitry. VCC drops to 0V when the chip shuts down. The MP3376is disabled until VCC exceeds the UVLO threshold.

Internal Clock

The MP3376hasa fixed 10MHz clock for the internal timer and counter to achieve ahigh dimming resolution.

Boost Converter Switching Frequency

The boost converter switching frequency can be set by the FS2:0bits of register01h.It can be set to350kHz,500kHz, 650kHz, 800kHz,950kHz, 1.2MHz, 1.8MHz, or 2.4MHz.

System Start-Up

When enabled, the MP3376 checks the topology connection. First, the IC draws current from FT to turn onthe input disconnect PMOSif this MOSFET is being used. Second, after a 500µs delay, the IC monitors the OUT voltage(V_{OUT}) to determine if the output is shorted to GND. If the output voltage is less than 1.2V,the IC is disabled.Lastly, the MP3376continues to check other safety limits, such asLEDopen and over-voltage protection (OVP). If all protection tests pass, the ICbeginsboosting the step-up converter with an internal softstart.

The MP3376 can start up properly regardless of the order in which VIN, PWM, and EN turn on. To achieve a quick response,the recommended power-on sequence is from VINpower on toPWM dimming signalonto EN on(see Figure2).When dimming is done just by the internal register, the PWM dimming signal can be ignored.

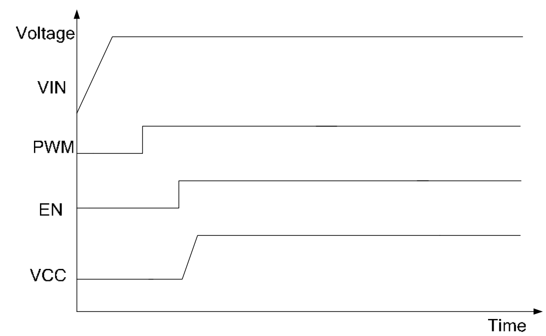


Figure2:Recommended Power-On Timing

Step-Up Converter

The MP3376 usespeak-current-mode control to regulate the output voltage. At the beginning of each switching cycle, the internal clock turns on the low-sideN-channel MOSFET. In normal operation, the minimum turn-on time is around 100ns. A stabilizing ramp added to the output of the current senseamplifier prevents subharmonic oscillations for duty cycles greater than 50%. This result is fed into the PWM comparator. When the summed voltage reaches the output voltage of the error amplifier, the low-sideMOSFET turns off.

The output voltage of the error amplifier is an amplified signal of the difference between the reference voltage and the feedback voltage. The converter chooses the lowest active LEDX voltage automatically as the feedback voltage to regulate an outputvoltage high enough andpower all of the LED arrays.

If the feedback voltage drops below the reference, the output of the error amplifier increases. Thisresults in increasedcurrent flowing through the MOSFET andincreased power delivered to the output. This forms a closed loop that regulates the output voltage.

Pulse-Skipping Mode

Under light-load operation, especially in the case of $V_{OUT} \approx$VIN,the converter runs in pulse-skipping mode, where the MOSFET turns on for a minimum ontime.In this mode, the device keeps the powerswitch off for several switching cycles to prevent the output voltage from rising above the regulated voltage.When the chip stops switching, theoutput capacitor discharges to the powerLED string.The device begins switching until the output voltage needs to be boosted again.

Full-Scale Current Setting

LED full-scale current for each channel can be set by the register ISET7:0bits from 0-50mA with 0.196mAper step.

Dimming Control

The MP3376 can provide flexible dimming methods based on the dimming mode setting shown below, including analog dimming mode and mix dimming mode(see Figure 3 and Figure 4).Each mode can control the brightness by an external PWMinput signal or I^2C interface.

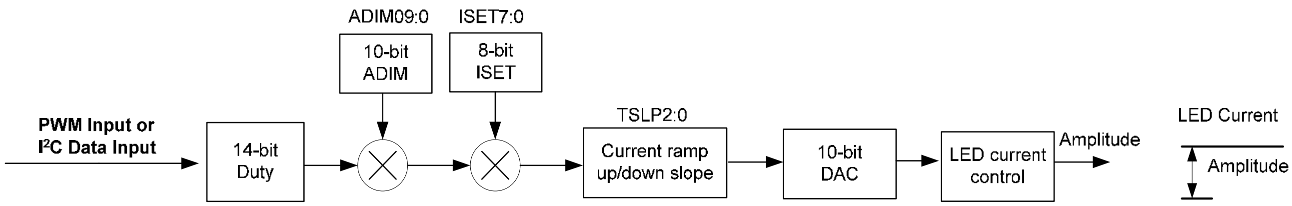


Figure 3: Analog Dimming Mode Flow Chart

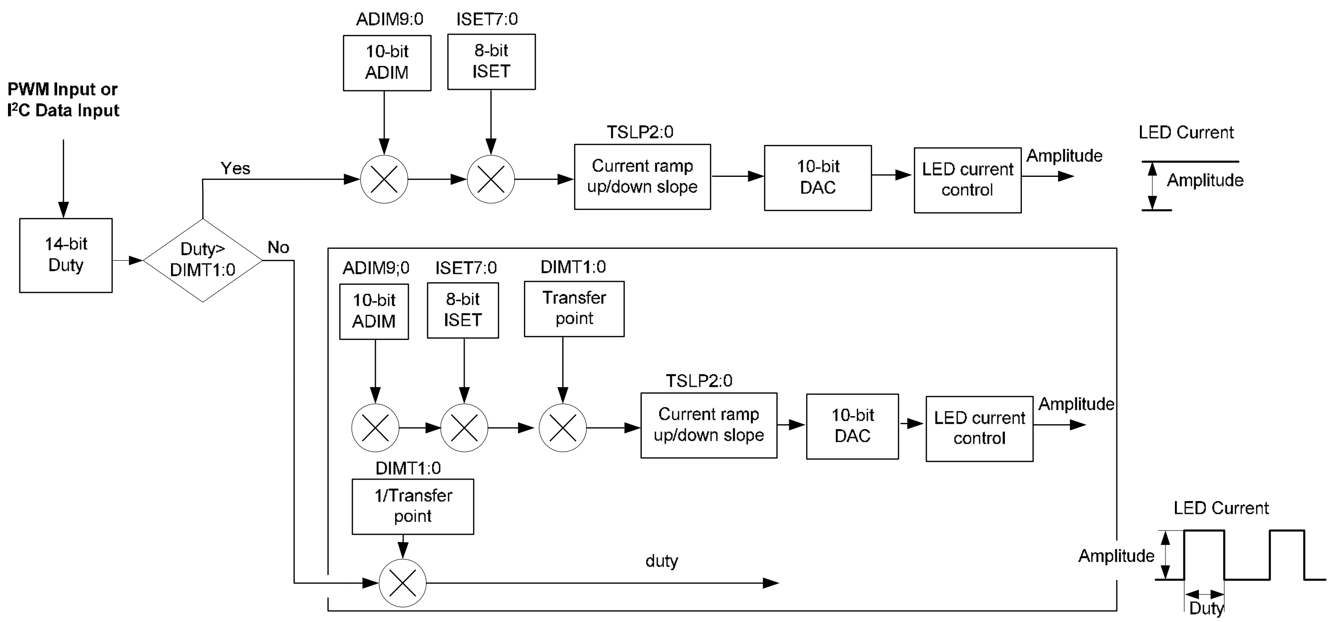


Figure 4: MixedDimming Mode Flow Chart

The MP3376 has four types of dimming modes total.

1. AnalogDimming Mode from PWM Pin

MOD2:0bits=000b. In analog dimming mode, the LED current amplitude is dependent on the duty cycle of the PWM input signal.

Note that the current amplitude can be changed by the register ADIM9:0 10-bitvalue(see Figure5).

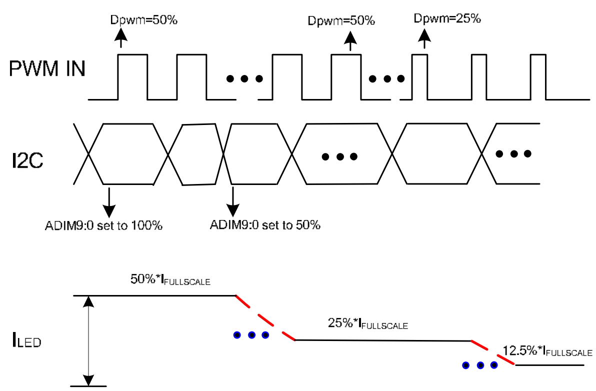


Figure 5: Analog Dimming from PWM Pin

2. AnalogDimming Mode from I^{2}C Interface

MOD2:0 bits = 001b. In analog dimming mode,the LED current amplitude is set by the internal register PWM13:0 bits.

Note that the current amplitude can be changed by the register ADIM9:0 10-bit value(see Figure6).

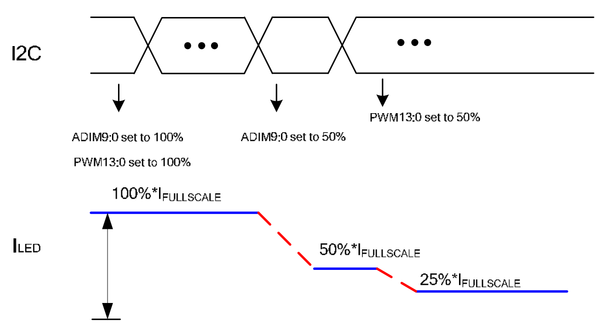


Figure 6: Analog Dimming from I^{2}C Interface

3. Mix Dimming Mode from PWM Input

MOD2:0 bits=100b. In mix dimmingmode, if the duty cycle from PWM is larger than the threshold set by the register DIMT1:0bits, the IC works in analog dimming mode. The LED current amplitudefollows the input duty. If the duty cycle from PWM is lower than the threshold set by the DIMT1:0bits, the IC works in PWM dimming mode, and the PWM frequency is set by the register FPWM3:0 bits. The PWM dimming duty is extended according to the transfer point selected.

For example, if the transfer point is 25%, then the PWM LED current duty = PWM input duty x 1/(25%). The PWM LED current amplitude is fixed to the value at the transfer point set by DIMT1:0.

Note that the current amplitude can be changed by the internal register ADIM9:0 10-bit value(see Figure7).

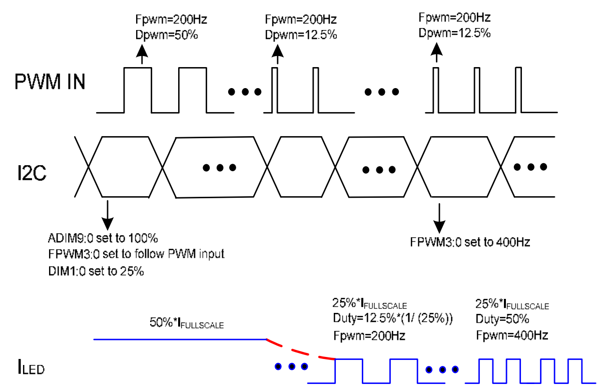


Figure 7: Mix Dimming from PWM Input

4. Mix Dimming Mode from I^{2}C Interface

MOD2:0bits=101b. In mix dimming mode, if the duty cycle from the internal register PWM13:0 bits is larger than the threshold set by register DIMT1:0bits, the IC works in analog dimming mode. The LED current amplitudefollowsthe register PWM13:0 bits. If the duty cycle from the register PWM13:0 bits is lower than the threshold set by register DIMT1:0bits, the IC works in PWM dimming mode, and the PWM frequency is set by the register FPWM3:0 bits.The PWM dimming duty is extended according to the transfer point selected.

For example, if the transfer point is 25%, then the PWM LED current duty = duty set by PWM13:0 bits x 1/(25%). The PWM LED current amplitude is fixed to the value at the transfer point duty set by DIMT1:0.

Note that the current amplitude can be changed by the internal register ADIM9:0 10-bit value(see Figure8).

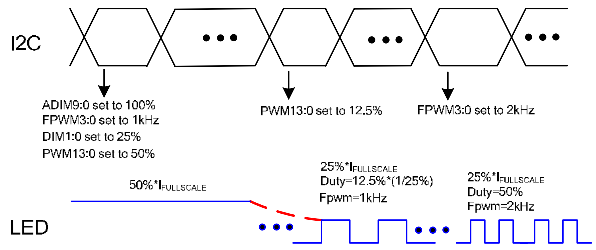


Figure 8: Mix Dimming from I²C Interface

Linear Dimming for Fade In/Out

The MP3376 provides linear current rise up or down. The LED current ramps up or down linearly.The current ramp-up or ramp-down slope can be set by the register TSLP2:0bits from 2μs to 128μs(0.049mA for each step).

Deep Dimming Ratio

To provide enough output energy for the LED load when the PWM LED dimming duty is very smalland the PWM dimming signal is off, the MP3376 provides at least four switching cycles to guarantee enough output voltage before the next PWM dimming oncycle. This way, the MP3376 can achieve a very wide dimming ratio range in PWM dimming mode. The dimming ratio is dependent on the PWM dimming frequency and LED current source turn-on/-off time. The lower the PWM dimming frequency, the deeper the PWM dimming ratio.

For the MP3376, it is recommended that theminimum on time of the LED string is higher than 1.5μsto achieve good dimming.The dimming ratio can reach 100:1 at 22kHzin mix dimming mode.

Unused LED Channel Setting

The MP3376can detect anunused LED string automatically and remove it from the control loop during start-up by either connectingthe unused LEDX pin to GND or settingthe corresponding register CHEN7:0bits to 0through the I²C interface.

Synchronous Rectifier

To save cost and reduce PCB size, the MP3376 works in synchronous rectifier mode by default. A 100nF ceramic capacitor and a 47Ω resistor inseries between BST and SW is the best BST supply choice for the synchronous converter.

In some cases, such as extremely high switching frequency and output power applications, it is recommended to use an external rectifier for better thermal and efficiency. To disable the internal synchronous rectifier, set theregister SYNC bitto 0.

Open-String Protection

Open-string protection is achieved bydetecting the voltage of OUT and LED1-8. During operation, if one string is open, the respective LEDX pin voltage ispulled low to ground, and the IC continues charging the output voltage until it reaches the OVP threshold. If the OVP point has been triggered, the chip stops switching and marks offthe fault string that hasan LEDX pin voltage lower than 100mV. Once marked, the remaining LED strings force the output voltage back to normal regulation. The string with the largest voltage drop determines the output regulation value.

Short-String Protection

The MP3376 monitors the LEDX pin voltages to determine if a short-string fault has occurred. If one or more strings are shorted, the respective LEDX pins tolerate high voltage stress. If an LEDX pin voltage is higher than the protection threshold (programmable by LEDS1:0 bits), an internal counter is started.Ifthis fault condition lasts for 1.8ms(f_{SW}=1.2MHz), the fault string is marked off and disabled. Once a string is marked off, it is disconnected from the output voltage loop until the part restarts. If all strings are shorted, the MP3376shuts down the step-up converter until the power is restarted(VIN supply switches on from off) or EN is toggled (EN switches on from off).

Cycle-by-Cycle Current Limit

To prevent the external components from exceeding the current stress rating, the IC uses a cycle-by-cycle current-limit protection.The limit value can be selected by the register ILIMbit. When the current exceeds the current limit value, the IC stops switching until the next clock cycle begins.

Latch-Off Current Limit Protection

To avoid device damage caused by a large current rating (such as inductor or diode short to GND), the MP3376 usesa latch-off current-limit protection when the current flowing through the low-side MOSFET reaches the threshold (3.5A) in around 200ns and lasts for five switching cycles.

Thermal Protection

To prevent the IC from operating at exceedingly high temperatures, thermal shutdown is implemented by detecting the silicon die temperature. When the die temperature exceeds the upper threshold (T_{ST}), the IC shuts down and resumes normal operation when the die temperature drops below the lower threshold. Typically, the hysteresis value is 20°C.

One-Time Program(OTP) Mode Operation

The MP3376 can change the register default valuesseveral timeswith the OTP function.The internal registers 00H, 01H, and 02H can be programmed five times.The internal registers 03H and 04H can only be programmed once.

It is recommended to use the sequence below for OTP operation.

1. Write the customized default into all internal registers with the I^2C when OTMD = 0 (02H - D11) and OTPEN = 0 (02H - D10).
2. Ensure that EN is high and VIN > 8V before entering OTP mode.
3. Set OTPMD = 1 (02H - D11). The IC enters one-time program mode, and the VCC voltage rises to about 6.3V.
4. Set OTPEN = 1 (02H - D10). The MP3376 begins burning the customized default one by one.
5. Burn the registers from 00H to 04H first after enabling the OTP function.
6. Burn the OTP timer (05H-D7:5) last.

The OTPEN bit resets to 0 after 400ms of burning time. The timer (05H-D7:5) counts the number of times the register has been burnt successfully.

Note that not all internal registers and bits are programmed respectively. Therefore, write all registers carefully with correct values before setting OTPEN = 1.

I^2C Interface Register Description

Please read/write the register after EN is ready for more than 2ms**.**

I^2C Chip Address

The 7-bit MSB device address is 0x28~0x2B. After the start condition, the I^2C-compatible master sends a 7-bit address followed by an eighth read (1) or write (0) bit.

The following bit indicates the register address to or from which the data is written or read.A0 and A1 can program the IC address.Therefore, the fourMP3376 chips share the same I^2C interface.

0	1	0	1	0	A0	A1	R/W

The I^2C Compatible Device Address

Register Mapping

Add	D15	D14	D13	D12	D11	D10	D9	D8
00H	ISET7	ISET6	ISET5	ISET4	ISET3	ISET2	ISET1	ISET0
Add	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
00H	CHEN7	CHEN6	CHEN5	CHEN4	CHEN3	CHEN2	CHEN1	CHEN0

Add	D15	D14	D13	D12	D11	D10	D9	D8
01H	NA	NA	NA	NA	NA	NA	OVP1	OVP1
Add	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
01H	SYNC	MOD2	MOD1	MOD0	ILIM	FS2	FS1	FS0

Add	D15	D14	D13	D12	D11	D10	D9	D8
02H	NA	NA	NA	NA	OTPMD	OTPEN	ADIM9	ADIM8
Add	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
02H	ADIM7	ADIM6	ADIM5	ADIM4	ADIM3	ADIM2	ADIM1	ADIM0

Add	D15	D14	D13	D12	D11	D10	D9	D8
03H	NA	NA	NA	NA	NA	TSLP2	TSLP1	TSLP0
Add	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
03H	LEDS1	LEDS0	FPWM3	FPWM2	FPWM1	FPWM0	DIMT1	DIMT0

Add	D15	D14	D13	D12	D11	D10	D9	D8
04H	NA	NA	PWM13	PWM12	PWM11	PWM10	PWM9	PWM8
Add	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
04H	PWM7	PWM6	PWM5	PWM4	PWM3	PWM2	PWM1	PWM0

Add	D15	D14	D13	D12	D11	D10	D9	D8
05H	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
Add	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
05H	TIME2	TIME1	TIME0	FT_OTP	FT_OCP	FT_OVP	FT_LEDO	FT_LEDS

NOTES:
The register(00H, 01H, 02H) bitsin redcan be written to a customized default five times.
The register (03H, 04H) bitsin bluecan be written to a customized default once.

Table1: LED Current Full-Scale and Channel Enable Register

Addr: 0x00				
Bit	**Bit Name**	**Access**	**Default**	**Description**
15:8	ISET7:0	RW	FFh	LED current full-scale current bits. These bits set the max current for each channel. 00h: 0mA; …; FFh: 50mA. 0.196mA/step.
7:0	CHEN7:0	RW	FFh	LED current source enable bits. Thesebits control the internal LED current sources respectively. CHEN0: 1 = LED current source 1 is enabled 0 = disabled CHEN1: 1 = LED current source 2 is enabled 0 = disabled CHEN2: 1 = LED current source 3 is enabled 0 = disabled CHEN3: 1 = LED current source 4 is enabled 0 = disabled CHEN4: 1= LED current source 5 is enabled 0 = disabled CHEN5: 1 = LED current source 6 is enabled 0 = disabled CHEN6: 1 = LED current source 7 is enabled 0 = disabled CHEN7: 1 = LED current source 8 is enabled 0 = disabled

Table2: Dimming Mode and Parameter Set Register

Addr: 0x01				
Bit	**Bit Name**	**Access**	**Default**	**Description**
15:10	NA	R	NA	Reserved.
9:8	OVP1:0	RW	01b	Output voltage OVP protection threshold bits. 00=24V 01=31V 10=36V 11= NA
7	SYNC	RW	1b	Boost converter rectifier operation mode bit. 0= IC works in non-synchronous mode 1= IC works in synchronous mode
6:4	MOD2:0	RW	100b	LED current dimming mode bits. 000=the IC works in analog dimming mode throughthe external PWM input signal.The LED current amplitude changes with the input PWM duty. 001=the IC works in analog dimming mode through the I^2C interface. The LED current amplitude changes with the register PWM13:0 bits. 100=the IC works in mix dimming mode throughthe external PWM input signal. If the input PWM duty is higher than the transfer point, the IC works in analog dimming mode. Otherwise,the IC works in PWM dimming mode. The DIMT1:0 bit determines the transfer point of mix dimming mode. 101=the IC works in mix dimming mode throughthe I^2C interface.If the duty set by the PWM13:0 bitis higher than the transfer point, the IC works in analog dimming mode. Otherwise, the IC works in PWM dimming mode. The DIMT1:0 bit determines the transfer point of mix dimming mode.
3	ILIM	RW	1b	Inductor cycle-by-cycle current-limit bit of the converter. 0= 1.8A current limit 1=2.5A current limit
2:0	FS2:0	RW	011b	The boost converter switching frequency bits. 000=350kHz 001=500kHz 010=650kHz 011=800kHz 100=950kHz 101=1.2MHz 110=1.8MHz 111=2.4MHz

Table3: One-Time Program Enable and Analog Dimming Register

Addr: 0x02				
Bit	**Bit Name**	**Access**	**Default**	**Description**
15:12	NA	R	NA	Reserved.
11	OTPMD	RW	0b	One-time program mode bit. OTP burning must be done in OTP mode. 0= notOTP mode 1= enter OTP mode. The VCC voltage rises to about 6.3V if the input voltage >8V.
10	OTPEN	RW	0b	One-time program enable bit. 1= enable OTP function. Burn the customer's default to all internal registers one by one (from 00H to 04H) and TIME1:0 bit. Reset to 0 after finishingOTP. 0= disable OTP function
9:0	ADIM9:0	RW	3FFh	Analog dimming bits. This controls the LED current amplitude in any dimming mode. 000h=0%; 0x001= 0.098%; …; 3FFh=100%.0.098% per step.

Table4: Slope and PWM Dimming Frequency Register

Addr: 0x03				
Bit	**Bit Name**	**Access**	**Default**	**Description**
15:11	NA	R	NA	Reserved.
10:8	TSLP2:0	RW	010b	LED current ramp-up/-down slope bit. 000=2μs per step 001=4μs per step 010=8μs per step 011=16μs per step 100=32μs per step 101=64μs per step 110=128μs per step 111= NA
7:6	LEDS1:0	RW	01b	LED short protection threshold bits. 00=2.5V 01=5V 10= 7.5V 11= 10V
5:2	FPWM3:0	RW	1111b	LED current dimming frequency bits when the device works in mix dimming mode and $D_{PWM}$is less than thetransfer point set by the DIM1:0 bit. 0000 = 120Hz 0001 = 240Hz 0010 = 400Hz 0011 = 800Hz 0100 = 1kHz 0101 = 2kHz 0110 = 4kHz 0111 = 10kHz 1000 = 14kHz 1001 = 18kHz 1010 = 22kHz 1011 = 26kHz 1100 = 29kHz 1101 = 33kHz 1110 = 37kHz 1111= followPWM input signal when dimming byan external PWM input signal
1:0	DIMT1:0	RW	10b	Transfer point bits in mix dimming mode. If the dimming duty is higher than the threshold, the IC works in analog dimming mode.If the dimming duty is lower than the threshold, the IC works in PWM dimming mode. 00=6.25% 01=12.5% 10=25% 11= 50%

Table5: PWM Dimming Register

Addr: 0x04				
Bit	**Bit Name**	**Access**	**Default**	**Description**
15:14	NA	R	NA	Reserved.
13:0	PWM13:0	RW	0000h	LED current dimming duty settingbit in PWM dimming or mix dimming mode.This controls the LED current dimming dutywhen MOD2:0 bit is set to 001bor 101b. 0000h: 0%; 0x0001: 0.006%; …; 3FFFh:100%. 0.006% per step.

Table6: ID and Fault Register

Addr: 0x05				
Bit	**Bit Name**	**Access**	**Default**	**Description**
15:8	ID7:0	R	00010001b	Device ID bits.
7:5	TIME 2:0	R	000b	OTP time bit. When OTP occurs once, TIME2:0 countsone time. 000=0 001=1 010=2 011=3 100=4 101=5
4	FT_OTP	R	0b	Over-temperature protection fault indication bit. 0=no fault 1=fault. The fault status can latch off until it is reset to 0 after this bit is read.
3	FT_OCP	R	0b	Over-current protection fault indication bit. 0= no fault 1= fault. The fault status can latch off until it is reset to 0 after this bit is read.
2	FT_OVP	R	0b	Over-voltage protection fault indication bit. 0= no fault 1= fault. The fault status can latch off until it is reset to 0 after this bit is read.
1	FT_LEDO	R	0b	LED current source open fault indication bit. 0=no fault 1= fault. The fault status can latch off until it is reset to 0 after this bit is read.
0	FT_LEDS	R	0b	LED short fault indication bit. 0= no fault 1= fault. The fault status can latch off until it is reset to 0 after this bit is read.

APPLICATION INFORMATION

Selecting the Switching Frequency

The switching frequency of the step-up converter is set by the register FS2:0bits(see Table 2).

Setting the LED Current

The LED string full-scale current is set by the register ISET7:0 bits from 0mA to 50mA with 0.196mA per step.

Selecting the Input Capacitor

The input capacitor reduces the surge current drawn from the input supply and the switching noise from the device. The input capacitor impedance at the switching frequency should be less than the input source impedance to prevent the high-frequency switching current from passing through to the input. Ceramic capacitors with X5R or X7R dielectrics are recommended for their low ESR and small temperature coefficients. For most applications, a 4.7μF ceramic capacitor is sufficient.

Selecting the Inductor

The MP3376 requires an inductor to supply a higher output voltage while being driven by the input voltage. A larger value inductor results in less ripple current,lower peak-inductor current, and reduced stress on the internal N-channel MOSFET. However, the larger value inductor also has a larger physical size, higher series resistance, and lower saturation current.

Choose an inductor that willnot saturate under the worst-case load conditions. Select the minimum inductor value to ensure that the boost converter works in continuous conduction mode with high efficiency and good EMI performance.

Calculate the required inductance value using Equation (1) and Equation (2):

$$L \geq \frac{\eta \times V_{OUT} \times D \times (1-D)^2}{2 \times f_{SW} \times I_{LOAD}} \quad (1)$$

$$D = 1 - \frac{V_{IN}}{V_{OUT}} \quad (2)$$

Where $V_{IN}$is the input voltage, $V_{OUT}$is the output voltage, f_{SW} is the switching frequency, I_{LOAD} is the LED load current, and η is the efficiency.

With a given inductor value, the inductor DC current rating is at least 40% higher than the maximum input peak inductor current for most applications. The inductor's DC resistance should be as small as possible to achieve higher efficiency.

Selecting the Output Capacitor

The output capacitor keeps the output voltage ripple small and ensures feedback loop stability. The output capacitor impedance must be low at the switching frequency. Ceramic capacitors with X7R dielectrics are recommended for their low ESR characteristics. For most applications, a 2.2μF ceramic capacitor is sufficient.

Setting the Over-Voltage Protection (OVP)

The output OVP voltage is set by the register OVP1:0bits(see Table 2).

PCB Layout Guidelines

Careful attention must be givento the PCB layout and component placement. Efficient PCB layout of the high-frequency switching path is critical to prevent noise and electromagnetic interference problems. For best results, follow the guidelines below.

1. Keep the loop of SW to PGND, the output diode (if needed),and the output capacitor as short as possible and flowing with high-frequency pulse current.
2. Place a ceramic capacitor close to the input and VCC, since they are susceptible to noise.

TYPICAL APPLICATION CIRCUITS

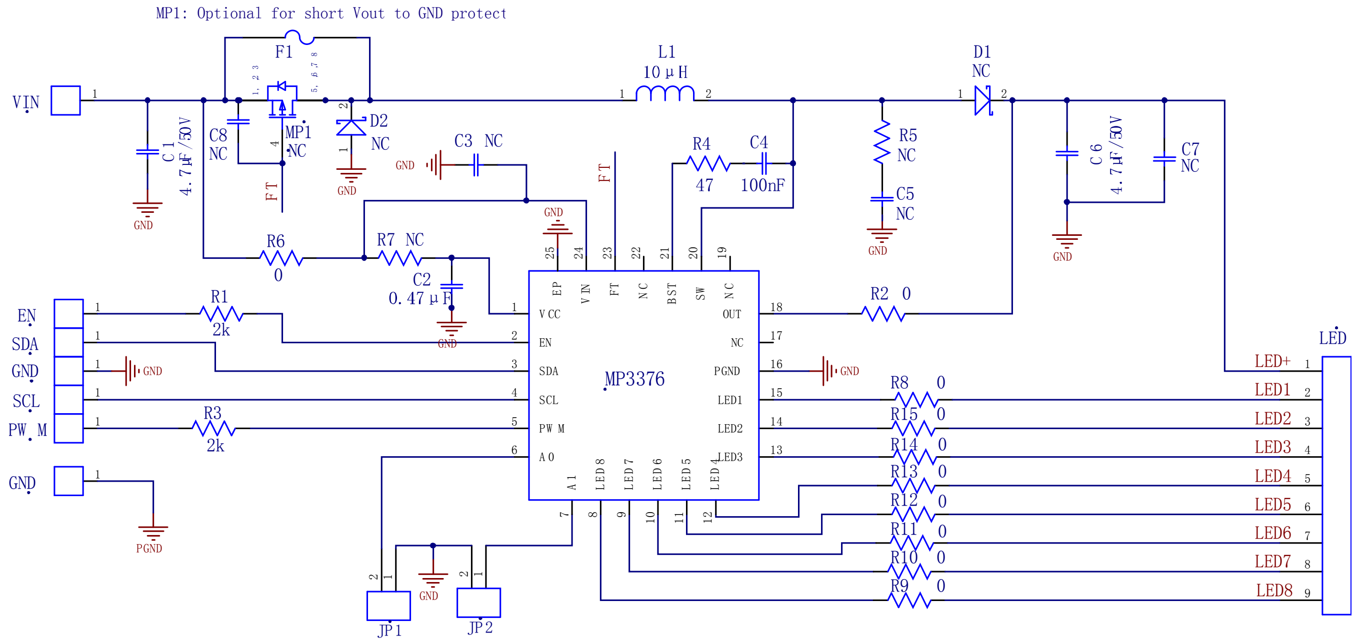
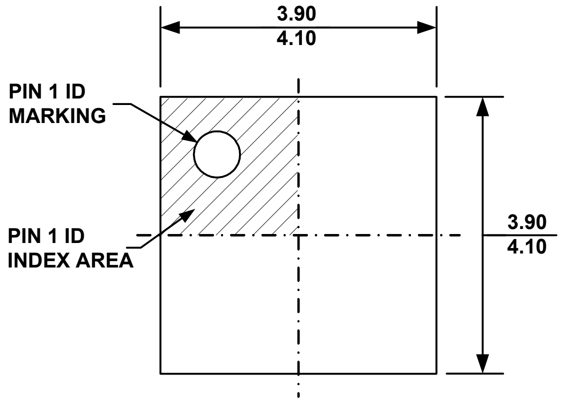


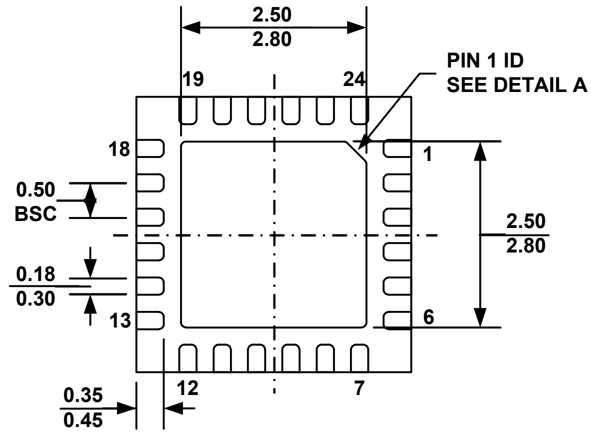
Figure 9: Typical Application Circuit

PACKAGE INFORMATION

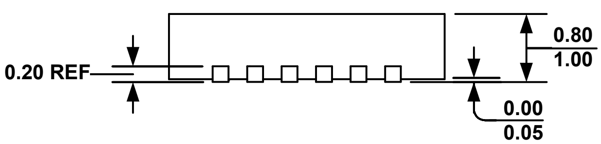
QFN-24 (4mmx4mm)



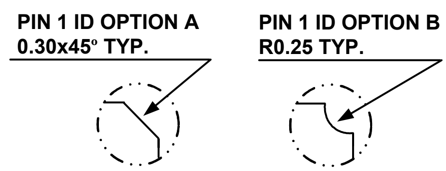
TOP VIEW



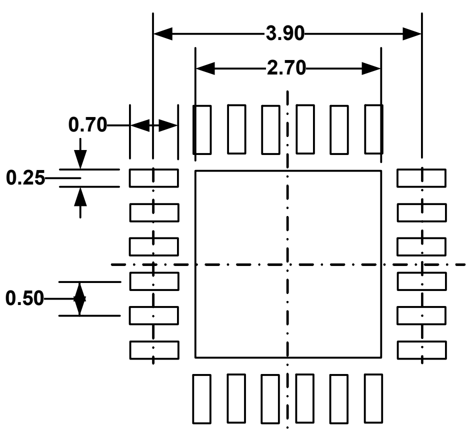
BOTTOM VIEW



SIDE VIEW



DETAIL A



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETER MAX.
4) DRAWING CONFIRMS TO JEDEC MO-220, VARIATION VGGD.
5) DRAWING IS NOT TO SCALE.